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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1938-e-ml

3.0 MEMORY ORGANIZATION

These devices contain the following types of memory:

- Program Memory
 - Configuration Words
 - Device ID
 - User ID
 - Flash Program Memory
- Data Memory
 - Core Registers
 - Special Function Registers
 - General Purpose RAM
 - Common RAM
- Data EEPROM memory⁽¹⁾

Note 1: The Data EEPROM Memory and the method to access Flash memory through the EECON registers is described in [Section 11.0 “Data EEPROM and Flash Program Memory Control”](#).

The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing

3.1 Program Memory Organization

The enhanced mid-range core has a 15-bit program counter capable of addressing a 32K x 14 program memory space. [Table 3-1](#) shows the memory sizes implemented for the PIC16(L)F1938/9 family. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see [Figure 3-1](#)).

TABLE 3-1: DEVICE SIZES AND ADDRESSES

Device	Program Memory Space (Words)	Last Program Memory Address
PIC16F1938/PIC16LF1938	16,384	3FFFh
PIC16F1939/PIC16LF1939	16,384	3FFFh

5.2.2 INTERNAL CLOCK SOURCES

The device may be configured to use the internal oscillator block as the system clock by performing one of the following actions:

- Program the FOSC<2:0> bits in Configuration Words to select the INTOSC clock source, which will be used as the default system clock upon a device Reset.
- Write the SCS<1:0> bits in the OSCCON register to switch the system clock source to the internal oscillator during run-time. See [Section 5.3 “Clock Switching”](#) for more information.

In **INTOSC** mode, OSC1/CLKIN is available for general purpose I/O. OSC2/CLKOUT is available for general purpose I/O or CLKOUT.

The function of the OSC2/CLKOUT pin is determined by the CLKOUTEN bit in Configuration Words.

The internal oscillator block has two independent oscillators and a dedicated Phase-Lock Loop, HFPLL that can produce one of three internal system clock sources.

1. The **HFINTOSC** (High-Frequency Internal Oscillator) is factory calibrated and operates at 16 MHz. The HFINTOSC source is generated from the 500 kHz MFINTOSC source and the dedicated Phase-Lock Loop, HFPLL. The frequency of the HFINTOSC can be user-adjusted via software using the OSCTUNE register ([Register 5-3](#)).
2. The **MFINTOSC** (Medium-Frequency Internal Oscillator) is factory calibrated and operates at 500 kHz. The frequency of the MFINTOSC can be user-adjusted via software using the OSCTUNE register ([Register 5-3](#)).
3. The **LFINTOSC** (Low-Frequency Internal Oscillator) is uncalibrated and operates at 31 kHz.

5.2.2.1 HFINTOSC

The High-Frequency Internal Oscillator (HFINTOSC) is a factory calibrated 16 MHz internal clock source. The frequency of the HFINTOSC can be altered via software using the OSCTUNE register ([Register 5-3](#)).

The output of the HFINTOSC connects to a postscaler and multiplexer (see [Figure 5-1](#)). One of multiple frequencies derived from the HFINTOSC can be selected via software using the IRCF<3:0> bits of the OSCCON register. See [Section 5.2.2.7 “Internal Oscillator Clock Switch Timing”](#) for more information.

The HFINTOSC is enabled by:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired HF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to ‘1x’.

A fast startup oscillator allows internal circuits to power up and stabilize before switching to HFINTOSC.

The High Frequency Internal Oscillator Ready bit (HFIOFR) of the OSCSTAT register indicates when the HFINTOSC is running.

The High Frequency Internal Oscillator Status Locked bit (HFIOFL) of the OSCSTAT register indicates when the HFINTOSC is running within 2% of its final value.

The High Frequency Internal Oscillator Stable bit (HFIOFS) of the OSCSTAT register indicates when the HFINTOSC is running within 0.5% of its final value.

5.2.2.2 MFINTOSC

The Medium-Frequency Internal Oscillator (MFINTOSC) is a factory calibrated 500 kHz internal clock source. The frequency of the MFINTOSC can be altered via software using the OSCTUNE register ([Register 5-3](#)).

The output of the MFINTOSC connects to a postscaler and multiplexer (see [Figure 5-1](#)). One of nine frequencies derived from the MFINTOSC can be selected via software using the IRCF<3:0> bits of the OSCCON register. See [Section 5.2.2.7 “Internal Oscillator Clock Switch Timing”](#) for more information.

The MFINTOSC is enabled by:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired HF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to ‘1x’.

The Medium Frequency Internal Oscillator Ready bit (MFIOFR) of the OSCSTAT register indicates when the MFINTOSC is running.

11.6 Write Verify

Depending on the application, good programming practice may dictate that the value written to the data EEPROM or program memory should be verified (see [Example 11-6](#)) to the desired value to be written. [Example 11-6](#) shows how to verify a write to EEPROM.

EXAMPLE 11-6: EEPROM WRITE VERIFY

```
BANKSEL EEDATL      ;  
MOVF    EEDATL, W    ;EEDATL not changed  
                ;from previous write  
BSF      EECON1, RD   ;YES, Read the  
                ;value written  
XORWF    EEDATL, W    ;  
BTFSS    STATUS, Z    ;Is data the same  
GOTO     WRITE_ERR    ;No, handle error  
:                ;Yes, continue
```

13.0 INTERRUPT-ON-CHANGE

The PORTB pins can be configured to operate as Interrupt-On-Change (IOC) pins. An interrupt can be generated by detecting a signal that has either a rising edge or a falling edge. Any individual PORT IOC pin, or combination of PORT IOC pins, can be configured to generate an interrupt. The Interrupt-on-change module has the following features:

- Interrupt-on-Change enable (Master Switch)
- Individual pin configuration
- Rising and falling edge detection
- Individual pin interrupt flags

Figure 13-1 is a block diagram of the IOC module.

13.1 Enabling the Module

To allow individual PORTB pins to generate an interrupt, the IOCIE bit of the INTCON register must be set. If the IOCIE bit is disabled, the edge detection on the pin will still occur, but an interrupt will not be generated.

13.2 Individual Pin Configuration

For each PORTB pin, a rising edge detector and a falling edge detector are present. To enable a pin to detect a rising edge, the associated IOCBP_x bit of the IOCBP register is set. To enable a pin to detect a falling edge, the associated IOCBN_x bit of the IOCBN register is set.

A pin can be configured to detect rising and falling edges simultaneously by setting both the IOCBP_x bit and the IOCBN_x bit of the IOCBP and IOCBN registers, respectively.

13.3 Interrupt Flags

The IOCBF_x bits located in the IOCBF register are status flags that correspond to the Interrupt-on-change pins of PORTB. If an expected edge is detected on an appropriately enabled pin, then the status flag for that pin will be set, and an interrupt will be generated if the IOCIE bit is set. The IOCIF bit of the INTCON register reflects the status of all IOCBF_x bits.

13.4 Clearing Interrupt Flags

The individual status flags, (IOCBF_x bits), can be cleared by resetting them to zero. If another edge is detected during this clearing operation, the associated status flag will be set at the end of the sequence, regardless of the value actually being written.

In order to ensure that no detected edge is lost while clearing flags, only AND operations masking out known changed bits should be performed. The following sequence is an example of what should be performed.

EXAMPLE 13-1: CLEARING INTERRUPT FLAGS (PORTA EXAMPLE)

```
MOVLW    0xff
XORWF    IOCBF, W
ANDWF    IOCBF, F
```

13.5 Operation in Sleep

The interrupt-on-change interrupt sequence will wake the device from Sleep mode, if the IOCIE bit is set.

If an edge is detected while in Sleep mode, the IOCBF register will be updated prior to the first instruction executed out of Sleep.

22.5 Register Definitions: Timer2/4/6 Control

REGISTER 22-1: TxCON: TIMER2/TIMER4/TIMER6 CONTROL REGISTER

U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	TxOUTPS<3:0>				TMRxON	TxCKPS<1:0>	
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7 **Unimplemented:** Read as '0'

bit 6-3 **TxOUTPS<3:0>:** Timerx Output Postscaler Select bits

1111 = 1:16 Postscaler
 1110 = 1:15 Postscaler
 1101 = 1:14 Postscaler
 1100 = 1:13 Postscaler
 1011 = 1:12 Postscaler
 1010 = 1:11 Postscaler
 1001 = 1:10 Postscaler
 1000 = 1:9 Postscaler
 0111 = 1:8 Postscaler
 0110 = 1:7 Postscaler
 0101 = 1:6 Postscaler
 0100 = 1:5 Postscaler
 0011 = 1:4 Postscaler
 0010 = 1:3 Postscaler
 0001 = 1:2 Postscaler
 0000 = 1:1 Postscaler

bit 2 **TMRxON:** Timerx On bit

1 = Timerx is on
 0 = Timerx is off

bit 1-0 **TxCKPS<1:0>:** Timer2-type Clock Prescale Select bits

11 = Prescaler is 64
 10 = Prescaler is 16
 01 = Prescaler is 4
 00 = Prescaler is 1

23.3.2 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for standard PWM operation:

1. Disable the CCPx pin output driver by setting the associated TRIS bit.
2. Timer2/4/6 resource selection:
 - Select the Timer2/4/6 resource to be used for PWM generation by setting the CxTSEL<1:0> bits in the CCPTMERSx register.
3. Load the PRx register with the PWM period value.
4. Configure the CCP module for the PWM mode by loading the CCPxCON register with the appropriate values.
5. Load the CCPRxL register and the DCxBx bits of the CCPxCON register, with the PWM duty cycle value.
6. Configure and start Timer2/4/6:
 - Clear the TMRxIF interrupt flag bit of the PIRx register. See Note below.
 - Configure the TxCKPS bits of the TxCON register with the Timer prescale value.
 - Enable the Timer by setting the TMRxON bit of the TxCON register.
7. Enable PWM output pin:
 - Wait until the Timer overflows and the TMRxIF bit of the PIRx register is set. See Note below.
 - Enable the CCPx pin output driver by clearing the associated TRIS bit.

Note: In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then step 6 may be ignored.

23.3.3 TIMER2/4/6 TIMER RESOURCE

The PWM standard mode makes use of one of the 8-bit Timer2/4/6 timer resources to specify the PWM period.

Configuring the CxTSEL<1:0> bits in the CCPTMRSx register selects which Timer2/4/6 timer is used.

23.3.4 PWM PERIOD

The PWM period is specified by the PRx register of Timer2/4/6. The PWM period can be calculated using the formula of [Equation 23-1](#).

EQUATION 23-1: PWM PERIOD

$$PWM\ Period = [(PRx) + 1] \cdot 4 \cdot TOSC \cdot (TMRx\ Prescale\ Value)$$

Note 1: $TOSC = 1/FOSC$

When TMRx is equal to PRx, the following three events occur on the next increment cycle:

- TMRx is cleared
- The CCPx pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is latched from CCPRxL into CCPRxH.

Note: The Timer postscaler (see [Section 22.1 "Timer2/4/6 Operation"](#)) is not used in the determination of the PWM frequency.

23.3.5 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to multiple registers: CCPRxL register and DCxB<1:0> bits of the CCPxCON register. The CCPRxL contains the eight MSBs and the DCxB<1:0> bits of the CCPxCON register contain the two LSBs. CCPRxL and DCxB<1:0> bits of the CCPxCON register can be written to at any time. The duty cycle value is not latched into CCPRxH until after the period completes (i.e., a match between PRx and TMRx registers occurs). While using the PWM, the CCPRxH register is read-only.

[Equation 23-2](#) is used to calculate the PWM pulse width.

[Equation 23-3](#) is used to calculate the PWM duty cycle ratio.

EQUATION 23-2: PULSE WIDTH

$$Pulse\ Width = (CCPRxL:CCPxCON<5:4>) \cdot TOSC \cdot (TMRx\ Prescale\ Value)$$

EQUATION 23-3: DUTY CYCLE RATIO

$$Duty\ Cycle\ Ratio = \frac{(CCPRxL:CCPxCON<5:4>)}{4(PRx + 1)}$$

The CCPRxH register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

The 8-bit timer TMRx register is concatenated with either the 2-bit internal system clock (FOSC), or two bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2/4/6 prescaler is set to 1:1.

When the 10-bit time base matches the CCPRxH and 2-bit latch, then the CCPx pin is cleared (see [Figure 23-4](#)).

23.4 PWM (Enhanced Mode)

The enhanced PWM function described in this section is available for CCP modules ECCP1, ECCP2 and ECCP3, with any differences between modules noted.

The enhanced PWM mode generates a Pulse-Width Modulation (PWM) signal on up to four different output pins with up to 10 bits of resolution. The period, duty cycle, and resolution are controlled by the following registers:

- PRx registers
- TxCON registers
- CCPRxL registers
- CCPxCON registers

The ECCP modules have the following additional PWM registers which control Auto-shutdown, Auto-restart, Dead-band Delay and PWM Steering modes:

- CCPxAS registers
- PSTRxCON registers
- PWMxCON registers

The enhanced PWM module can generate the following five PWM Output modes:

- Single PWM
- Half-Bridge PWM
- Full-Bridge PWM, Forward mode
- Full-Bridge PWM, Reverse mode
- Single PWM with PWM Steering mode

To select an Enhanced PWM Output mode, the PxM bits of the CCPxCON register must be configured appropriately.

The PWM outputs are multiplexed with I/O pins and are designated PxA, PxB, PxC and PxD. The polarity of the PWM pins is configurable and is selected by setting the CCPxM bits in the CCPxCON register appropriately.

Figure 23-5 shows an example of a simplified block diagram of the Enhanced PWM module.

Table 23-9 shows the pin assignments for various Enhanced PWM modes.

- Note 1:** The corresponding TRIS bit must be cleared to enable the PWM output on the CCPx pin.
- 2:** Clearing the CCPxCON register will relinquish control of the CCPx pin.
- 3:** Any pin not used in the enhanced PWM mode is available for alternate pin functions, if applicable.
- 4:** To prevent the generation of an incomplete waveform when the PWM is first enabled, the ECCP module waits until the start of a new PWM period before generating a PWM signal.

FIGURE 23-5: EXAMPLE SIMPLIFIED BLOCK DIAGRAM OF THE ENHANCED PWM MODE

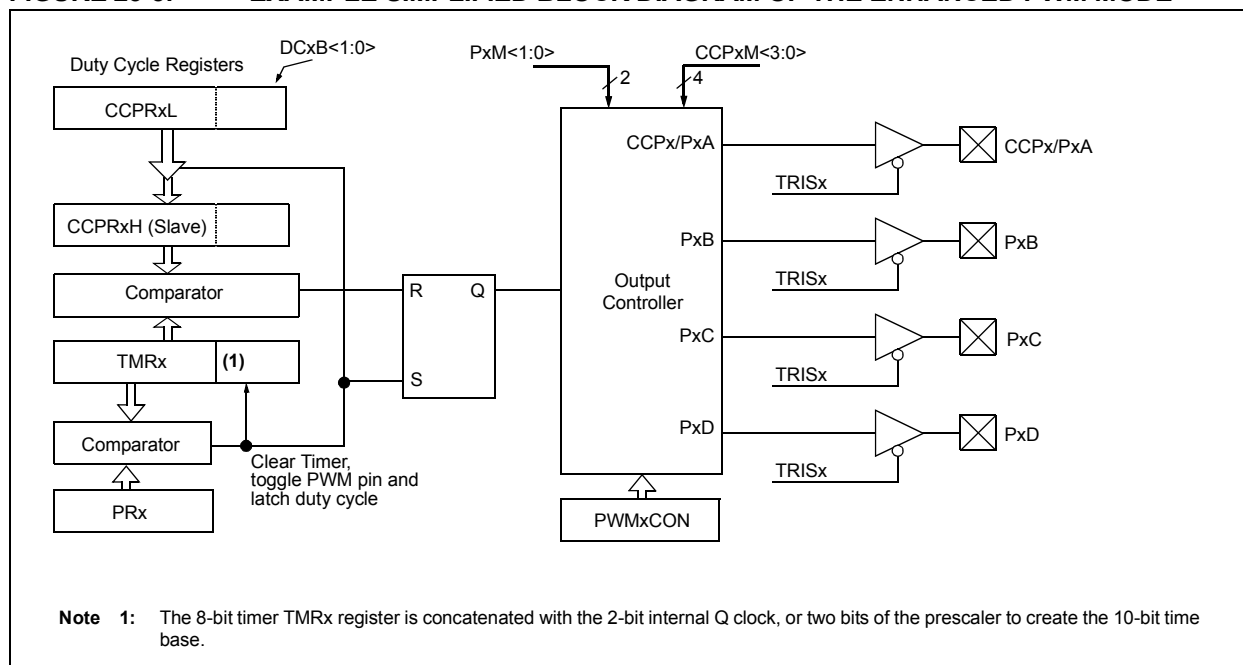


FIGURE 25-7: AUTO-WAKE-UP BIT (WUE) TIMING DURING NORMAL OPERATION

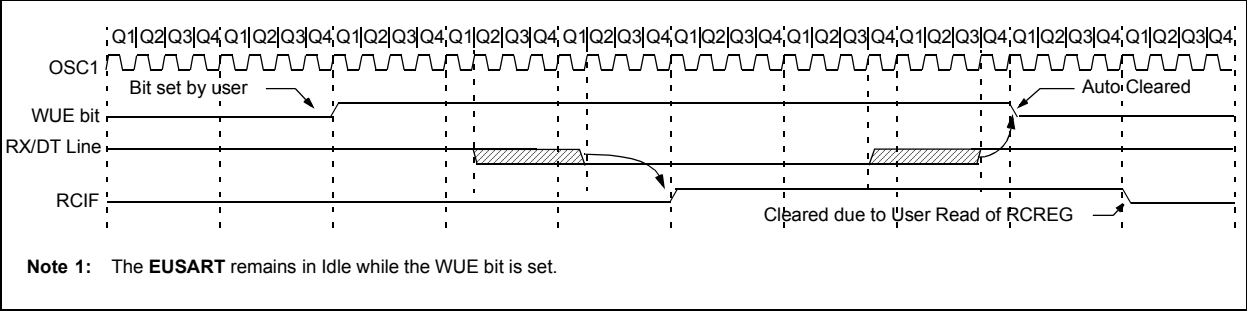
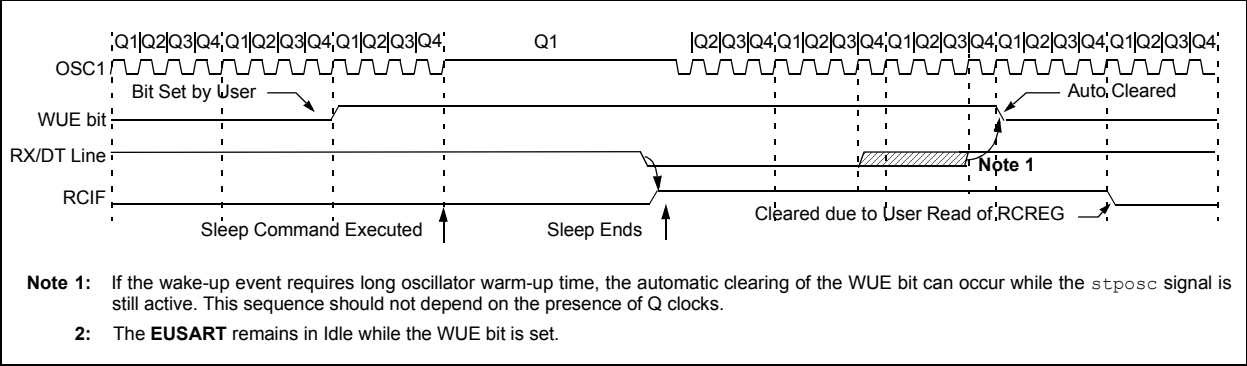


FIGURE 25-8: AUTO-WAKE-UP BIT (WUE) TIMINGS DURING SLEEP



25.5.1.5 Synchronous Master Reception

Data is received at the RX/DT pin. The RX/DT pin output driver is automatically disabled when the EUSART is configured for synchronous master receive operation.

In Synchronous mode, reception is enabled by setting either the Single Receive Enable bit (SREN of the RCSTA register) or the Continuous Receive Enable bit (CREN of the RCSTA register).

When SREN is set and CREN is clear, only as many clock cycles are generated as there are data bits in a single character. The SREN bit is automatically cleared at the completion of one character. When CREN is set, clocks are continuously generated until CREN is cleared. If CREN is cleared in the middle of a character the CK clock stops immediately and the partial character is discarded. If SREN and CREN are both set, then SREN is cleared at the completion of the first character and CREN takes precedence.

To initiate reception, set either SREN or CREN. Data is sampled at the RX/DT pin on the trailing edge of the TX/CK clock pin and is shifted into the Receive Shift Register (RSR). When a complete character is received into the RSR, the RCIF bit is set and the character is automatically transferred to the two character receive FIFO. The Least Significant eight bits of the top character in the receive FIFO are available in RCREG. The RCIF bit remains set as long as there are unread characters in the receive FIFO.

25.5.1.6 Slave Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a slave receives the clock on the TX/CK line. The TX/CK pin output driver is automatically disabled when the device is configured for synchronous slave transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One data bit is transferred for each clock cycle. Only as many clock cycles should be received as there are data bits.

25.5.1.7 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before RCREG is read to access the FIFO. When this happens the OERR bit of the RCSTA register is set. Previous data in the FIFO will not be overwritten. The two characters in the FIFO buffer can be read, however, no additional characters will be received until the error is cleared. The OERR bit can only be cleared by clearing the overrun condition. If the overrun error occurred when the SREN bit is set and CREN is clear then the error is cleared by reading RCREG. If the overrun occurred when the CREN bit is

set then the error condition is cleared by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit which resets the EUSART.

25.5.1.8 Receiving 9-bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCSTA register is set the EUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RCSTA register is the ninth, and Most Significant, data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCREG.

25.5.1.9 Synchronous Master Reception Set-up:

1. Initialize the SPBRGH, SPBRGL register pair for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
2. Clear the ANSEL bit for the RX pin (if applicable).
3. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
4. Ensure bits CREN and SREN are clear.
5. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
6. If 9-bit reception is desired, set bit RX9.
7. Start reception by setting the SREN bit or for continuous reception, set the CREN bit.
8. Interrupt flag bit RCIF will be set when reception of a character is complete. An interrupt will be generated if the enable bit RCIE was set.
9. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
10. Read the 8-bit received data by reading the RCREG register.
11. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit which resets the EUSART.

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REGISTER 27-4: LCDCST: LCD CONTRAST CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	—	LCDCST<2:0>		
bit 7					bit 0		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

C = Only clearable bit

bit 7-3

Unimplemented: Read as '0'

bit 2-0

LCDCST<2:0>: LCD Contrast Control bits

Selects the resistance of the LCD contrast control resistor ladder

Bit Value = Resistor ladder

000 = Minimum Resistance (maximum contrast). Resistor ladder is shorted.

001 = Resistor ladder is at 1/7th of maximum resistance

010 = Resistor ladder is at 2/7th of maximum resistance

011 = Resistor ladder is at 3/7th of maximum resistance

100 = Resistor ladder is at 4/7th of maximum resistance

101 = Resistor ladder is at 5/7th of maximum resistance

110 = Resistor ladder is at 6/7th of maximum resistance

111 = Resistor ladder is at maximum resistance (minimum contrast).

REGISTER 27-5: LCDSEn: LCD SEGMENT ENABLE REGISTERS

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
SEn	SEn	SEn	SEn	SEn	SEn	SEn	SEn
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-0

SEn: Segment Enable bits

1 = Segment function of the pin is enabled

0 = I/O function of the pin is enabled

REGISTER 27-6: LCDDATAn: LCD DATA REGISTERS

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
SEGx-COMy	SEGx-COMy	SEGx-COMy	SEGx-COMy	SEGx-COMy	SEGx-COMy	SEGx-COMy	SEGx-COMy
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-0

SEGx-COMy: Pixel On bits

1 = Pixel on (dark)

0 = Pixel off (clear)

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27.3 LCD Clock Source Selection

The LCD module has three possible clock sources:

- $F_{osc}/256$
- T1OSC
- LFINTOSC

The first clock source is the system clock divided by 256 ($F_{osc}/256$). This divider ratio is chosen to provide about 1 kHz output when the system clock is 8 MHz. The divider is not programmable. Instead, the LCD prescaler bits LP<3:0> of the LCDPS register are used to set the LCD frame clock rate.

The second clock source is the T1OSC. This also gives about 1 kHz when a 32.768 kHz crystal is used with the Timer1 oscillator. To use the Timer1 oscillator as a clock source, the T1OSCEN bit of the T1CON register should be set.

The third clock source is the 31 kHz LFINTOSC, which provides approximately 1 kHz output.

The second and third clock sources may be used to continue running the LCD while the processor is in Sleep.

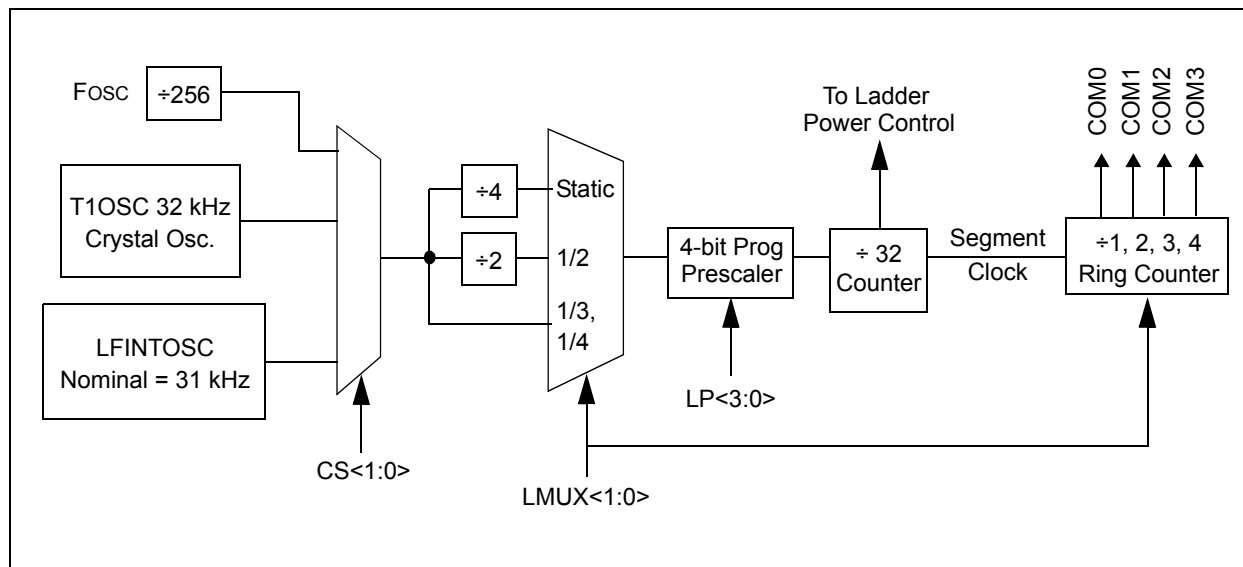
Using bits CS<1:0> of the LCDCON register can select any of these clock sources.

27.3.1 LCD PRESCALER

A 4-bit counter is available as a prescaler for the LCD clock. The prescaler is not directly readable or writable; its value is set by the LP<3:0> bits of the LCDPS register, which determine the prescaler assignment and prescale ratio.

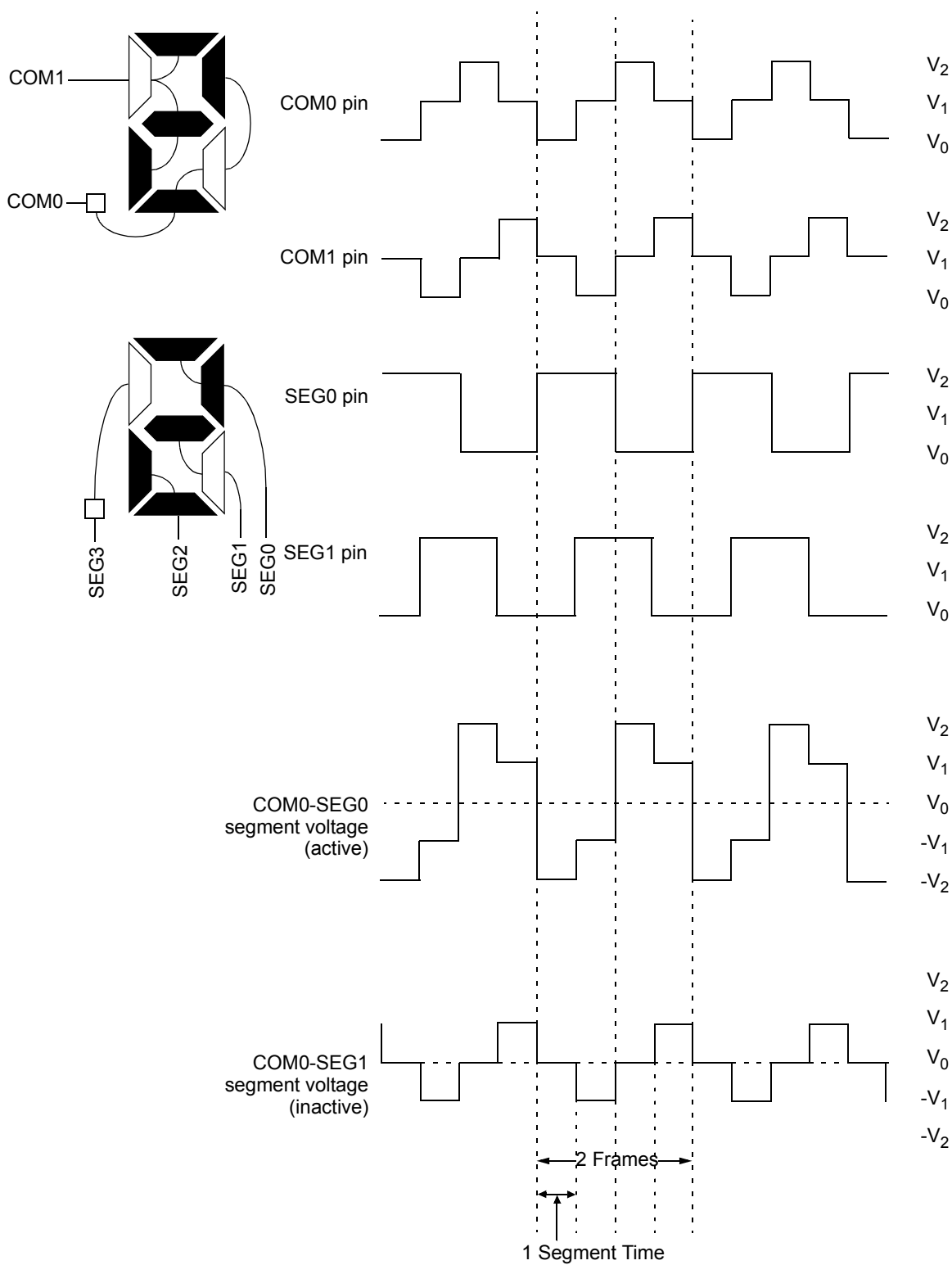
The prescale values are selectable from 1:1 through 1:16.

FIGURE 27-2: LCD CLOCK GENERATION



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FIGURE 27-10: TYPE-B WAVEFORMS IN 1/2 MUX, 1/2 BIAS DRIVE



Note: 1 Frame = 2 single segment times.

PIC16(L)F1938/9

30.6 Thermal Considerations

Standard Operating Conditions (unless otherwise stated)					
Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$					
Param No.	Sym.	Characteristic	Typ.	Units	Conditions
TH01	θ_{JA}	Thermal Resistance Junction to Ambient	60.0	$^{\circ}\text{C}/\text{W}$	28-pin SPDIP package
			69.7	$^{\circ}\text{C}/\text{W}$	28-pin SOIC package
			71.0	$^{\circ}\text{C}/\text{W}$	28-pin SSOP package
			27.5	$^{\circ}\text{C}/\text{W}$	28-pin UQFN 4x4mm package
			31.1	$^{\circ}\text{C}/\text{W}$	28-pin QFN 6x6mm package
			47.2	$^{\circ}\text{C}/\text{W}$	40-pin PDIP package
			49.8	$^{\circ}\text{C}/\text{W}$	44-pin TQFP package
			29.0	$^{\circ}\text{C}/\text{W}$	44-pin QFN 8x8mm package
TH02	θ_{JC}	Thermal Resistance Junction to Case	29.0	$^{\circ}\text{C}/\text{W}$	28-pin SPDIP package
			18.9	$^{\circ}\text{C}/\text{W}$	28-pin SOIC package
			24.0	$^{\circ}\text{C}/\text{W}$	28-pin SSOP package
			24.0	$^{\circ}\text{C}/\text{W}$	28-pin UQFN 4x4mm package
			5.0	$^{\circ}\text{C}/\text{W}$	28-pin QFN 6x6mm package
			24.7	$^{\circ}\text{C}/\text{W}$	40-pin PDIP package
			26.7	$^{\circ}\text{C}/\text{W}$	44-pin TQFP package
			2.0	$^{\circ}\text{C}/\text{W}$	44-pin QFN 8x8mm package
TH03	T_{JMAX}	Maximum Junction Temperature	150	$^{\circ}\text{C}$	
TH04	PD	Power Dissipation	—	W	$PD = P_{INTERNAL} + P_{I/O}$
TH05	$P_{INTERNAL}$	Internal Power Dissipation	—	W	$P_{INTERNAL} = I_{DD} \times V_{DD}^{(1)}$
TH06	$P_{I/O}$	I/O Power Dissipation	—	W	$P_{I/O} = \sum (I_{OL} \times V_{OL}) + \sum (I_{OH} \times (V_{DD} - V_{OH}))$
TH07	P_{DER}	Derated Power	—	W	$P_{DER} = P_{DMAX} (T_J - T_A) / \theta_{JA}^{(2)}$

Note 1: I_{DD} is current to run the chip alone without driving any load on the output pins.

2: T_A = Ambient Temperature

3: T_J = Junction Temperature

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TABLE 30-10: COMPARATOR SPECIFICATIONS

Operating Conditions: $1.8V < V_{DD} < 5.5V$, $-40^{\circ}C < T_A < +125^{\circ}C$ (unless otherwise stated).							
Param No.	Sym.	Characteristics	Min.	Typ.	Max.	Units	Comments
CM01	V _{IOFF}	Input Offset Voltage	—	±7.5	±60	mV	High-Power mode, $V_{ICM} = V_{DD}/2$
CM02	V _{ICM}	Input Common Mode Voltage	0	—	V _{DD}	V	
CM03	CMRR	Common Mode Rejection Ratio	—	50	—	dB	
CM04A	T _{RESP}	Response Time Rising Edge	—	400	800	ns	High-Power mode
CM04B		Response Time Falling Edge	—	200	400	ns	High-Power mode
CM04C		Response Time Rising Edge	—	1200	—	ns	Low-Power mode
CM04D		Response Time Falling Edge	—	550	—	ns	Low-Power mode
CM05	T _{MC2OV}	Comparator Mode Change to Output Valid*	—	—	10	μs	
CM06	CHYSTER	Comparator Hysteresis	—	45	—	mV	Hysteresis ON

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at $V_{DD}/2$, while the other input transitions from V_{SS} to V_{DD} .

2: Comparator Hysteresis is available when the CxHYS bit of the CMxCON0 register is enabled.

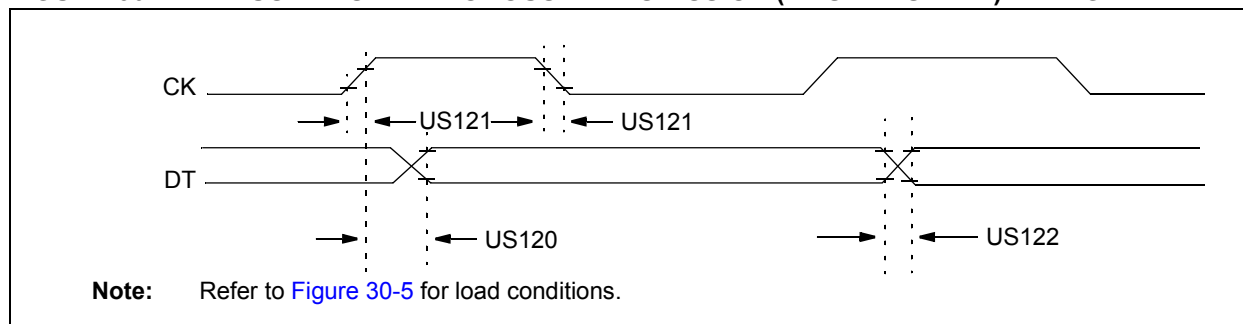
TABLE 30-11: DIGITAL-TO-ANALOG CONVERTER (DAC) SPECIFICATIONS

Operating Conditions: $2.5V < V_{DD} < 5.5V$, $-40^{\circ}C < T_A < +125^{\circ}C$ (unless otherwise stated).							
Param No.	Sym.	Characteristics	Min.	Typ.	Max.	Units	Comments
DAC01*	CLSB	Step Size	—	$V_{DD}/32$	—	V	
DAC02*	CACC	Absolute Accuracy	—	—	± 1/2	LSb	
DAC03*	CR	Unit Resistor Value (R)	—	5000	—	Ω	
DAC04*	CST	Settling Time ⁽¹⁾	—	—	10	μs	

* These parameters are characterized but not tested.

Note 1: Settling time measured while DACR<4:0> transitions from '0000' to '1111'.

FIGURE 30-14: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING



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FIGURE 31-45: I_{PD}, CAPACITIVE SENSING (CPS) MODULE, HIGH-CURRENT RANGE (CPSRM = 0, CPSRNG = 11), PIC16LF1938/9 ONLY

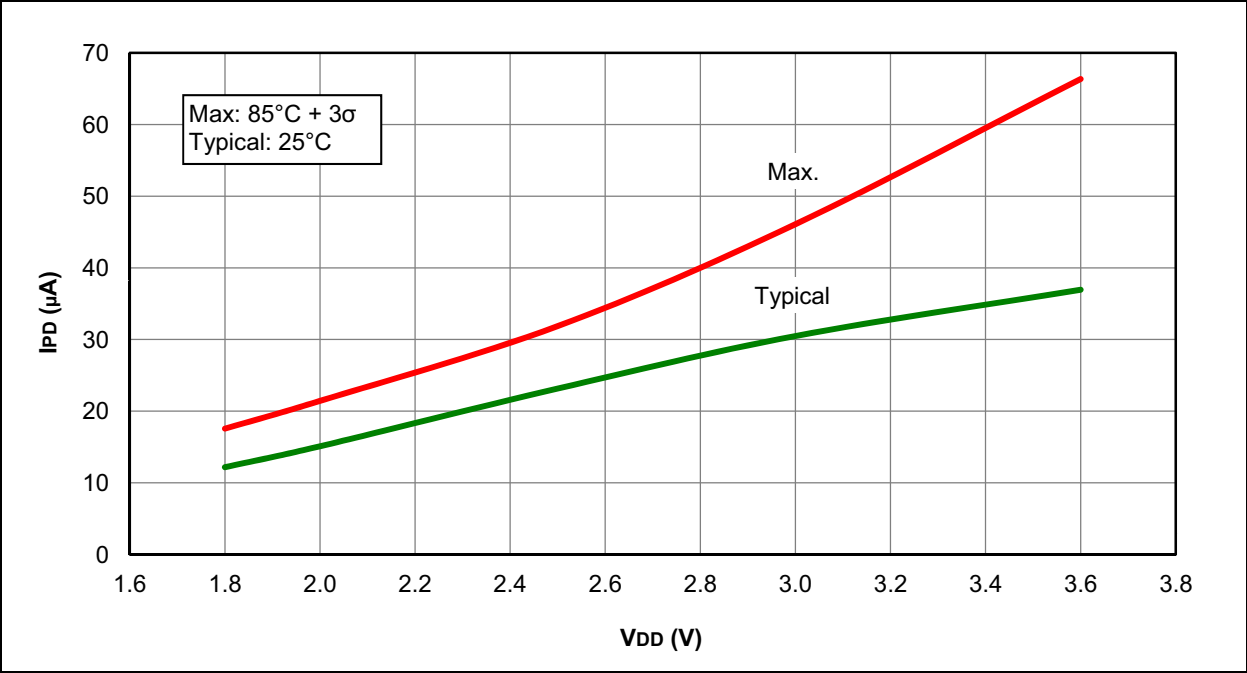
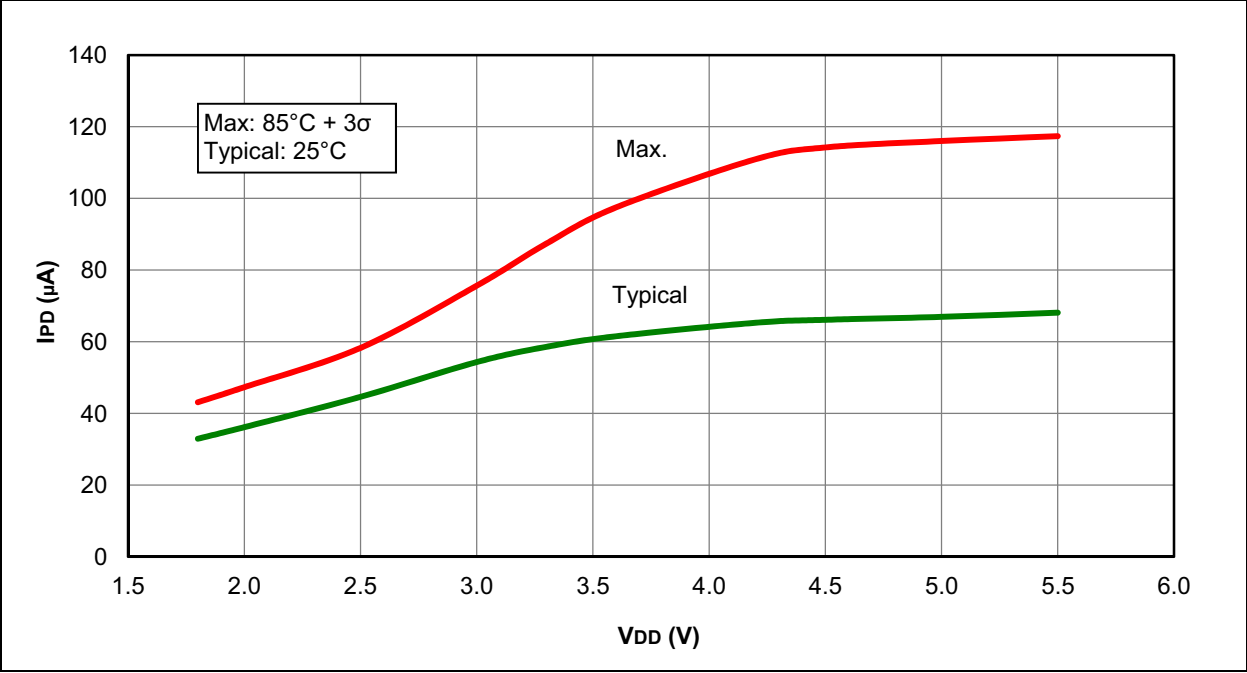


FIGURE 31-46: I_{PD}, CAPACITIVE SENSING (CPS) MODULE, HIGH-CURRENT RANGE (CPSRM = 0, CPSRNG = 11), PIC16F1938/9 ONLY

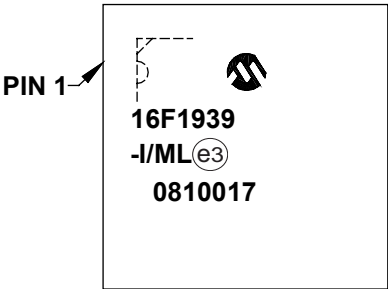
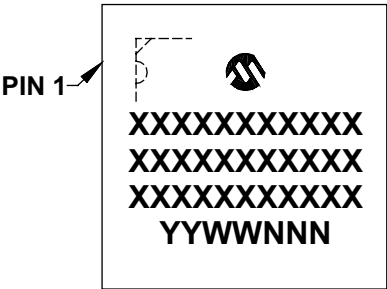


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Package Marking Information (Continued)

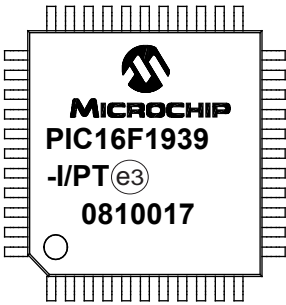
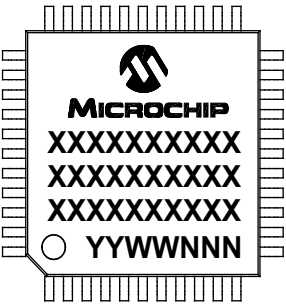
44-Lead QFN (8x8x0.9 mm)

Example



44-Lead TQFP (10x10x1 mm)

Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

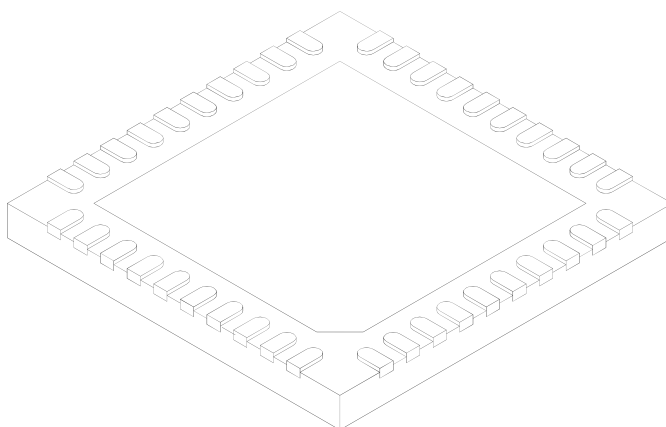
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

* Standard PICmicro® device marking consists of Microchip part number, year code, week code and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

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40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packages>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	40		
Pitch	e	0.40 BSC		
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.127 REF		
Overall Width	E	5.00 BSC		
Exposed Pad Width	E2	3.60	3.70	3.80
Overall Length	D	5.00 BSC		
Exposed Pad Length	D2	3.60	3.70	3.80
Contact Width	b	0.15	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

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U

USART

Synchronous Master Mode

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V

VREF. *SEE* ADC Reference Voltage

W

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NOTES: