

RECERCIC

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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1939t-i-mv

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Name	Function	Input Type	Output Type	Description
RA0/AN0/C12IN0-/C2OUT ⁽¹⁾ /	RA0	TTL	CMOS	General purpose I/O.
SRNQ ⁽¹⁾ / SS⁽¹⁾/VCAP⁽²⁾/SEG12	AN0	AN		A/D Channel 0 input.
	C12IN0-	AN	_	Comparator C1 or C2 negative input.
	C2OUT	_	CMOS	Comparator C2 output.
	SRNQ	_	CMOS	SR Latch inverting output.
	SS	ST		Slave Select input.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator (PIC16F1938/9 only).
	SEG12	_	AN	LCD Analog output.
RA1/AN1/C12IN1-/SEG7	RA1	TTL	CMOS	General purpose I/O.
	AN1	AN		A/D Channel 1 input.
	C12IN1-	AN	_	Comparator C1 or C2 negative input.
	SEG7	_	AN	LCD Analog output.
RA2/AN2/C2IN+/VREF-/	RA2	TTL	CMOS	General purpose I/O.
DACOUT/COM2	AN2	AN		A/D Channel 2 input.
	C2IN+	AN	_	Comparator C2 positive input.
	VREF-	AN	_	A/D Negative Voltage Reference input.
	DACOUT	_	AN	Voltage Reference output.
	COM2		AN	LCD Analog output.
RA3/AN3/C1IN+/VREF+/	RA3	TTL	CMOS	General purpose I/O.
COM3 ⁽³⁾ /SEG15	AN3	AN		A/D Channel 3 input.
	C1IN+	AN	—	Comparator C1 positive input.
	VREF+	AN		A/D Voltage Reference input.
	COM3 ⁽³⁾		AN	LCD Analog output.
	SEG15		AN	LCD Analog output.
RA4/C1OUT/CPS6/T0CKI/SRQ/	RA4	TTL	CMOS	General purpose I/O.
CCP5/SEG4	C10UT		CMOS	Comparator C1 output.
	CPS6	AN		Capacitive sensing input 6.
	TOCKI	ST		Timer0 clock input.
	SRQ		CMOS	SR Latch non-inverting output.
	CCP5	ST	CMOS	Capture/Compare/PWM5.
	SEG4		AN	LCD Analog output.
RA5/AN4/C2OUT ⁽¹⁾ /CPS7/	RA5	TTL	CMOS	General purpose I/O.
SRNQ(''/SS(''/VCAP(2)/SEG5	AN4	AN		A/D Channel 4 input.
	C2OUT	—	CMOS	Comparator C2 output.
	CPS7	AN		Capacitive sensing input 7.
	SRNQ	—	CMOS	SR Latch inverting output.
	SS	ST	—	Slave Select input.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator (PIC16F1938/9 only).
	SEG5	—	AN	LCD Analog output.

TABLE 1-2: PIC16(L)F1938/9 PINOUT DESCRIPTION

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain

TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels XTAL = Crystal

HV = High Voltage I^2C^{TM} = Schmitt Trigger input with I²C levels

Note 1: Pin function is selectable via the APFCON register.

- 2: PIC16F1938/9 devices only.
- 3: PIC16(L)F1938 devices only.
- 4: PORTD is available on PIC16(L)F1939 devices only.
- 5: RE<2:0> are available on PIC16(L)F1939 devices only.

FIGURE 3-1:

PROGRAM MEMORY MAP AND STACK FOR

16 KW PARTS

PC<14:0> CALL, CALLW 15 RETURN, RETLW Interrupt, RETFIE Stack Level 0 Stack Level 1 Stack Level 15 Reset Vector 0000h Interrupt Vector 0004h 0005h Page 0 07FFh 0800h Page 1 0FFFh 1000h On-chip Page 2 Program 17FFh Memory 1800h Page 3 1FFFh Page 4 2000h Page 7 3FFFh 4000h Rollover to Page 0 Rollover to Page 7 7FFFh

3.1.1 READING PROGRAM MEMORY AS DATA

There are two methods of accessing constants in program memory. The first method is to use tables of RETLW instructions. The second method is to set an FSR to point to the program memory.

3.1.1.1 RETLW Instruction

The RETLW instruction can be used to provide access to tables of constants. The recommended way to create such a table is shown in Example 3-1.

EXAMPLE 3-1:	RETTW INSTRUCTION

constants	
BRW	;Add Index in W to
	;program counter to
	;select data
RETLW DATA0	;Index0 data
RETLW DATA1	;Index1 data
RETLW DATA2	
RETLW DATA3	
my_function	
; LOTS OF CODE	
MOVLW DATA_IN	DEX
call constants	
; THE CONSTANT IS	IN W

The BRW instruction makes this type of table very simple to implement. If your code must remain portable with previous generations of microcontrollers, then the BRW instruction is not available so the older table read method must be used.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	, Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 8											
400h ⁽²⁾	INDF0	Addressing (not a phys	this location ical register)	uses contents	s of FSR0H/F	SR0L to addr	ess data mer	mory		XXXX XXXX	****
401h ⁽²⁾	INDF1	Addressing (not a phys	this location ical register)	uses content	s of FSR1H/F	SR1L to addr	ess data mer	nory		XXXX XXXX	XXXX XXXX
402h ⁽²⁾	PCL	Program Co	ounter (PC) L	east Significa	ant Byte					0000 0000	0000 0000
403h ⁽²⁾	STATUS	_	_	_	TO	PD	Z	DC	С	1 1000	q quuu
404h ⁽²⁾	FSR0L	Indirect Dat	ta Memory Ad	Idress 0 Low	Pointer					0000 0000	uuuu uuuu
405h ⁽²⁾	FSR0H	Indirect Dat	ta Memory Ad	ldress 0 High	Pointer					0000 0000	0000 0000
406h ⁽²⁾	FSR1L	Indirect Dat	ta Memory Ad	ldress 1 Low	Pointer					0000 0000	uuuu uuuu
407h ⁽²⁾	FSR1H	Indirect Dat	ta Memory Ad	ldress 1 High	Pointer					0000 0000	0000 0000
408h ⁽²⁾	BSR	_	_	_		I	BSR<4:0>			0 0000	0 0000
409h ⁽²⁾	WREG	Working Re	egister							0000 0000	uuuu uuuu
40Ah ^(1, 2)	PCLATH	_	Write Buffer	for the upper	7 bits of the F	Program Cour	nter			-000 0000	-000 0000
40Bh ⁽²⁾	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000
40Ch	—	Unimpleme	Unimplemented							_	_
40Dh	—	Unimpleme	Unimplemented						_	_	
40Eh	—	Unimpleme	nted							_	_
40Fh	—	Unimpleme	nted							_	_
410h	—	Unimpleme	nted							_	-
411h	—	Unimpleme	nted							_	_
412h	—	Unimpleme	nted							_	_
413h	—	Unimpleme	nted							_	_
414h	—	Unimpleme	nted							_	_
415h	TMR4	Timer 4 Mo	dule Register							0000 0000	0000 0000
416h	PR4	Timer 4 Per	riod Register							1111 1111	1111 1111
417h	T4CON	—		T4OUT	PS<3:0>		TMR4ON	T4CK	PS<1:0>	-000 0000	-000 0000
418h	—	Unimpleme	nted							_	_
419h	—	Unimpleme	nted							_	_
41Ah	—	Unimpleme	Unimplemented							_	_
41Bh	—	Unimpleme	nted							_	_
41Ch	TMR6	Timer 6 Mo	dule Register							0000 0000	0000 0000
41Dh	PR6	Timer 6 Per	riod Register							1111 1111	1111 1111
41Eh	T6CON	—		T6OUT	PS<3:0>		TMR6ON	T6CK	PS<1:0>	-000 0000	-000 0000
41Fh		Unimpleme	ented							_	_

TABLE 3-10: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<14:8>, whose contents are transferred to the upper byte of the program counter.

2: These registers can be addressed from any bank.

3: These registers/bits are not implemented on PIC16(L)F1938 devices, read as '0'.

4: Unimplemented, read as '1'.

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10.6 Register Definitions: Watchdog Control

REGISTER 10-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

U-0	U-0	R/W-0/0	R/W-1/1	R/W-0/0	R/W-1/1	R/W-1/1	R/W-0/0
	—			WDTPS<4:0>			SWDTEN
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplem	ented bit, read	l as '0'	
u = Bit is uncha	anged	x = Bit is unkr	nown	-m/n = Value a	at POR and BC	R/Value at all	other Resets
'1' = Bit is set		'0' = Bit is clea	ared				
bit 7-6	Unimplemen	ted: Read as '	0'				
bit 5-1	WDTPS<4:0>	: Watchdog Ti	mer Period Se	elect bits			
	Bit Value = P	Prescale Rate					
	00000 = 1:3	2 (Interval 1 m	s typ)				
	00001 = 1:6	4 (Interval 2 m	s typ)				
	00010 = 1:1	28 (Interval 4 r	ns typ) ns typ)				
	00011 = 1.2 00100 = 1.5	12 (Interval 16	ms typ)				
	00101 = 1:1	024 (Interval 3	2 ms typ)				
	00110 = 1:2	048 (Interval 6	4 ms typ)				
	00111 = 1:4	096 (Interval 1	28 ms typ)				
	01000 = 1:8	192 (Interval 2	56 ms typ)				
	01001 = 1.1	2768 (Interval	51∠ms typ) 1s typ)				
	01010 = 1:6	5536 (Interval	2s tvp) (Rese	et value)			
	01100 = 1:1	31072 (2 ¹⁷) (Ir	iterval 4s typ)	,			
	01101 = 1:2	62144 (2 ¹⁸) (Ir	iterval 8s typ)				
	01110 = 1:5	24288 (2 ¹⁹) (Ir	iterval 16s typ)			
	01111 = 1:1	$048576(2^{20})($	Interval 32s ty	(p)			
	10000 = 1.2 10001 = 1.4	.097152(2)(.194304(2 ²²)(Interval 128s	γρ) tvn)			
	10010 = 1.4	388608 (2 ²³) (Interval 256s	typ)			
				517			
	10011 = Re	served. Result	s in minimum	interval (1:32)			
	•						
	•						
	11111 = Re:	served. Result	s in minimum	interval (1:32)			
bit 0	SWDTEN: So	oftware Enable/	Disable for W	atchdog Timer b	oit		
	<u>If WDTE<1:0></u>	> = <u>00</u> :					
	This bit is igno	ored.					
	If WDTE<1:0>	<u>> = 01</u> :					
		urned on					
		> = 1x					
	This bit is igno	ored.					
	5						

12.9 PORTD Registers (PIC16(L)F1939 only)

PORTD is a 8-bit wide, bidirectional port. The corresponding data direction register is TRISD (Register 12-14). Setting a TRISD bit (= 1) will make the corresponding PORTD pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISD bit (= 0) will make the corresponding PORTD pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 12-1 shows how to initialize an I/O port.

Reading the PORTD register (Register 12-14) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATD).

Note:	PORTD is	available on	PIC16(L)F1939
	only.		

The TRISD register (Register 12-15) controls the PORTD pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISD register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

12.9.1 ANSELD REGISTER

The ANSELD register (Register 12-17) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELD bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELD bits has no effect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note:	The ANSELD bits default to the Analog
	mode after Reset. To use any pins as
	digital general purpose or peripheral
	inputs, the corresponding ANSEL bits
	must be initialized to '0' by user software.

12.9.2 PORTD FUNCTIONS AND OUTPUT PRIORITIES

Each PORTD pin is multiplexed with other functions. The pins, their combined functions and their output priorities are shown in Table 12-10.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the highest priority.

Analog input and some digital input functions are not included in the list below. These input functions can remain active when the pin is configured as an output. Certain digital input functions override other port functions and are included in priority list.

Pin Name	Function Priority ⁽¹⁾
RD0	COM3 (LCD) RD0
RD1	CCP4 (CCP) RD1
RD2	P2B (CCP) RD2
RD3	SEG16 (LCD) P2C (CCP) RD3
RD4	SEG17 (LCD) P2D (CCP) RD4
RD5	SEG18 (LCD) P1B (CCP) RD5
RD6	SEG19 (LCD) P1C (CCP) RD6
RD7	SEG20 (LCD) P1D (CCP) RD7

TABLE 12-10: PORTD OUTPUT PRIORITY

Note 1: Priority listed from highest to lowest.

14.3 Register Definitions: FVR Control

REGISTER 14-1: FVRCON: FIXED VOLTAGE REFERENCE CONTROL REGISTER

R/W-0/0	0 R-q/q	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
FVREN	FVRRDY ⁽¹⁾	TSEN	TSRNG	CDAF	/R<1:0>	ADFV	R<1:0>
bit 7							bit 0
Lowende							
Legena:	- 1 - 1- 1- 14		L.14				
R = Reada		vv = vvritable	DIT		nented bit, read		
u = Bit is u	inchanged	x = Bit is unki	nown	-n/n = Value a	at POR and BO	R/Value at all c	other Resets
'1' = Bit is	set	'0' = Bit is cle	ared	q = Value dep	pends on condit	ion	
bit 7	FVREN: Fixed 1 = Fixed Vol 0 = Fixed Vol	d Voltage Refe Itage Referenc Itage Referenc	rence Enable e is enabled e is disabled	bit			
bit 6 FVRRDY: Fixed Voltage Reference Ready Flag bit ⁽¹⁾ 1 = Fixed Voltage Reference output is ready for use 0 = Fixed Voltage Reference output is not ready or not enabled							
bit 5	TSEN: Temperature Indicator Enable bit ⁽³⁾ 1 = Temperature Indicator is enabled 0 = Temperature Indicator is disabled						
bit 4	TSRNG: Temperature Indicator Range Selection bit ⁽³⁾ 1 = VOUT = VDD - 4VT (High Range) 0 = VOUT = VDD - 2VT (Low Range)						
bit 3-2 CDAFVR<1:0> : Comparator and DAC Fixed Voltage Reference Selection bit 11 = Comparator and DAC and CPS Fixed Voltage Reference Peripheral output is 4x (4.096V) ⁽²⁾ 10 = Comparator and DAC and CPS Fixed Voltage Reference Peripheral output is 2x (2.048V) ⁽²⁾ 01 = Comparator and DAC and CPS Fixed Voltage Reference Peripheral output is 1x (1.024V) 00 = Comparator and DAC and CPS Fixed Voltage Reference Peripheral output is 1x (1.024V)						(4.096∨) ⁽²⁾ (2.048∨) ⁽²⁾ (1.024∨)	
bit 1-0 ADFVR<1:0>: ADC Fixed Voltage Reference Selection bit 11 = ADC Fixed Voltage Reference Peripheral output is 4x (4.096V) ⁽²⁾ 10 = ADC Fixed Voltage Reference Peripheral output is 2x (2.048V) ⁽²⁾ 01 = ADC Fixed Voltage Reference Peripheral output is 1x (1.024V) 00 = ADC Fixed Voltage Reference Peripheral output is of							
Note 1: 2:	FVRRDY is always Fixed Voltage Refe	s '1' on devices erence output o	with LDO (Pl cannot exceed	IC16F193X). I Vdd.			

3: See Section 16.0 "Temperature Indicator Module" for additional information.

TABLE 14-1: SUMMARY OF REGISTERS ASSOCIATED WITH FIXED VOLTAGE REFERENCE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFV	′R<1:0>	ADFV	R<1:0>	148

Legend: Shaded cells are not used with the Fixed Voltage Reference.

15.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 10-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 10-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESH:ADRESL register pair). Figure 15-1 shows the block diagram of the ADC.

The ADC voltage reference is software selectable to be either internally generated or externally supplied.

FIGURE 15-1: ADC BLOCK DIAGRAM

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.





19.0 SR LATCH

The module consists of a single SR Latch with multiple Set and Reset inputs as well as separate latch outputs. The SR Latch module includes the following features:

- Programmable input selection
- SR Latch output is available externally
- Separate Q and \overline{Q} outputs
- · Firmware Set and Reset

The SR Latch can be used in a variety of analog applications, including oscillator circuits, one-shot circuit, hysteretic controllers, and analog timing applications.

19.1 Latch Operation

The latch is a Set-Reset Latch that does not depend on a clock source. Each of the Set and Reset inputs are active-high. The latch can be Set or Reset by:

- Software control (SRPS and SRPR bits)
- Comparator C1 output (sync_C1OUT)
- Comparator C2 output (sync_C2OUT)
- SRI pin
- Programmable clock (SRCLK)

The SRPS and the SRPR bits of the SRCON0 register may be used to Set or Reset the SR Latch, respectively. The latch is Reset-dominant. Therefore, if both Set and Reset inputs are high, the latch will go to the Reset state. Both the SRPS and SRPR bits are self resetting which means that a single write to either of the bits is all that is necessary to complete a latch Set or Reset operation.

The output from Comparator C1 or C2 can be used as the Set or Reset inputs of the SR Latch. The output of either Comparator can be synchronized to the Timer1 clock source. See **Section 18.0 "Comparator Module"** and **Section 21.0 "Timer1 Module with Gate Control"** for more information.

An external source on the SRI pin can be used as the Set or Reset inputs of the SR Latch.

An internal clock source is available that can periodically Set or Reset the SR Latch. The SRCLK<2:0> bits in the SRCON0 register are used to select the clock source period. The SRSCKE and SRRCKE bits of the SRCON1 register enable the clock source to Set or Reset the SR Latch, respectively.

23.2 Compare Mode

The Compare mode function described in this section is available and identical for CCP modules ECCP1, ECCP2, ECCP3, CCP4 and CCP5.

Compare mode makes use of the 16-bit Timer1 resource. The 16-bit value of the CCPRxH:CCPRxL register pair is constantly compared against the 16-bit value of the TMR1H:TMR1L register pair. When a match occurs, one of the following events can occur:

- Toggle the CCPx output
- · Set the CCPx output
- · Clear the CCPx output
- · Generate a Special Event Trigger
- Generate a Software Interrupt

The action on the pin is based on the value of the CCPxM<3:0> control bits of the CCPxCON register. At the same time, the interrupt flag CCPxIF bit is set.

All Compare modes can generate an interrupt.

Figure 23-2 shows a simplified diagram of the Compare operation.

FIGURE 23-2: COMPARE MODE OPERATION BLOCK DIAGRAM



23.2.1 CCP PIN CONFIGURATION

The user must configure the CCPx pin as an output by clearing the associated TRIS bit.

Also, the CCPx pin function can be moved to alternative pins using the APFCON register. Refer to **Section 12.1 "Alternate Pin Function"** for more details.

Note:	Clearing the CCPxCON register will force
	the CCPx compare output latch to the
	default low level. This is not the PORT I/O
	data latch.

23.2.2 TIMER1 MODE RESOURCE

In Compare mode, Timer1 must be running in either Timer mode or Synchronized Counter mode. The compare operation may not work in Asynchronous Counter mode.

See Section 21.0 "Timer1 Module with Gate Control" for more information on configuring Timer1.

Note: Clocking Timer1 from the system clock (Fosc) should not be used in Compare mode. In order for Compare mode to recognize the trigger event on the CCPx pin, TImer1 must be clocked from the instruction clock (Fosc/4) or from an external clock source.

23.2.3 SOFTWARE INTERRUPT MODE

When Generate Software Interrupt mode is chosen (CCPxM<3:0> = 1010), the CCPx module does not assert control of the CCPx pin (see the CCPxCON register).

23.2.4 SPECIAL EVENT TRIGGER

When Special Event Trigger mode is chosen (CCPxM<3:0> = 1011), the CCPx module does the following:

- Resets Timer1
- · Starts an ADC conversion if ADC is enabled

The CCPx module does not assert control of the CCPx pin in this mode.

The Special Event Trigger output of the CCP occurs immediately upon a match between the TMR1H, TMR1L register pair and the CCPRxH, CCPRxL register pair. The TMR1H, TMR1L register pair is not reset until the next rising edge of the Timer1 clock. The Special Event Trigger output starts an A/D conversion (if the A/D module is enabled). This allows the CCPRxH, CCPRxL register pair to effectively provide a 16-bit programmable period register for Timer1.

TABLE 23-3: SPECIAL EVENT TRIGGER

Device	CCPx/ECCPx				
PIC16F193X/LF193X	CCP5				

Refer to Section 15.2.5 "Special Event Trigger" for more information.

- Note 1: The Special Event Trigger from the CCP module does not set interrupt flag bit TMR1IF of the PIR1 register.
 - 2: Removing the match condition by changing the contents of the CCPRxH and CCPRxL register pair, between the clock edge that generates the Special Event Trigger and the clock edge that generates the Timer1 Reset, will preclude the Reset from occurring.

24.2 SPI Mode Overview

The Serial Peripheral Interface (SPI) bus is a synchronous serial data communication bus that operates in Full-Duplex mode. Devices communicate in a master/slave environment where the master device initiates the communication. A slave device is controlled through a Chip Select known as Slave Select.

The SPI bus specifies four signal connections:

- Serial Clock (SCK)
- Serial Data Out (SDO)
- Serial Data In (SDI)
- Slave Select (SS)

Figure 24-1 shows the block diagram of the MSSP module when operating in SPI mode.

The SPI bus operates with a single master device and one or more slave devices. When multiple slave devices are used, an independent Slave Select connection is required from the master device to each slave device.

Figure 24-4 shows a typical connection between a master device and multiple slave devices.

The master selects only one slave at a time. Most slave devices have tri-state outputs so their output signal appears disconnected from the bus when they are not selected.

Transmissions involve two shift registers, eight bits in size, one in the master and one in the slave. With either the master or the slave device, data is always shifted out one bit at a time, with the Most Significant bit (MSb) shifted out first. At the same time, a new Least Significant bit (LSb) is shifted into the same register.

Figure 24-5 shows a typical connection between two processors configured as master and slave devices.

Data is shifted out of both shift registers on the programmed clock edge and latched on the opposite edge of the clock.

The master device transmits information out on its SDO output pin which is connected to, and received by, the slave's SDI input pin. The slave device transmits information out on its SDO output pin, which is connected to, and received by, the master's SDI input pin.

To begin communication, the master device first sends out the clock signal. Both the master and the slave devices should be configured for the same clock polarity.

The master device starts a transmission by sending out the MSb from its shift register. The slave device reads this bit from that same line and saves it into the LSb position of its shift register.

During each SPI clock cycle, a full-duplex data transmission occurs. This means that while the master device is sending out the MSb from its shift register (on

its SDO pin) and the slave device is reading this bit and saving it as the LSb of its shift register, that the slave device is also sending out the MSb from its shift register (on its SDO pin) and the master device is reading this bit and saving it as the LSb of its shift register.

After eight bits have been shifted out, the master and slave have exchanged register values.

If there is more data to exchange, the shift registers are loaded with new data and the process repeats itself.

Whether the data is meaningful or not (dummy data), depends on the application software. This leads to three scenarios for data transmission:

- Master sends useful data and slave sends dummy data.
- Master sends useful data and slave sends useful data.
- Master sends dummy data and slave sends useful data.

Transmissions may involve any number of clock cycles. When there is no more data to be transmitted, the master stops sending the clock signal and it deselects the slave.

Every slave device connected to the bus that has not been selected through its slave select line must disregard the clock and transmission signals and must not transmit out any data of its own.



FIGURE 24-9: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 0)

FIGURE 24-10: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 1)



When one device is transmitting a logical one, or letting the line float, and a second device is transmitting a logical zero, or holding the line low, the first device can detect that the line is not a logical one. This detection, when used on the SCL line, is called clock stretching. Clock stretching gives slave devices a mechanism to control the flow of data. When this detection is used on the SDA line, it is called arbitration. Arbitration ensures that there is only one master device communicating at any single time.

24.3.1 CLOCK STRETCHING

When a slave device has not completed processing data, it can delay the transfer of more data through the process of Clock Stretching. An addressed slave device may hold the SCL clock line low after receiving or sending a bit, indicating that it is not yet ready to continue. The master that is communicating with the slave will attempt to raise the SCL line in order to transfer the next bit, but will detect that the clock line has not yet been released. Because the SCL connection is open-drain, the slave has the ability to hold that line low until it is ready to continue communicating.

Clock stretching allows receivers that cannot keep up with a transmitter to control the flow of incoming data.

24.3.2 ARBITRATION

Each master device must monitor the bus for Start and Stop bits. If the device detects that the bus is busy, it cannot begin a new message until the bus returns to an Idle state.

However, two master devices may try to initiate a transmission on or about the same time. When this occurs, the process of arbitration begins. Each transmitter checks the level of the SDA data line and compares it to the level that it expects to find. The first transmitter to observe that the two levels do not match, loses arbitration, and must stop transmitting on the SDA line.

For example, if one transmitter holds the SDA line to a logical one (lets it float) and a second transmitter holds it to a logical zero (pulls it low), the result is that the SDA line will be low. The first transmitter then observes that the level of the line is different than expected and concludes that another transmitter is communicating.

The first transmitter to notice this difference is the one that loses arbitration and must stop driving the SDA line. If this transmitter is also a master device, it also must stop driving the SCL line. It then can monitor the lines for a Stop condition before trying to reissue its transmission. In the meantime, the other device that has not noticed any difference between the expected and actual levels on the SDA line continues with its original transmission. It can do so without any complications, because so far, the transmission appears exactly as expected with no other transmitter disturbing the message. Slave Transmit mode can also be arbitrated, when a master addresses multiple slaves, but this is less common.

If two master devices are sending a message to two different slave devices at the address stage, the master sending the lower slave address always wins arbitration. When two master devices send messages to the same slave address, and addresses can sometimes refer to multiple slaves, the arbitration process must continue into the data stage.

Arbitration usually occurs very rarely, but it is a necessary process for proper multi-master support.

24.4 I²C[™] Mode Operation

All MSSP I²C communication is byte oriented and shifted out MSb first. Six SFR registers and 2 interrupt flags interface the module with the PIC[®] microcontroller and user software. Two pins, SDA and SCL, are exercised by the module to communicate with other external I²C devices.

24.4.1 BYTE FORMAT

All communication in 1^2 C is done in 9-bit segments. A byte is sent from a Master to a Slave or vice-versa, followed by an Acknowledge bit sent back. After the eighth falling edge of the SCL line, the device outputting data on the SDA changes that pin to an input and reads in an acknowledge value on the next clock pulse.

The clock signal, SCL, is provided by the master. Data is valid to change while the SCL signal is low, and sampled on the rising edge of the clock. Changes on the SDA line while the SCL line is high define special conditions on the bus, explained below.

24.4.2 DEFINITION OF I²C TERMINOLOGY

There is language and terminology in the description of I^2C communication that have definitions specific to I^2C . That word usage is defined below and may be used in the rest of this document without explanation. This table was adapted from the Philips I^2C specification.

24.4.3 SDA AND SCL PINS

Selection of any I²C mode with the SSPEN bit set, forces the SCL and SDA pins to be open-drain. These pins should be set by the user to inputs by setting the appropriate TRIS bits.

Note: Data is tied to output zero when an I²C mode is enabled.



24.5.6 CLOCK STRETCHING

Clock stretching occurs when a device on the bus holds the SCL line low effectively pausing communication. The slave may stretch the clock to allow more time to handle data or prepare a response for the master device. A master device is not concerned with stretching as anytime it is active on the bus and not transferring data it is stretching. Any stretching done by a slave is invisible to the master software and handled by the hardware that generates SCL.

The CKP bit of the SSPCON1 register is used to control stretching in software. Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. Setting CKP will release SCL and allow more communication.

24.5.6.1 Normal Clock Stretching

Following an \overline{ACK} if the R/ \overline{W} bit of SSPSTAT is set, a read request, the slave hardware will clear CKP. This allows the slave time to update SSPBUF with data to transfer to the master. If the SEN bit of SSPCON2 is set, the slave hardware will always stretch the clock after the \overline{ACK} sequence. Once the slave is ready; CKP is set by software and communication resumes.

- Note 1: The BF bit has no effect on if the clock will be stretched or not. This is different than previous versions of the module that would not stretch the clock, clear CKP, if SSPBUF was read before the ninth falling edge of SCL.
 - 2: Previous versions of the module did not stretch the clock for a transmission if SSPBUF was loaded before the ninth falling edge of SCL. It is now always cleared for read requests.

24.5.6.2 10-bit Addressing Mode

In 10-bit Addressing mode, when the UA bit is set, the clock is always stretched. This is the only time the SCL is stretched without CKP being cleared. SCL is released immediately after a write to SSPADD.

Note:	Previous versions of the module did not
	stretch the clock if the second address byte
	did not match.

24.5.6.3 Byte NACKing

When AHEN bit of SSPCON3 is set; CKP is cleared by hardware after the eighth falling edge of SCL for a received matching address byte. When DHEN bit of SSPCON3 is set; CKP is cleared after the eighth falling edge of SCL for received data.

Stretching after the eighth falling edge of SCL allows the slave to look at the received address or data and decide if it wants to ACK the received data.

24.5.7 CLOCK SYNCHRONIZATION AND THE CKP BIT

Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. However, clearing the CKP bit will not assert the SCL output low until the SCL output is already sampled low. Therefore, the CKP bit will not assert the SCL line until an external I^2C master device has already asserted the SCL line. The SCL output will remain low until the CKP bit is set and all other devices on the I^2C bus have released SCL. This ensures that a write to the CKP bit will not violate the minimum high time requirement for SCL (see Figure 24-23).



FIGURE 24-23: CLOCK SYNCHRONIZATION TIMING

24.6.8 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable bit, ACKEN bit of the SSPCON2 register. When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit are presented on the SDA pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The Baud Rate Generator then counts for one rollover period (TBRG) and the SCL pin is deasserted (pulled high). When the SCL pin is sampled high (clock arbitration), the Baud Rate Generator counts for TBRG. The SCL pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the Baud Rate Generator is turned off and the MSSP module then goes into Idle mode (Figure 24-30).

24.6.8.1 WCOL Status Flag

If the user writes the SSPBUF when an Acknowledge sequence is in progress, then WCOL is set and the contents of the buffer are unchanged (the write does not occur).

24.6.9 STOP CONDITION TIMING

A Stop bit is asserted on the SDA pin at the end of a receive/transmit by setting the Stop Sequence Enable bit, PEN bit of the SSPCON2 register. At the end of a receive/transmit, the SCL line is held low after the falling edge of the ninth clock. When the PEN bit is set, the master will assert the SDA line low. When the SDA line is sampled low, the Baud Rate Generator is reloaded and counts down to '0'. When the Baud Rate Generator times out, the SCL pin will be brought high and one TBRG (Baud Rate Generator rollover count) later, the SDA pin will be deasserted. When the SDA pin is sampled high while SCL is high, the P bit of the SSPSTAT register is set. A TBRG later, the PEN bit is cleared and the SSPIF bit is set (Figure 24-31).

24.6.9.1 WCOL Status Flag

If the user writes the SSPBUF when a Stop sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

FIGURE 24-30: ACKNOWLEDGE SEQUENCE WAVEFORM



FIGURE 24-31: STOP CONDITION RECEIVE OR TRANSMIT MODE



DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$					
Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions
		Program Memory Programming Specifications					
D110	VIHH	Voltage on MCLR/VPP/RE3 pin	8.0	_	9.0	V	(Note 3, Note 4)
D111	IDDP	Supply Current during Programming	—	—	10	mA	
D112		VDD for Bulk Erase	2.7	_	VDD max.	V	
D113	VPEW	VDD for Write or Row Erase	Vdd min.	_	V _{DD} max.	V	
D114	IPPPGM	Current on MCLR/VPP during Erase/ Write	_	1.0	_	mA	
D115	IDDPGM	Current on VDD during Erase/Write	—	5.0		mA	
		Data EEPROM Memory					
D116	ED	Byte Endurance	100K	—	—	E/W	-40°C to +85°C
D117	Vdrw	VDD for Read/Write	Vdd min.	—	VDD max.	V	
D118	TDEW	Erase/Write Cycle Time	—	4.0	5.0	ms	
D119	TRETD	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated
D120	TREF	Number of Total Erase/Write Cycles before Refresh ⁽²⁾	1M	10M	—	E/W	-40°C to +85°C
		Program Flash Memory					
D121	Eр	Cell Endurance	10K	—	—	E/W	-40°C to +85°C (Note 1)
D122	Vprw	VDD for Read/Write	Vdd min.	—	VDD max.	V	
D123	Tiw	Self-timed Write Cycle Time	—	2	2.5	ms	
D124	TRETD	Characteristic Retention	_	40	_	Year	Provided no other specifications are violated

30.5 Memory Programming Requirements

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Self-write and Block Erase.

2: Refer to Section 11.2 "Using the Data EEPROM" for a more detailed discussion on data EEPROM endurance.

3: Required only if single-supply programming is disabled.

4: The MPLAB ICD 2 does not support variable VPP output. Circuitry to limit the MPLAB ICD 2 VPP voltage must be placed between the MPLAB ICD 2 and target system when programming or debugging with the MPLAB ICD 2.

TABLE 30-10: COMPARATOR SPECIFICATIONS

Operating Conditions: 1.8V < VDD < 5.5V, -40°C < TA < +125°C (unless otherwise stated).								
Param No.	Sym.	Characteristics	Min.	Тур.	Max.	Units	Comments	
CM01	VIOFF	Input Offset Voltage		±7.5	±60	mV	High-Power mode, Viсм = Vpp/2	
CM02	VICM	Input Common Mode Voltage	0	_	Vdd	V		
CM03	CMRR	Common Mode Rejection Ratio		50		dB		
CM04A		Response Time Rising Edge	_	400	800	ns	High-Power mode	
CM04B	Тогео	Response Time Falling Edge		200	400	ns	High-Power mode	
CM04C	TRESP	Response Time Rising Edge		1200		ns	Low-Power mode	
CM04D		Response Time Falling Edge		550		ns	Low-Power mode	
CM05	Тмс2о∨	Comparator Mode Change to Output Valid*			10	μS		
CM06	CHYSTER	Comparator Hysteresis	_	45	-	mV	Hysteresis ON	

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at VDD/2, while the other input transitions from Vss to VDD.

2: Comparator Hysteresis is available when the CxHYS bit of the CMxCON0 register is enabled.

TABLE 30-11: DIGITAL-TO-ANALOG CONVERTER (DAC) SPECIFICATIONS

Operating Conditions: $2.5V < V_{DD} < 5.5V$, $-40^{\circ}C < T_A < +125^{\circ}C$ (unless otherwise stated).							
Param No.	Sym.	Characteristics	Min.	Тур.	Max.	Units	Comments
DAC01*	Clsb	Step Size	—	VDD/32	_	V	
DAC02*	CACC	Absolute Accuracy	_	—	± 1/2	LSb	
DAC03*	CR	Unit Resistor Value (R)	_	5000		Ω	
DAC04*	CST	Settling Time ⁽¹⁾	—	—	10	μS	

* These parameters are characterized but not tested.

Note 1: Settling time measured while DACR<4:0> transitions from '0000' to '1111'.

FIGURE 30-14: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING





FIGURE 31-56: Vol VS. IoL OVER TEMPERATURE, VDD = 1.8V

