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#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16f1939t-i-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic16f1939t-i-pt</a>

# PIC16(L)F1938/9

**TABLE 1-2: PIC16(L)F1938/9 PINOUT DESCRIPTION (CONTINUED)**

Name	Function	Input Type	Output Type	Description
RA6/OSC2/CLKOUT/VCAP <sup>(2)</sup> /SEG1	RA6	TTL	CMOS	General purpose I/O.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKOUT	—	CMOS	Fosc/4 output.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator (PIC16F1938/9 only).
	SEG1	—	AN	LCD Analog output.
RA7/OSC1/CLKIN/SEG2	RA7	TTL	CMOS	General purpose I/O.
	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
	CLKIN	CMOS	—	External clock input (EC mode).
	SEG2	—	AN	LCD Analog output.
RB0/AN12/CPS0/CCP4/SRI/INT/SEG0	RB0	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN12	AN	—	A/D Channel 12 input.
	CPS0	AN	—	Capacitive sensing input 0.
	CCP4	ST	CMOS	Capture/Compare/PWM4.
	SRI	—	ST	SR Latch input.
	INT	ST	—	External interrupt.
	SEG0	—	AN	LCD analog output.
RB1/AN10/C12IN3-/CPS1/P1C/VLCD1	RB1	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN10	AN	—	A/D Channel 10 input.
	C12IN3-	AN	—	Comparator C1 or C2 negative input.
	CPS1	AN	—	Capacitive sensing input 1.
	P1C	—	CMOS	PWM output.
	VLCD1	AN	—	LCD analog input.
RB2/AN8/CPS2/P1B/VLCD2	RB2	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN8	AN	—	A/D Channel 8 input.
	CPS2	AN	—	Capacitive sensing input 2.
	P1B	—	CMOS	PWM output.
	VLCD2	AN	—	LCD analog input.
RB3/AN9/C12IN2-/CPS3/CCP2 <sup>(1)</sup> /P2A <sup>(1)</sup> /VLCD3	RB3	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN9	AN	—	A/D Channel 9 input.
	C12IN2-	AN	—	Comparator C1 or C2 negative input.
	CPS3	AN	—	Capacitive sensing input 3.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
	P2A	—	CMOS	PWM output.
	VLCD3	AN	—	LCD analog input.

**Legend:** AN = Analog input or output    CMOS = CMOS compatible input or output    OD = Open Drain  
TTL = TTL compatible input    ST = Schmitt Trigger input with CMOS levels    XTAL = Crystal  
HV = High Voltage    I<sup>2</sup>C™ = Schmitt Trigger input with I<sup>2</sup>C levels

- Note** 1: Pin function is selectable via the APFCON register.  
2: PIC16F1938/9 devices only.  
3: PIC16(L)F1938 devices only.  
4: PORTD is available on PIC16(L)F1939 devices only.  
5: RE<2:0> are available on PIC16(L)F1939 devices only.

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**TABLE 3-10: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets	
Bank 6												
300h <sup>(2)</sup>	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx	
301h <sup>(2)</sup>	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx	
302h <sup>(2)</sup>	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000	
303h <sup>(2)</sup>	STATUS	—	—	—	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	---1 1000	---q quuu	
304h <sup>(2)</sup>	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu	
305h <sup>(2)</sup>	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000	
306h <sup>(2)</sup>	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu	
307h <sup>(2)</sup>	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000	
308h <sup>(2)</sup>	BSR	—	—	—	BSR<4:0>					---0 0000	---0 0000	
309h <sup>(2)</sup>	WREG	Working Register								0000 0000	uuuu uuuu	
30Ah <sup>(1, 2)</sup>	PCLATH	—	Write Buffer for the upper 7 bits of the Program Counter								-000 0000	-000 0000
30Bh <sup>(2)</sup>	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000	
30Ch	—	Unimplemented								—	—	
30Dh	—	Unimplemented								—	—	
30Eh	—	Unimplemented								—	—	
30Fh	—	Unimplemented								—	—	
310h	—	Unimplemented								—	—	
311h	CCPR3L	Capture/Compare/PWM Register 3 (LSB)								xxxx xxxx	uuuu uuuu	
312h	CCPR3H	Capture/Compare/PWM Register 3 (MSB)								xxxx xxxx	uuuu uuuu	
313h	CCP3CON	P3M<1:0>		DC3B<1:0>		CCP3M<1:0>				0000 0000	0000 0000	
314h	PWM3CON	P3RSEN	P3DC<6:0>								0000 0000	0000 0000
315h	CCP3AS	CCP3ASE	CCP3AS2	CCP3AS1	CCP3AS0	PSS3AC<1:0>		PSS3BD<1:0>		0000 0000	0000 0000	
316h	PSTR3CON	—	—	—	STR3SYNC	STR3D	STR3C	STR3B	STR3A	---0 0001	---0 0001	
317h	—	Unimplemented								—	—	
318h	CCPR4L	Capture/Compare/PWM Register 4 (LSB)								xxxx xxxx	uuuu uuuu	
319h	CCPR4H	Capture/Compare/PWM Register 4 (MSB)								xxxx xxxx	uuuu uuuu	
31Ah	CCP4CON	—	—	DC4B<1:0>		CCP4M<3:0>				--00 0000	--00 0000	
31Bh	—	Unimplemented								—	—	
31Ch	CCPR5L	Capture/Compare/PWM Register 5 (LSB)								xxxx xxxx	uuuu uuuu	
31Dh	CCPR5H	Capture/Compare/PWM Register 5 (MSB)								xxxx xxxx	uuuu uuuu	
31Eh	CCP5CON	—	—	DC5B<1:0>		CCP5M<3:0>				--00 0000	--00 0000	
31Fh	—	Unimplemented								—	—	

**Legend:** x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.  
Shaded locations are unimplemented, read as '0'.

- Note** 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<14:8>, whose contents are transferred to the upper byte of the program counter.  
2: These registers can be addressed from any bank.  
3: These registers/bits are not implemented on PIC16(L)F1938 devices, read as '0'.  
4: Unimplemented, read as '1'.

## 5.2.2.3 Internal Oscillator Frequency Adjustment

The 500 kHz internal oscillator is factory calibrated. This internal oscillator can be adjusted in software by writing to the OSCTUNE register (Register 5-3). Since the HFINTOSC and MFINTOSC clock sources are derived from the 500 kHz internal oscillator a change in the OSCTUNE register value will apply to both.

The default value of the OSCTUNE register is '0'. The value is a 6-bit two's complement number. A value of 1Fh will provide an adjustment to the maximum frequency. A value of 20h will provide an adjustment to the minimum frequency.

When the OSCTUNE register is modified, the oscillator frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

## 5.2.2.4 LFINTOSC

The Low-Frequency Internal Oscillator (LFINTOSC) is an uncalibrated 31 kHz internal clock source.

The output of the LFINTOSC connects to a multiplexer (see Figure 5-1). Select 31 kHz, via software, using the IRCF<3:0> bits of the OSCCON register. See Section 5.2.2.7 "Internal Oscillator Clock Switch Timing" for more information. The LFINTOSC is also the frequency for the Power-up Timer (PWRT), Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

The LFINTOSC is enabled by selecting 31 kHz (IRCF<3:0> bits of the OSCCON register = 000) as the system clock source (SCS bits of the OSCCON register = 1x), or when any of the following are enabled:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired LF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to '1x'

Peripherals that use the LFINTOSC are:

- Power-up Timer (PWRT)
- Watchdog Timer (WDT)
- Fail-Safe Clock Monitor (FSCM)

The Low Frequency Internal Oscillator Ready bit (LFIOFR) of the OSCSTAT register indicates when the LFINTOSC is running.

## 5.2.2.5 Internal Oscillator Frequency Selection

The system clock speed can be selected via software using the Internal Oscillator Frequency Select bits IRCF<3:0> of the OSCCON register.

The output of the 16 MHz HFINTOSC and 31 kHz LFINTOSC connects to a postscaler and multiplexer (see Figure 5-1). The Internal Oscillator Frequency Select bits IRCF<3:0> of the OSCCON register select the frequency output of the internal oscillators. One of the following frequencies can be selected via software:

- HFINTOSC
  - 32 MHz (requires 4X PLL)
  - 16 MHz
  - 8 MHz
  - 4 MHz
  - 2 MHz
  - 1 MHz
  - 500 kHz (Default after Reset)
  - 250 kHz
  - 125 kHz
  - 62.5 kHz
  - 31.25 kHz
- LFINTOSC
  - 31 kHz

**Note:** Following any Reset, the IRCF<3:0> bits of the OSCCON register are set to '0111' and the frequency selection is set to 500 kHz. The user can modify the IRCF bits to select a different frequency.

The IRCF<3:0> bits of the OSCCON register allow duplicate selections for some frequencies. These duplicate choices can offer system design trade-offs. Lower power consumption can be obtained when changing oscillator sources for a given frequency. Faster transition times can be obtained between frequency changes that use the same oscillator source.

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## 6.4 MCLR

The  $\overline{\text{MCLR}}$  is an optional external input that can reset the device. The  $\overline{\text{MCLR}}$  function is controlled by the MCLRE bit of Configuration Words and the LVP bit of Configuration Words (Table 6-2).

TABLE 6-2:  $\overline{\text{MCLR}}$  CONFIGURATION

MCLRE	LVP	$\overline{\text{MCLR}}$
0	0	Disabled
1	0	Enabled
x	1	Enabled

### 6.4.1 MCLR ENABLED

When  $\overline{\text{MCLR}}$  is enabled and the pin is held low, the device is held in Reset. The  $\overline{\text{MCLR}}$  pin is connected to VDD through an internal weak pull-up.

The device has a noise filter in the  $\overline{\text{MCLR}}$  Reset path. The filter will detect and ignore small pulses.

**Note:** A Reset does not drive the  $\overline{\text{MCLR}}$  pin low.

### 6.4.2 MCLR DISABLED

When  $\overline{\text{MCLR}}$  is disabled, the pin functions as a general purpose input and the internal weak pull-up is under software control. See Section 12.11 “[PORTE Registers](#)” for more information.

## 6.5 Watchdog Timer (WDT) Reset

The Watchdog Timer generates a Reset if the firmware does not issue a `CLRWD` instruction within the time-out period. The  $\overline{\text{TO}}$  and  $\overline{\text{PD}}$  bits in the STATUS register are changed to indicate the WDT Reset. See Section 10.0 “[Watchdog Timer](#)” for more information.

## 6.6 RESET Instruction

A `RESET` instruction will cause a device Reset. The RI bit in the PCON register will be set to ‘0’. See Table 6-4 for default conditions after a `RESET` instruction has occurred.

## 6.7 Stack Overflow/Underflow Reset

The device can reset when the Stack Overflows or Underflows. The STKOVF or STKUNF bits of the PCON register indicate the Reset condition. These Resets are enabled by setting the STVREN bit in Configuration Words. See Section 3.5.2 “[Overflow/Underflow Reset](#)” for more information.

## 6.8 Programming Mode Exit

Upon exit of Programming mode, the device will behave as if a POR had just occurred.

## 6.9 Power-Up Timer

The Power-up Timer optionally delays device execution after a BOR or POR event. This timer is typically used to allow VDD to stabilize before allowing the device to start running.

The Power-up Timer is controlled by the  $\overline{\text{PWRTE}}$  bit of Configuration Words.

## 6.10 Start-up Sequence

Upon the release of a POR or BOR, the following must occur before the device will begin executing:

1. Power-up Timer runs to completion (if enabled).
2. Oscillator start-up timer runs to completion (if required for oscillator source).
3.  $\overline{\text{MCLR}}$  must be released (if enabled).

The total time-out will vary based on oscillator configuration and Power-up Timer configuration. See Section 5.0 “[Oscillator Module \(With Fail-Safe Clock Monitor\)](#)” for more information.

The Power-up Timer and oscillator start-up timer run independently of  $\overline{\text{MCLR}}$  Reset. If  $\overline{\text{MCLR}}$  is kept low long enough, the Power-up Timer and oscillator start-up timer will expire. Upon bringing  $\overline{\text{MCLR}}$  high, the device will begin execution immediately (see Figure 6-3). This is useful for testing purposes or to synchronize more than one device operating in parallel.

## REGISTER 7-4: PIE3: PERIPHERAL INTERRUPT ENABLE REGISTER 3

U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	U-0
—	CCP5IE	CCP4IE	CCP3IE	TMR6IE	—	TMR4IE	—
bit 7						bit 0	

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

- bit 7      **Unimplemented:** Read as '0'
- bit 6      **CCP5IE:** CCP5 Interrupt Enable bit
  - 1 = Enables the CCP5 interrupt
  - 0 = Disables the CCP5 interrupt
- bit 5      **CCP4IE:** CCP4 Interrupt Enable bit
  - 1 = Enables the CCP4 interrupt
  - 0 = Disables the CCP4 interrupt
- bit 4      **CCP3IE:** CCP3 Interrupt Enable bit
  - 1 = Enables the CCP3 interrupt
  - 0 = Disables the CCP3 interrupt
- bit 3      **TMR6IE:** TMR6 to PR6 Match Interrupt Enable bit
  - 1 = Enables the TMR6 to PR6 Match interrupt
  - 0 = Disables the TMR6 to PR6 Match interrupt
- bit 2      **Unimplemented:** Read as '0'
- bit 1      **TMR4IE:** TMR4 to PR4 Match Interrupt Enable bit
  - 1 = Enables the TMR4 to PR4 Match interrupt
  - 0 = Disables the TMR4 to PR4 Match interrupt
- bit 0      **Unimplemented:** Read as '0'

**Note:** Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

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## REGISTER 12-5: ANSELA: PORTA ANALOG SELECT REGISTER

U-0	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **ANSA<5:0>:** Analog Select between Analog or Digital Function on pins RA<5:0>, respectively

0 = Digital I/O. Pin is assigned to port or digital special function.

1 = Analog input. Pin is assigned as analog input<sup>(1)</sup>. Digital input buffer disabled.

**Note 1:** When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

**TABLE 12-9: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON	—	CCP3SEL	T1GSEL	P2BSEL	SRNQSEL	C2OUTSEL	SSSEL	CCP2SEL	<a href="#">123</a>
CCPxCON	PxM<1:0>		DCxB<1:0>		CCPxM<3:0>				<a href="#">228</a>
LATC	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	<a href="#">134</a>
LCDCON	LCDEN	SLPEN	WERR	—	CS<1:0>		LMUX<1:0>		<a href="#">327</a>
LCDSE0	SE7	SE6	SE5	SE4	SE3	SE2	SE1	SE0	<a href="#">331</a>
LCDSE1	SE15	SE14	SE13	SE12	SE11	SE10	SE9	SE8	<a href="#">331</a>
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	<a href="#">134</a>
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	<a href="#">297</a>
SSPCON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				<a href="#">283</a>
SSPSTAT	SMP	CKE	D/A	P	S	R/W	UA	BF	<a href="#">282</a>
T1CON	TMR1CS<1:0>		T1CKPS<1:0>		T1OSCEN	T1SYNC	—	TMR1ON	<a href="#">197</a>
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	<a href="#">296</a>
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	<a href="#">134</a>

**Legend:** x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTC.



## 12.11 PORTE Registers

PORTE is a 4-bit wide, bidirectional port. The corresponding data direction register is TRISE. Setting a TRISE bit (= 1) will make the corresponding PORTE pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISE bit (= 0) will make the corresponding PORTE pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). The exception is RE3, which is input only and its TRIS bit will always read as '1'. [Example 12-1](#) shows how to initialize an I/O port.

Reading the PORTE register ([Register 12-18](#)) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATE). RE3 reads '0' when MCLRE = 1.

**Note:** RE<2:0> and TRISE<2:0> pins are available on PIC16(L)F1939 only.

### 12.11.1 ANSELE REGISTER

The ANSELE register ([Register 12-21](#)) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELE bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELE bits has no effect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

The TRISE register ([Register 12-19](#)) controls the PORTE pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISE register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

**Note:** The ANSELE bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

### 12.11.2 PORTE FUNCTIONS AND OUTPUT PRIORITIES

Each PORTE pin is multiplexed with other functions. The pins, their combined functions and their output priorities are shown in [Table 12-12](#).

When multiple outputs are enabled, the actual pin control goes to the peripheral with the lowest number in the following lists.

Analog input and some digital input functions are not included in the list below. These input functions can remain active when the pin is configured as an output. Certain digital input functions override other port functions and are included in priority list.

**TABLE 12-12: PORTE OUTPUT PRIORITY**

Pin Name	Function Priority <sup>(1)</sup>
RE0	SEG21 (LCD) CCP3/P3A (CCP) RE0
RE1	SEG22 (LCD) P3B (CCP) RE1
RE2	SEG23 (LCD) CCP5 (CCP) RE2

**Note 1:** Priority listed from highest to lowest.

FIGURE 17-1: DIGITAL-TO-ANALOG CONVERTER BLOCK DIAGRAM

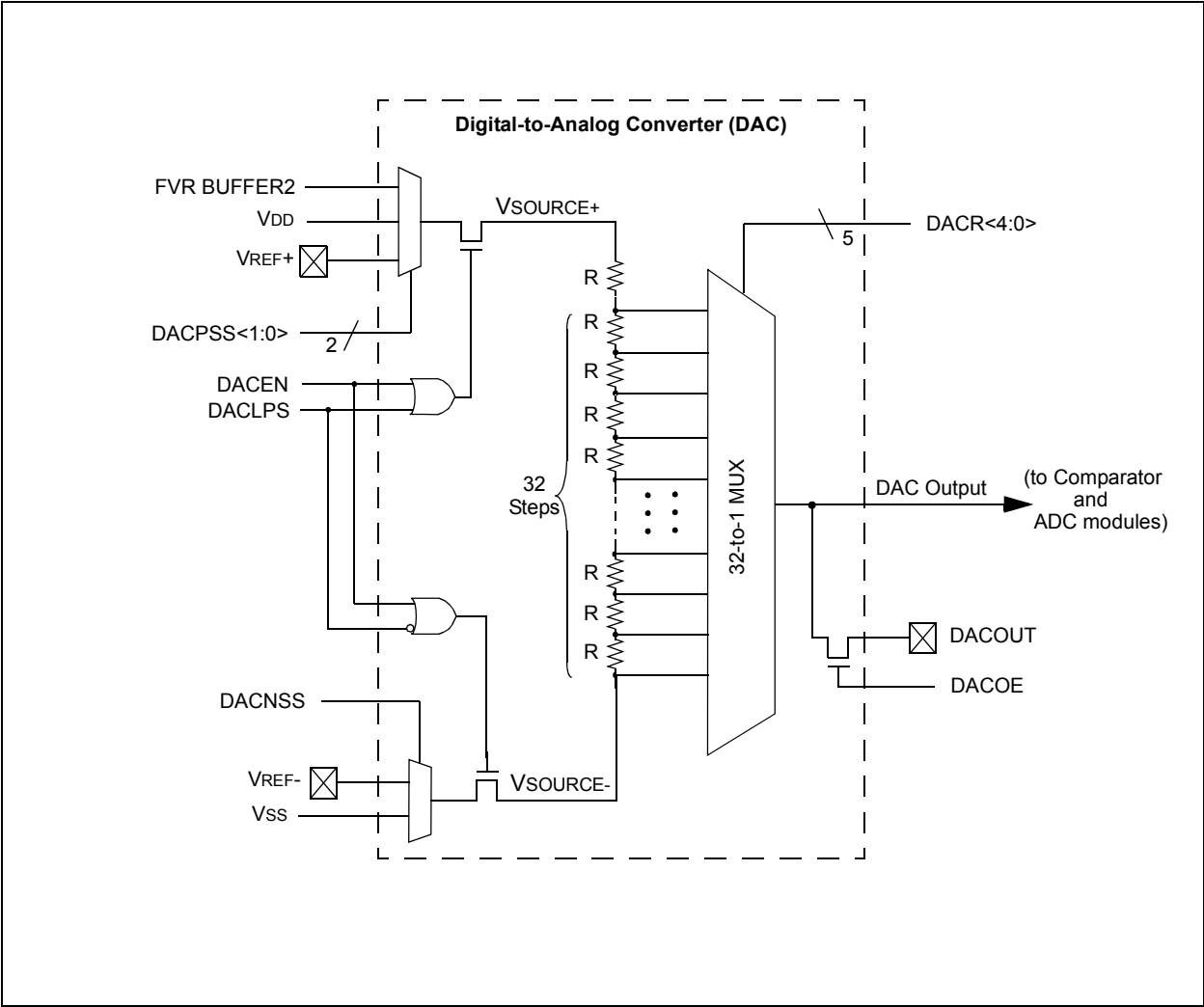
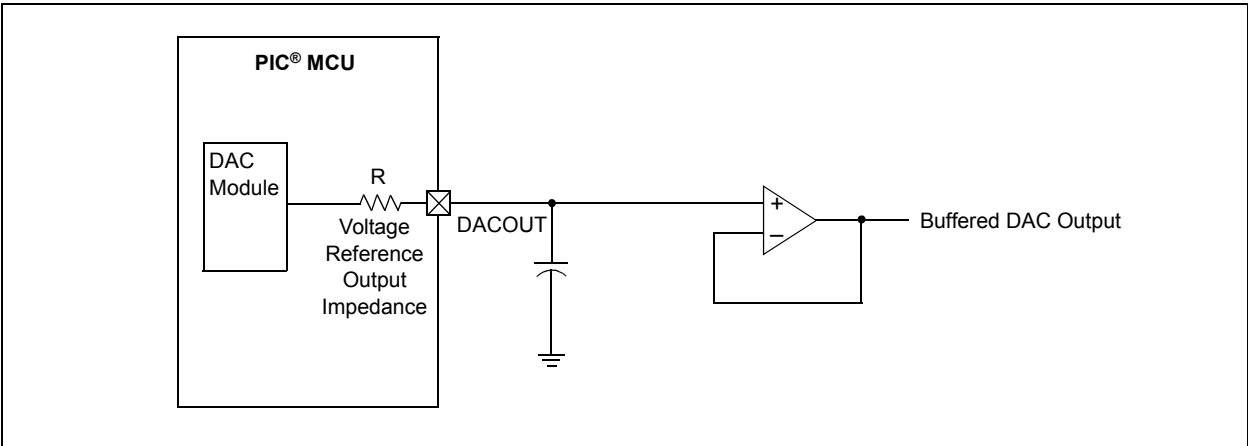


FIGURE 17-2: VOLTAGE REFERENCE OUTPUT BUFFER EXAMPLE



## 18.7 Comparator Negative Input Selection

The CxNCH<1:0> bits of the CMxCON0 register direct one of four analog pins to the comparator inverting input.

**Note:** To use CxIN+ and CxINx- pins as analog input, the appropriate bits must be set in the ANSEL register and the corresponding TRIS bits must also be set to disable the output drivers.

## 18.8 Comparator Response Time

The comparator output is indeterminate for a period of time after the change of an input source or the selection of a new reference voltage. This period is referred to as the response time. The response time of the comparator differs from the settling time of the voltage reference. Therefore, both of these times must be considered when determining the total response time to a comparator input change. See the Comparator and Voltage Reference Specifications in [Section 30.0 “Electrical Specifications”](#) for more details.

## 18.9 Interaction with ECCP Logic

The C1 and C2 comparators can be used as general purpose comparators. Their outputs can be brought out to the C1OUT and C2OUT pins. When the ECCP Auto-Shutdown is active it can use one or both comparator signals. If auto-restart is also enabled, the comparators can be configured as a closed loop analog feedback to the ECCP, thereby, creating an analog controlled PWM.

**Note:** When the Comparator module is first initialized the output state is unknown. Upon initialization, the user should verify the output state of the comparator prior to relying on the result, primarily when using the result in connection with other peripheral features, such as the ECCP Auto-Shutdown mode.

## 18.10 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in [Figure 18-3](#). Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to VDD and VSS. The analog input, therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

A maximum source impedance of 10 kΩ is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

**Note 1:** When reading a PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as an analog input, according to the input specification.

**2:** Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.

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## 23.1 Capture Mode

The Capture mode function described in this section is available and identical for CCP modules ECCP1, ECCP2, ECCP3, CCP4 and CCP5.

Capture mode makes use of the 16-bit Timer1 resource. When an event occurs on the CCPx pin, the 16-bit CCPRxH:CCPRxL register pair captures and stores the 16-bit value of the TMR1H:TMR1L register pair, respectively. An event is defined as one of the following and is configured by the CCPxM<3:0> bits of the CCPxCON register:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

When a capture is made, the Interrupt Request Flag bit CCPxIF of the PIRx register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPRxH, CCPRxL register pair is read, the old captured value is overwritten by the new captured value.

Figure 23-1 shows a simplified diagram of the Capture operation.

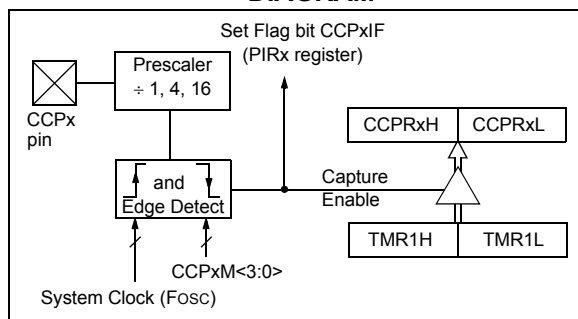
### 23.1.1 CCP PIN CONFIGURATION

In Capture mode, the CCPx pin should be configured as an input by setting the associated TRIS control bit.

Also, the CCPx pin function can be moved to alternative pins using the APFCON register. Refer to Section 12.1 “Alternate Pin Function” for more details.

**Note:** If the CCPx pin is configured as an output, a write to the port can cause a capture condition.

**FIGURE 23-1: CAPTURE MODE OPERATION BLOCK DIAGRAM**



### 23.1.2 TIMER1 MODE RESOURCE

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

See Section 21.0 “Timer1 Module with Gate Control” for more information on configuring Timer1.

### 23.1.3 SOFTWARE INTERRUPT MODE

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCPxIE interrupt enable bit of the PIRx register clear to avoid false interrupts. Additionally, the user should clear the CCPxIF interrupt flag bit of the PIRx register following any change in Operating mode.

**Note:** Clocking Timer1 from the system clock (Fosc) should not be used in Capture mode. In order for Capture mode to recognize the trigger event on the CCPx pin, Timer1 must be clocked from the instruction clock (Fosc/4) or from an external clock source.

### 23.1.4 CCP PRESCALER

There are four prescaler settings specified by the CCPxM<3:0> bits of the CCPxCON register. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another does not clear the prescaler and may generate a false interrupt. To avoid this unexpected operation, turn the module off by clearing the CCPxCON register before changing the prescaler. Example 23-1 demonstrates the code to perform this function.

#### EXAMPLE 23-1: CHANGING BETWEEN CAPTURE PRESCALERS

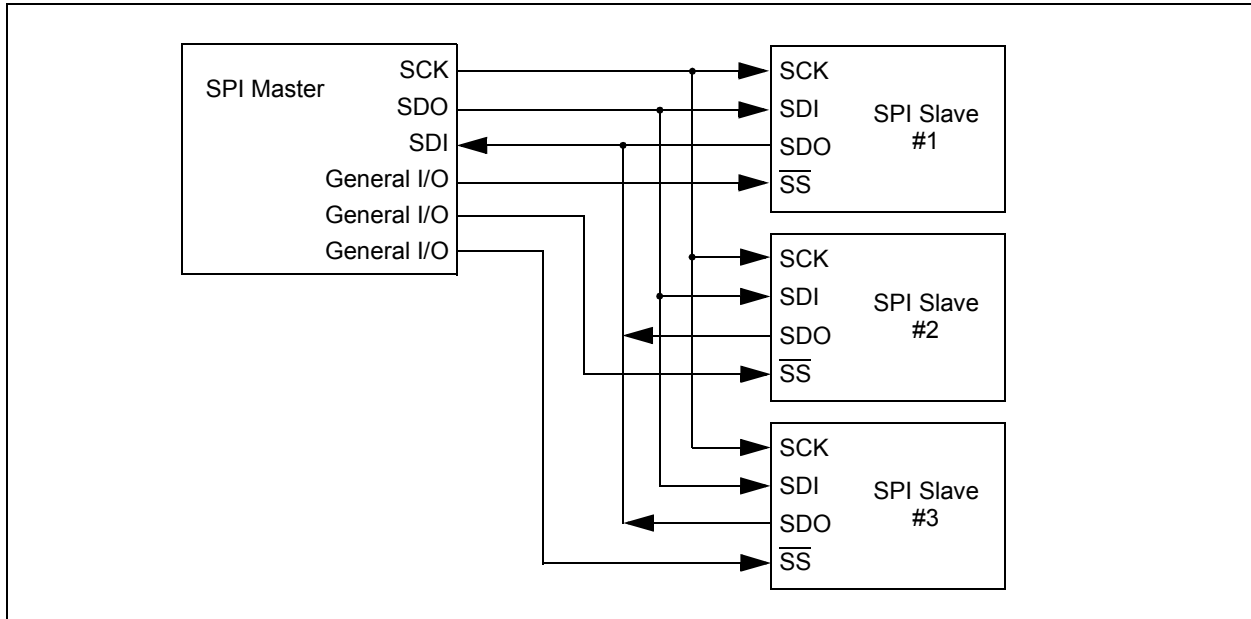
```
BANKSEL CCPxCON    ;Set Bank bits to point
                    ;to CCPxCON
CLRf    CCPxCON    ;Turn CCP module off
MOVLW   NEW_CAPT_PS;Load the W reg with
                    ;the new prescaler
MOVWF   CCPxCON    ;move value and CCP ON
                    ;Load CCPxCON with this
                    ;value
```

### 23.1.5 CAPTURE DURING SLEEP

Capture mode depends upon the Timer1 module for proper operation. There are two options for driving the Timer1 module in Capture mode. It can be driven by the instruction clock (Fosc/4), or by an external clock source.

When Timer1 is clocked by Fosc/4, Timer1 will not increment during Sleep. When the device wakes from Sleep, Timer1 will continue from its previous state. Capture mode will operate during Sleep when Timer1 is clocked by an external clock source.

**FIGURE 24-4: SPI MASTER AND MULTIPLE SLAVE CONNECTION**



## 24.2.1 SPI MODE REGISTERS

The MSSP module has five registers for SPI mode operation. These are:

- MSSP STATUS register (SSPSTAT)
- MSSP Control Register 1 (SSPCON1)
- MSSP Control Register 3 (SSPCON3)
- MSSP Data Buffer register (SSPBUF)
- MSSP Address register (SSPADD)
- MSSP Shift register (SSPSR)  
(Not directly accessible)

SSPCON1 and SSPSTAT are the control and STATUS registers in SPI mode operation. The SSPCON1 register is readable and writable. The lower six bits of the SSPSTAT are read-only. The upper two bits of the SSPSTAT are read/write.

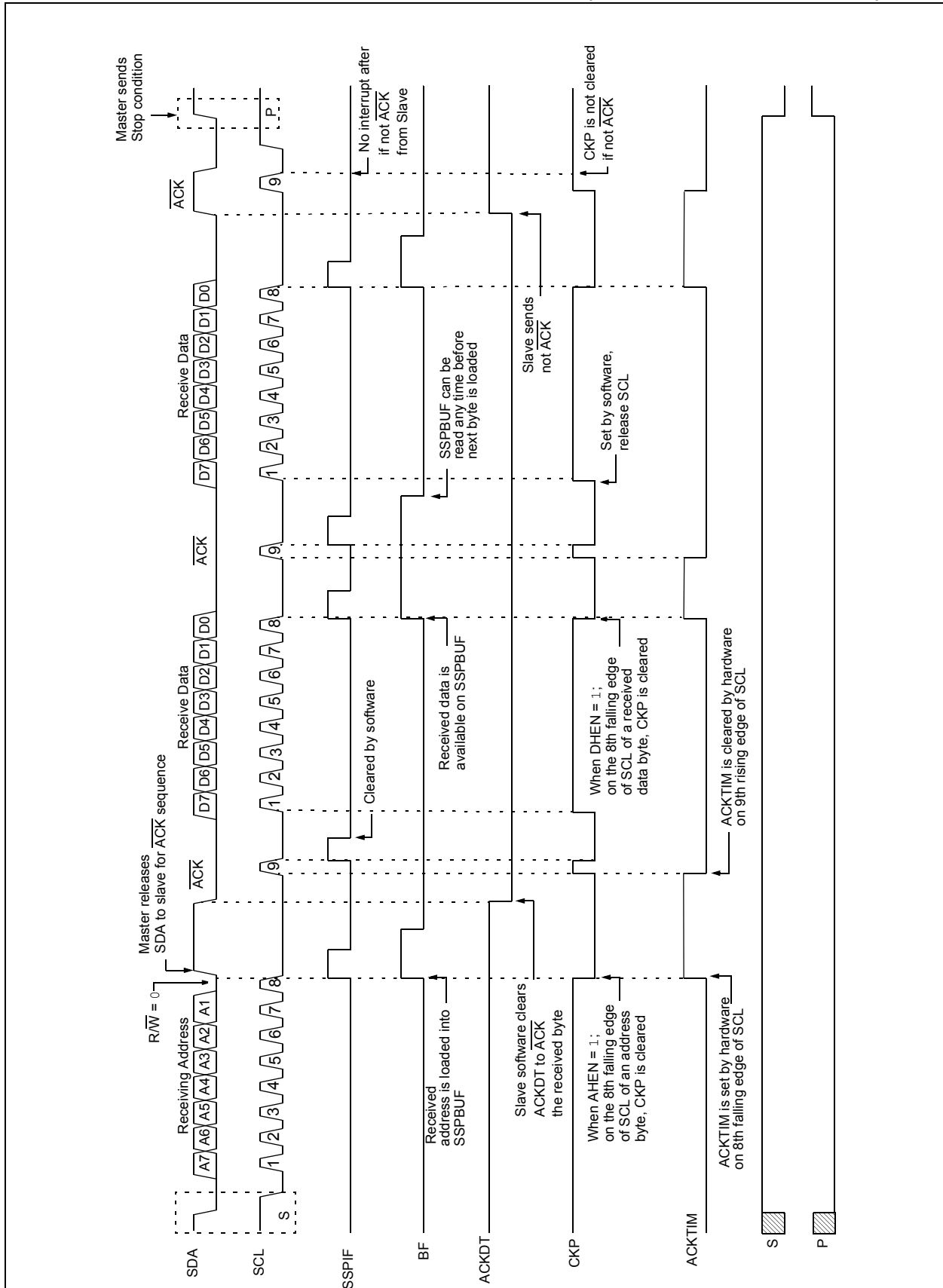
In one SPI Master mode, SSPADD can be loaded with a value used in the Baud Rate Generator. More information on the Baud Rate Generator is available in [Section 24.7 “Baud Rate Generator”](#).

SSPSR is the shift register used for shifting data in and out. SSPBUF provides indirect access to the SSPSR register. SSPBUF is the buffer register to which data bytes are written, and from which data bytes are read.

In receive operations, SSPSR and SSPBUF together create a buffered receiver. When SSPSR receives a complete byte, it is transferred to SSPBUF and the SSPIF interrupt is set.

During transmission, the SSPBUF is not buffered. A write to SSPBUF will write to both SSPBUF and SSPSR.

**FIGURE 24-17: I<sup>2</sup>C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 1, DHEN = 1)**





## 26.9 Register Definitions: CPS Control

**REGISTER 26-1: CPSCON0: CAPACITIVE SENSING CONTROL REGISTER 0**

R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R-0/0	R/W-0/0
CPSON	CPSRM	—	—	CPSRNG<1:0>	CPSOUT	T0XCS	
bit 7						bit 0	

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

- bit 7      **CPSON:** CPS Module Enable bit  
1 = CPS module is enabled  
0 = CPS module is disabled
- bit 6      **CPSRM:** Capacitive Sensing Reference Mode bit  
1 = Capacitive Sensing module is in Variable Voltage Reference mode.  
0 = Capacitive Sensing module is in Fixed Variable Voltage Reference mode.
- bit 5-4      **Unimplemented:** Read as '0'
- bit 3-2      **CPSRNG<1:0>:** Capacitive Sensing Current Range  
If CPSRM = 0 (Fixed Voltage Reference mode):  
00 = Oscillator is off  
01 = Oscillator is in Low-Current Range  
10 = Oscillator is in Medium-Current Range  
11 = Oscillator is in High-Current Range  
  
If CPSRM = 1 (Variable Voltage Reference mode):  
00 = Oscillator is on. Noise Detection mode.  
01 = Oscillator is in Low-Current Range.  
10 = Oscillator is in Medium-Current Range.  
11 = Oscillator is in High-Current Range.
- bit 1      **CPSOUT:** Capacitive Sensing Oscillator Status bit  
1 = Oscillator is sourcing current (Current flowing out of the pin)  
0 = Oscillator is sinking current (Current flowing into the pin)
- bit 0      **T0XCS:** Timer0 External Clock Source Select bit  
If TMR0CS = 1:  
The T0XCS bit controls which clock external to the core/Timer0 module supplies Timer0:  
1 = Timer0 clock source is the capacitive sensing oscillator, CPSCCLK  
0 = Timer0 clock source is the T0CKI pin  
If TMR0CS = 0:  
Timer0 clock source is controlled by the core/Timer0 module and is Fosc/4



# PIC16(L)F1938/9

## RETFIE Return from Interrupt

**Syntax:** [ *label* ] RETFIE

**Operands:** None

**Operation:** TOS → PC,  
1 → GIE

**Status Affected:** None

**Description:** Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a 2-cycle instruction.

**Words:** 1

**Cycles:** 2

**Example:**

```

RETFIE
After Interrupt
PC = TOS
GIE = 1

```

## RETLW Return with literal in W

**Syntax:** [ *label* ] RETLW *k*

**Operands:**  $0 \leq k \leq 255$

**Operation:** *k* → (W);  
TOS → PC

**Status Affected:** None

**Description:** The W register is loaded with the 8-bit literal '*k*'. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.

**Words:** 1

**Cycles:** 2

**Example:**

```

CALL TABLE;W contains table
;offset value
• ;W now has table value
•
•
ADDWF PC ;W = offset
RETLW k1 ;Begin table
RETLW k2 ;
•
•
•
RETLW kn ; End of table

```

**TABLE**

**Before Instruction**  
W = 0x07

**After Instruction**  
W = value of k8

## RETURN Return from Subroutine

**Syntax:** [ *label* ] RETURN

**Operands:** None

**Operation:** TOS → PC

**Status Affected:** None

**Description:** Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a 2-cycle instruction.

## RLF Rotate Left f through Carry

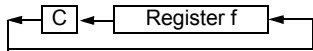
**Syntax:** [ *label* ] RLF *f*,*d*

**Operands:**  $0 \leq f \leq 127$   
*d* ∈ [0,1]

**Operation:** See description below

**Status Affected:** C

**Description:** The contents of register '*f*' are rotated one bit to the left through the Carry flag. If '*d*' is '0', the result is placed in the W register. If '*d*' is '1', the result is stored back in register '*f*'.



**Words:** 1

**Cycles:** 1

**Example:**

```

RLF    REG1,0

```

**Before Instruction**

REG1	=	1110 0110
C	=	0

**After Instruction**

REG1	=	1110 0110
W	=	1100 1100
C	=	1

# PIC16(L)F1938/9

## 30.4 DC Characteristics: PIC16(L)F1938/39-I/E (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
D101*	COSC2	Capacitive Loading Specs on Output Pins					
		OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101A*	Cio	All I/O pins	—	—	50	pF	
D102 D102A		VCAP Capacitor Charging					
		Charging current	—	200	—	μA	
		Source/sink capability when charging complete	—	0.0	—	mA	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

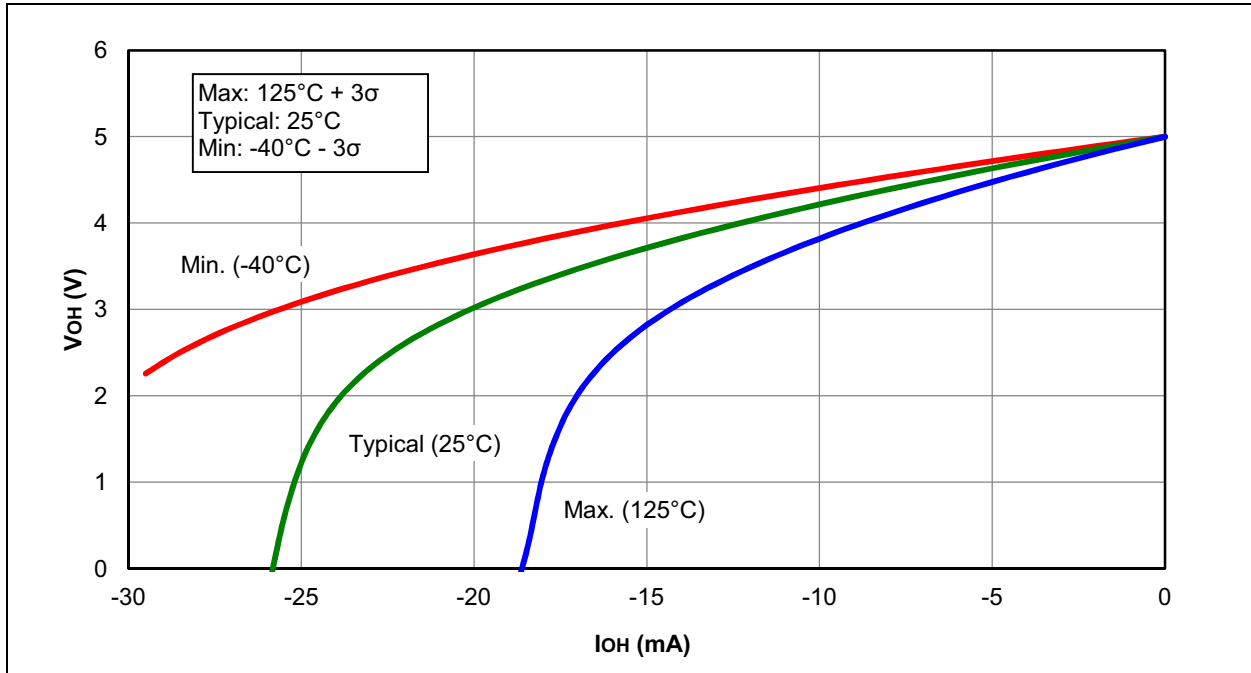
**Note 1:** In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

**2:** Negative current is defined as current sourced by the pin.

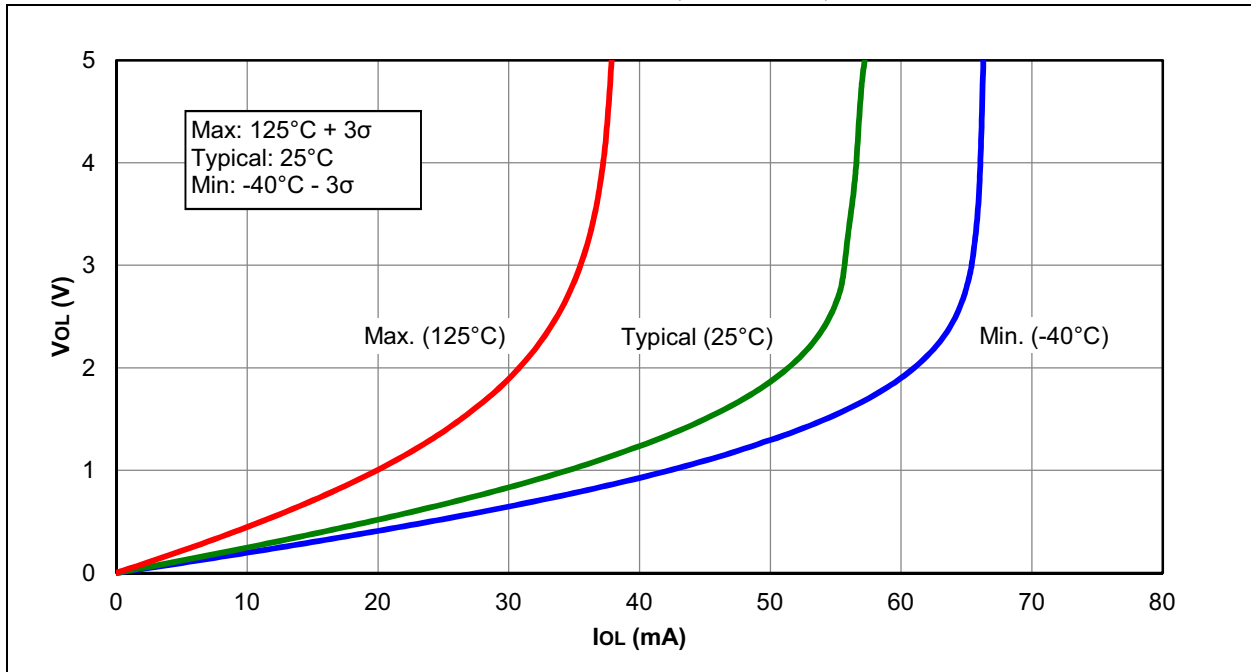
**3:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**4:** Including OSC2 in CLKOUT mode.

**FIGURE 31-51:  $V_{OH}$  VS.  $I_{OH}$  OVER TEMPERATURE,  $V_{DD} = 5.0V$ , PIC16F1938/9 ONLY**



**FIGURE 31-52:  $V_{OL}$  VS.  $I_{OL}$  OVER TEMPERATURE,  $V_{DD} = 5.0V$ , PIC16F1938/9 ONLY**



## 32.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/  
MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for  
Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICKit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards,  
Evaluation Kits and Starter Kits
- Third-party development tools

## 32.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

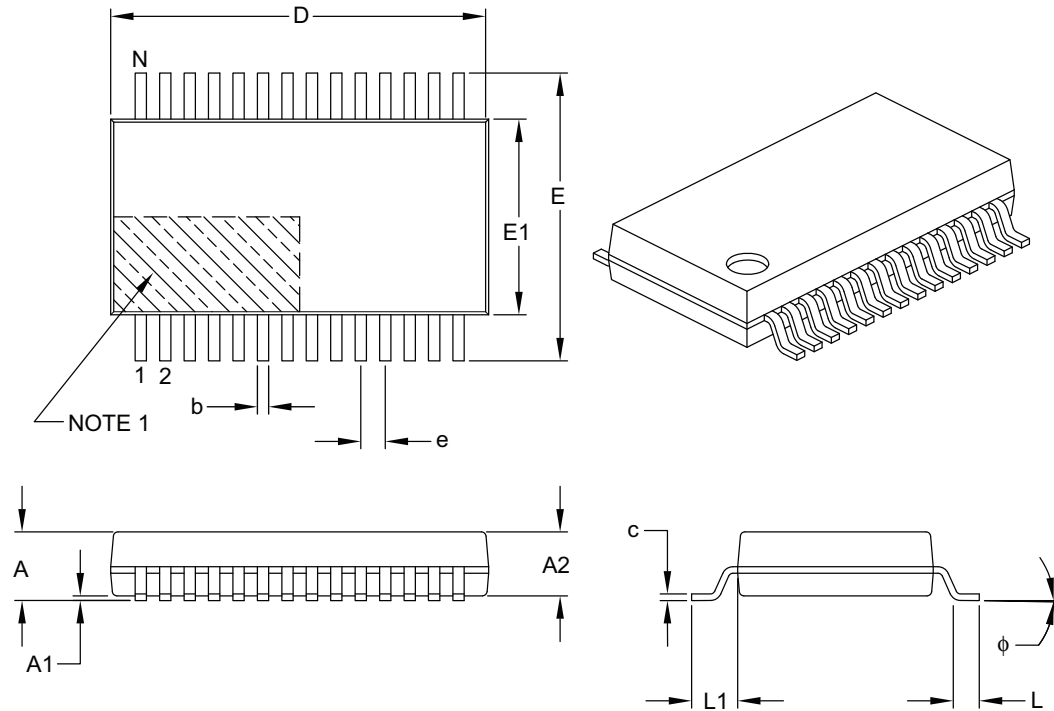
- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

## 28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1	1.25 REF		
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B