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#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1939-e-p">https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1939-e-p</a>

# PIC16(L)F1938/9

## Peripheral Features (Continued):

- Master Synchronous Serial Port (MSSP) with SPI and I<sup>2</sup>C™ with:
  - 7-bit address masking
  - SMBus/PMBus™ compatibility
  - Auto-wake-up on start
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART):
  - RS-232, RS-485 and LIN compatible
  - Auto-Baud Detect
- SR Latch (555 Timer):
  - Multiple Set/Reset input options
  - Emulates 555 Timer applications

- 2 Comparators:
  - Rail-to-rail inputs/outputs
  - Power mode control
  - Software enable hysteresis
- Voltage Reference module:
  - Fixed Voltage Reference (FVR) with 1.024V, 2.048V and 4.096V output levels
  - 5-bit rail-to-rail resistive DAC with positive and negative reference selection

## PIC16(L)F193X/194X FAMILY TYPES

Device	Data Sheet Index	Program Memory Flash (words)	Data EEPROM (bytes)	Data SRAM (bytes)	I/O's <sup>(2)</sup>	10-bit ADC (ch)	Cap Sense (ch)	Comparators	Timers (8/16-bit)	EUSART	MSSP (I <sup>2</sup> C™/SPI)	ECCP	CCP	LCD (Com/Seg/Total)	Debug <sup>(1)</sup>	XLP
PIC16(L)F1933	(1)	4096	256	256	25	11	8	2	4/1	1	1	3	2	4/16/60 <sup>(3)</sup>	I/H/E	Y
PIC16(L)F1934	(2)	4096	256	256	36	14	16	2	4/1	1	1	3	2	4/24/96	I/H/E	Y
PIC16(L)F1936	(2)	8192	256	512	25	11	8	2	4/1	1	1	3	2	4/16/60 <sup>(3)</sup>	I/H/E	Y
PIC16(L)F1937	(2)	8192	256	512	36	14	16	2	4/1	1	1	3	2	4/24/96	I/H/E	Y
PIC16(L)F1938	(3)	16384	256	1024	25	11	8	2	4/1	1	1	3	2	4/16/60 <sup>(3)</sup>	I/H/E	Y
PIC16(L)F1939	(3)	16384	256	1024	36	14	16	2	4/1	1	1	3	2	4/24/96	I/H/E	Y
PIC16(L)F1946	(4)	8192	256	512	54	17	17	3	4/1	2	2	3	2	4/46/184	I	Y
PIC16(L)F1947	(4)	16384	256	1024	54	17	17	3	4/1	2	2	3	2	4/46/184	I	Y

**Note 1:** Debugging Methods: (I) – Integrated On-Chip; (H) – using Debug Header; (E) – using Emulation Header.

**Note 2:** One pin is input-only.

**Note 3:** COM3 and SEG15 share the same physical pin, therefore SEG15 is not available when using 1/4 multiplex displays.

**Data Sheet Index:** (Unshaded devices are described in this document.)

- 1: DS41575 [PIC16\(L\)F1933 Data Sheet, 28-Pin Flash, 8-bit Microcontrollers.](#)
- 2: DS41364 [PIC16\(L\)F1934/6/7 Data Sheet, 28/40/44-Pin Flash, 8-bit Microcontrollers.](#)
- 3: DS41574 [PIC16\(L\)F1938/9 Data Sheet, 28/40/44-Pin Flash, 8-bit Microcontrollers.](#)
- 4: DS41414 [PIC16\(L\)F1946/1947 Data Sheet, 64-Pin Flash, 8-bit Microcontrollers.](#)

**Note:** For other small form-factor package availability and marking information, please visit <http://www.microchip.com/packaging> or contact your local sales office.

# PIC16(L)F1938/9

**TABLE 3-10: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets	
Bank 5												
280h <sup>(2)</sup>	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx	
281h <sup>(2)</sup>	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx	
282h <sup>(2)</sup>	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000	
283h <sup>(2)</sup>	STATUS	—	—	—	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	---1 1000	---q quuu	
284h <sup>(2)</sup>	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu	
285h <sup>(2)</sup>	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000	
286h <sup>(2)</sup>	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu	
287h <sup>(2)</sup>	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000	
288h <sup>(2)</sup>	BSR	—	—	—	BSR<4:0>					---0 0000	---0 0000	
289h <sup>(2)</sup>	WREG	Working Register								0000 0000	uuuu uuuu	
28Ah <sup>(1, 2)</sup>	PCLATH	—	Write Buffer for the upper 7 bits of the Program Counter								-000 0000	-000 0000
28Bh <sup>(2)</sup>	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000	
28Ch	—	Unimplemented								—	—	
28Dh	—	Unimplemented								—	—	
28Eh	—	Unimplemented								—	—	
28Fh	—	Unimplemented								—	—	
290h	—	Unimplemented								—	—	
291h	CCPR1L	Capture/Compare/PWM Register 1 (LSB)								xxxx xxxx	uuuu uuuu	
292h	CCPR1H	Capture/Compare/PWM Register 1 (MSB)								xxxx xxxx	uuuu uuuu	
293h	CCP1CON	P1M<1:0>		DC1B<1:0>		CCP1M<3:0>				0000 0000	0000 0000	
294h	PWM1CON	P1RSEN	P1DC<6:0>								0000 0000	0000 0000
295h	CCP1AS	CCP1ASE	CCP1AS2	CCP1AS1	CCP1AS0	PSS1AC<1:0>		PSS1BD<1:0>		0000 0000	0000 0000	
296h	PSTR1CON	—	—	—	STR1SYNC	STR1D	STR1C	STR1B	STR1A	---0 0001	---0 0001	
297h	—	Unimplemented								—	—	
298h	CCPR2L	Capture/Compare/PWM Register 2 (LSB)								xxxx xxxx	uuuu uuuu	
299h	CCPR2H	Capture/Compare/PWM Register 2 (MSB)								xxxx xxxx	uuuu uuuu	
29Ah	CCP2CON	P2M<1:0>		DC2B<1:0>		CCP2M<3:0>				0000 0000	0000 0000	
29Bh	PWM2CON	P2RSEN	P2DC<6:0>								0000 0000	0000 0000
29Ch	CCP2AS	CCP2ASE	CCP2AS2	CCP2AS1	CCP2AS0	PSS2AC<1:0>		PSS2BD<1:0>		0000 0000	0000 0000	
29Dh	PSTR2CON	—	—	—	STR2SYNC	STR2D	STR2C	STR2B	STR2A	---0 0001	---0 0001	
29Eh	CCPTMRS0	C4TSEL1	C4TSEL0	C3TSEL1	C3TSEL0	C2TSEL1	C2TSEL0	C1TSEL1	C1TSEL0	0000 0000	0000 0000	
29Fh	CCPTMRS1	—	—	—	—	—	—	C5TSEL<1:0>		---- --00	---- --00	

**Legend:** x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.  
Shaded locations are unimplemented, read as '0'.

- Note 1:** The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<14:8>, whose contents are transferred to the upper byte of the program counter.
- 2:** These registers can be addressed from any bank.
- 3:** These registers/bits are not implemented on PIC16(L)F1938 devices, read as '0'.
- 4:** Unimplemented, read as '1'.

## 3.5 Stack

All devices have a 16-level x 15-bit wide hardware stack (refer to Figure 3-1). The stack space is not part of either program or data space. The PC is PUSHed onto the stack when `CALL` or `CALLW` instructions are executed or an interrupt causes a branch. The stack is POPed in the event of a `RETURN`, `RETLW` or a `RETFIE` instruction execution. `PCLATH` is not affected by a `PUSH` or `POP` operation.

The stack operates as a circular buffer if the `STVREN` bit is programmed to '0' (Configuration Words). This means that after the stack has been PUSHed sixteen times, the seventeenth PUSH overwrites the value that was stored from the first PUSH. The eighteenth PUSH overwrites the second PUSH (and so on). The `STKOVF` and `STKUNF` flag bits will be set on an Overflow/Underflow, regardless of whether the Reset is enabled.

**Note 1:** There are no instructions/mnemonics called `PUSH` or `POP`. These are actions that occur from the execution of the `CALL`, `CALLW`, `RETURN`, `RETLW` and `RETFIE` instructions or the vectoring to an interrupt address.

### 3.5.1 ACCESSING THE STACK

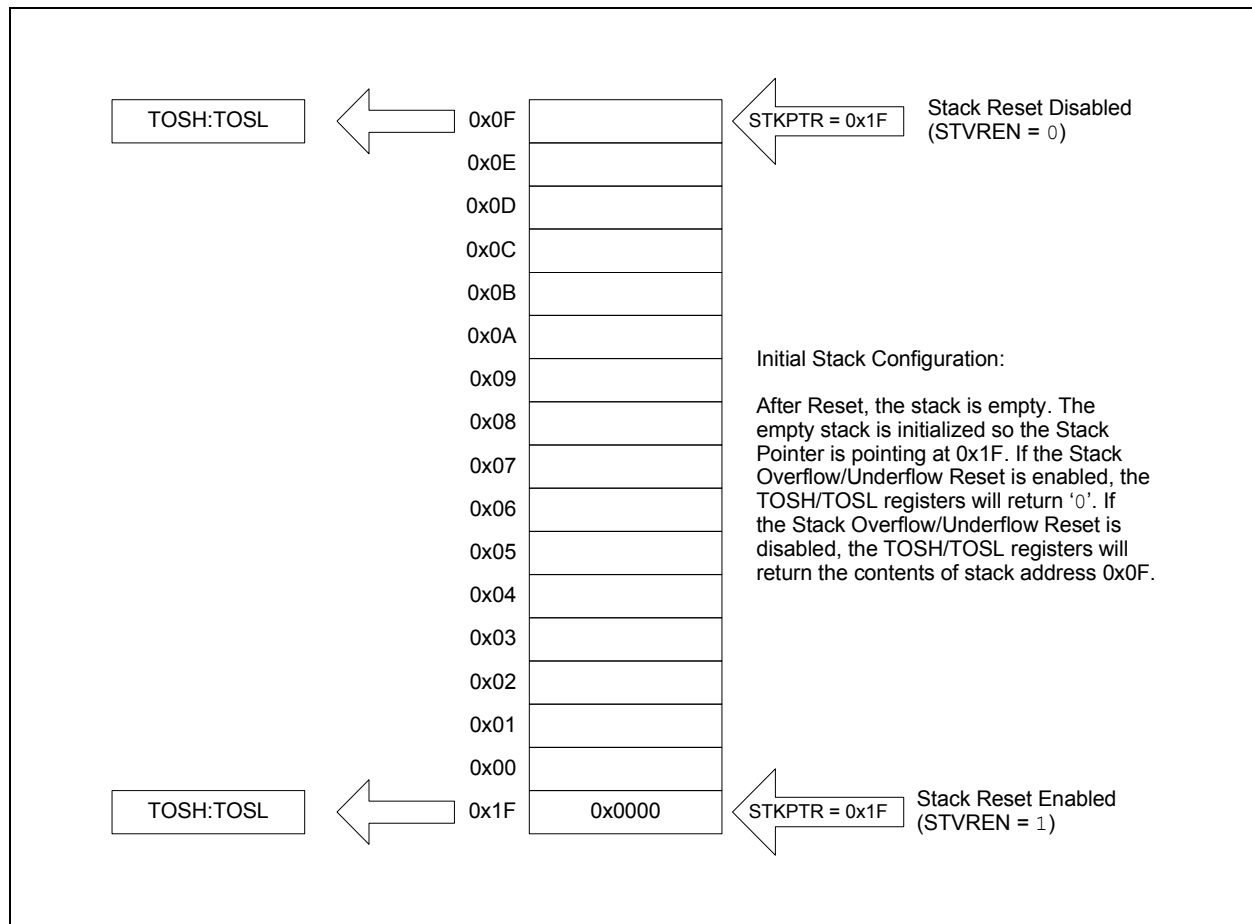
The stack is available through the `TOSH`, `TOSL` and `STKPTR` registers. `STKPTR` is the current value of the Stack Pointer. `TOSH:TOSL` register pair points to the TOP of the stack. Both registers are read/writable. `TOS` is split into `TOSH` and `TOSL` due to the 15-bit size of the PC. To access the stack, adjust the value of `STKPTR`, which will position `TOSH:TOSL`, then read/write to `TOSH:TOSL`. `STKPTR` is 5 bits to allow detection of overflow and underflow.

**Note:** Care should be taken when modifying the `STKPTR` while interrupts are enabled.

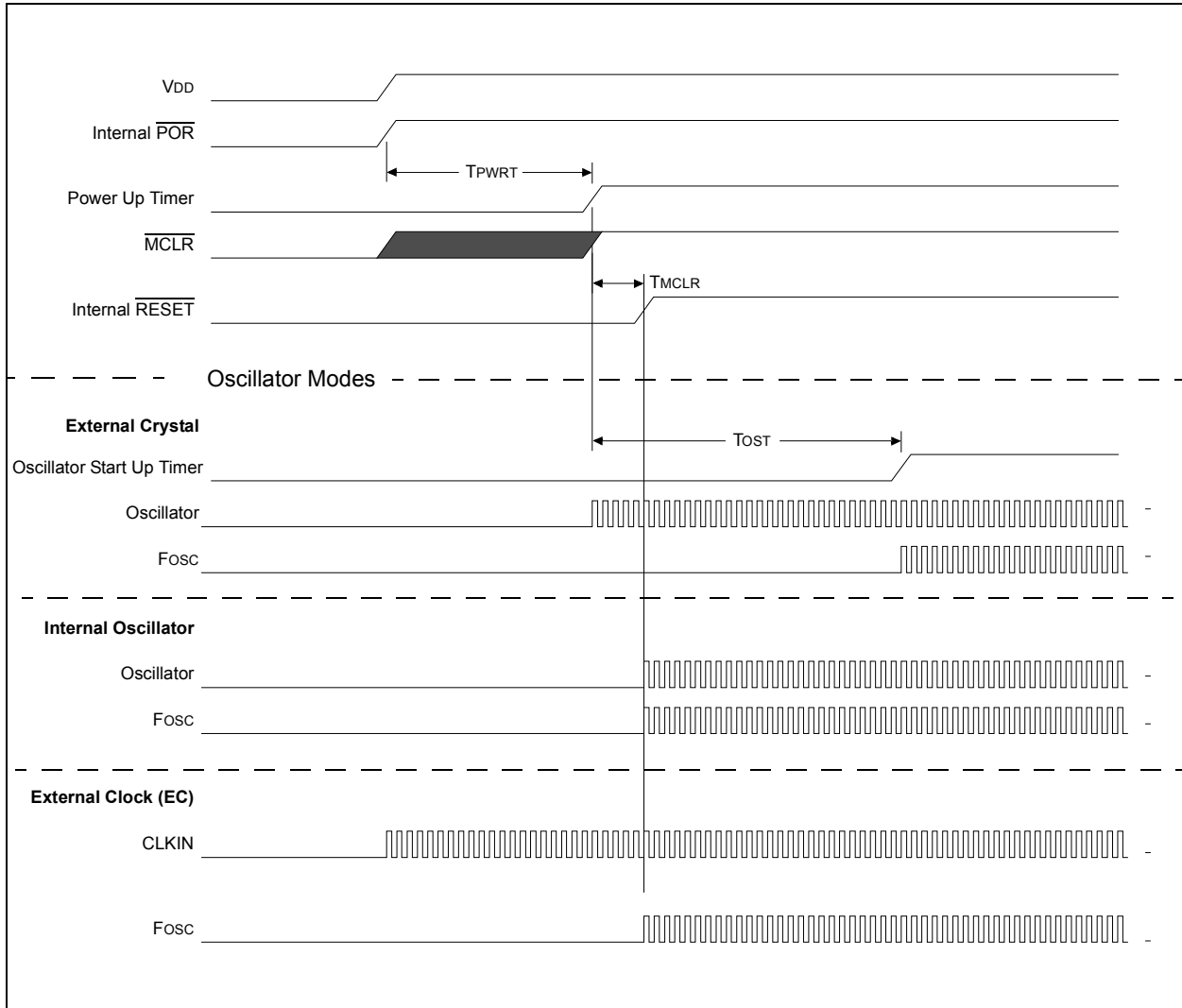
During normal program operation, `CALL`, `CALLW` and Interrupts will increment `STKPTR` while `RETLW`, `RETURN`, and `RETFIE` will decrement `STKPTR`. At any time `STKPTR` can be inspected to see how much stack is left. The `STKPTR` always points at the currently used place on the stack. Therefore, a `CALL` or `CALLW` will increment the `STKPTR` and then write the PC, and a return will unload the PC and then decrement the `STKPTR`.

Reference Figure 3-4 through Figure 3-7 for examples of accessing the stack.

**FIGURE 3-4: ACCESSING THE STACK EXAMPLE 1**



**FIGURE 6-3: RESET START-UP SEQUENCE**



## 11.0 DATA EEPROM AND FLASH PROGRAM MEMORY CONTROL

The Data EEPROM and Flash program memory are readable and writable during normal operation (full  $V_{DD}$  range). These memories are not directly mapped in the register file space. Instead, they are indirectly addressed through the Special Function Registers (SFRs). There are six SFRs used to access these memories:

- EECON1
- EECON2
- EEDATL
- EEDATH
- EEADRL
- EEADRH

When interfacing the data memory block, EEDATL holds the 8-bit data for read/write, and EEADRL holds the address of the EEDATL location being accessed. These devices have 256 bytes of data EEPROM with an address range from 0h to 0FFh.

When accessing the program memory block, the EEDATH:EEDATL register pair forms a 2-byte word that holds the 14-bit data for read/write, and the EEADRL and EEADRH registers form a 2-byte word that holds the 15-bit address of the program memory location being read.

The EEPROM data memory allows byte read and write. An EEPROM byte write automatically erases the location and writes the new data (erase before write).

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump rated to operate over the voltage range of the device for byte or word operations.

Depending on the setting of the Flash Program Memory Self Write Enable bits  $WRT<1:0>$  of the Configuration Words, the device may or may not be able to write certain blocks of the program memory. However, reads from the program memory are always allowed.

When the device is code-protected, the device programmer can no longer access data or program memory. When code-protected, the CPU may continue to read and write the data EEPROM memory and Flash program memory.

## 11.1 EEADRL and EEADRH Registers

The EEADRH:EEADRL register pair can address up to a maximum of 256 bytes of data EEPROM or up to a maximum of 32K words of program memory.

When selecting a program address value, the MSB of the address is written to the EEADRH register and the LSB is written to the EEADRL register. When selecting a EEPROM address value, only the LSB of the address is written to the EEADRL register.

### 11.1.1 EECON1 AND EECON2 REGISTERS

EECON1 is the control register for EE memory accesses.

Control bit EEPGD determines if the access will be a program or data memory access. When clear, any subsequent operations will operate on the EEPROM memory. When set, any subsequent operations will operate on the program memory. On Reset, EEPROM is selected by default.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set, in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation to occur. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit and execute the appropriate error handling routine.

Interrupt flag bit EEIF of the PIR2 register is set when write is complete. It must be cleared in the software.

Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the data EEPROM write sequence. To enable writes, a specific pattern must be written to EECON2.

## 11.3.2 ERASING FLASH PROGRAM MEMORY

While executing code, program memory can only be erased by rows. To erase a row:

1. Load the EEADRH:EEADRL register pair with the address of new row to be erased.
2. Clear the CFGS bit of the EECON1 register.
3. Set the EEPGD, FREE, and WREN bits of the EECON1 register.
4. Write 55h, then AAh, to EECON2 (Flash programming unlock sequence).
5. Set control bit WR of the EECON1 register to begin the erase operation.
6. Poll the FREE bit in the EECON1 register to determine when the row erase has completed.

See [Example 11-4](#).

After the “BSF EECON1, WR” instruction, the processor requires two cycles to set up the erase operation. The user must place two NOP instructions after the WR bit is set. The processor will halt internal operations for the typical 2 ms erase time. This is not Sleep mode as the clocks and peripherals will continue to run. After the erase cycle, the processor will resume operation with the third instruction after the EECON1 write instruction.

## 11.3.3 WRITING TO FLASH PROGRAM MEMORY

Program memory is programmed using the following steps:

1. Load the starting address of the word(s) to be programmed.
2. Load the write latches with data.
3. Initiate a programming operation.
4. Repeat steps 1 through 3 until all data is written.

Before writing to program memory, the word(s) to be written must be erased or previously unwritten. Program memory can only be erased one row at a time. No automatic erase occurs upon the initiation of the write.

Program memory can be written one or more words at a time. The maximum number of words written at one time is equal to the number of write latches. See [Figure 11-2](#) (block writes to program memory with 8 write latches) for more details. The write latches are aligned to the address boundary defined by EEADRL as shown in [Table 11-1](#). Write operations do not cross these boundaries. At the completion of a program memory write operation, the write latches are reset to contain 0x3FFF.

The following steps should be completed to load the write latches and program a block of program memory. These steps are divided into two parts. First, all write latches are loaded with data except for the last program memory location. Then, the last write latch is loaded and the programming sequence is initiated. A special unlock sequence is required to load a write latch with data or initiate a Flash programming operation. This unlock sequence should not be interrupted.

1. Set the EEPGD and WREN bits of the EECON1 register.
2. Clear the CFGS bit of the EECON1 register.
3. Set the LWLO bit of the EECON1 register. When the LWLO bit of the EECON1 register is ‘1’, the write sequence will only load the write latches and will not initiate the write to Flash program memory.
4. Load the EEADRH:EEADRL register pair with the address of the location to be written.
5. Load the EEDATH:EEDATL register pair with the program memory data to be written.
6. Write 55h, then AAh, to EECON2, then set the WR bit of the EECON1 register (Flash programming unlock sequence). The write latch is now loaded.
7. Increment the EEADRH:EEADRL register pair to point to the next location.
8. Repeat steps 5 through 7 until all but the last write latch has been loaded.
9. Clear the LWLO bit of the EECON1 register. When the LWLO bit of the EECON1 register is ‘0’, the write sequence will initiate the write to Flash program memory.
10. Load the EEDATH:EEDATL register pair with the program memory data to be written.
11. Write 55h, then AAh, to EECON2, then set the WR bit of the EECON1 register (Flash programming unlock sequence). The entire latch block is now written to Flash program memory.

It is not necessary to load the entire write latch block with user program data. However, the entire write latch block will be written to program memory.

An example of the complete write sequence for eight words is shown in [Example 11-5](#). The initial address is loaded into the EEADRH:EEADRL register pair; the eight words of data are loaded using indirect addressing.

**Note:** The code sequence provided in [Example 11-5](#) must be repeated multiple times to fully program an erased program memory row.

# PIC16(L)F1938/9

## 12.6 Register Definitions: PORTB Control

### REGISTER 12-6: PORTB: PORTB REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
bit 7							bit 0

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-0

**RB<7:0>**: PORTB I/O Pin bit

1 = Port pin is > VIH

0 = Port pin is < VIL

### REGISTER 12-7: TRISB: PORTB TRI-STATE REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0
bit 7							bit 0

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-0

**TRISB<7:0>**: PORTB Tri-State Control bits

1 = PORTB pin configured as an input (tri-stated)

0 = PORTB pin configured as an output

### REGISTER 12-8: LATB: PORTB DATA LATCH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0
bit 7							bit 0

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-0

**LATB<7:0>**: PORTB Output Latch Value bits<sup>(1)</sup>

**Note 1:** Writes to PORTB are actually written to corresponding LATB register. Reads from PORTB register is return of actual I/O pin values.



# PIC16(L)F1938/9

## 12.12 Register Definitions: PORTE Control

### REGISTER 12-18: PORTE: PORTE REGISTER

U-0	U-0	U-0	U-0	R-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	—	—	RE3	RE2 <sup>(1)</sup>	RE1 <sup>(1)</sup>	RE0 <sup>(1)</sup>
bit 7							bit 0

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **RE<3:0>:** PORTE I/O Pin bits<sup>(1)</sup>

1 = Port pin is > V<sub>IH</sub>

0 = Port pin is < V<sub>IL</sub>

**Note 1:** RE<2:0> are not implemented on the PIC16(L)F1938. Read as '0'.

### REGISTER 12-19: TRISE: PORTE TRI-STATE REGISTER

U-0	U-0	U-0	U-0	U-1 <sup>(2)</sup>	R/W-1	R/W-1	R/W-1
—	—	—	—	—	TRISE2 <sup>(1)</sup>	TRISE1 <sup>(1)</sup>	TRISE0 <sup>(1)</sup>
bit 7							bit 0

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **Unimplemented:** Read as '1'

bit 2-0 **TRISE<2:0>:** RE<2:0> Tri-State Control bits<sup>(1)</sup>

1 = PORTE pin configured as an input (tri-stated)

0 = PORTE pin configured as an output

**Note 1:** TRISE<2:0> are not implemented on the PIC16(L)F1938. Read as '0'.

**2:** Unimplemented, read as '1'.

NOTES:

## 21.11 Register Definitions: Timer1 Control

### REGISTER 21-1: T1CON: TIMER1 CONTROL REGISTER

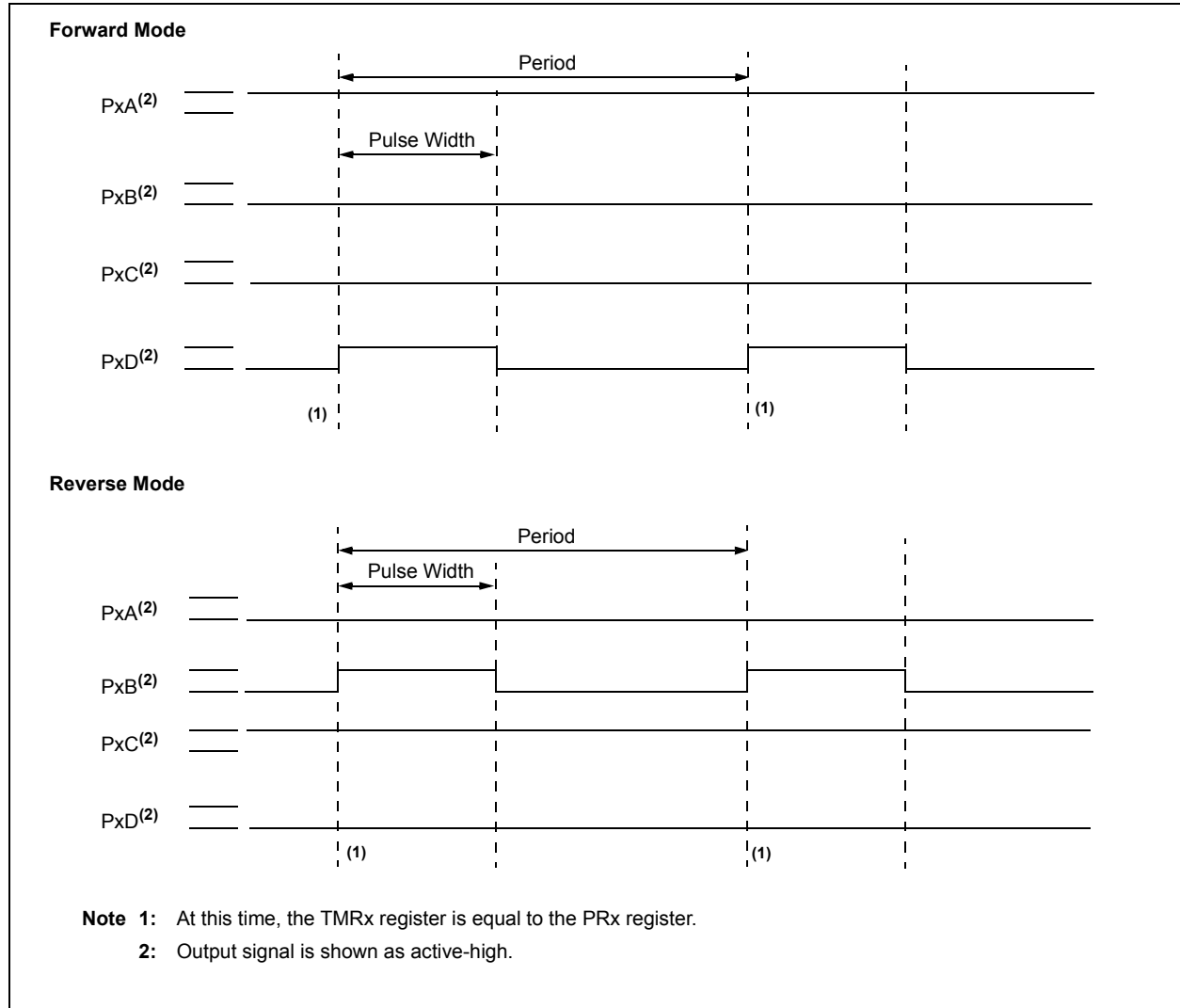
R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	U-0	R/W-0/u
TMR1CS<1:0>		T1CKPS<1:0>		T1OSCEN	$\overline{T1SYNC}$	—	TMR1ON
bit 7							bit 0

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6	<b>TMR1CS&lt;1:0&gt;</b> : Timer1 Clock Source Select bits 11 = Timer1 clock source is Capacitive Sensing Oscillator (CPSClk) 10 = Timer1 clock source is pin or oscillator: If <b>T1OSCEN</b> = 0: External clock from T1CKI pin (on the rising edge) If <b>T1OSCEN</b> = 1: Crystal oscillator on T1OSI/T1OSO pins 01 = Timer1 clock source is system clock (Fosc) 00 = Timer1 clock source is instruction clock (Fosc/4)
bit 5-4	<b>T1CKPS&lt;1:0&gt;</b> : Timer1 Input Clock Prescale Select bits 11 = 1:8 Prescale value 10 = 1:4 Prescale value 01 = 1:2 Prescale value 00 = 1:1 Prescale value
bit 3	<b>T1OSCEN</b> : LP Oscillator Enable Control bit 1 = Dedicated Timer1 oscillator circuit enabled 0 = Dedicated Timer1 oscillator circuit disabled
bit 2	<b><math>\overline{T1SYNC}</math></b> : Timer1 Synchronization Control bit 1 = Do not synchronize asynchronous clock input 0 = Synchronize asynchronous clock input with system clock (Fosc)
bit 1	<b>Unimplemented</b> : Read as '0'
bit 0	<b>TMR1ON</b> : Timer1 On bit 1 = Enables Timer1 0 = Stops Timer1 Clears Timer1 gate flip-flop

**FIGURE 23-11: EXAMPLE OF FULL-BRIDGE PWM OUTPUT**



# PIC16(L)F1938/9

## 24.6.13.1 Bus Collision During a Start Condition

During a Start condition, a bus collision occurs if:

- SDA or SCL are sampled low at the beginning of the Start condition (Figure 24-33).
- SCL is sampled low before SDA is asserted low (Figure 24-34).

During a Start condition, both the SDA and the SCL pins are monitored.

If the SDA pin is already low, or the SCL pin is already low, then all of the following occur:

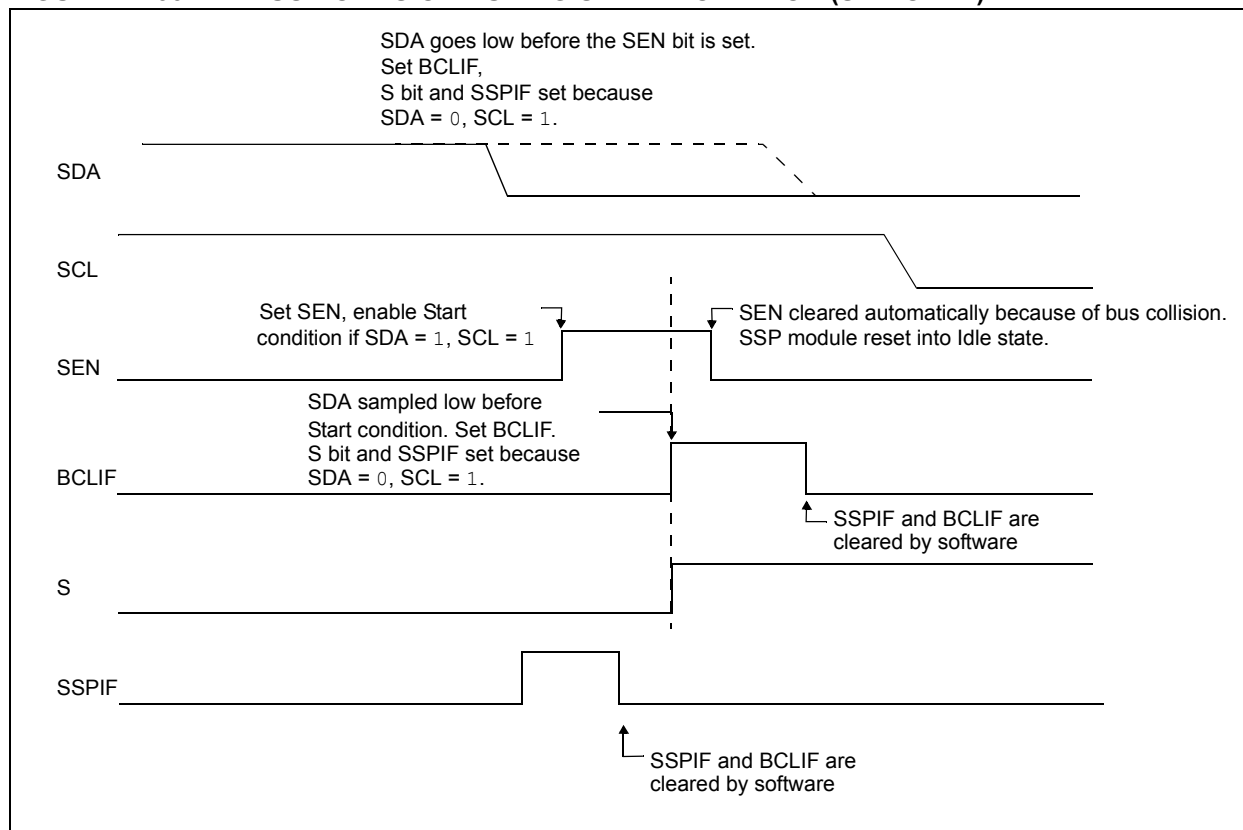
- the Start condition is aborted,
- the BCLIF flag is set and
- the MSSP module is reset to its Idle state (Figure 24-33).

The Start condition begins with the SDA and SCL pins deasserted. When the SDA pin is sampled high, the Baud Rate Generator is loaded and counts down. If the SCL pin is sampled low while SDA is high, a bus collision occurs because it is assumed that another master is attempting to drive a data '1' during the Start condition.

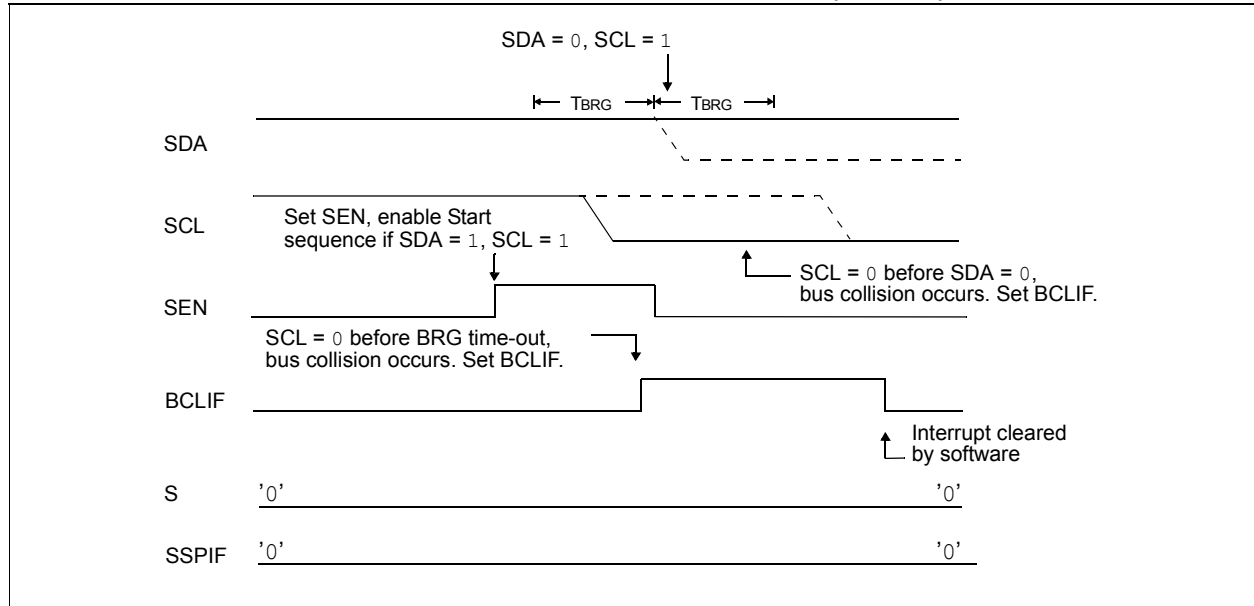
If the SDA pin is sampled low during this count, the BRG is reset and the SDA line is asserted early (Figure 24-35). If, however, a '1' is sampled on the SDA pin, the SDA pin is asserted low at the end of the BRG count. The Baud Rate Generator is then reloaded and counts down to zero; if the SCL pin is sampled as '0' during this time, a bus collision does not occur. At the end of the BRG count, the SCL pin is asserted low.

**Note:** The reason that bus collision is not a factor during a Start condition is that no two bus masters can assert a Start condition at the exact same time. Therefore, one master will always assert SDA before the other. This condition does not cause a bus collision because the two masters must be allowed to arbitrate the first address following the Start condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated Start or Stop conditions.

**FIGURE 24-33: BUS COLLISION DURING START CONDITION (SDA ONLY)**



**FIGURE 24-34: BUS COLLISION DURING START CONDITION (SCL = 0)**



**FIGURE 24-35: BRG RESET DUE TO SDA ARBITRATION DURING START CONDITION**

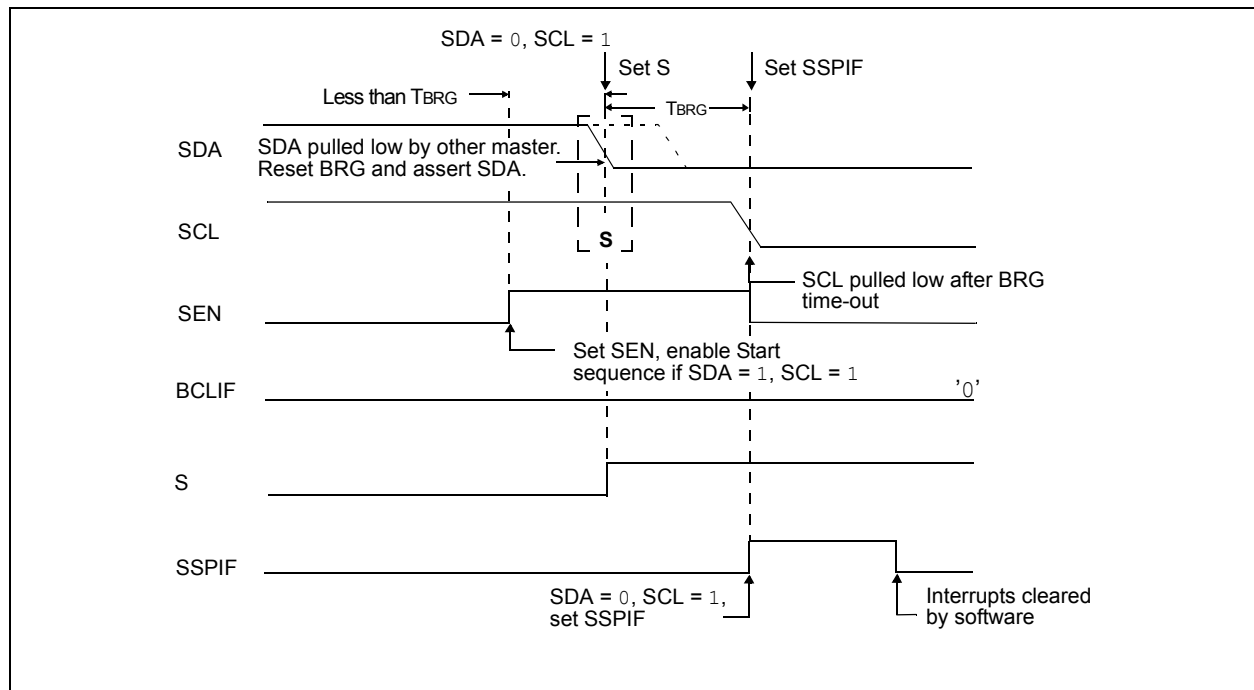


FIGURE 25-7: AUTO-WAKE-UP BIT (WUE) TIMING DURING NORMAL OPERATION

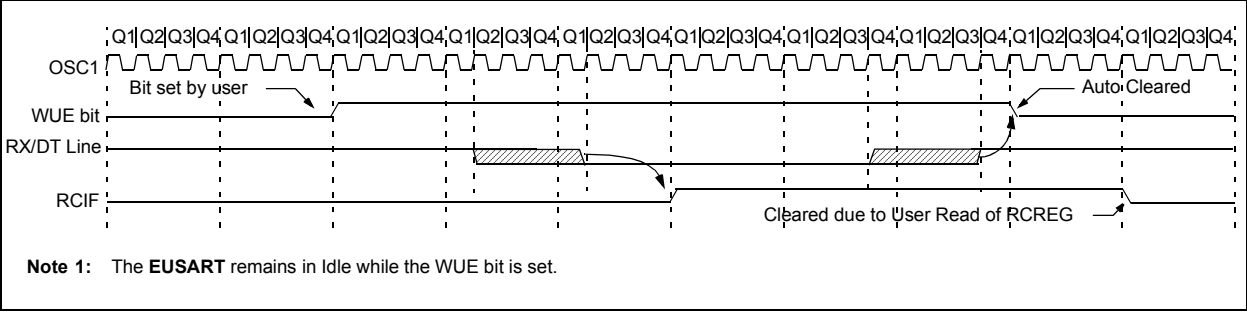
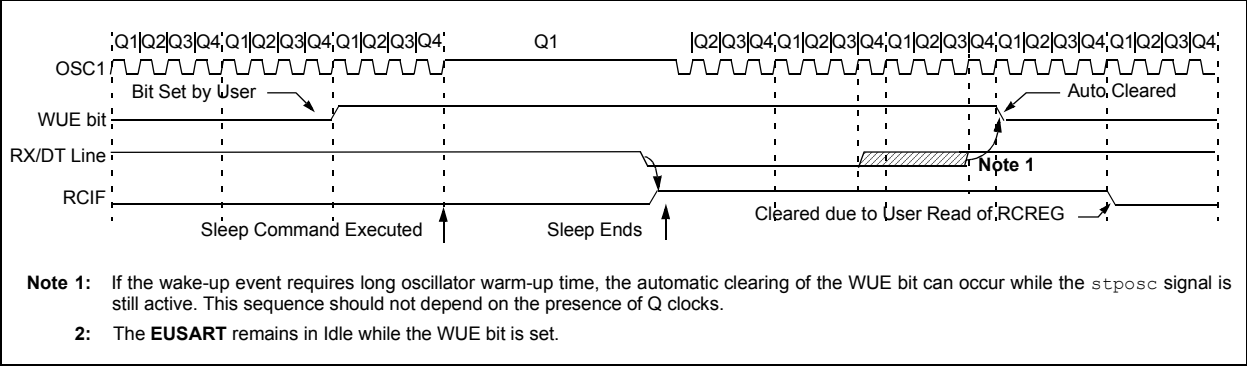


FIGURE 25-8: AUTO-WAKE-UP BIT (WUE) TIMINGS DURING SLEEP



## 25.6 EUSART Operation During Sleep

The EUSART will remain active during Sleep only in the Synchronous Slave mode. All other modes require the system clock and therefore cannot generate the necessary signals to run the Transmit or Receive Shift registers during Sleep.

Synchronous Slave mode uses an externally generated clock to run the Transmit and Receive Shift registers.

### 25.6.1 SYNCHRONOUS RECEIVE DURING SLEEP

To receive during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for Synchronous Slave Reception (see [Section 25.5.2.4 “Synchronous Slave Reception Set-up:”](#)).
- If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- The RCIF interrupt flag must be cleared by reading RCREG to unload any pending characters in the receive buffer.

Upon entering Sleep mode, the device will be ready to accept data and clocks on the RX/DT and TX/CK pins, respectively. When the data word has been completely clocked in by the external device, the RCIF interrupt flag bit of the PIR1 register will be set. Thereby, waking the processor from Sleep.

Upon waking from Sleep, the instruction following the `SLEEP` instruction will be executed. If the GIE global interrupt enable bit of the INTCON register is also set, then the Interrupt Service Routine at address 004h will be called.

### 25.6.2 SYNCHRONOUS TRANSMIT DURING SLEEP

To transmit during Sleep, all the following conditions must be met before entering Sleep mode:

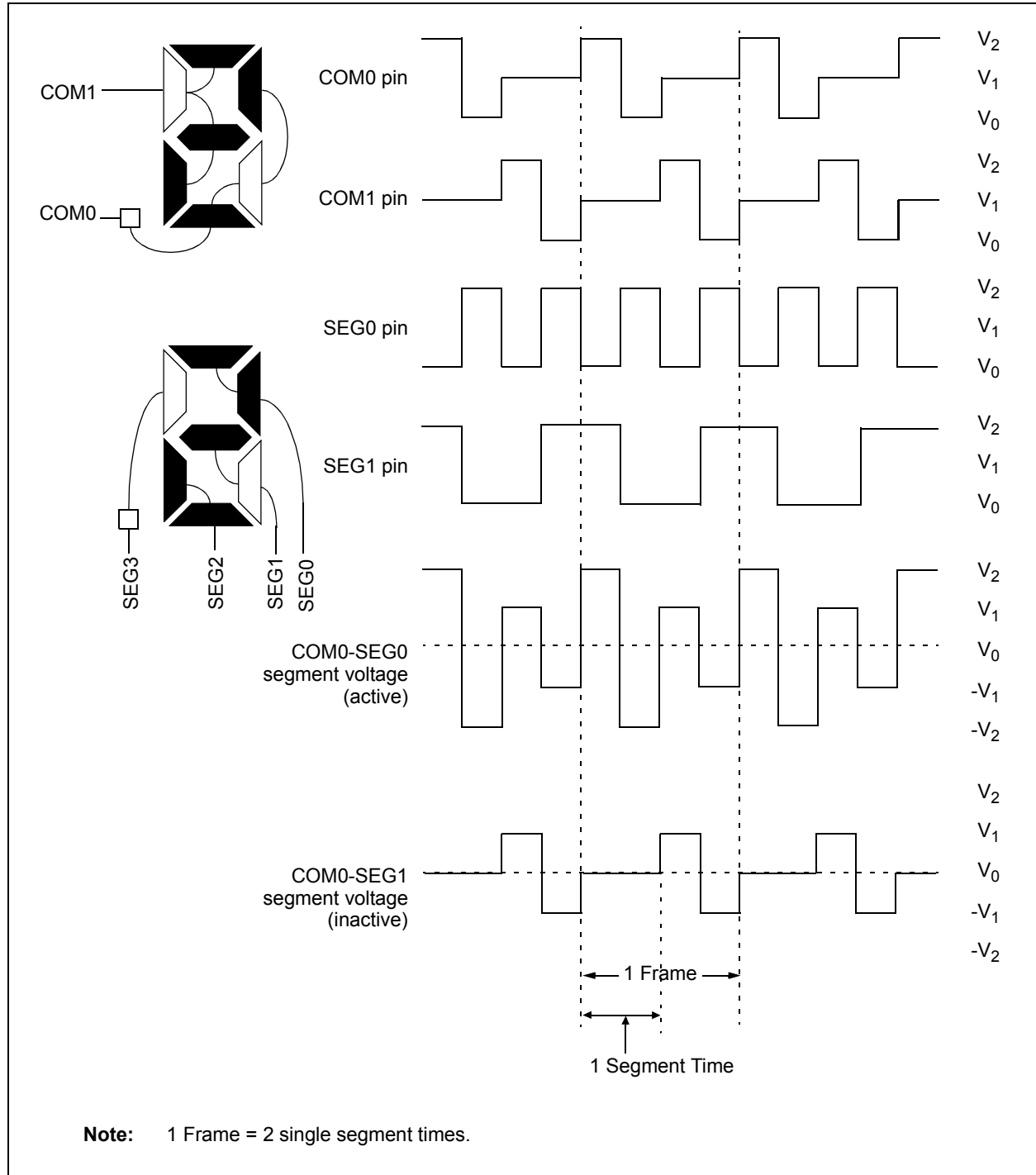
- RCSTA and TXSTA Control registers must be configured for Synchronous Slave Transmission (see [Section 25.5.2.2 “Synchronous Slave Transmission Set-up:”](#)).
- The TXIF interrupt flag must be cleared by writing the output data to the TXREG, thereby filling the TSR and transmit buffer.
- If interrupts are desired, set the TXIE bit of the PIE1 register and the PEIE bit of the INTCON register.
- Interrupt enable bits TXIE of the PIE1 register and PEIE of the INTCON register must set.

Upon entering Sleep mode, the device will be ready to accept clocks on TX/CK pin and transmit data on the RX/DT pin. When the data word in the TSR has been completely clocked out by the external device, the pending byte in the TXREG will transfer to the TSR and the TXIF flag will be set. Thereby, waking the processor from Sleep. At this point, the TXREG is available to accept another character for transmission, which will clear the TXIF flag.

Upon waking from Sleep, the instruction following the `SLEEP` instruction will be executed. If the Global Interrupt Enable (GIE) bit is also set then the Interrupt Service Routine at address 0004h will be called.



**FIGURE 27-9: TYPE-A WAVEFORMS IN 1/2 MUX, 1/2 BIAS DRIVE**



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**TABLE 27-9: SUMMARY OF REGISTERS ASSOCIATED WITH LCD OPERATION**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCF	TMR0IF	INTF	IOCF	90
LCDCON	LCDEN	SLPEN	WERR	—	CS<1:0>		LMUX<1:0>		327
LCDCST	—	—	—	—	—	LCDCST<2:0>			330
LCDDATA0	SEG7 COM0	SEG6 COM0	SEG5 COM0	SEG4 COM0	SEG3 COM0	SEG2 COM0	SEG1 COM0	SEG0 COM0	331
LCDDATA1	SEG15 COM0	SEG14 COM0	SEG13 COM0	SEG12 COM0	SEG11 COM0	SEG10 COM0	SEG9 COM0	SEG8 COM0	331
LCDDATA2	SEG23 COM0	SEG22 COM0	SEG21 COM0	SEG20 COM0	SEG19 COM0	SEG18 COM0	SEG17 COM0	SEG16 COM0	331
LCDDATA3	SEG7 COM1	SEG6 COM1	SEG5 COM1	SEG4 COM1	SEG3 COM1	SEG2 COM1	SEG1 COM1	SEG0 COM1	331
LCDDATA4	SEG15 COM1	SEG14 COM1	SEG13 COM1	SEG12 COM1	SEG11 COM1	SEG10 COM1	SEG9 COM1	SEG8 COM1	331
LCDDATA5	SEG23 COM1	SEG22 COM1	SEG21 COM1	SEG20 COM1	SEG19 COM1	SEG18 COM1	SEG17 COM1	SEG16 COM1	331
LCDDATA6	SEG7 COM2	SEG6 COM2	SEG5 COM2	SEG4 COM2	SEG3 COM2	SEG2 COM2	SEG1 COM2	SEG0 COM2	331
LCDDATA7	SEG15 COM2	SEG14 COM2	SEG13 COM2	SEG12 COM2	SEG11 COM2	SEG10 COM2	SEG9 COM2	SEG8 COM2	331
LCDDATA8	SEG23 COM2	SEG22 COM2	SEG21 COM2	SEG20 COM2	SEG19 COM2	SEG18 COM2	SEG17 COM2	SEG16 COM2	331
LCDDATA9	SEG7 COM3	SEG6 COM3	SEG5 COM3	SEG4 COM3	SEG3 COM3	SEG2 COM3	SEG1 COM3	SEG0 COM3	331
LCDDATA10	SEG15 COM3	SEG14 COM3	SEG13 COM3	SEG12 COM3	SEG11 COM3	SEG10 COM3	SEG9 COM3	SEG8 COM3	331
LCDDATA11	SEG23 COM3	SEG22 COM3	SEG21 COM3	SEG20 COM3	SEG19 COM3	SEG18 COM3	SEG17 COM3	SEG16 COM3	331
LCDPS	WFT	BIASMD	LCDA	WA	LP<3:0>				328
LCDREF	LCDIRE	LCDIRS	LCDIRI	—	VLCD3PE	VLCD2PE	VLCD1PE	—	329
LCDRL	LRLAP<1:0>		LRLBP<1:0>		—	LRLAT<2:0>			338
LCDSE0	SE<7:0>								331
LCDSE1	SE<15:8>								331
LCDSE2	SE<23:16>								331
PIE2	OSFIE	C2IE	C1IE	EEIE	BCLIE	LCDIE	—	CCP2IE	92
PIR2	OSFIF	C2IF	C1IF	EEIF	BCLIF	LCDIF	—	CCP2IF	95
T1CON	TMR1CS<1:0>		T1CKPS<1:0>		T1OSCEN	T1SYNC	—	TMR1ON	197

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by the LCD module.

# PIC16(L)F1938/9

## RETFIE Return from Interrupt

**Syntax:** [ *label* ] RETFIE

**Operands:** None

**Operation:** TOS → PC,  
1 → GIE

**Status Affected:** None

**Description:** Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a 2-cycle instruction.

**Words:** 1

**Cycles:** 2

**Example:**

```
RETFIE

After Interrupt
PC = TOS
GIE = 1
```

## RETLW Return with literal in W

**Syntax:** [ *label* ] RETLW *k*

**Operands:**  $0 \leq k \leq 255$

**Operation:** *k* → (W);  
TOS → PC

**Status Affected:** None

**Description:** The W register is loaded with the 8-bit literal '*k*'. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.

**Words:** 1

**Cycles:** 2

**Example:**

```
CALL TABLE;W contains table
;offset value
• ;W now has table value
•
•
ADDWF PC ;W = offset
RETLW k1 ;Begin table
RETLW k2 ;
•
•
•
RETLW kn ; End of table
```

TABLE

Before Instruction  
W = 0x07

After Instruction  
W = value of k8

## RETURN Return from Subroutine

**Syntax:** [ *label* ] RETURN

**Operands:** None

**Operation:** TOS → PC

**Status Affected:** None

**Description:** Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a 2-cycle instruction.

## RLF Rotate Left f through Carry

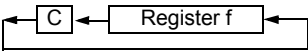
**Syntax:** [ *label* ] RLF *f*,*d*

**Operands:**  $0 \leq f \leq 127$   
 $d \in [0,1]$

**Operation:** See description below

**Status Affected:** C

**Description:** The contents of register '*f*' are rotated one bit to the left through the Carry flag. If '*d*' is '0', the result is placed in the W register. If '*d*' is '1', the result is stored back in register '*f*'.



**Words:** 1

**Cycles:** 1

**Example:**

```
RLF REG1,0
```

Before Instruction

REG1	=	1110 0110
C	=	0

After Instruction

REG1	=	1110 0110
W	=	1100 1100
C	=	1

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**TABLE 30-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET**

Standard Operating Conditions (unless otherwise stated) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$							
Param No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
30	TMCL	MCLR Pulse Width (low)	2	—	—	$\mu\text{s}$	
31	TWDTLP	Low-Power Watchdog Timer Time-out Period	10	16	27	ms	$V_{DD} = 3.3\text{V}-5\text{V}$ 1:16 Prescaler used
32	TOST	Oscillator Start-up Timer Period <sup>(1)</sup>	—	1024	—	Tosc	
33*	TPWRT	Power-up Timer Period, $\overline{\text{PWRTE}} = 0$	40	65	140	ms	
34*	TIOZ	I/O high-impedance from MCLR Low or Watchdog Timer Reset	—	—	2.0	$\mu\text{s}$	
35	VBOR	Brown-out Reset Voltage <sup>(2)</sup>	2.55 1.80	2.7 1.9	2.85 2.11	V V	BORV = 0 BORV = 1
36*	VHYS	Brown-out Reset Hysteresis	20	35	60	mV	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
37*	TBORDC	Brown-out Reset DC Response Time	1	3	35	$\mu\text{s}$	$V_{DD} \leq V_{BOR}$

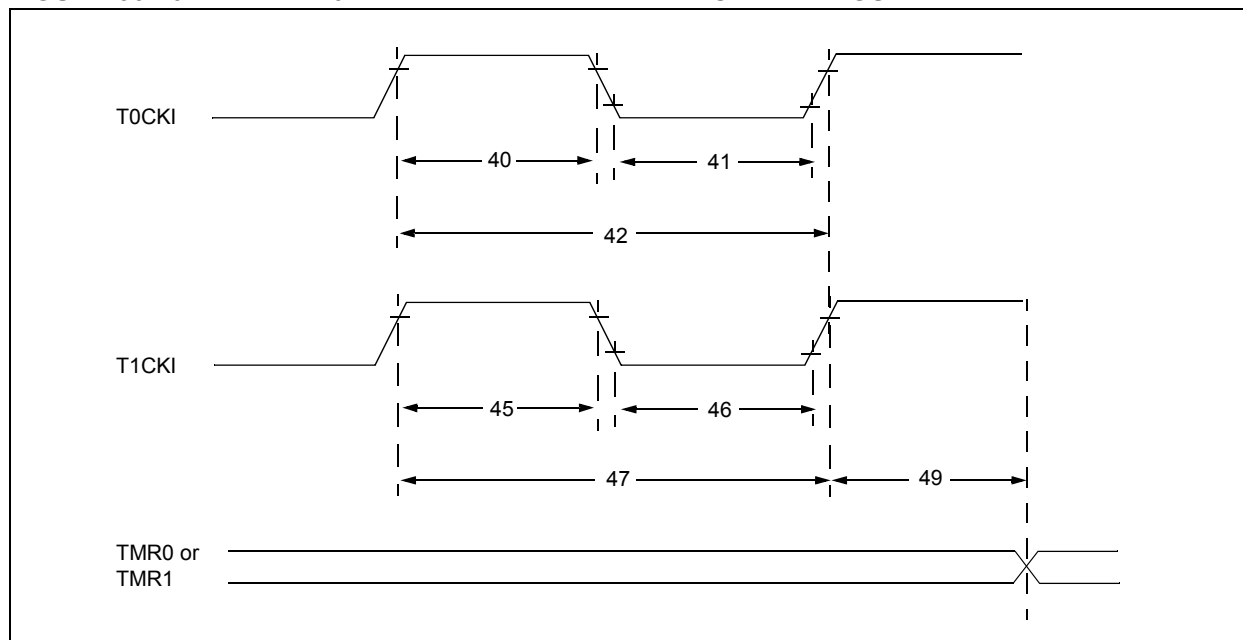
\* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

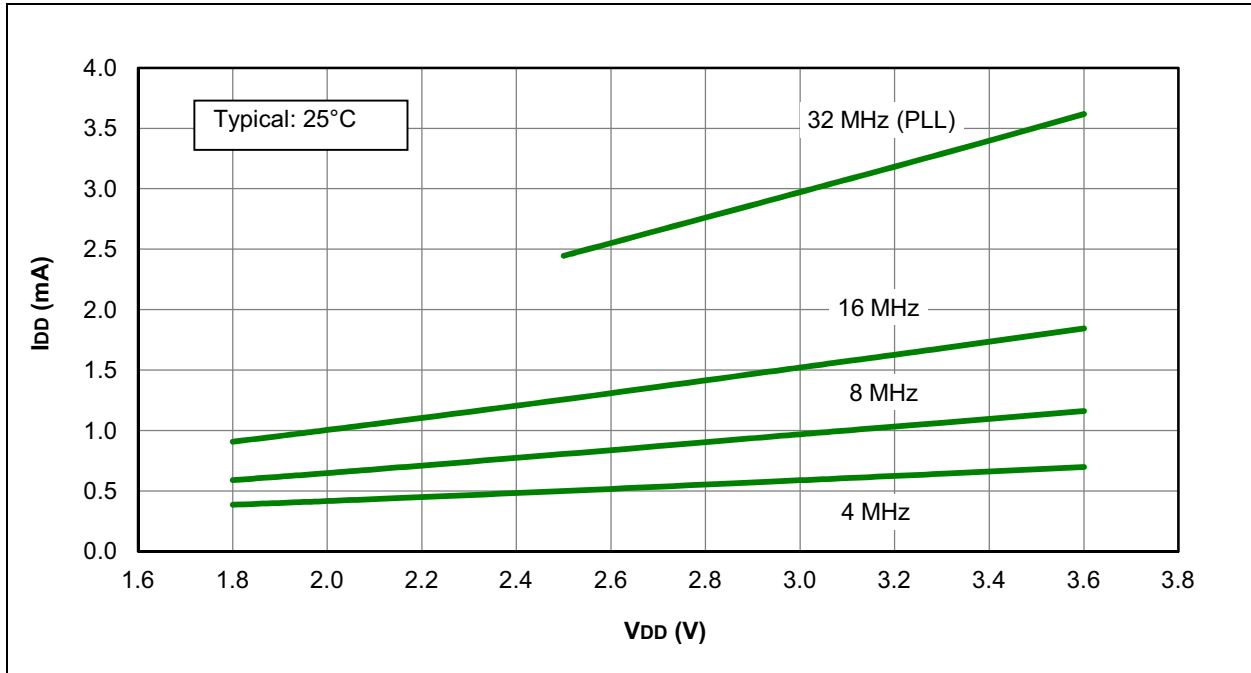
**Note 1:** By design, the Oscillator Start-up Timer (OST) counts the first 1024 cycles, independent of frequency.

**2:** To ensure these voltage tolerances,  $V_{DD}$  and  $V_{SS}$  must be capacitively decoupled as close to the device as possible. 0.1  $\mu\text{F}$  and 0.01  $\mu\text{F}$  values in parallel are recommended.

**FIGURE 30-10: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS**



**FIGURE 31-23: I<sub>DD</sub> TYPICAL, HFINTOSC, PIC16LF1938/9 ONLY**



**FIGURE 31-24: I<sub>DD</sub> MAXIMUM, HFINTOSC, PIC16LF1938/9 ONLY**

