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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1939-i-p

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Diagram – 44-Pin QFN 8x8



Pin Diagram – 44-Pin TQFP



RD6 ⁽⁴⁾ /CPS14/P1C/SEG19 RD6 ST CMOS General purpose I/O. CPS14 AN — Capacitive sensing input 14. P1C — CMOS PWM output. SEG19 — AN LCD analog output. RD7 ⁽⁴⁾ /CPS15/P1D/SEG20 RD7 ST CMOS General purpose I/O.	
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RD7 ⁽⁴⁾ /CPS15/P1D/SEG20 RD7 ST CMOS General purpose I/O.	
CPS15 AN Capacitive consing input 15	
CFSTS AN — Capacitive sensing input T5.	
P1D — CMOS PWM output.	
SEG20 — AN LCD analog output.	
RE0 ⁽⁵⁾ /AN5/P3A ⁽¹⁾ /CCP3 ⁽¹⁾ / RE0 ST CMOS General purpose I/O.	
SEG21 AN5 AN — A/D Channel 5 input.	
P3A — CMOS PWM output.	
CCP3 ST CMOS Capture/Compare/PWM3.	
SEG21 — AN LCD analog output.	
RE1 ⁽⁵⁾ /AN6/P3B/SEG22 RE1 ST CMOS General purpose I/O.	
AN6 AN — A/D Channel 6 input.	
P3B — CMOS PWM output.	
SEG22 — AN LCD analog output.	
RE2 ⁽⁵⁾ /AN7/CCP5/SEG23 RE2 ST CMOS General purpose I/O.	
AN7 AN — A/D Channel 7 input.	
CCP5 ST CMOS Capture/Compare/PWM5.	
SEG23 — AN LCD analog output.	
RE3/MCLR/VPP RE3 TTL — General purpose input.	
MCLR ST — Master Clear with internal pull-up.	
VPP HV — Programming voltage.	
VDD VDD Power — Positive supply.	
Vss Vss Power — Ground reference.	

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain

TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels XTAL = Crystal

HV = High Voltage I^2C^{TM} = Schmitt Trigger input with I²C levels

Note 1: Pin function is selectable via the APFCON register.

2: PIC16F1938/9 devices only.

3: PIC16(L)F1938 devices only.

4: PORTD is available on PIC16(L)F1939 devices only.

5: RE<2:0> are available on PIC16(L)F1939 devices only.

5.4.2 TWO-SPEED START-UP SEQUENCE

- 1. Wake-up from Power-on Reset or Sleep.
- Instructions begin execution by the internal oscillator at the frequency set in the IRCF<3:0> bits of the OSCCON register.
- 3. OST enabled to count 1024 clock cycles.
- 4. OST timed out, wait for falling edge of the internal oscillator.
- 5. OSTS is set.
- 6. System clock held low until the next falling edge of new clock (LP, XT or HS mode).
- 7. System clock is switched to external clock source.

5.4.3 CHECKING TWO-SPEED CLOCK STATUS

Checking the state of the OSTS bit of the OSCSTAT register will confirm if the microcontroller is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Words, or the internal oscillator.



FIGURE 5-8: TWO-SPEED START-UP

PIC16(L)F1938/9

R/W-0/	0 R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	
_	CCP5IF	CCP4IF	CCP3IF	TMR6IF		TMR4IF		
bit 7							bit 0	
Legend:								
R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'								
u = Bit is ι	unchanged	x = Bit is unkr	nown	-n/n = Value a	at POR and BO	R/Value at all c	other Resets	
'1' = Bit is	set	'0' = Bit is cle	ared					
bit 7	Unimplemer	nted: Read as '	0'					
bit 6	CCP5IF: CC	P5 Interrupt Fla	g bit					
	1 = Interrupt	is pending						
L:4 C		IS not pending	- 1-14					
DIL D	1 = Interrunt	P4 Interrupt Fla	g bit					
	0 = Interrupt	is not pending						
bit 4	CCP3IF: CC	P3 Interrupt Fla	g bit					
	1 = Interrupt	is pending						
	0 = Interrupt	is not pending						
bit 3	TMR6IF: TM	R6 to PR6 Mate	ch Interrupt Fl	ag bit				
	1 = Interrupt	is pending						
hit O		is not pending	o '					
DIL Z		Redu as	∪ Sh Intorrunt El	ag hit				
DILI	1 = Interrunt	is nendina	in interrupt i i	ag bit				
	0 = Interrupt	is not pending						
bit 0	Unimplemer	nted: Read as '	0'					
	-							
Note:	Interrupt flag bits a condition occurs, r its corresponding Enable bit, GIE, o User software	are set when an regardless of the enable bit or th of the INTCON should ensu	interrupt e state of e Global register. ure the					

REGISTER 7-7: PIR3: PERIPHERAL INTERRUPT REQUEST REGISTER 3

appropriate interrupt flag bits are clear prior to enabling an interrupt.

TABLE 15-1: ADC CLOCK PERIOD (TAD) Vs. DEVICE OPERATING FREQUENCIES

ADC Clock P	eriod (TAD)	Device Frequency (Fosc) Device Frequency (Fosc)								
ADC Clock Source	ADCS<2:0>	32 MHz	20 MHz	20 MHz 16 MHz 8 N		4 MHz	1 MHz			
Fosc/2	000	62.5ns ⁽²⁾	100 ns ⁽²⁾	125 ns ⁽²⁾	250 ns ⁽²⁾	500 ns ⁽²⁾	2.0 μs			
Fosc/4	100	125 ns ⁽²⁾	200 ns ⁽²⁾	250 ns ⁽²⁾	500 ns ⁽²⁾	1.0 μs	4.0 μs			
Fosc/8	001	0.5 μs ⁽²⁾	400 ns ⁽²⁾	0.5 μs ⁽²⁾	1.0 μs	2.0 μs	8.0 μs ⁽³⁾			
Fosc/16	101	800 ns	800 ns	1.0 μs	2.0 μs	4.0 μs	16.0 μs ⁽³⁾			
Fosc/32	010	1.0 μs	1.6 μs	2.0 μs	4.0 μs	8.0 μs ⁽³⁾	32.0 μs ⁽³⁾			
Fosc/64	110	2.0 μs	3.2 μs	4.0 μs	8.0 μs ⁽³⁾	16.0 μs ⁽³⁾	64.0 μs ⁽³⁾			
FRC	x11	1.0-6.0 μs ^(1,4)	1.0-6.0 μs ^(1,4)	1.0-6.0 μs ^(1,4)	1.0-6.0 μs ^(1,4)	1.0-6.0 μs ^(1,4)	1.0-6.0 μs ^(1,4)			

Legend: Shaded cells are outside of recommended range.

Note 1: The FRC source has a typical TAD time of 1.6 µs for VDD.

2: These values violate the minimum required TAD time.

3: For faster conversion times, the selection of another clock source is recommended.

4: The ADC clock period (TAD) and total ADC conversion time can be minimized when the ADC clock is derived from the system clock FOSC. However, the FRC clock source must be used when conversions are to be performed with the device in Sleep mode.

FIGURE 15-2: ANALOG-TO-DIGITAL CONVERSION TAD CYCLES

TCY - TAD	TAD1	TAD2	TAD3	TAD4	TAD5	Tad6	TAD7	Tad8	TAD9	TAD10	TAD11	l I	
≜ ↑ 1		b9	b8	b7	b6	b5	b4	b3	b2	b1	b0		
	Conver	sion sta	arts										
Holding	g capa	citor is	discon	nected	from a	nalog i	nput (t	ypically	/ 100 n	s)			
 Set CO	hit												
Sel GO	DIL				~	a tha f	↓ allouin						
On the following cycle: ADRESH:ADRESL is loaded. GO bit is cleared.													
					A	DIF bit	is set,	holdin	g capa	citor is	connec	cted to analog i	nput.

18.0 COMPARATOR MODULE

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. Comparators are very useful mixed signal building blocks because they provide analog functionality independent of program execution. The analog comparator module includes the following features:

- · Independent comparator control
- Programmable input selection
- · Comparator output is available internally/externally
- Programmable output polarity
- Interrupt-on-change
- · Wake-up from Sleep
- Programmable Speed/Power optimization
- · PWM shutdown
- · Programmable and fixed voltage reference

18.1 Comparator Overview

A single comparator is shown in Figure 18-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level.

FIGURE 18-1:

SINGLE COMPARATOR



23.1.6 ALTERNATE PIN LOCATIONS

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function register, APFCON. To determine which pins can be moved and what their default locations are upon a Reset, see Section 12.1 "Alternate Pin Function" for more information.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3 Bit 2		Bit 1	Bit 0	Register on Page	
APFCON	—	CCP3SEL	T1GSEL	P2BSEL	SRNQSEL	C2OUTSEL	SSSEL	CCP2SEL	123	
CCPxCON	PxM<	1:0> ⁽¹⁾	DCxB	<1:0>		CCPxM<	:3:0>		228	
CCPRxL	Capture/Compare/PWM Register x Low Byte (LSB)									
CCPRxH	Capture/Co	mpare/PWM	Register x I	High Byte (M	ISB)				206	
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	90	
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	91	
PIE2	OSFIE	C2IE	C1IE	EEIE	BCLIE	LCDIE	-	CCP2IE	92	
PIE3	—	CCP5IE	CCP4IE	CCP3IE	TMR6IE	_	- TMR4IE		93	
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	SPIF CCP1IF TMR2IF TM		TMR1IF	94	
PIR2	OSFIF	C2IF	C1IF	EEIF	BCLIF	LCDIF	_CDIF — CCP2IF		95	
PIR3	—	CCP5IF	CCP4IF	CCP3IF	TMR6IF	—	TMR4IF	—	95	
T1CON	TMR1C	:S<1:0>	T1CKP	S<1:0>	T1OSCEN	T1SYNC		TMR10N	197	
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/DONE	T1GVAL	T1GS	S<1:0>	198	
TMR1L	Holding Reg	gister for the	Least Signif	icant Byte of	f the 16-bit TMR	1 Register			193	
TMR1H	Holding Reg	gister for the	Most Signifi	cant Byte of	the 16-bit TMR1	Register			193	
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	125	
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB3 TRISB2 TRISB1 TRISB0		TRISB0	130	
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	134	
TRISD ⁽²⁾	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	137	
TRISE				—	(3)	TRISE2 ⁽²⁾	TRISE1 ⁽²⁾	TRISE0 ⁽²⁾	140	

TABLE 23-2: SUMMARY OF REGISTERS ASSOCIATED WITH CAPTURE

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by Capture mode.

Note 1: Applies to ECCP modules only.

2: These registers/bits are not implemented on PIC16(L)F1938 devices, read as '0'.

3: Unimplemented, read as '1'.

23.3.2 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for standard PWM operation:

- 1. Disable the CCPx pin output driver by setting the associated TRIS bit.
- 2. Timer2/4/6 resource selection:
 - Select the Timer2/4/6 resource to be used for PWM generation by setting the CxTSEL<1:0> bits in the CCPTMERSx register.
- 3. Load the PRx register with the PWM period value.
- Configure the CCP module for the PWM mode by loading the CCPxCON register with the appropriate values.
- Load the CCPRxL register and the DCxBx bits of the CCPxCON register, with the PWM duty cycle value.
- 6. Configure and start Timer2/4/6:
 - Clear the TMRxIF interrupt flag bit of the PIRx register. See Note below.
 - Configure the TxCKPS bits of the TxCON register with the Timer prescale value.
 - Enable the Timer by setting the TMRxON bit of the TxCON register.
- 7. Enable PWM output pin:
 - Wait until the Timer overflows and the TMRxIF bit of the PIRx register is set. See Note below.
 - Enable the CCPx pin output driver by clearing the associated TRIS bit.
- **Note:** In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then step 6 may be ignored.

23.3.3 TIMER2/4/6 TIMER RESOURCE

The PWM standard mode makes use of one of the 8-bit Timer2/4/6 timer resources to specify the PWM period.

Configuring the CxTSEL<1:0> bits in the CCPTMRSx register selects which Timer2/4/6 timer is used.

23.3.4 PWM PERIOD

The PWM period is specified by the PRx register of Timer2/4/6. The PWM period can be calculated using the formula of Equation 23-1.

EQUATION 23-1: PWM PERIOD

 $PWM Period = [(PRx) + 1] \bullet 4 \bullet TOSC \bullet$ (TMRx Prescale Value)

Note 1: Tosc = 1/Fosc

When TMRx is equal to PRx, the following three events occur on the next increment cycle:

- TMRx is cleared
- The CCPx pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is latched from CCPRxL into CCPRxH.

Note: The Timer postscaler (see Section 22.1 "Timer2/4/6 Operation") is not used in the determination of the PWM frequency.

23.3.5 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to multiple registers: CCPRxL register and DCxB<1:0> bits of the CCPxCON register. The CCPRxL contains the eight MSbs and the DCxB<1:0> bits of the CCPxCON register contain the two LSbs. CCPRxL and DCxB<1:0> bits of the CCPxCON register can be written to at any time. The duty cycle value is not latched into CCPRxH until after the period completes (i.e., a match between PRx and TMRx registers occurs). While using the PWM, the CCPRxH register is read-only.

Equation 23-2 is used to calculate the PWM pulse width.

Equation 23-3 is used to calculate the PWM duty cycle ratio.

EQUATION 23-2: PULSE WIDTH

 $Pulse Width = (CCPRxL:CCPxCON < 5:4>) \bullet$

TOSC • (TMRx Prescale Value)

EQUATION 23-3: DUTY CYCLE RATIO

 $Duty Cycle Ratio = \frac{(CCPRxL:CCPxCON < 5:4>)}{4(PRx + 1)}$

The CCPRxH register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

The 8-bit timer TMRx register is concatenated with either the 2-bit internal system clock (FOSC), or two bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2/4/6 prescaler is set to 1:1.

When the 10-bit time base matches the CCPRxH and 2-bit latch, then the CCPx pin is cleared (see Figure 23-4).

23.4.6.1 Steering Synchronization

The STRxSYNC bit of the PSTRxCON register gives the user two selections of when the steering event will happen. When the STRxSYNC bit is '0', the steering event will happen at the end of the instruction that writes to the PSTRxCON register. In this case, the output signal at the Px<D:A> pins may be an incomplete PWM waveform. This operation is useful when the user firmware needs to immediately remove a PWM signal from the pin.

When the STRxSYNC bit is '1', the effective steering update will happen at the beginning of the next PWM period. In this case, steering on/off the PWM output will always produce a complete PWM waveform.

Figures 23-19 and 23-20 illustrate the timing diagrams of the PWM steering depending on the STRxSYNC setting.

23.4.7 START-UP CONSIDERATIONS

When any PWM mode is used, the application hardware must use the proper external pull-up and/or pull-down resistors on the PWM output pins.

The CCPxM<1:0> bits of the CCPxCON register allow the user to choose whether the PWM output signals are active-high or active-low for each pair of PWM output pins (PxA/PxC and PxB/PxD). The PWM output polarities must be selected before the PWM pin output drivers are enabled. Changing the polarity configuration while the PWM pin output drivers are enable is not recommended since it may result in damage to the application circuits.

The PxA, PxB, PxC and PxD output latches may not be in the proper states when the PWM module is initialized. Enabling the PWM pin output drivers at the same time as the Enhanced PWM modes may cause damage to the application circuit. The Enhanced PWM modes must be enabled in the proper Output mode and complete a full PWM cycle before enabling the PWM pin output drivers. The completion of a full PWM cycle is indicated by the TMRxIF bit of the PIRx register being set as the second PWM period begins.

Note: When the microcontroller is released from Reset, all of the I/O pins are in the high-impedance state. The external circuits must keep the power switch devices in the Off state until the microcontroller drives the I/O pins with the proper signal levels or activates the PWM output(s).

FIGURE 23-19: EXAMPLE OF STEERING EVENT AT END OF INSTRUCTION (STRxSYNC = 0)



FIGURE 23-20: EXAMPLE OF STEERING EVENT AT BEGINNING OF INSTRUCTION (STRxSYNC = 1)



24.0 MASTER SYNCHRONOUS SERIAL PORT MODULE

24.1 Master SSP (MSSP) Module Overview

The Master Synchronous Serial Port (MSSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be Serial EEPROMs, shift registers, display drivers, A/D converters, etc. The MSSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I²C[™])

The SPI interface supports the following modes and features:

- Master mode
- · Slave mode
- Clock Parity
- Slave Select Synchronization (Slave mode only)
- Daisy-chain connection of slave devices

Figure 24-1 is a block diagram of the SPI Interface module.





24.2.2 SPI MODE OPERATION

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits (SSPCON1<5:0> and SSPSTAT<7:6>). These control bits allow the following to be specified:

- Master mode (SCK is the clock output)
- · Slave mode (SCK is the clock input)
- Clock Polarity (Idle state of SCK)
- Data Input Sample Phase (middle or end of data output time)
- Clock Edge (output data on rising/falling edge of SCK)
- Clock Rate (Master mode only)
- · Slave Select mode (Slave mode only)

To enable the serial port, SSP Enable bit, SSPEN of the SSPCON1 register, must be set. To reset or reconfigure SPI mode, clear the SSPEN bit, re-initialize the SSPCONx registers and then set the SSPEN bit. This configures the SDI, SDO, SCK and SS pins as serial port pins. For the pins to behave as the serial port function, some must have their data direction bits (in the TRIS register) appropriately programmed as follows:

- · SDI must have corresponding TRIS bit set
- · SDO must have corresponding TRIS bit cleared
- SCK (Master mode) must have corresponding TRIS bit cleared
- SCK (Slave mode) must have corresponding
 TRIS bit set
- SS must have corresponding TRIS bit set

Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value. The MSSP consists of a transmit/receive shift register (SSPSR) and a buffer register (SSPBUF). The SSPSR shifts the data in and out of the device, MSb first. The SSPBUF holds the data that was written to the SSPSR until the received data is ready. Once the eight bits of data have been received, that byte is moved to the SSPBUF register. Then, the Buffer Full Detect bit, BF of the SSPSTAT register, and the interrupt flag bit, SSPIF, are set. This double-buffering of the received data (SSPBUF) allows the next byte to start reception before reading the data that was just received. Any write to the SSPBUF register durina transmission/reception of data will be ignored and the write collision detect bit WCOL of the SSPCON1 register, will be set. User software must clear the WCOL bit to allow the following write(s) to the SSPBUF register to complete successfully.

When the application software is expecting to receive valid data, the SSPBUF should be read before the next byte of data to transfer is written to the SSPBUF. The Buffer Full bit, BF of the SSPSTAT register, indicates when SSPBUF has been loaded with the received data (transmission is complete). When the SSPBUF is read, the BF bit is cleared. This data may be irrelevant if the SPI is only a transmitter. Generally, the MSSP interrupt is used to determine when the transmission/reception has completed. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur.

The SSPSR is not directly readable or writable and can only be accessed by addressing the SSPBUF register. Additionally, the SSPSTAT register indicates the various Status conditions.



FIGURE 24-5: SPI MASTER/SLAVE CONNECTION

24.4.4 SDA HOLD TIME

The hold time of the SDA pin is selected by the SDAHT bit of the SSPCON3 register. Hold time is the time SDA is held valid after the falling edge of SCL. Setting the SDAHT bit selects a longer 300 ns minimum hold time and may help on buses with large capacitance.

TABLE 24-2: I²C BUS TERMS

TERM	Description					
Transmitter	The device which shifts data out onto the bus.					
Receiver	The device which shifts data in from the bus.					
Master	The device that initiates a transfer, generates clock signals and terminates a transfer.					
Slave	The device addressed by the master.					
Multi-master	A bus with more than one device that can initiate data transfers.					
Arbitration	Procedure to ensure that only one master at a time controls the bus. Winning arbitration ensures that the message is not corrupted.					
Synchronization	Procedure to synchronize the clocks of two or more devices on the bus.					
Idle	No master is controlling the bus, and both SDA and SCL lines are high.					
Active	Any time one or more master devices are controlling the bus.					
Addressed Slave	Slave device that has received a matching address and is actively being clocked by a master.					
Matching Address	Address byte that is clocked into a slave that matches the value stored in SSPADD.					
Write Request	Slave receives <u>a matching</u> address with R/W bit clear, and is ready to clock in data.					
Read Request	Master sends an address byte with the R/W bit set, indicating that it wishes to clock data out of the Slave. This data is the next and all following bytes until a Restart or Stop.					
Clock Stretching	When a device on the bus hold SCL low to stall communication.					
Bus Collision	Any time the SDA line is sampled low by the module while it is out- putting and expected high state.					

REGISTER 24-5: SSPMSK: SSP MASK REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1			
			MSK	<7:0>						
bit 7							bit 0			
Legend:										
R = Readable bit W = Writable bit				U = Unimpler	nented bit, read	l as '0'				
u = Bit is unchanged x = Bit is unknow			nown	-n/n = Value at POR and BOR/Value at all other Resets						
'1' = Bit is set		'0' = Bit is cle	ared							
bit 7-1	MSK<7:1>:	Mask bits								
	1 = The rec 0 = The rec	eived address b eived address b	it n is compar it n is not use	ed to SSPADD d to detect I ² C	<n> to detect l² address match</n>	C address mat	tch			
bit 0	 0 = The received address bit n is not used to detect I²C address match MSK<0>: Mask bit for I²C Slave mode, 10-bit Address I²C Slave mode, 10-bit address (SSPM<3:0> = 0111 or 1111): 1 = The received address bit 0 is compared to SSPADD<0> to detect I²C address match 0 = The received address bit 0 is not used to detect I²C address match 									

I²C Slave mode, 7-bit address, the bit is ignored

'0' = Bit is cleared

REGISTER 24-6: SSPADD: MSSP ADDRESS AND BAUD RATE REGISTER (I²C MODE)

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0		
			ADD	<7:0>					
bit 7							bit 0		
Legend:									
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'						d as '0'			
u = Bit is unch	anged	x = Bit is unkn	iown	n -n/n = Value at POR and BOR/Value at all other Res					

Master mode:

'1' = Bit is set

bit 7-0 ADD<7:0>: Baud Rate Clock Divider bits SCL pin clock period = ((ADD<7:0> + 1) *4)/Fosc

<u>10-Bit Slave mode – Most Significant Address Byte:</u>

- bit 7-3 **Not used:** Unused for Most Significant Address byte. Bit state of this register is a "don't care". Bit pattern sent by master is fixed by I²C specification and must be equal to '11110'. However, those bits are compared by hardware and are not affected by the value in this register.
- bit 2-1 ADD<2:1>: Two Most Significant bits of 10-bit address
- bit 0 Not used: Unused in this mode. Bit state is a "don't care".

10-Bit Slave mode – Least Significant Address Byte:

bit 7-0 ADD<7:0>: Eight Least Significant bits of 10-bit address

7-Bit Slave mode:

bit 0 Not used: Unused in this mode. Bit state is a "don't care".

25.4.2 AUTO-BAUD OVERFLOW

During the course of automatic baud detection, the ABDOVF bit of the BAUDCON register will be set if the baud rate counter overflows before the fifth rising edge is detected on the RX pin. The ABDOVF bit indicates that the counter has exceeded the maximum count that can fit in the 16 bits of the SPBRGH:SPBRGL register pair. After the ABDOVF has been set, the counter continues to count until the fifth rising edge is detected on the RX pin. Upon detecting the fifth RX edge, the hardware will set the RCIF interrupt flag and clear the ABDEN bit of the BAUDCON register. The RCIF flag can be subsequently cleared by reading the RCREG register. The ABDOVF flag of the BAUDCON register can be cleared by software directly.

To terminate the auto-baud process before the RCIF flag is set, clear the ABDEN bit then clear the ABDOVF bit of the BAUDCON register. The ABDOVF bit will remain set if the ABDEN bit is not cleared first.

25.4.3 AUTO-WAKE-UP ON BREAK

During Sleep mode, all clocks to the EUSART are suspended. Because of this, the Baud Rate Generator is inactive and a proper character reception cannot be performed. The Auto-Wake-up feature allows the controller to wake-up due to activity on the RX/DT line. This feature is available only in Asynchronous mode.

The Auto-Wake-up feature is enabled by setting the WUE bit of the BAUDCON register. Once set, the normal receive sequence on RX/DT is disabled, and the EUSART remains in an Idle state, monitoring for a wake-up event independent of the CPU mode. A wake-up event consists of a high-to-low transition on the RX/DT line. (This coincides with the start of a Sync Break or a wake-up signal character for the LIN protocol.)

The EUSART module generates an RCIF interrupt coincident with the wake-up event. The interrupt is generated synchronously to the Q clocks in normal CPU operating modes (Figure 25-7), and asynchronously if the device is in Sleep mode (Figure 25-8). The interrupt condition is cleared by reading the RCREG register.

The WUE bit is automatically cleared by the low-to-high transition on the RX line at the end of the Break. This signals to the user that the Break event is over. At this point, the EUSART module is in Idle mode waiting to receive the next character.

25.4.3.1 Special Considerations

Break Character

To avoid character errors or character fragments during a wake-up event, the wake-up character must be all zeros.

When the wake-up is enabled the function works independent of the low time on the data stream. If the WUE bit is set and a valid non-zero character is received, the low time from the Start bit to the first rising edge will be interpreted as the wake-up event. The remaining bits in the character will be received as a fragmented character and subsequent characters can result in framing or overrun errors.

Therefore, the initial character in the transmission must be all '0's. This must be 10 or more bit times, 13-bit times recommended for LIN bus, or any number of bit times for standard RS-232 devices.

Oscillator Start-up Time

Oscillator start-up time must be considered, especially in applications using oscillators with longer start-up intervals (i.e., LP, XT or HS/PLL mode). The Sync Break (or wake-up signal) character must be of sufficient length, and be followed by a sufficient interval, to allow enough time for the selected oscillator to start and provide proper initialization of the EUSART.

WUE Bit

The wake-up event causes a receive interrupt by setting the RCIF bit. The WUE bit is cleared in hardware by a rising edge on RX/DT. The interrupt condition is then cleared in software by reading the RCREG register and discarding its contents.

To ensure that no actual data is lost, check the RCIDL bit to verify that a receive operation is not in process before setting the WUE bit. If a receive operation is not occurring, the WUE bit may then be set just prior to entering the Sleep mode.

TABLE 30-2: OSCILLATOR PARAMETERS

Standard Operating Conditions (unless otherwise stated)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$											
Param No.	Sym.	Characteristic	Freq. Tolerance	Min.	Тур†	Max.	Units	Conditions			
OS08	HFosc	Internal Calibrated HFINTOSC Frequency ⁽¹⁾	±2% ±3%	_	16.0 16.0		MHz MHz	$\begin{array}{l} 0^{\circ}C \leq TA \leq +60^{\circ}C, \ VDD \geq 2.5V \\ 60^{\circ}C \leq TA \leq 85^{\circ}C, \ VDD \geq 2.5V \end{array}$			
			±5%	_	16.0	_	MHz	$-40^{\circ}C \leq T_A \leq +125^{\circ}C$			
OS08A	MFosc	Internal Calibrated MFINTOSC Frequency ⁽¹⁾	±2% ±3%	_	500 500	_	kHz kHz	$\begin{array}{l} 0^{\circ}C \leq TA \leq +60^{\circ}C, \ VDD \geq 2.5V \\ 60^{\circ}C \leq TA \leq 85^{\circ}C, \ VDD \geq 2.5V \end{array}$			
			±5%	_	500	_	kHz	$-40^{\circ}C \leq T_A \leq +125^{\circ}C$			
OS09	LFosc	Internal LFINTOSC Frequency	—		31	-	kHz	$-40^\circ C \le T_A \le +125^\circ C$			
OS10*	TIOSC ST	HFINTOSC Wake-up from Sleep Start-up Time MFINTOSC	_	_	3.2 24	8 35	μs μs				
		Wake-up from Sleep Start-up Time									

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

TABLE 30-3: PLL CLOCK TIMING SPECIFICATIONS (VDD = 2.7V TO 5.5V)

Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions
F10	Fosc	Oscillator Frequency Range	4	_	8	MHz	
F11	Fsys	On-Chip VCO System Frequency	16		32	MHz	
F12	TRC	PLL Start-up Time (Lock Time)	—	-	2	ms	
F13*	ΔCLK	CLKOUT Stability (Jitter)	-0.25%		+0.25%	%	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 30-7: CLKOUT AND I/O TIMING





FIGURE 30-12: PIC16(L)F1938/39 A/D CONVERSION TIMING (NORMAL MODE)





PIC16(L)F1938/9



FIGURE 31-66: COMPARATOR HYSTERESIS, LOW-POWER MODE (CxSP = 0, CxHYS = 1)



PIC16(L)F1938/9





44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units			MILLIMETERS			
Dimension	MIN	NOM	MAX				
Contact Pitch	E		0.80 BSC				
Contact Pad Spacing	C1		11.40				
Contact Pad Spacing	C2		11.40				
Contact Pad Width (X44)	X1			0.55			
Contact Pad Length (X44)	Y1			1.50			
Distance Between Pads	G	0.25					

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B

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