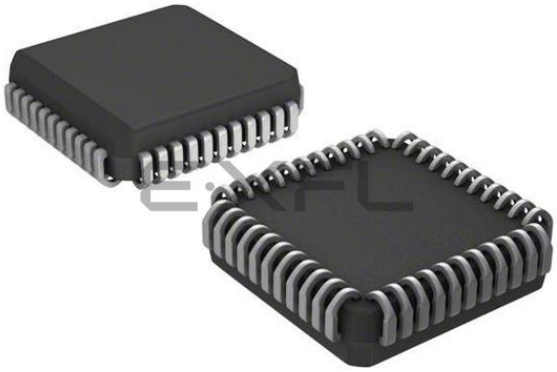
Microchip Technology - SST89E516RD2-40-C-NJE-T Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	36
Program Memory Size	72KB (72K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sst89e516rd2-40-c-nje-t

Table 1: Pin Descriptions (Continued) (2 of 3)

Symbol	Type[1]	Name and Functions
P3[7:0]	I/O with internal pull-up	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins are pulled high by the internal pull-ups when "1"s are written to them and can be used as inputs in this state. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Port 3 also receives some control signals and a partial of high-order address bits during the external host mode programming and verification.
P3[0]	I	**RXD:** Universal Asynchronous Receiver/Transmitter (UART) - Receive input
P3[1]	O	**TXD:** UART - Transmit output
P3[2]	I	**INT0#:** External Interrupt 0 Input
P3[3]	I	**INT1#:** External Interrupt 1 Input
P3[4]	I	**T0:** External count input to Timer/Counter 0
P3[5]	I	**T1:** External count input to Timer/Counter 1
P3[6]	O	**WR#:** External Data Memory Write strobe
P3[7]	O	**RD#:** External Data Memory Read strobe
PSEN#	I/O	**Program Store Enable:** PSEN# is the Read strobe to External Program Store. When the device is executing from Internal Program Memory, PSEN# is inactive (V_{OH}). When the device is executing code from External Program Memory, PSEN# is activated twice each machine cycle, except when access to External Data Memory while one PSEN# activation is skipped in each machine cycle. A forced high-to-low input transition on the PSEN# pin while the RST input is continually held high for more than ten machine cycles will cause the device to enter External Host mode for programming.
RST	I	**Reset:** While the oscillator is running, a high logic state on this pin for two machine cycles will reset the device. After a reset, if the PSEN# pin is driven by a high-to-low input transition while the RST input pin is held high, the device will enter the External Host mode, otherwise the device will enter the Normal operation mode.
EA#	I	**External Access Enable:** EA# must be driven to V_{IL} in order to enable the device to fetch code from the External Program Memory. EA# must be driven to V_{IH} for internal program execution. However, Security lock level 4 will disable EA#, and program execution is only possible from internal program memory. The EA# pin can tolerate a high voltage[2] of 12V.
ALE/ PROG#	I/O	**Address Latch Enable:** ALE is the output signal for latching the low byte of the address during an access to external memory. This pin is also the programming pulse input (PROG#) for flash programming. Normally the ALE[3] is emitted at a constant rate of 1/6 the crystal frequency[4] and can be used for external timing and clocking. One ALE pulse is skipped during each access to external data memory. However, if AO is set to 1, ALE is disabled.
P4[3:0][5]	I/O with internal pull-ups	**Port 4:** Port 4 is an 4-bit bi-directional I/O port with internal pull-ups. The port 4 output buffers can drive LS TTL inputs. Port 4 pins are pulled high by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, port 4 pins that are externally pulled low will source current because of the internal pull-ups.
P4[0]	I/O	Bit 0 of port 4
P4[1]	I/O	Bit 1 of port 4
P4[2] / INT3#	I/O	Bit 2 of port 4 / INT3# External interrupt 3 input

Memory Organization

The device has separate address spaces for program and data memory.

Program Flash Memory

There are two internal flash memory blocks in the device. The primary flash memory block (Block 0) has 64 KByte. The secondary flash memory block (Block 1) has 8 KByte. Since the total program address space is limited to 64 KByte, the SFCF[1:0] bit are used to control program bank selection. Please refer to Figure 6 for the program memory configuration. Program bank selection is described in the next section.

The 64K x8 primary SuperFlash block is organized as 512 sectors, each sector consists of 128 Bytes.

The 8K x8 secondary SuperFlash block is organized as 64 sectors, each sector consists also of 128 Bytes.

For both blocks, the 7 least significant program address bits select the byte within the sector. The remainder of the program address bits select the sector within the block.

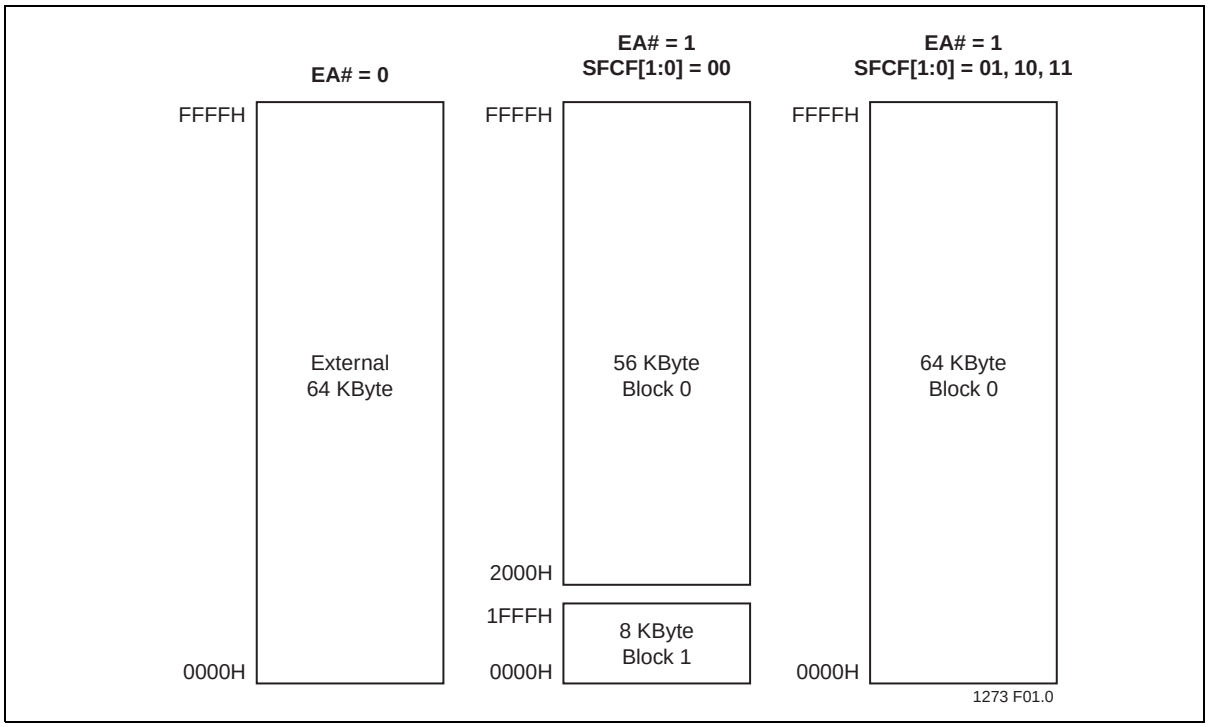

Figure 6: Program Memory Organization

Program Memory Block Switching

The program memory block switching feature of the device allows either Block 1 or the lowest 8 KByte of Block 0 to be used for the lowest 8 KByte of the program address space. SFCF[1:0] controls program memory block switching.

Table 2: SFCF Values for Program Memory Block Switching

SFCF[1:0]	Program Memory Block Switching
01, 10, 11	Block 1 is not visible to the program counter (PC). Block 1 is reachable only via in-application programming from 0000H - 1FFFH.
00	Block 1 is overlaid onto the low 8K of the program address space; occupying address locations 0000H - 1FFFH. When the PC falls within 0000H - 1FFFH, the instruction will be fetched from Block 1 instead of Block 0. Outside of 0000H - 1FFFH, Block 0 is used. Locations 0000H - 1FFFH of Block 0 are reachable through in-application programming.

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Reset Configuration of Program Memory Block Switching

Program memory block switching is initialized after reset according to the state of the Start-up Configuration bit SC0. The SC0 bit is programmed via an external host mode command or an IAP Mode command. See Table 14.

Once out of reset, the SFCF[0] bit can be changed dynamically by the program for desired effects. Changing SFCF[0] will not change the SC0 bit.

Caution must be taken when dynamically changing the SFCF[0] bit. Since this will cause different physical memory to be mapped to the logical program address space. The user must avoid executing block switching instructions within the address range 0000H to 1FFFH.

Table 3: SFCF Values Under Different Reset Conditions

	State of SFCF[1:0] after:		
SC0[1]	Power-on or External Reset	WDT Reset or Brown-out Reset	Software Reset
U (1)	00 (default)	x0	10
P (0)	01	x1	11

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1. P = Programmed (Bit logic state = 0),
   U = Unprogrammed (Bit logic state = 1)

Data RAM Memory

The data RAM has 1024 bytes of internal memory. The RAM can be addressed up to 64KB for external data memory.

Table 9: Timer/Counters SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB LSB								Reset Value
TMOD	Timer/Counter Mode Control	89H	Timer 1				Timer 0				00H
			GATE	C/T#	M1	M0	GATE	C/T#	M1	M0	
TCON[1]	Timer/Counter Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
TH0	Timer 0 MSB	8CH	TH0[7:0]								00H
TL0	Timer 0 LSB	8AH	TL0[7:0]								00H
TH1	Timer 1 MSB	8DH	TH1[7:0]								00H
TL1	Timer 1 LSB	8BH	TL1[7:0]								00H
T2CON[1]	Timer / Counter 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#	00H
T2MOD	Timer2 Mode Control	C9H	-	-	-	-	-	-	T2OE	DCEN	xxxxxx00b
TH2	Timer 2 MSB	CDH	TH2[7:0]								00H
TL2	Timer 2 LSB	CCH	TL2[7:0]								00H
RCAP2H	Timer 2 Capture MSB	CBH	RCAP2H[7:0]								00H
RCAP2L	Timer 2 Capture LSB	CAH	RCAP2L[7:0]								00H

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1. Bit Addressable SFRs

Table 11: PCA SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	RESET Value
CH CL	PCA Timer/Counter	F9H E9H	CH[7:0] CL[7:0]								00H 00H
CCON[1]	PCA Timer/Counter Control Register	D8H	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0	00x0000 0b
CMOD	PCA Timer/Counter Mode Register	D9H	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF	00xxx000 b
CCAP0H	PCA Module 0 Compare/Capture Registers	FAH	CCAP0H[7:0]								00H
CCAP0L		EAH	CCAP0L[7:0]								00H
CCAP1H	PCA Module 1 Compare/Capture Registers	FBH	CCAP1H[7:0]								00H
CCAP1L		EBH	CCAP1L[7:0]								00H
CCAP2H	PCA Module 2 Compare/Capture Registers	FCH	CCAP2H[7:0]								00H
CCAP2L		ECH	CCAP2L[7:0]								00H
CCAP3H	PCA Module 3 Compare/Capture Registers	FDH	CCAP3H[7:0]								00H
CCAP3L		EDH	CCAP3L[7:0]								00H
CCAP4H	PCA Module 4 Compare/Capture Registers	FEH	CCAP4H[7:0]								00H
CCAP4L		EEH	CCAP4L[7:0]								00H
CCAPM0	PCA Compare/Capture Module Mode Registers	DAH	-	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0	x000000 0b
CCAPM1		DBH	-	ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1	x000000 0b
CCAPM2		DCH	-	ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2	x000000 0b
CCAPM3		DDH	-	ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3	x000000 0b
CCAPM4		DEH	-	ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4	x000000 0b

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1. Bit Addressable SFRs

Interrupt Enable (IE)

Location	7	6	5	4	3	2	1	0	Reset Value
A8H	EA	EC	ET2	ES	ET1	EX1	ET0	EX0	00H

Symbol	Function
EA	Global Interrupt Enable. 0 = Disable 1 = Enable
EC	PCA Interrupt Enable.
ET2	Timer 2 Interrupt Enable.
ES	Serial Interrupt Enable.
ET1	Timer 1 Interrupt Enable.
EX1	External 1 Interrupt Enable.
ET0	Timer 0 Interrupt Enable.
EX0	External 0 Interrupt Enable.

Interrupt Enable A (IEA)

Location	7	6	5	4	3	2	1	0	Reset Value
E8H	-	-	-	-	EBO	-	-	-	xxxx0xxxb

Symbol	Function
EBO	Brown-out Interrupt Enable. 1 = Enable the interrupt 0 = Disable the interrupt

Auxiliary Register (AUXR)

Location	7	6	5	4	3	2	1	0	Reset Value
8EH	-	-	-	-	-	-	EXTRAM	AO	xxxxxx00b

Symbol Function

EXTRAM Internal/External RAM access
0: Internal Expanded RAM access within range of 00H to 2FFH using MOVX @Ri / @DPTR. Beyond 300H, the MCU always accesses external data memory.
For details, refer to Section , “Expanded Data RAM Addressing” .
1: External data memory access.

AO Disable/Enable ALE
0: ALE is emitted at a constant rate of 1/3 the oscillator frequency in 6 clock mode, 1/6 f_{OSC} in 12 clock mode.
1: ALE is active only during a MOVX or MOVC instruction.

Auxiliary Register 1 (AUXR1)

Location	7	6	5	4	3	2	1	0	Reset Value
A2H	-	-	-	-	GF2	0	-	DPS	xxxx00x0b

Symbol Function

GF2 General purpose user-defined flag.

DPS DPTR registers select bit.
0: DPTR0 is selected.
1: DPTR1 is selected.

Watchdog Timer Control Register (WDTC)

Location	7	6	5	4	3	2	1	0	Reset Value
C0H	-	-	-	WDOUT	WDRE	WDTS	WDT	SWDT	xxx00000b

Symbol Function

WDOUT Watchdog output enable.
0: Watchdog reset will not be exported on Reset pin.
1: Watchdog reset if enabled by WDRE, will assert Reset pin for 32 clocks.

WDRE Watchdog timer reset enable.
0: Disable watchdog timer reset.
1: Enable watchdog timer reset.

WDTS Watchdog timer reset flag.
0: External hardware reset or power-on reset clears the flag.
Flag can also be cleared by writing a 1.
Flag survives if chip reset happened because of watchdog timer overflow.
1: Hardware sets the flag on watchdog overflow.

WDT Watchdog timer refresh.
0: Hardware resets the bit when refresh is done.
1: Software sets the bit to force a watchdog timer refresh.

SWDT Start watchdog timer.
0: Stop WDT.
1: Start WDT.

Watchdog Timer Data/Reload Register (WDTD)

Location	7	6	5	4	3	2	1	0	Reset Value
85H	Watchdog Timer Data/Reload								00H

Symbol	Function
WDTD	Initial/Reload value in Watchdog Timer. New value won't be effective until WDT is set.

PCA Timer/Counter Control Register[1] (CCON)

Location	7	6	5	4	3	2	1	0	Reset Value
D8H	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0	00x00000b

1. Bit addressable

Symbol	Function
CF	PCA Counter Overflow Flag Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software, but can only cleared by software.
CR	PCA Counter Run control bit Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.
-	Not implemented, reserved for future use. **Note:** User should not write '1's to reserved bits. The value read from a reserved bit is indeterminate.
CCF4	PCA Module 4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF3	PCA Module 3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF2	PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF1	PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF0	PCA Module 0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.

SPI Control Register (SPCR)

Location	7	6	5	4	3	2	1	0	Reset Value
D5H	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	00H

Symbol **Function**

SPIE If both SPIE and ES are set to one, SPI interrupts are enabled.

SPE SPI enable bit.
0: Disables SPI.
1: Enables SPI and connects SS#, MOSI, MISO, and SCK to pins P1.4, P1.5, P1.6, P1.7.

DORD Data Transmission Order.
0: MSB first in data transmission.
1: LSB first in data transmission.

MSTR Master/Slave select.
0: Selects Slave mode.
1: Selects Master mode.

CPOL Clock Polarity
0: SCK is low when idle (Active High).
1: SCK is high when idle (Active Low).

CPHA Clock Phase control bit. The CPHA bit with the CPOL bit control the clock and data relationship between master and slave. See Figures 21 and 22.
0: Shift triggered on the leading edge of the clock.
1: Shift triggered on the trailing edge of the clock.

SPR1, SPR0SPI Clock Rate Select bits. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, f_{OSC}, is as follows:

SPR1	SPR0	SCK = f_{OSC} divided by
0	0	4
0	1	16
1	0	64
1	1	128

SPI Status Register (SPSR)

Location	7	6	5	4	3	2	1	0	Reset Value
AAH	SPIF	WCOL	-	-	-	-	-	-	00xxxxxxb

Symbol **Function**

SPIF SPI Interrupt Flag.
Upon completion of data transfer, this bit is set to 1.
If SPIE =1 and ES =1, an interrupt is then generated.
This bit is cleared by software.

WCOL Write Collision Flag.
Set if the SPI data register is written to during data transfer.
This bit is cleared by software.

External Interrupt Control (XICON)

Location	7	6	5	4	3	2	1	0	Reset Value
AEH	-	EX3	IE3	IT3	0	EX2	IE2	IT2	00H

Symbol	Function
EX2	External Interrupt 2 Enable bit if set
IE2	Interrupt Enable If IT2=1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced.
IT2	External Interrupt 2 is falling-edge/low-level triggered when this bit is cleared by software.
EX3	External Interrupt 3 Enable bit if set
IE3	Interrupt Enable If IT3=1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced.
IT3	External Interrupt3 is falling-edge/low-level triggered when this bit is cleared by software.

Serial I/O

Full-Duplex, Enhanced UART

The device serial I/O port is a full-duplex port that allows data to be transmitted and received simultaneously in hardware by the transmit and receive registers, respectively, while the software is performing other tasks. The transmit and receive registers are both located in the Serial Data Buffer (SBUF) special function register. Writing to the SBUF register loads the transmit register, and reading from the SBUF register obtains the contents of the receive register.

The UART has four modes of operation which are selected by the Serial Port Mode Specifier (SM0 and SM1) bits of the Serial Port Control (SCON) special function register. In all four modes, transmission is initiated by any instruction that uses the SBUF register as a destination register. Reception is initiated in mode 0 when the Receive Interrupt (RI) flag bit of the Serial Port Control (SCON) SFR is cleared and the Reception Enable/ Disable (REN) bit of the SCON register is set. Reception is initiated in the other modes by the incoming start bit if the REN bit of the SCON register is set.

Framing Error Detection

Framing Error Detection is a feature, which allows the receiving controller to check for valid stop bits in modes 1, 2, or 3. Missing stops bits can be caused by noise in serial lines or from simultaneous transmission by two CPUs.

Framing Error Detection is selected by going to the PCON register and changing SMOD0 = 1 (see Figure 17). If a stop bit is missing, the Framing Error bit (FE) will be set. Software may examine the FE bit after each reception to check for data errors. After the FE bit has been set, it can only be cleared by software. Valid stop bits do not clear FE. When FE is enabled, RI rises on the stop bit, instead of the last data bit (see Figure 18 and Figure 19).

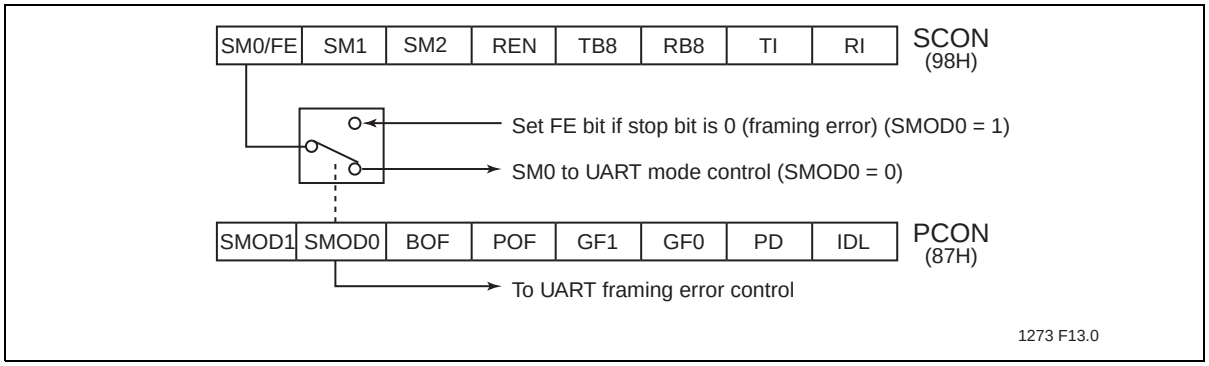

Figure 17: Framing Error Block Diagram

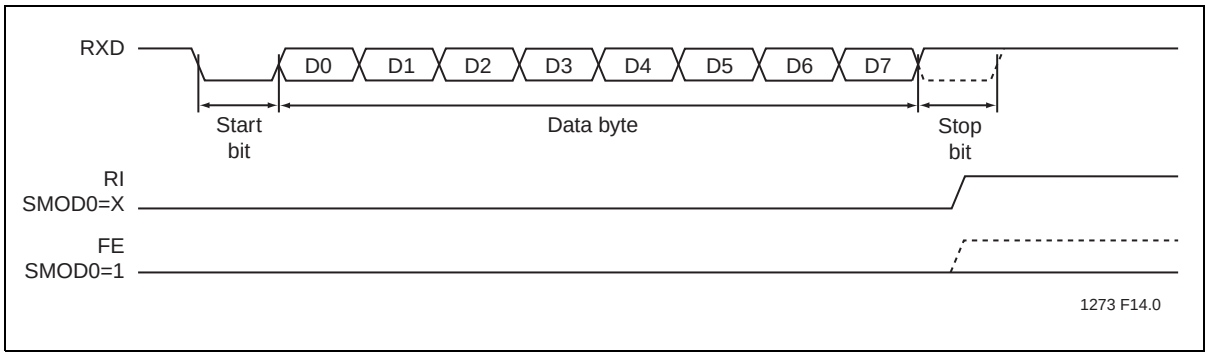

Figure 18: UART Timings in Mode 1

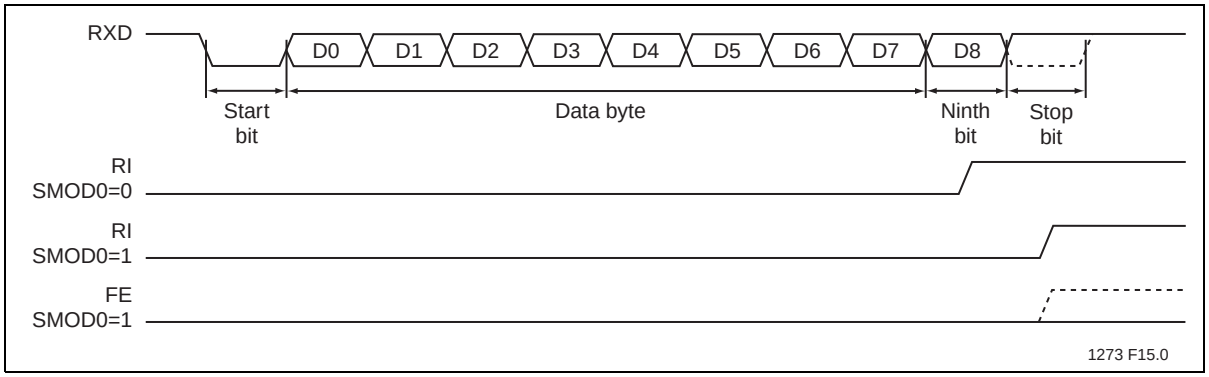

Figure 19: UART Timings in Modes 2 and 3

Automatic Address Recognition

Automatic Address Recognition helps to reduce the MCU time and power required to talk to multiple serial devices. Each device is hooked together sharing the same serial link with its own address. In this configuration, a device is only interrupted when it receives its own address, thus eliminating the software overhead to compare addresses.

This same feature helps to save power because it can be used in conjunction with idle mode to reduce the system's overall power consumption. Since there may be multiple slaves hooked up serial to one master, only one slave would have to be interrupted from idle mode to respond to the master's transmission. Automatic Address Recognition (AAR) allows the other slaves to remain in idle mode while only one is interrupted. By limiting the number of interruptions, the total current draw on the system is reduced.

There are two ways to communicate with slaves: a group of them at once, or all of them at once. To communicate with a group of slaves, the master sends out an address called the given address. To communicate with all the slaves, the master sends out an address called the "broadcast" address.

AAR can be configured as mode 2 or 3 (9-bit modes) and setting the SM2 bit in SCON. Each slave has its own SM2 bit set waiting for an address byte (9th bit = 1). The Receive Interrupt (RI) flag will only be set when the received byte matches either the given address or the broadcast address. Next, the slave then clears its SM2 bit to enable reception of the data bytes (9th bit = 0) from the master. When the 9th bit = 1, the master is sending an address. When the 9th bit = 0, the master is sending actual data.

Serial Peripheral Interface

SPI Features

- Master or slave operation
- 10 MHz bit frequency (max)
- LSB first or MSB first data transfer
- Four programmable bit rates
- End of transmission (SPIF)
- Write collision flag protection (WCOL)
- Wake up from idle mode (slave mode only)

SPI Description

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the SST89E/V516RDx and peripheral devices or between several SST89E/V516RDx devices.

Figure 20 shows the correspondence between master and slave SPI devices. The SCK pin is the clock output and input for the master and slave modes, respectively. The SPI clock generator will start following a write to the master devices SPI data register. The written data is then shifted out of the MOSI pin on the master device into the MOSI pin of the slave device. Following a complete transmission of one byte of data, the SPI clock generator is stopped and the SPIF flag is set. An SPI interrupt request will be generated if the SPI Interrupt Enable bit (SPIE) and the Serial Port Interrupt Enable bit (ES) are both set.

An external master drives the Slave Select input pin, SS#/P1[4], low to select the SPI module as a slave. If SS#/P1[4] has not been driven low, then the slave SPI unit is not active and the MOSI/P1[5] port can also be used as an input port pin.

CPHA and CPOL control the phase and polarity of the SPI clock. Figures 21 and 22 show the four possible combinations of these two bits.

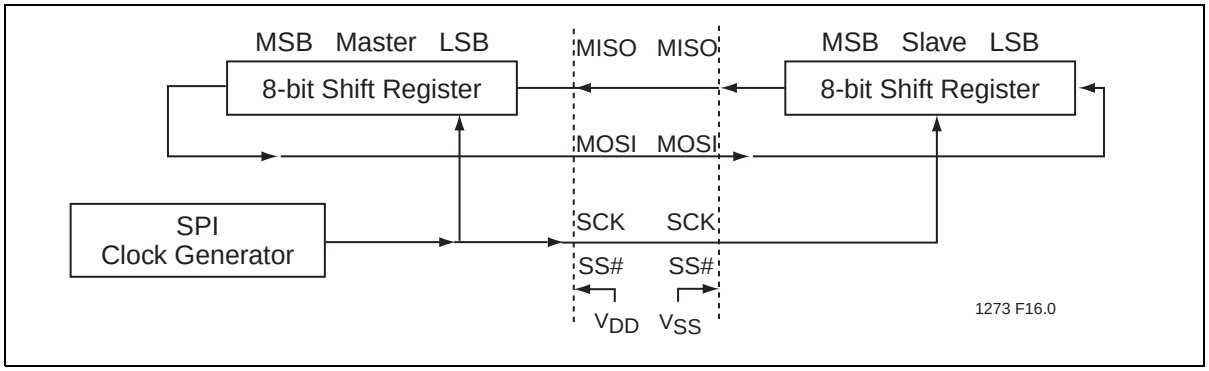

Figure 20: SPI Master-slave Interconnection

Watchdog Timer

The device offers a programmable Watchdog Timer (WDT) for fail safe protection against software deadlock and automatic recovery.

To protect the system against software deadlock, the user software must refresh the WDT within a user-defined time period. If the software fails to do this periodical refresh, an internal hardware reset will be initiated if enabled (WDRE= 1). The software can be designed such that the WDT times out if the program does not work properly.

The WDT in the device uses the system clock (XTAL1) as its time base. So strictly speaking, it is a watchdog counter rather than a watchdog timer. The WDT register will increment every 344,064 crystal clocks. The upper 8-bits of the time base register (WDTD) are used as the reload register of the WDT.

The WDTS flag bit is set by WDT overflow and is not changed by WDT reset. User software can clear WDTS by writing “1” to it.

Figure 23 provides a block diagram of the WDT. Two SFRs (WDTC and WDTD) control watchdog timer operation. During idle mode, WDT operation is temporarily suspended, and resumes upon an interrupt exit from idle.

The time-out period of the WDT is calculated as follows:

Period = (255 - WDTD) * 344064 * $1/f_{CLK\ (XTAL1)}$

where WDTD is the value loaded into the WDTD register and f_{OSC} is the oscillator frequency.

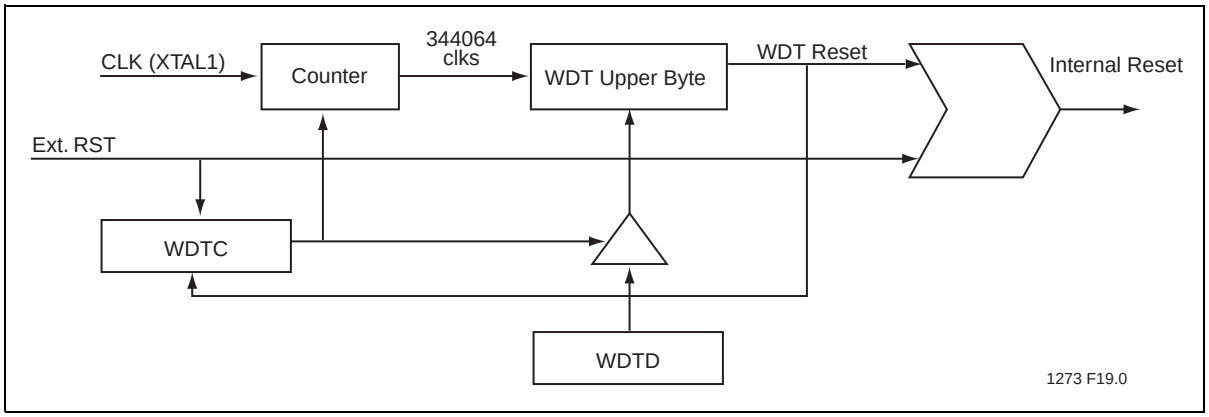

Figure 23: Block Diagram of Programmable Watchdog Timer

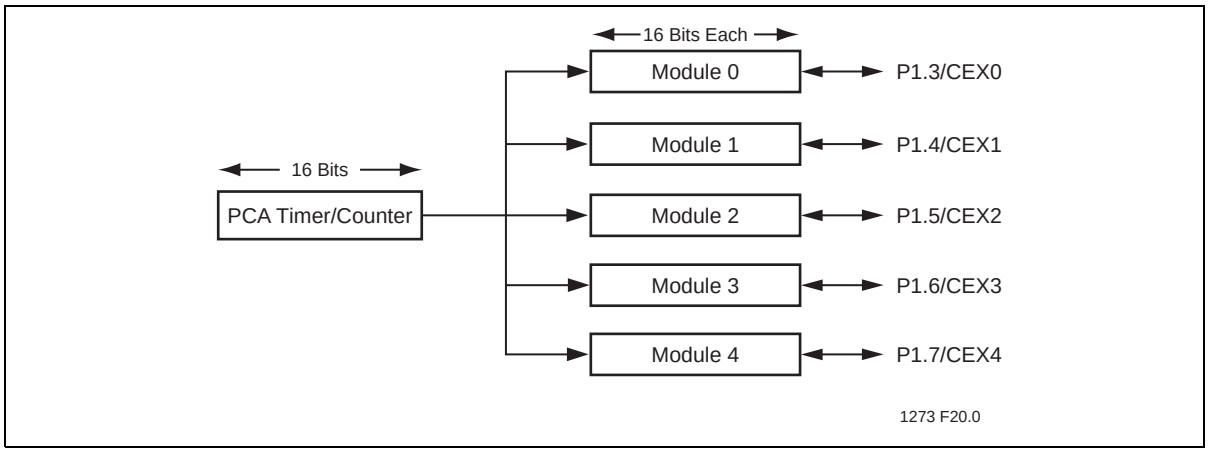

Figure 24: PCA Timer/Counter and Compare/Capture Modules

The table below summarizes various clock inputs at two common frequencies.

Table 19: PCA Timer/Counter Inputs

PCA Timer/Counter Mode	Clock Increments	
	12 MHz	**16 MHz**
Mode 0: $f_{OSC}/12$	1 µsec	0.75 µsec
Mode 1:	330 nsec	250 nsec
Mode 2: Timer 0 Overflows[1]		
Timer 0 programmed in:		
8-bit mode	256 µsec	192 µsec
16-bit mode	65 msec	49 µsec
8-bit auto-reload	1 to 255 µsec	0.75 to 191 µsec
Mode 3: External Input MAX	0.66 µsec	0.50 µsec

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1. In Mode 2, the overflow interrupt for Timer 0 does not need to be enabled.

The four possible CMOD timer modes with and without the overflow interrupt enabled are shown below. This list assumes that PCA will be left running during idle mode.

Table 20: CMOD Values

PCA Count Pulse Selected	CMOD Value	
	Without Interrupt Enabled	**With Interrupt Enabled**
Internal clock, $f_{OSC}/12$	00H	01H
Internal clock, $f_{OSC}/4$	02H	03H
Timer 0 overflow	04H	05H
External clock at P1.2	06H	07H

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The CCON register is associated with all PCA timer functions. It contains run control bits and flags for the PCA timer (CF) and all modules. To run the PCA the CR bit (CCON.6) must be set by software. Clearing the bit, will turn off PCA. When the PCA counter overflows, the CF (CCON.7) will be set, and

16-Bit Software Timer Mode

The 16-bit software timer mode is used to trigger interrupt routines, which must occur at periodic intervals. It is setup by setting both the ECOM and MAT bits in the module's CCAPMn register. The PCA timer will be compared to the module's capture registers (CCAPnL and CCAPnH) and when a match occurs, an interrupt will occur, if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set.

If necessary, a new 16-bit compare value can be loaded into CCAPnH and CCAPnL during the interrupt routine. The user should be aware that the hardware temporarily disables the comparator function while these registers are being updated so that an invalid match will not occur. Thus, it is recommended that the user write to the low byte first (CCAPnL) to disable the comparator, then write to the high byte (CCAPnH) to re-enable it. If any updates to the registers are done, the user may want to hold off any interrupts from occurring by clearing the EA bit. (See Figure 26)

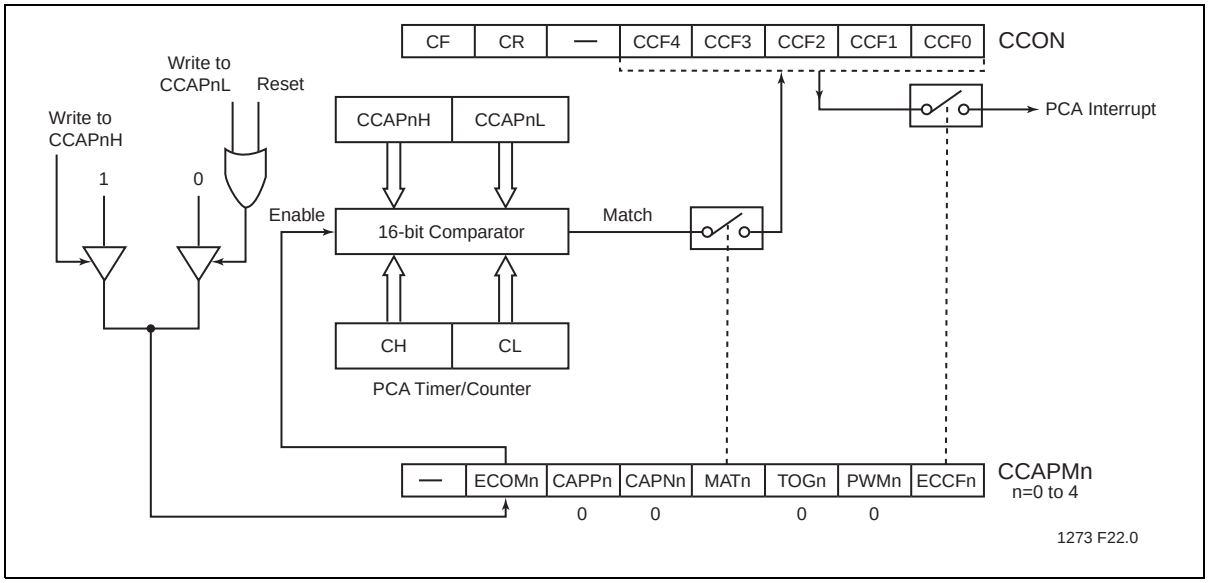

Figure 26: PCA Compare Mode (Software Timer)

High Speed Output Mode

The high speed output mode is used to toggle a port pin when a match occurs between the PCA timer and the preloaded value in the compare registers. In this mode, the CEX output pin (on port 1) associated with the PCA module will toggle every time there is a match between the PCA counter (CH and CL) and the capture registers (CCAPnH and CCAPnL). To activate this mode, the user must set TOG, MAT, and ECOM bits in the module's CCAPMn SFR.

High speed output mode is much more accurate than toggling pins since the toggle occurs before branching to an interrupt. In this case, interrupt latency will not affect the accuracy of the output. When using high speed output, using an interrupt is optional. Only if the user wishes to change the time for the next toggle is it necessary to update the compare registers. Otherwise, the next toggle will occur when the PCA timer rolls over and matches the last compare value. (See Figure 27)

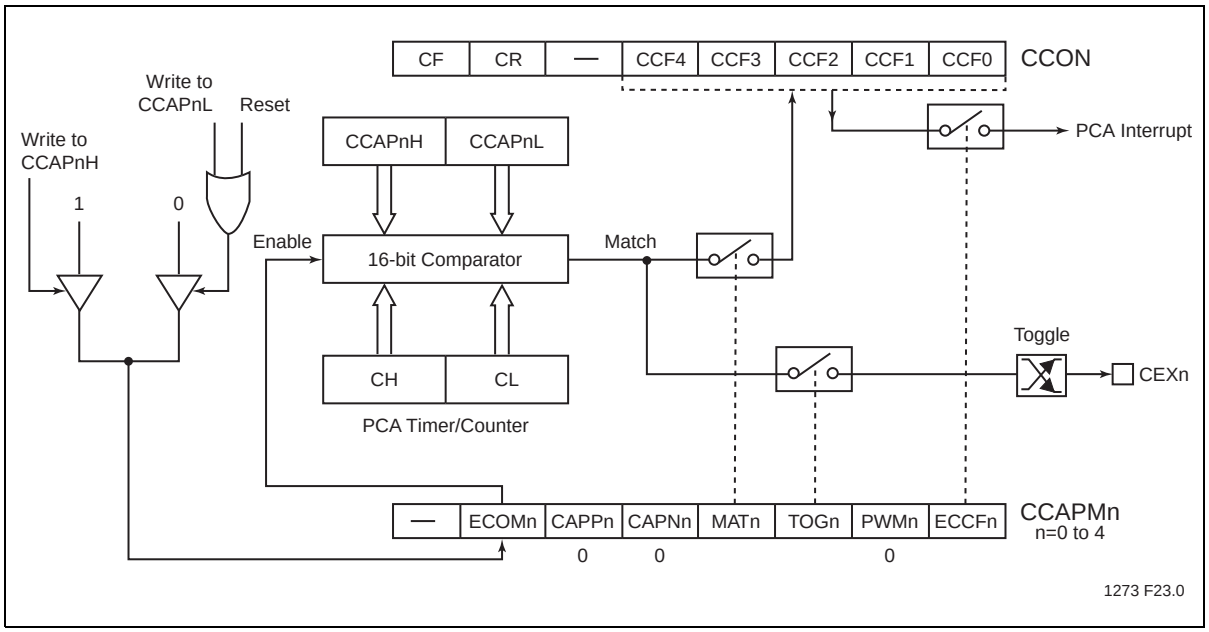

Figure 27: PCA High Speed Output Mode

Pulse Width Modulator

The Pulse Width Modulator (PWM) mode is used to generate 8-bit PWMs by comparing the low byte of the PCA timer (CL) with the low byte of the compare register (CCAPnL). When CL < CCAPnL the output is low. When CL ≥ CCAPnL the output is high. To activate this mode, the user must set the PWM and ECOM bits in the module's CCAPMn SFR. (See Figure 28 and Table 24)

In PWM mode, the frequency of the output depends on the source for the PCA timer. Since there is only one set of CH and CL registers, all modules share the PCA timer and frequency. Duty cycle of the output is controlled by the value loaded into the high byte (CCAPnH). Since writes to the CCAPnH register are asynchronous, a new value written to the high byte will not be shifted into CCAPnL for comparison until the next period of the output (when CL rolls over from 255 to 00).

To calculate values for CCAPnH for any duty cycle, use the following equation:

CCAPnH = 256(1 - Duty Cycle)

where CCAPnH is an 8-bit integer and Duty Cycle is a fraction.

Watchdog Timer

The Watchdog Timer mode is used to improve reliability in the system without increasing chip count (See Figure 29). Watchdog Timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. It can also be used to prevent a software deadlock. If during the execution of the user's code, there is a deadlock, the Watchdog Timer will time out and an internal reset will occur. Only module 4 can be programmed as a Watchdog Timer (but still can be programmed to other modes if the Watchdog Timer is not used).

To use the Watchdog Timer, the user pre-loads a 16-bit value in the compare register. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven high.

In order to hold off the reset, the user has three options:

1. periodically change the compare value so it will never match the PCA timer,
2. periodically change the PCA timer value so it will never match the compare values, or
3. disable the watchdog timer by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the Watchdog Timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for all modules; changing the time base for other modules would not be a good idea. Thus, in most application the first solution is the best option.

Use the code below to initialize the Watchdog Timer. Module 4 can be configured in either compare mode, and the WDTE bit in CMOD must also be set. The user's software then must periodically change (CCAP4H, CCAP4L) to keep a match from occurring with the PCA timer (CH, CL). This code is given in the Watchdog routine below.

```
;===========================================

Init_Watchdog:

MOVCCAPM4, #4CH; Module 4 in compare mode

MOVCCAP4L, #0FFH; Write to low byte first

MOVCCAP4H, #0FFH; Before PCA timer counts up
; to FFFF Hex, these compare
; values must be changed.

ORLCMOD, #40H; Set the WDTE bit to enable the
; watchdog timer without
; changing the other bits in
; CMOD

;===========================================

;Main program goes here, but call WATCHDOG periodically.

;===========================================

WATCHDOG:
```

Valid Combinations

Valid combinations for SST89E516RD2

SST89E516RD2-40-C-NJE	SST89E516RD2-40-C-TQJE
SST89E516RD2-40-I-NJE	SST89E516RD2-40-I-TQJE

Valid combinations for SST89V516RD2

SST89V516RD2-33-C-NJE	SST89V516RD2-33-C-TQJE
SST89V516RD2-33-I-NJE	SST89V516RD2-33-I-TQJE

Valid combinations for SST89E516RD

SST89E516RD-40-C-PIE	SST89E516RD-40-C-QIF
	SST89E516RD-40-I-QIF

Valid combinations for SST89V516RD

SST89V516RD-33-C-PIE	SST89V516RD-33-C-QIF
	SST89V516RD-33-I-QIF

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

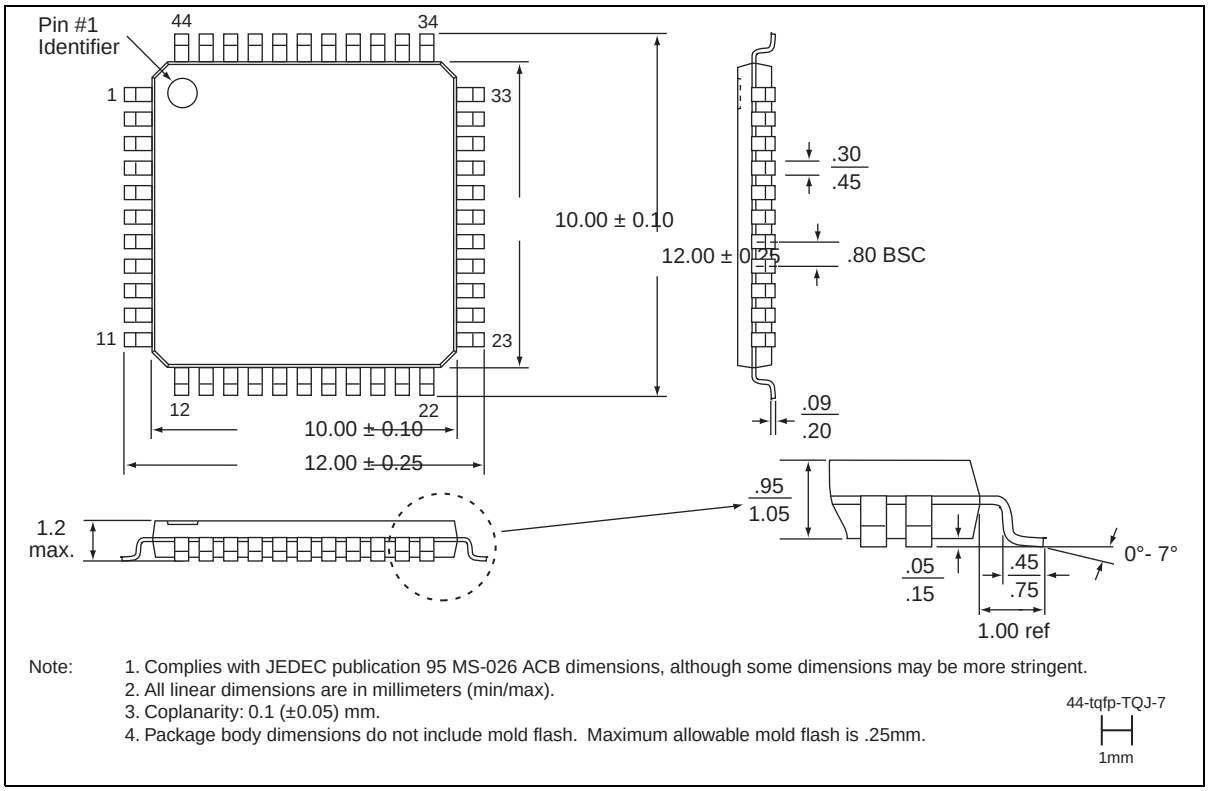

Figure 50: 44-lead Thin Quad Flat Pack (TQFP)
SST Package Code: TQJ