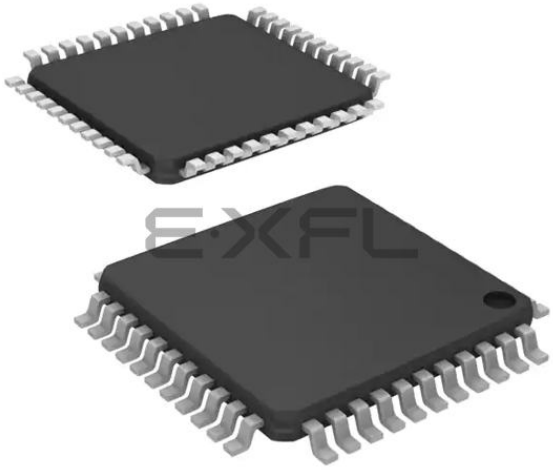

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	36
Program Memory Size	72KB (72K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sst89e516rd2-40-c-tqje

Functional Blocks

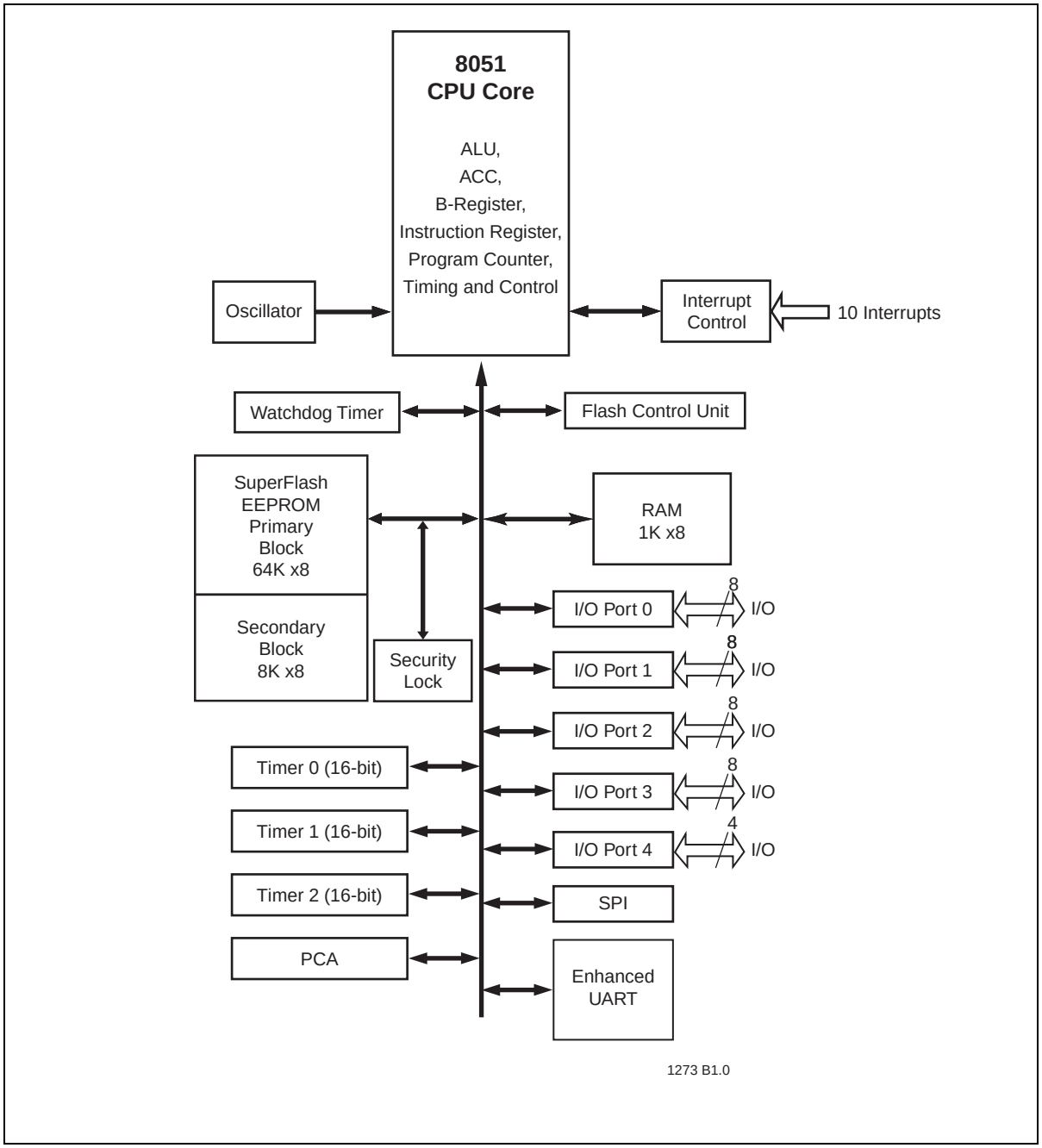

Figure 1: Functional Block Diagram

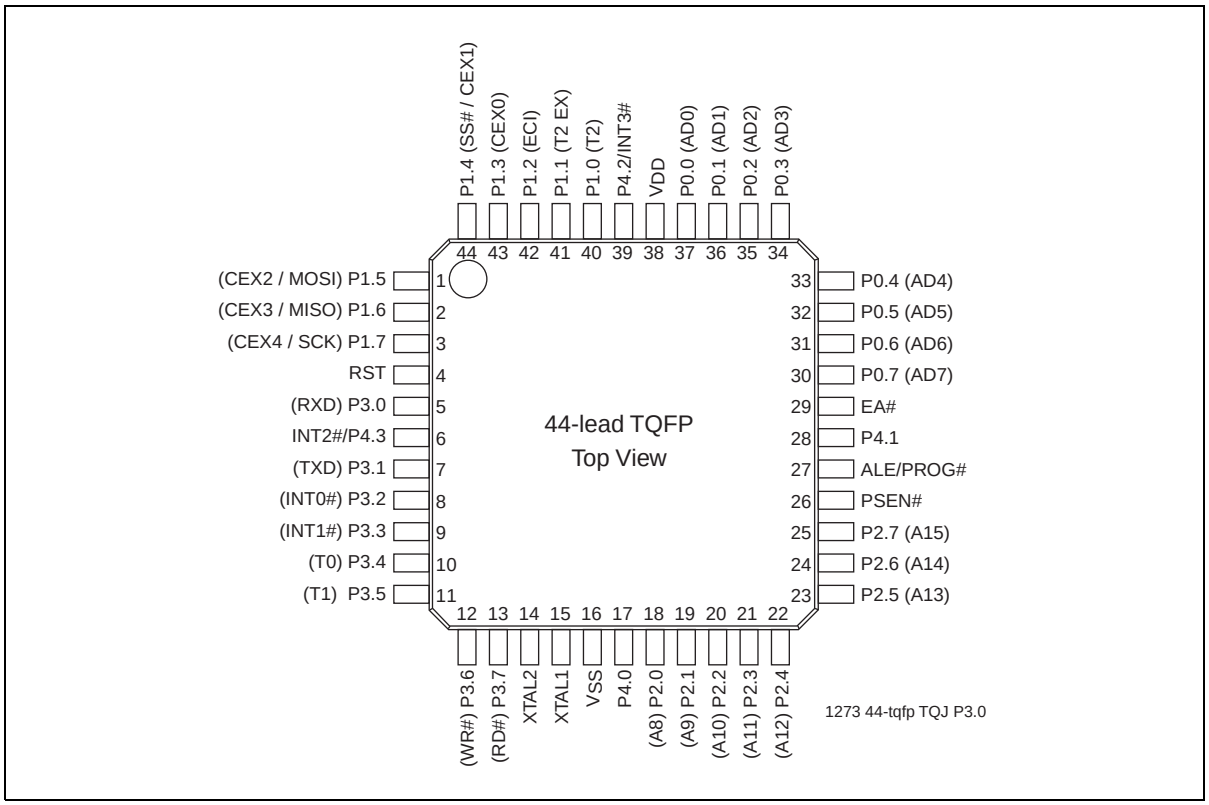

Figure 4: Pin Assignments for 44-lead TQFP

Table 1: Pin Descriptions (Continued) (2 of 3)

Symbol	Type[1]	Name and Functions
P3[7:0]	I/O with internal pull-up	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins are pulled high by the internal pull-ups when "1"s are written to them and can be used as inputs in this state. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Port 3 also receives some control signals and a partial of high-order address bits during the external host mode programming and verification.
P3[0]	I	**RXD:** Universal Asynchronous Receiver/Transmitter (UART) - Receive input
P3[1]	O	**TXD:** UART - Transmit output
P3[2]	I	**INT0#:** External Interrupt 0 Input
P3[3]	I	**INT1#:** External Interrupt 1 Input
P3[4]	I	**T0:** External count input to Timer/Counter 0
P3[5]	I	**T1:** External count input to Timer/Counter 1
P3[6]	O	**WR#:** External Data Memory Write strobe
P3[7]	O	**RD#:** External Data Memory Read strobe
PSEN#	I/O	**Program Store Enable:** PSEN# is the Read strobe to External Program Store. When the device is executing from Internal Program Memory, PSEN# is inactive (V_{OH}). When the device is executing code from External Program Memory, PSEN# is activated twice each machine cycle, except when access to External Data Memory while one PSEN# activation is skipped in each machine cycle. A forced high-to-low input transition on the PSEN# pin while the RST input is continually held high for more than ten machine cycles will cause the device to enter External Host mode for programming.
RST	I	**Reset:** While the oscillator is running, a high logic state on this pin for two machine cycles will reset the device. After a reset, if the PSEN# pin is driven by a high-to-low input transition while the RST input pin is held high, the device will enter the External Host mode, otherwise the device will enter the Normal operation mode.
EA#	I	**External Access Enable:** EA# must be driven to V_{IL} in order to enable the device to fetch code from the External Program Memory. EA# must be driven to V_{IH} for internal program execution. However, Security lock level 4 will disable EA#, and program execution is only possible from internal program memory. The EA# pin can tolerate a high voltage[2] of 12V.
ALE/ PROG#	I/O	**Address Latch Enable:** ALE is the output signal for latching the low byte of the address during an access to external memory. This pin is also the programming pulse input (PROG#) for flash programming. Normally the ALE[3] is emitted at a constant rate of 1/6 the crystal frequency[4] and can be used for external timing and clocking. One ALE pulse is skipped during each access to external data memory. However, if AO is set to 1, ALE is disabled.
P4[3:0][5]	I/O with internal pull-ups	**Port 4:** Port 4 is an 4-bit bi-directional I/O port with internal pull-ups. The port 4 output buffers can drive LS TTL inputs. Port 4 pins are pulled high by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, port 4 pins that are externally pulled low will source current because of the internal pull-ups.
P4[0]	I/O	Bit 0 of port 4
P4[1]	I/O	Bit 1 of port 4
P4[2] / INT3#	I/O	Bit 2 of port 4 / INT3# External interrupt 3 input

Program Memory Block Switching

The program memory block switching feature of the device allows either Block 1 or the lowest 8 KByte of Block 0 to be used for the lowest 8 KByte of the program address space. SFCF[1:0] controls program memory block switching.

Table 2: SFCF Values for Program Memory Block Switching

SFCF[1:0]	Program Memory Block Switching
01, 10, 11	Block 1 is not visible to the program counter (PC). Block 1 is reachable only via in-application programming from 0000H - 1FFFH.
00	Block 1 is overlaid onto the low 8K of the program address space; occupying address locations 0000H - 1FFFH. When the PC falls within 0000H - 1FFFH, the instruction will be fetched from Block 1 instead of Block 0. Outside of 0000H - 1FFFH, Block 0 is used. Locations 0000H - 1FFFH of Block 0 are reachable through in-application programming.

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Reset Configuration of Program Memory Block Switching

Program memory block switching is initialized after reset according to the state of the Start-up Configuration bit SC0. The SC0 bit is programmed via an external host mode command or an IAP Mode command. See Table 14.

Once out of reset, the SFCF[0] bit can be changed dynamically by the program for desired effects. Changing SFCF[0] will not change the SC0 bit.

Caution must be taken when dynamically changing the SFCF[0] bit. Since this will cause different physical memory to be mapped to the logical program address space. The user must avoid executing block switching instructions within the address range 0000H to 1FFFH.

Table 3: SFCF Values Under Different Reset Conditions

	State of SFCF[1:0] after:		
SC0[1]	Power-on or External Reset	WDT Reset or Brown-out Reset	Software Reset
U (1)	00 (default)	x0	10
P (0)	01	x1	11

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1. P = Programmed (Bit logic state = 0),
   U = Unprogrammed (Bit logic state = 1)

Data RAM Memory

The data RAM has 1024 bytes of internal memory. The RAM can be addressed up to 64KB for external data memory.

Table 6: CPU related SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
ACC[1]	Accumulator	E0H	ACC[7:0]								00H
B[1]	B Register	F0H	B[7:0]								00H
PSW[1]	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00H
SP	Stack Pointer	81H	SP[7:0]								07H
DPL	Data Pointer Low	82H	DPL[7:0]								00H
DPH	Data Pointer High	83H	DPH[7:0]								00H
IE[1]	Interrupt Enable	A8H	EA	EC	ET2	ES	ET1	EX1	ET0	EX0	00H
IEA[1]	Interrupt Enable A	E8H	-	-	-	-	EBO	-	-	-	xxxx0xxx b
IP[1]	Interrupt Priority Reg	B8H	-	PPC	PT2	PS	PT1	PX1	PT0	PX0	x0000000 b
IPH	Interrupt Priority Reg High	B7H	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	x0000000 b
IP1[1]	Interrupt Priority Reg A	F8H	-	-	-	-	PBO	PX3	PX2	-	xxxx0xxx b
IP1H	Interrupt Priority Reg A High	F7H	-	-	-	-	PBOH	PX3H	PX2H	-	xxxx0xxx b
PCON	Power Control	87H	SMOD1	SMOD0	BOF	POF	GF1	GF0	PD	IDL	00010000 b
AUXR	Auxiliary Reg	8EH	-	-	-	-	-	-	EXTRAM	AO	xxxxxxx0 0b
AUXR1	Auxiliary Reg 1	A2H	-	-	-	-	GF2	0	-	DPS	xxxx00x0 b
XICON	External Interrupt Control	AEH	-	EX3	IE3	IT3	0	EX2	IE2	IT2	00H

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1. Bit Addressable SFRs

Table 11: PCA SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	RESET Value
CH CL	PCA Timer/Counter	F9H E9H	CH[7:0] CL[7:0]								00H 00H
CCON[1]	PCA Timer/Counter Control Register	D8H	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0	00x0000 0b
CMOD	PCA Timer/Counter Mode Register	D9H	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF	00xxx000 b
CCAP0H	PCA Module 0 Compare/Capture Registers	FAH	CCAP0H[7:0]								00H
CCAP0L		EAH	CCAP0L[7:0]								00H
CCAP1H	PCA Module 1 Compare/Capture Registers	FBH	CCAP1H[7:0]								00H
CCAP1L		EBH	CCAP1L[7:0]								00H
CCAP2H	PCA Module 2 Compare/Capture Registers	FCH	CCAP2H[7:0]								00H
CCAP2L		ECH	CCAP2L[7:0]								00H
CCAP3H	PCA Module 3 Compare/Capture Registers	FDH	CCAP3H[7:0]								00H
CCAP3L		EDH	CCAP3L[7:0]								00H
CCAP4H	PCA Module 4 Compare/Capture Registers	FEH	CCAP4H[7:0]								00H
CCAP4L		EEH	CCAP4L[7:0]								00H
CCAPM0	PCA Compare/Capture Module Mode Registers	DAH	-	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0	x000000 0b
CCAPM1		DBH	-	ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1	x000000 0b
CCAPM2		DCH	-	ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2	x000000 0b
CCAPM3		DDH	-	ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3	x000000 0b
CCAPM4		DEH	-	ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4	x000000 0b

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1. Bit Addressable SFRs

SPI Control Register (SPCR)

Location	7	6	5	4	3	2	1	0	Reset Value
D5H	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	00H

Symbol **Function**

SPIE If both SPIE and ES are set to one, SPI interrupts are enabled.

SPE SPI enable bit.
0: Disables SPI.
1: Enables SPI and connects SS#, MOSI, MISO, and SCK to pins P1.4, P1.5, P1.6, P1.7.

DORD Data Transmission Order.
0: MSB first in data transmission.
1: LSB first in data transmission.

MSTR Master/Slave select.
0: Selects Slave mode.
1: Selects Master mode.

CPOL Clock Polarity
0: SCK is low when idle (Active High).
1: SCK is high when idle (Active Low).

CPHA Clock Phase control bit. The CPHA bit with the CPOL bit control the clock and data relationship between master and slave. See Figures 21 and 22.
0: Shift triggered on the leading edge of the clock.
1: Shift triggered on the trailing edge of the clock.

SPR1, SPR0SPI Clock Rate Select bits. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, f_{OSC}, is as follows:

SPR1	SPR0	SCK = f_{OSC} divided by
0	0	4
0	1	16
1	0	64
1	1	128

SPI Status Register (SPSR)

Location	7	6	5	4	3	2	1	0	Reset Value
AAH	SPIF	WCOL	-	-	-	-	-	-	00xxxxxxb

Symbol **Function**

SPIF SPI Interrupt Flag.
Upon completion of data transfer, this bit is set to 1.
If SPIE =1 and ES =1, an interrupt is then generated.
This bit is cleared by software.

WCOL Write Collision Flag.
Set if the SPI data register is written to during data transfer.
This bit is cleared by software.

External Interrupt Control (XICON)

Location	7	6	5	4	3	2	1	0	Reset Value
AEH	-	EX3	IE3	IT3	0	EX2	IE2	IT2	00H

Symbol	Function
EX2	External Interrupt 2 Enable bit if set
IE2	Interrupt Enable If IT2=1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced.
IT2	External Interrupt 2 is falling-edge/low-level triggered when this bit is cleared by software.
EX3	External Interrupt 3 Enable bit if set
IE3	Interrupt Enable If IT3=1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced.
IT3	External Interrupt3 is falling-edge/low-level triggered when this bit is cleared by software.

Prog-SC0

Prog-SC0 command is used to program the SC0 bit. This command only changes the SC0 bit and has no effect on BSEL bit until after a reset cycle.

SC0 bit previously in un-programmed state can be programmed by this command. The Prog-SC0 command should reside only in Block 1 or external code memory.

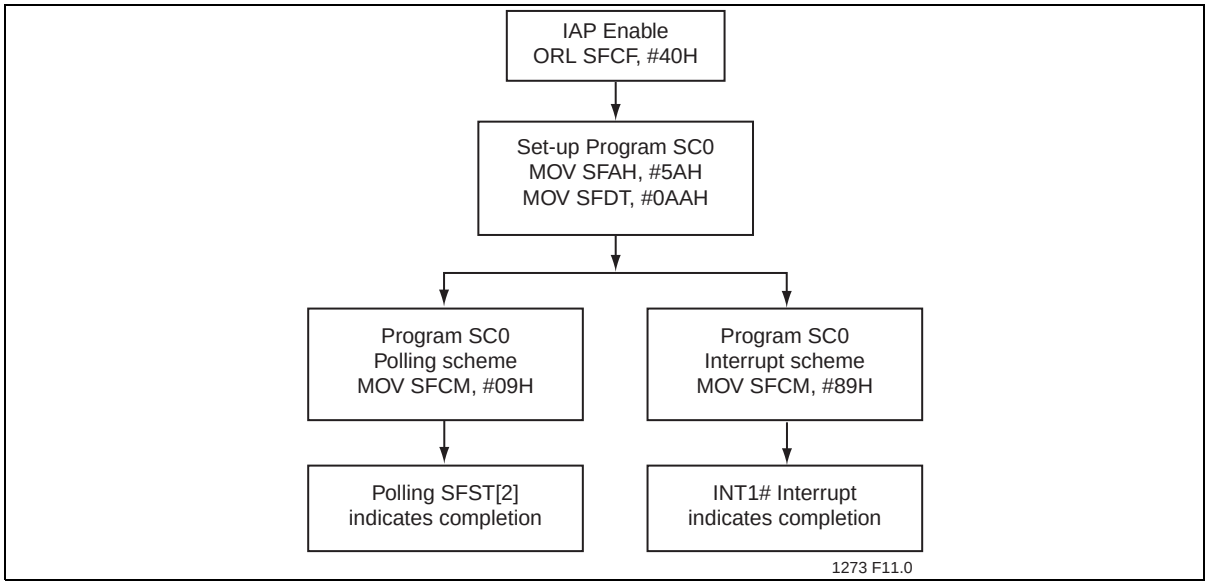

Figure 15: Prog-SC0

Enable-Clock-Double

Enable-Clock-Double command is used to make the MCU run at 6 clocks per machine cycle. The standard (default) is 12 clocks per machine cycle (i.e. clock double command disabled).

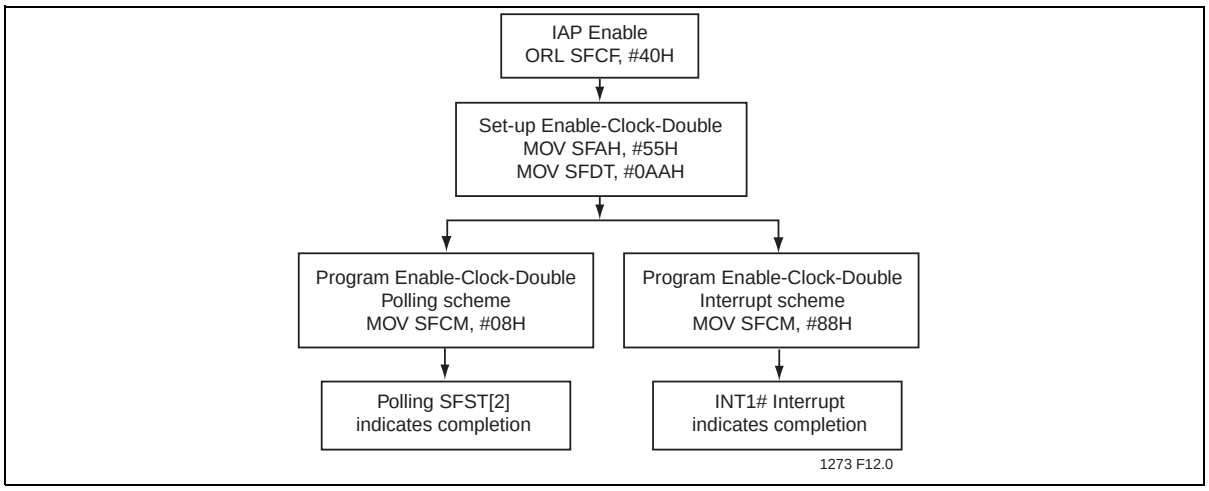

Figure 16: Enable-Clock-Double

There are no IAP counterparts for the external host commands Select-Block0 and Select-Block1.

Table 22: PCA Module Modes

Without Interrupt enabled								
-[1]	ECOMy[2]	CAPPy[2]	CAPNy[2]	MATy[2]	TOGy[2]	PWMy[2]	ECCFy[2]	Module Code
-	0	0	0	0	0	0	0	No Operation
-	0	1	0	0	0	0	0	16-bit capture on positive-edge trigger at CEX[4:0]
-	0	0	1	0	0	0	0	16-bit capture on negative-edge trigger at CEX[4:0]
-	0	1	1	0	0	0	0	16-bit capture on positive/negative-edge trigger at CEX[4:0]
-	1	0	0	1	0	0	0	Compare: software timer
-	1	0	0	1	1	0	0	Compare: high-speed output
-	1	0	0	0	0	1	0	Compare: 8-bit PWM
-	1	0	0	1	0 or 1[3]	0	0	Compare: PCA WDT (CCAPM4 only)[4]

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1. User should not write ‘1’s to reserved bits. The value read from a reserved bit is indeterminate.
2. y = 0, 1, 2, 3, 4
3. A 0 disables toggle function. A 1 enables toggle function on CEX[4:0] pin.
4. For PCA WDT mode, also set the WDTE bit in the CMOD register to enable the reset output signal.

Table 23: PCA Module Modes

With Interrupt enabled								
-[1]	ECOMy[2]	CAPPy[2]	CAPNy[2]	MATy[2]	TOGy[2]	PWMy[2]	ECCFy[2]	Module Code
-	0	1	0	0	0	0	1	16-bit capture on positive-edge trigger at CEX[4:0]
-	0	0	1	0	0	0	1	16-bit capture on negative-edge trigger at CEX[4:0]
-	0	1	1	0	0	0	1	16-bit capture on positive/negative-edge trigger at CEX[4:0]
-	1	0	0	1	0	0	1	Compare: software timer
-	1	0	0	1	1	0	1	Compare: high-speed output
-	1	0	0	0	0	1	X[3]	Compare: 8-bit PWM
-	1	0	0	1	0 or 1[4]	0	X[5]	Compare: PCA WDT (CCAPM4 only)[6]

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1. User should not write ‘1’s to reserved bits. The value read from a reserved bit is indeterminate.
2. y = 0, 1, 2, 3, 4
3. No PCA interrupt is needed to generate the PWM.
4. A 0 disables toggle function. A 1 enables toggle function on CEX[4:0] pin.
5. Enabling an interrupt for the Watchdog Timer would defeat the purpose of the Watchdog Timer.
6. For PCA WDT mode, also set the WDTE bit in the CMOD register to enable the reset output signal.

Capture Mode

Capture mode is used to capture the PCA timer/counter value into a module's capture registers (CCAPnH and CCAPnL). The capture will occur on a positive edge, negative edge, or both on the corresponding module's pin. To use one of the PCA modules in the capture mode, either one or both the CCAPM bits CAPN and CAPP for that module must be set. When a valid transition occurs on the CEX pin corresponding to the module used, the PCA hardware loads the 16-bit value of the PCA counter register (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set, then an interrupt will be generated. In the interrupt service routine, the 16-bit capture value must be saved in RAM before the next event capture occurs. If a subsequent capture occurred, the original capture values would be lost. After flag event flag has been set by hardware, the user must clear the flag in software. (See Figure 25)

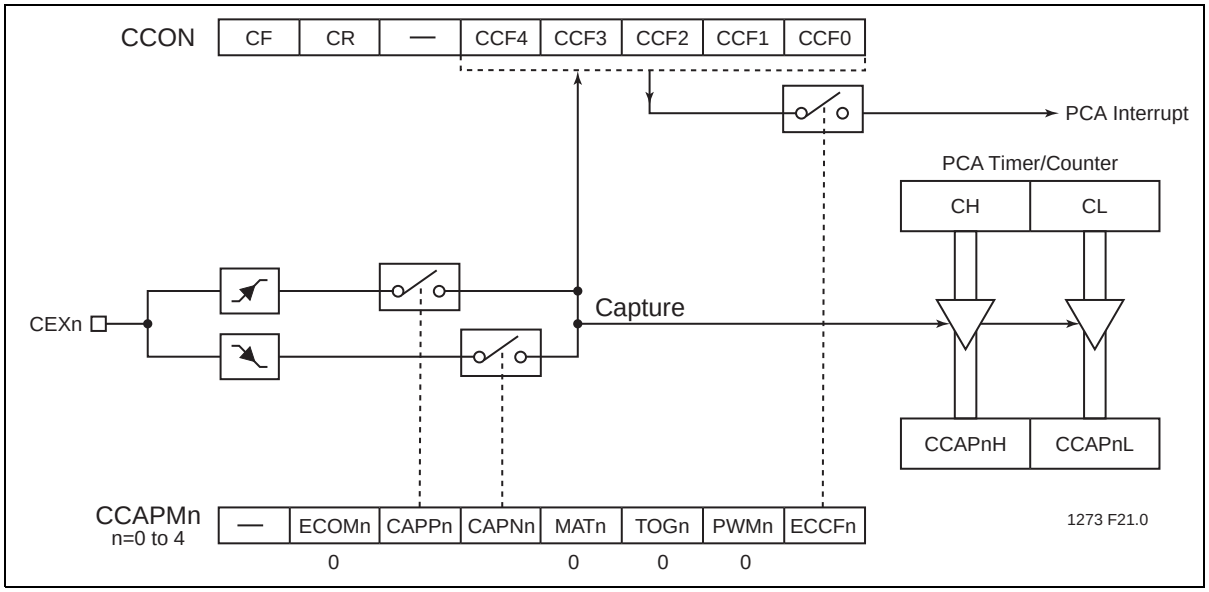

Figure 25: PCA Capture Mode

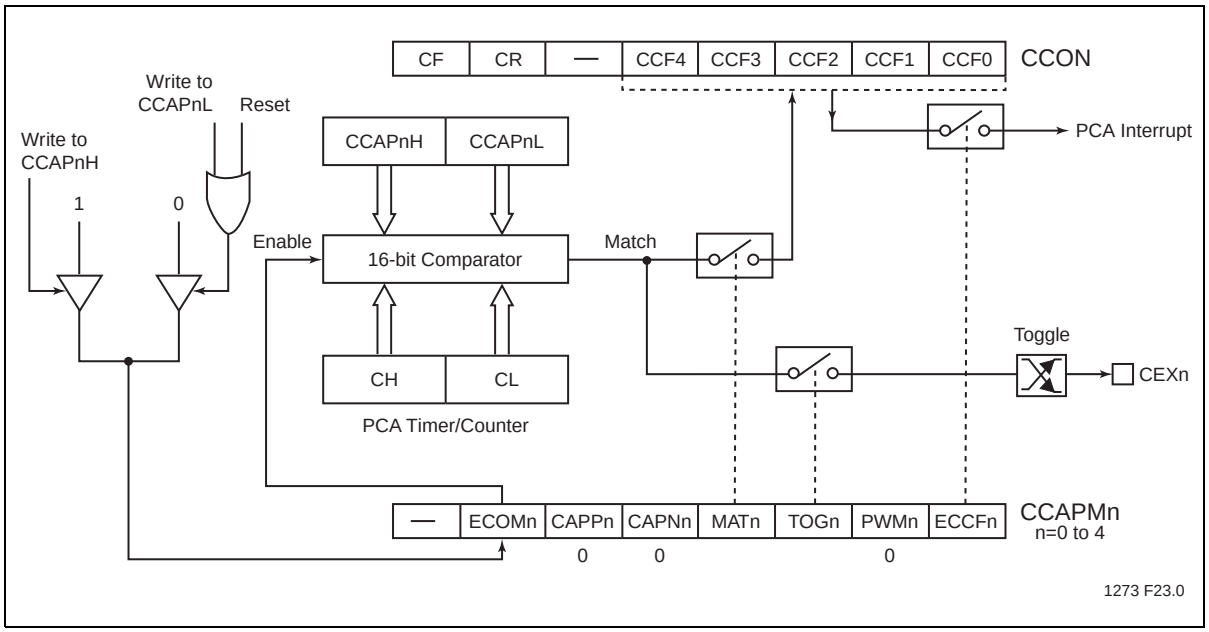

Figure 27: PCA High Speed Output Mode

Pulse Width Modulator

The Pulse Width Modulator (PWM) mode is used to generate 8-bit PWMs by comparing the low byte of the PCA timer (CL) with the low byte of the compare register (CCAPnL). When CL < CCAPnL the output is low. When CL ≥ CCAPnL the output is high. To activate this mode, the user must set the PWM and ECOM bits in the module's CCAPMn SFR. (See Figure 28 and Table 24)

In PWM mode, the frequency of the output depends on the source for the PCA timer. Since there is only one set of CH and CL registers, all modules share the PCA timer and frequency. Duty cycle of the output is controlled by the value loaded into the high byte (CCAPnH). Since writes to the CCAPnH register are asynchronous, a new value written to the high byte will not be shifted into CCAPnL for comparison until the next period of the output (when CL rolls over from 255 to 00).

To calculate values for CCAPnH for any duty cycle, use the following equation:

CCAPnH = 256(1 - Duty Cycle)

where CCAPnH is an 8-bit integer and Duty Cycle is a fraction.

Watchdog Timer

The Watchdog Timer mode is used to improve reliability in the system without increasing chip count (See Figure 29). Watchdog Timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. It can also be used to prevent a software deadlock. If during the execution of the user's code, there is a deadlock, the Watchdog Timer will time out and an internal reset will occur. Only module 4 can be programmed as a Watchdog Timer (but still can be programmed to other modes if the Watchdog Timer is not used).

To use the Watchdog Timer, the user pre-loads a 16-bit value in the compare register. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven high.

In order to hold off the reset, the user has three options:

1. periodically change the compare value so it will never match the PCA timer,
2. periodically change the PCA timer value so it will never match the compare values, or
3. disable the watchdog timer by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the Watchdog Timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for all modules; changing the time base for other modules would not be a good idea. Thus, in most application the first solution is the best option.

Use the code below to initialize the Watchdog Timer. Module 4 can be configured in either compare mode, and the WDTE bit in CMOD must also be set. The user's software then must periodically change (CCAP4H, CCAP4L) to keep a match from occurring with the PCA timer (CH, CL). This code is given in the Watchdog routine below.

```
;===========================================

Init_Watchdog:

MOVCCAPM4, #4CH; Module 4 in compare mode

MOVCCAP4L, #0FFH; Write to low byte first

MOVCCAP4H, #0FFH; Before PCA timer counts up
; to FFFF Hex, these compare
; values must be changed.

ORLCMOD, #40H; Set the WDTE bit to enable the
; watchdog timer without
; changing the other bits in
; CMOD

;===========================================

;Main program goes here, but call WATCHDOG periodically.

;===========================================

WATCHDOG:
```

```
CLR EA; Hold off interrupts

MOVCCAP4L, #00; Next compare value is within

MOVCCAP4H, CH; 65,535 counts of the
; current PCA

SETBEA; timer value

RET

;===========================================
```

This routine should not be part of an interrupt service routine. If the program counter goes astray and gets stuck in an infinite loop, interrupts will still be serviced and the watchdog will keep getting reset. Thus, the purpose of the watchdog would be defeated. Instead, call this subroutine from the main program of the PCA timer.

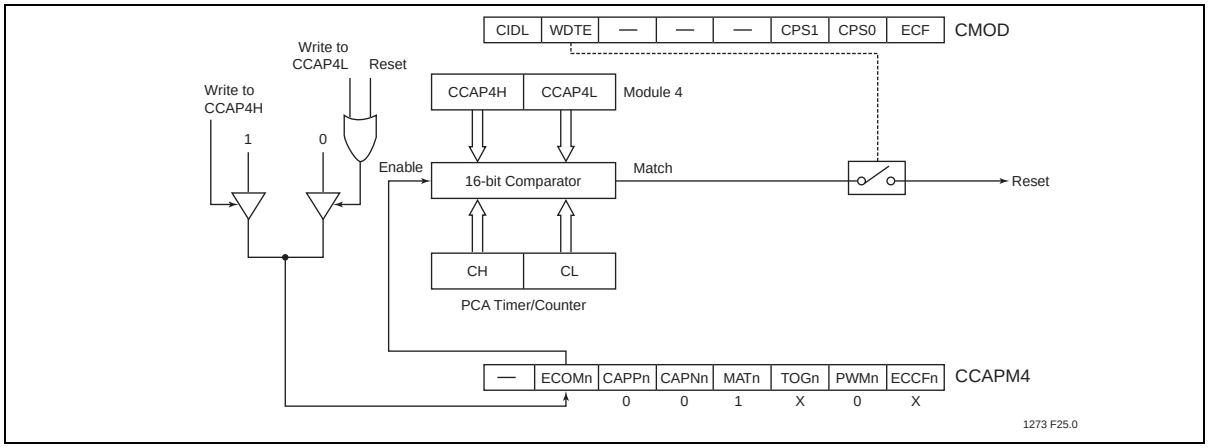

Figure 29: PCA Watchdog Timer (Module 4 only)

Table 26: Security Lock Access Table

Level	SFST[7:5]	Source Address[1]	Target Address[2]	Byte-Verify Allowed		MOVC Allowed
				External Host[3]	IAP	516RDx
1	000b (unlock)	Block 0	Block 0	Y	N	Y
			Block 1	Y	Y	Y
			External	N/A	N/A	N
		Block 1	Block 0	Y	Y	Y
			Block 1	Y	N	Y
			External	N/A	N/A	N
		External	Block 0/1	Y	Y	N
			External	N/A	N/A	Y

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1. Location of MOVC or IAP instruction
2. Target address is the location of the byte being read
3. External host Byte-Verify access does not depend on a source address.

Electrical Specification

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Ambient Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on EA# Pin to V_{SS} . . . . . -0.5V to +14.0V
D.C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20ns) on Any Other Pin to V_{SS} . . . . . -1.0V to V_{DD}+1.0V
Maximum I_{OL} per I/O Pins P1.5, P1.6, P1.7 . . . . . 20mA
Maximum I_{OL} per I/O for All Other Pins 15mA
Package Power Dissipation Capability (T_A = 25°C) 1.5W
Through Hole Lead Soldering Temperature (10 Seconds) . . . . . 300°C
Surface Mount Solder Reflow Temperature[1] . . . . . 260°C for 10 seconds
Output Short Circuit Current[2] . . . . . 50 mA

1. Excluding certain with-Pb 32-PLCC units, all packages are 260°C capable in both non-Pb and with-Pb solder versions. Certain with-Pb 32-PLCC package types are capable of 240°C for 10 seconds; please consult the factory for the latest information.
2. Outputs shorted for no more than one second. No more than one output shorted at a time.
(Based on package heat transfer limitations, not device power consumption.

Note: This specification contains preliminary information on new products in production.
The specifications are subject to change without notice.

Table 31: Operating Range

Symbol	Description	Min.	Max	Unit
T_A	Ambient Temperature Under Bias			
	Standard	0	+70	°C
	Industrial	-40	+85	°C
V_{DD}	Supply Voltage			
	SST89E516RDx	4.5	5.5	V
	SST89V516RDx	2.7	3.6	V
f_{OSC}	Oscillator Frequency			
	SST89E516RDx	0	40	MHz
	SST89V516RDx	0	33	MHz
	Oscillator Frequency for IAP			
	SST89E516RDx	.25	40	MHz
	SST89V516RDx	.25	33	MHz

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1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 15mA
   Maximum I_{OL} per 8-bit port: 26mA
   Maximum I_{OL} total for all outputs: 71mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification.
   Pins are not guaranteed to sink current greater than the listed test conditions.
2. Capacitive loading on Ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and Ports 1 & 3. The noise due to external bus capacitance discharging into the Port 0 & 2 pins when the pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
3. Load capacitance for Port 0, ALE & PSEN#= 100pF, load capacitance for all other outputs = 80pF.
4. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and PSEN# to momentarily fall below the V_{DD} - 0.7 specification when the address bits are stabilizing.
5. Pins of Ports 1, 2, and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
6. Pin capacitance is characterized but not tested. EA# is 25pF (max).

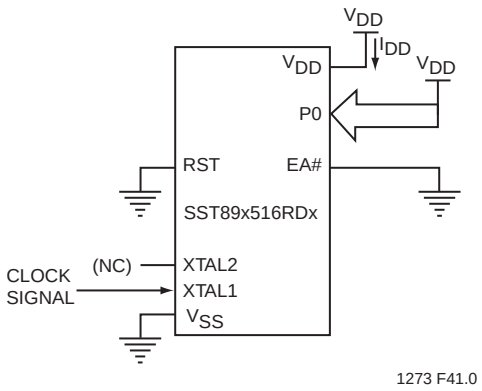

Figure 45: I_{DD} Test Condition, Idle Mode

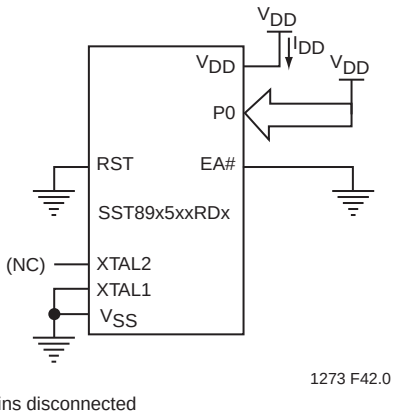

Figure 46: I_{DD} Test Condition, Power-down Mode

Table 41: Flash Memory Programming/Verification Parameters[1]

Parameter[2]	Max	Units
Chip-Erase Time	150	ms
Block-Erase Time	100	ms
Sector-Erase Time	30	ms
Byte-Program Time[3]	50	µs
Select-Block Program Time	500	ns
Re-map or Security bit Program Time	80	µs

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1. For IAP operations, the program execution overhead must be added to the above timing parameters.
2. Program and Erase times will scale inversely proportional to programming clock frequency.
3. Each byte must be erased before programming.

Packaging Diagrams

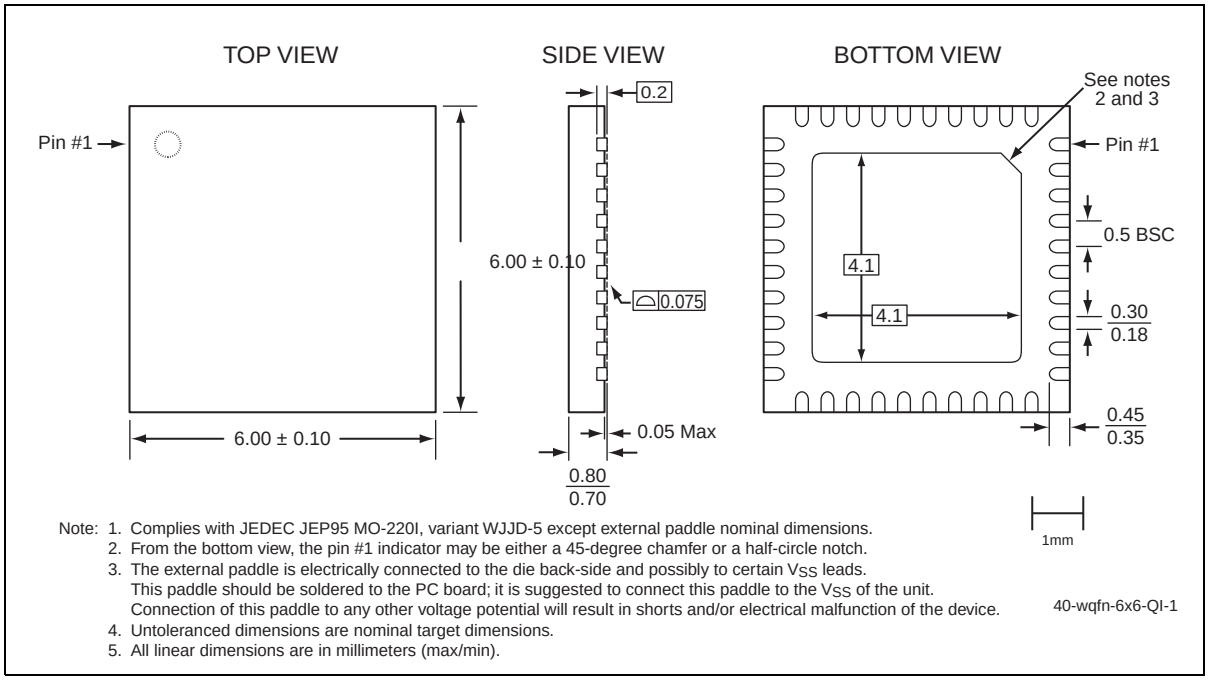
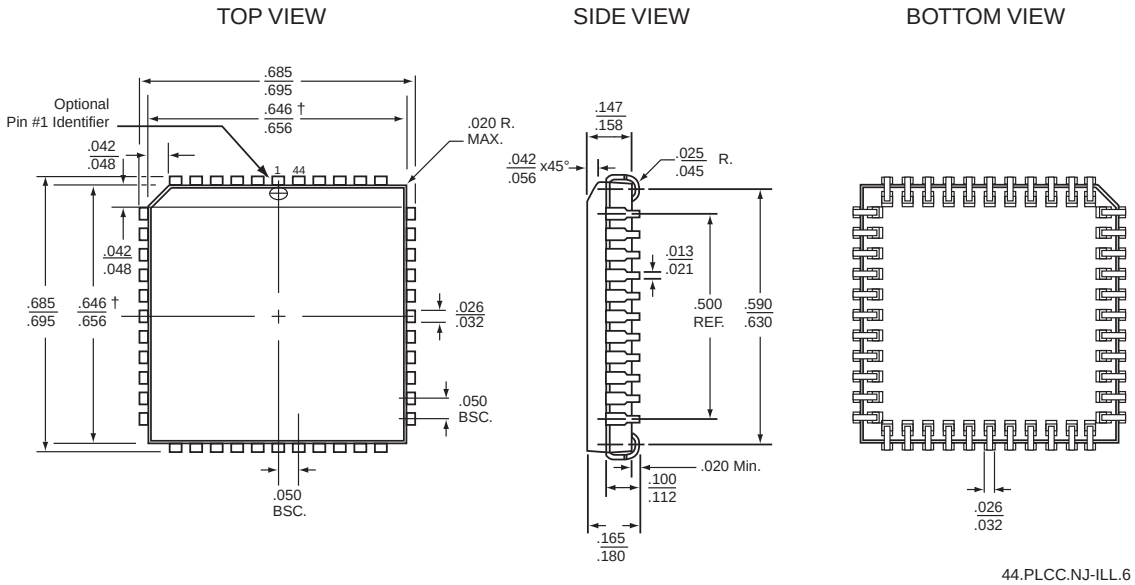


Figure 47: 40-contact Very-very-thin Quad Flat No-lead (WQFN)
SST Package Code: QI



Note:
1. Complies with JEDEC publication 95 MS-018 AC dimensions (except as noted), although some dimensions may be more stringent.
   † = JEDEC min is .650; SST min is *less*stringent
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.
4. Coplanarity: ± 4 mils.

Figure 49: 44-lead Plastic Lead Chip Carrier (PLCC)
SST Package Code: NJ