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Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	36
Program Memory Size	72KB (72K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sst89e516rd2-40-i-nje-nxx

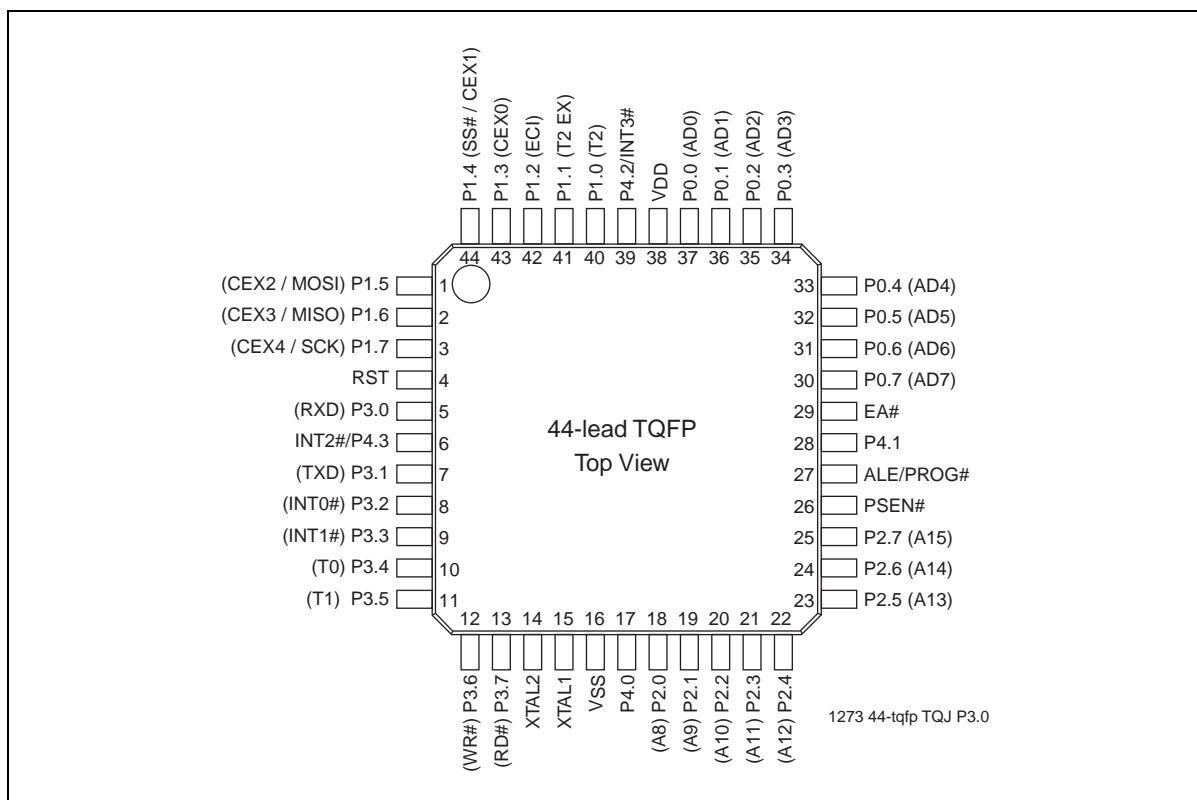


Figure 4: Pin Assignments for 44-lead TQFP

Memory Organization

The device has separate address spaces for program and data memory.

Program Flash Memory

There are two internal flash memory blocks in the device. The primary flash memory block (Block 0) has 64 KByte. The secondary flash memory block (Block 1) has 8 KByte. Since the total program address space is limited to 64 KByte, the SFCF[1:0] bit are used to control program bank selection. Please refer to Figure 6 for the program memory configuration. Program bank selection is described in the next section.

The 64K x8 primary SuperFlash block is organized as 512 sectors, each sector consists of 128 Bytes.

The 8K x8 secondary SuperFlash block is organized as 64 sectors, each sector consists also of 128 Bytes.

For both blocks, the 7 least significant program address bits select the byte within the sector. The remainder of the program address bits select the sector within the block.

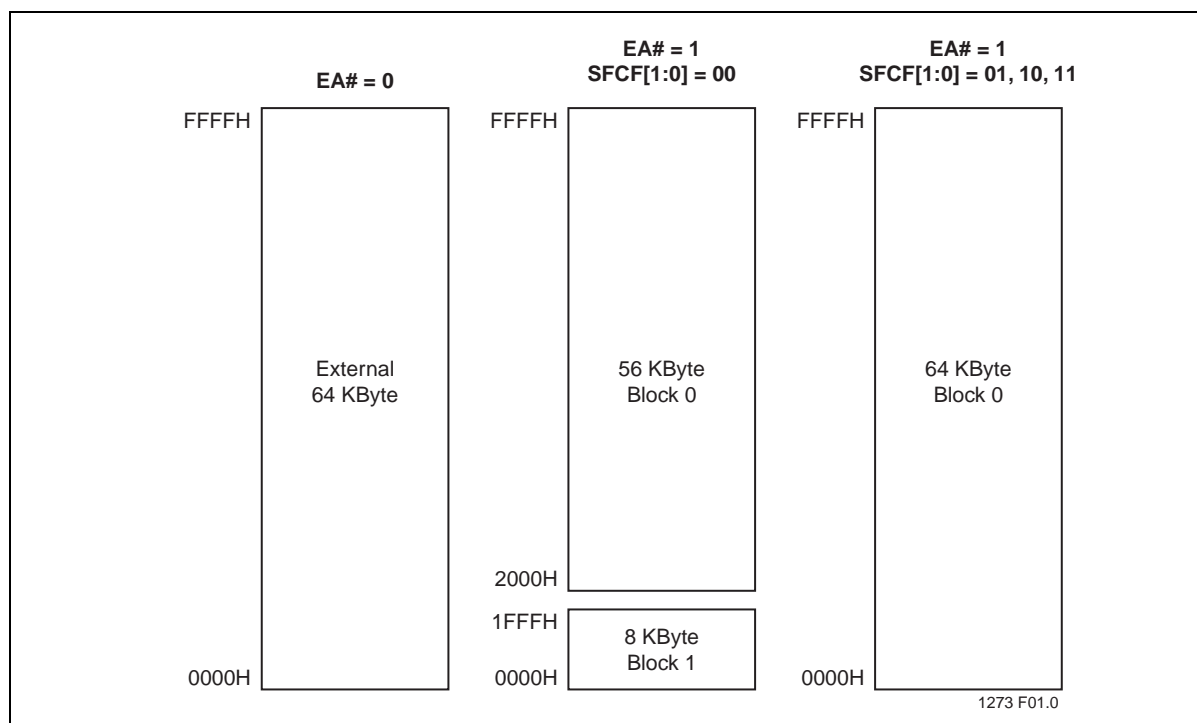


Figure 6: Program Memory Organization

Expanded Data RAM Addressing

The SST89E/V516RDx have the capability of 1 KByte RAM. See Figure 7.

The device has four sections of internal data memory:

1. The lower 128 Bytes of RAM (00H to 7FH) are directly and indirectly addressable.
2. The higher 128 Bytes of RAM (80H to FFH) are indirectly addressable.
3. The special function registers (80H to FFH) are directly addressable only.
4. The expanded RAM of 768 Bytes (00H to 2FFH) is indirectly addressable by the move external instruction (MOVX) and clearing the EXTRAM bit. (See “Auxiliary Register (AUXR)” in Section , “Special Function Registers”)

Since the upper 128 Bytes occupy the same addresses as the SFRs, the RAM must be accessed indirectly. The RAM and SFRs space are physically separate even though they have the same addresses.

When instructions access addresses in the upper 128 Bytes (above 7FH), the MCU determines whether to access the SFRs or RAM by the type of instruction given. If it is indirect, then RAM is accessed. If it is direct, then an SFR is accessed. See the examples below.

Indirect Access:

`MOV @R0, #data; R0 contains 90H`

Register R0 points to 90H which is located in the upper address range. Data in “#data” is written to RAM location 90H rather than port 1.

Direct Access:

`MOV 90H, #data; write data to P1`

Data in “#data” is written to port 1. Instructions that write directly to the address write to the SFRs.

To access the expanded RAM, the EXTRAM bit must be cleared and MOVX instructions must be used. The extra 768 bytes of memory is physically located on the chip and logically occupies the first 768 bytes of external memory (addresses 000H to 2FFH).

When EXTRAM = 0, the expanded RAM is indirectly addressed using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. Accessing the expanded RAM does not affect ports P0, P3.6 (WR#), P3.7 (RD#), or P2. With EXTRAM = 0, the expanded RAM can be accessed as in the following example.

Expanded RAM Access (Indirect Addressing only):

`MOVX @DPTR, A; DPTR contains 0A0H`

DPTR points to 0A0H and data in “A” is written to address 0A0H of the expanded RAM rather than external memory. Access to external memory higher than 2FFH using the MOVX instruction will access external memory (0300H to FFFFH) and will perform in the same way as the standard 8051, with P0 and P2 as data/address bus, and P3.6 and P3.7 as write and read timing signals.

When EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 8051. Using MOVX @Ri provides an 8-bit address with multiplexed data on Port 0. Other output port pins can be used to output higher order address bits. This provides external paging capabilities. Using MOVX @DPTR generates a 16-bit address. This allows external addressing up to 64K. Port 2 provides the

Table 7: Flash Memory Programming SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function								Reset Value
			MSB				LSB				
SFCF	SuperFlash Configuration	B1H	-	IAPE N	-	-	-	-	SW R	BSE L	x0xxxx00 b
SFCM	SuperFlash Command	B2H	FIE	FCM[6:0]							00H
SFAL	SuperFlash Address Low	B3H	SuperFlash Low Order Byte Address Register - A ₇ to A ₀ (SFAL)								00H
SFAH	SuperFlash Address High	B4H	SuperFlash High Order Byte Address Register - A ₁₅ to A ₈ (SFAH)								00H
SFDT	SuperFlash Data	B5H	SuperFlash Data Register								00H
SFST	SuperFlash Status	B6H	SB1 _i	SB2_ i	SB3 _i	-	EDC_i	FLASH_BU SY	-	-	000x00xx b

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Table 8: Watchdog Timer SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function								Reset Value
			MSB					LSB			
WDTC ₁	Watchdog Timer Control	C0H	-	-	-	WDOUT	WDRE	WDTS	WDT	SWDT	xxx00x00 b
WDTD	Watchdog Timer Data/Reload	85H	Watchdog Timer Data/Reload								00H

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1. Bit Addressable SFRs

SuperFlash Address Registers (SFAH)

Location	7	6	5	4	3	2	1	0	Reset Value
B4H	SuperFlash High Order Byte Address Register								00H

Symbol Function

SFAH Mailbox register for interfacing with flash memory block. (High order address register).

SuperFlash Data Register (SFDT)

Location	7	6	5	4	3	2	1	0	Reset Value
B5H	SuperFlash Data Register								00H

Symbol Function

SFDT Mailbox register for interfacing with flash memory block. (Data register).

SuperFlash Status Register (SFST) (Read Only Register)

Location	7	6	5	4	3	2	1	0	Reset Value
B6H	SB1_i	SB2_i	SB3_i	-	EDC_i	FLASH_BU SY	-	-	xxxxx0xxb

Symbol Function

SB1_i Security Bit 1 status (inverse of SB1 bit)

SB2_i Security Bit 2 status (inverse of SB2 bit)

SB3_i Security Bit 3 status (inverse of SB3 bit)

Please refer to Table 25 for security lock options.

EDC_i Double Clock Status

0: 12 clocks per machine cycle

1: 6 clocks per machine cycle

FLASH_BUSY Flash operation completion polling bit.

0: Device has fully completed the last IAP command.

1: Device is busy with flash operation.

External Interrupt Control (XICON)

Location	7	6	5	4	3	2	1	0	Reset Value
AEH	-	EX3	IE3	IT3	0	EX2	IE2	IT2	00H

Symbol Function

EX2	External Interrupt 2 Enable bit if set
IE2	Interrupt Enable If IT2=1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced.
IT2	External Interrupt 2 is falling-edge/low-level triggered when this bit is cleared by software.
EX3	External Interrupt 3 Enable bit if set
IE3	Interrupt Enable If IT3=1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced.
IT3	External Interrupt3 is falling-edge/low-level triggered when this bit is cleared by software.

Table 17: Timer/Counter 2

	Mode	T2CON	
		Internal Control ¹	External Control ²
Used as Timer	16-bit Auto-Reload	00H	08H
	16-bit Capture	01H	09H
	Baud rate generator receive and transmit same baud rate	34H	36H
	Receive only	24H	26H
	Transmit only	14H	16H
Used as Counter	16-bit Auto-Reload	02H	0AH
	16-bit Capture	03H	0BH

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1. Capture/Reload occurs only on timer/counter overflow.
2. Capture/Reload occurs on timer/counter overflow and a 1 to 0 transition on T2EX (P1.1) pin except when Timer 2 is used in the baud rate generating mode.

Programmable Clock-Out

A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed:

1. to input the external clock for Timer/Counter 2, or
2. to output a 50% duty cycle clock ranging from 122 Hz to 8 MHz at a 16 MHz operating frequency (61 Hz to 4 MHz in 12 clock mode).

To configure Timer/Counter 2 as a clock generator, bit C/#T2 (in T2CON) must be cleared and bit T2OE in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

$$\frac{\text{Oscillator Frequency}}{n \times (65536 - \text{RCAP2H}, \text{RCAP2L})}$$

n =2 (in 6 clock mode)
4 (in 12 clock mode)

Where (RCAP2H, RCAP2L) = the contents of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode, Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and the Clock-Out frequency will not be the same.

Serial I/O

Full-Duplex, Enhanced UART

The device serial I/O port is a full-duplex port that allows data to be transmitted and received simultaneously in hardware by the transmit and receive registers, respectively, while the software is performing other tasks. The transmit and receive registers are both located in the Serial Data Buffer (SBUF) special function register. Writing to the SBUF register loads the transmit register, and reading from the SBUF register obtains the contents of the receive register.

The UART has four modes of operation which are selected by the Serial Port Mode Specifier (SM0 and SM1) bits of the Serial Port Control (SCON) special function register. In all four modes, transmission is initiated by any instruction that uses the SBUF register as a destination register. Reception is initiated in mode 0 when the Receive Interrupt (RI) flag bit of the Serial Port Control (SCON) SFR is cleared and the Reception Enable/ Disable (REN) bit of the SCON register is set. Reception is initiated in the other modes by the incoming start bit if the REN bit of the SCON register is set.

Framing Error Detection

Framing Error Detection is a feature, which allows the receiving controller to check for valid stop bits in modes 1, 2, or 3. Missing stop bits can be caused by noise in serial lines or from simultaneous transmission by two CPUs.

Framing Error Detection is selected by going to the PCON register and changing SMOD0 = 1 (see Figure 17). If a stop bit is missing, the Framing Error bit (FE) will be set. Software may examine the FE bit after each reception to check for data errors. After the FE bit has been set, it can only be cleared by software. Valid stop bits do not clear FE. When FE is enabled, RI rises on the stop bit, instead of the last data bit (see Figure 18 and Figure 19).

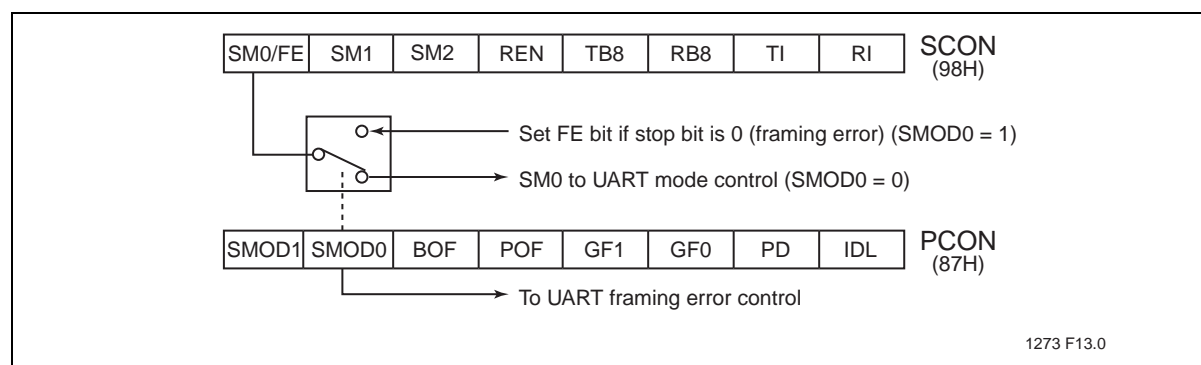


Figure 17:Framing Error Block Diagram

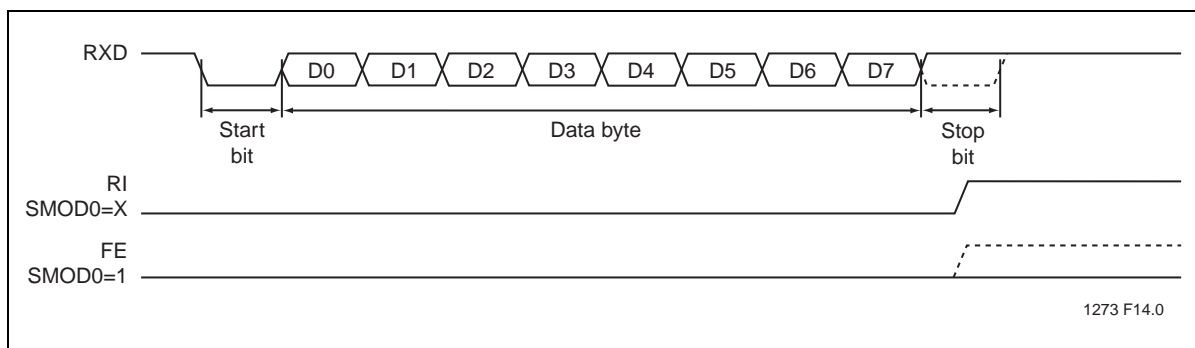


Figure 18:UART Timings in Mode 1

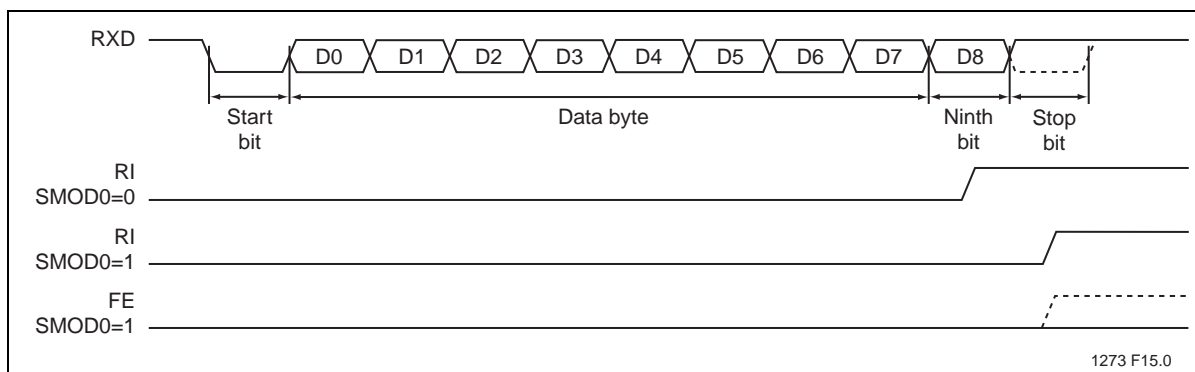


Figure 19:UART Timings in Modes 2 and 3

Automatic Address Recognition

Automatic Address Recognition helps to reduce the MCU time and power required to talk to multiple serial devices. Each device is hooked together sharing the same serial link with its own address. In this configuration, a device is only interrupted when it receives its own address, thus eliminating the software overhead to compare addresses.

This same feature helps to save power because it can be used in conjunction with idle mode to reduce the system's overall power consumption. Since there may be multiple slaves hooked up serial to one master, only one slave would have to be interrupted from idle mode to respond to the master's transmission. Automatic Address Recognition (AAR) allows the other slaves to remain in idle mode while only one is interrupted. By limiting the number of interruptions, the total current draw on the system is reduced.

There are two ways to communicate with slaves: a group of them at once, or all of them at once. To communicate with a group of slaves, the master sends out an address called the given address. To communicate with all the slaves, the master sends out an address called the "broadcast" address.

AAR can be configured as mode 2 or 3 (9-bit modes) and setting the SM2 bit in SCON. Each slave has its own SM2 bit set waiting for an address byte (9th bit = 1). The Receive Interrupt (RI) flag will only be set when the received byte matches either the given address or the broadcast address. Next, the slave then clears its SM2 bit to enable reception of the data bytes (9th bit = 0) from the master. When the 9th bit = 1, the master is sending an address. When the 9th bit = 0, the master is sending actual data.

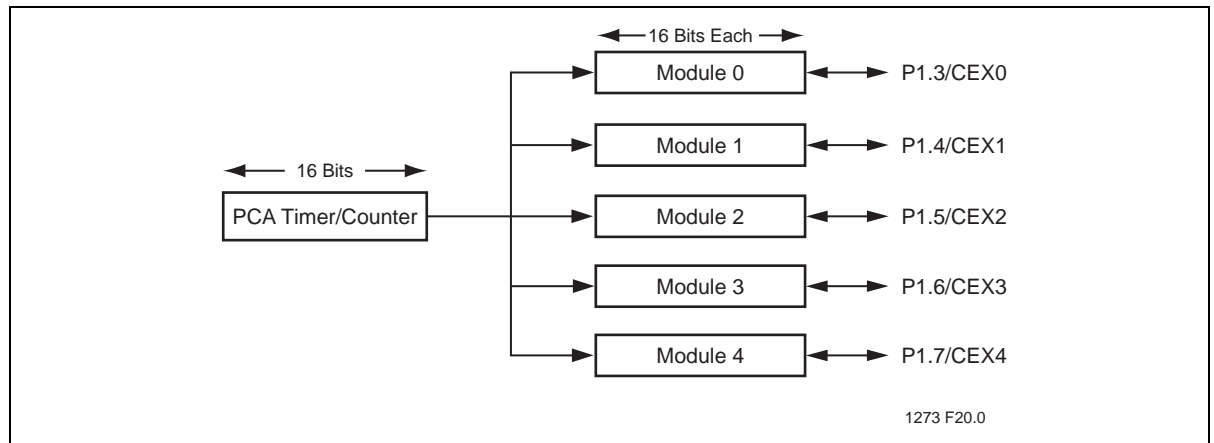


Figure 24:PCA Timer/Counter and Compare/Capture Modules

The table below summarizes various clock inputs at two common frequencies.

Table 19: PCA Timer/Counter Inputs

PCA Timer/Counter Mode	Clock Increments	
	12 MHz	16 MHz
Mode 0: $f_{osc}/12$	1 μ sec	0.75 μ sec
Mode 1:	330 nsec	250 nsec
Mode 2: Timer 0 Overflows ¹		
Timer 0 programmed in:		
8-bit mode	256 μ sec	192 μ sec
16-bit mode	65 msec	49 μ sec
8-bit auto-reload	1 to 255 μ sec	0.75 to 191 μ sec
Mode 3: External Input MAX	0.66 μ sec	0.50 μ sec

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1. In Mode 2, the overflow interrupt for Timer 0 does not need to be enabled.

The four possible CMOD timer modes with and without the overflow interrupt enabled are shown below. This list assumes that PCA will be left running during idle mode.

Table 20: CMOD Values

PCA Count Pulse Selected	CMOD Value	
	Without Interrupt Enabled	With Interrupt Enabled
Internal clock, $f_{osc}/12$	00H	01H
Internal clock, $f_{osc}/4$	02H	03H
Timer 0 overflow	04H	05H
External clock at P1.2	06H	07H

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The CCON register is associated with all PCA timer functions. It contains run control bits and flags for the PCA timer (CF) and all modules. To run the PCA the CR bit (CCON.6) must be set by software. Clearing the bit, will turn off PCA. When the PCA counter overflows, the CF (CCON.7) will be set, and

Table 22: PCA Module Modes

Without Interrupt enabled								
⁻¹	ECOMy ²	CAPPy ²	CAPNy ²	MATy ²	TOGy ²	PWMy ²	ECCFy ²	Module Code
-	0	0	0	0	0	0	0	No Operation
-	0	1	0	0	0	0	0	16-bit capture on positive-edge trigger at CEX[4:0]
-	0	0	1	0	0	0	0	16-bit capture on negative-edge trigger at CEX[4:0]
-	0	1	1	0	0	0	0	16-bit capture on positive/negative-edge trigger at CEX[4:0]
-	1	0	0	1	0	0	0	Compare: software timer
-	1	0	0	1	1	0	0	Compare: high-speed output
-	1	0	0	0	0	1	0	Compare: 8-bit PWM
-	1	0	0	1	0 or 1 ³	0	0	Compare: PCA WDT (CCAPM4 only) ⁴

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1. User should not write '1's to reserved bits. The value read from a reserved bit is indeterminate.
2. y = 0, 1, 2, 3, 4
3. A 0 disables toggle function. A 1 enables toggle function on CEX[4:0] pin.
4. For PCA WDT mode, also set the WDTE bit in the CMOD register to enable the reset output signal.

Table 23: PCA Module Modes

With Interrupt enabled								
⁻¹	ECOMy ²	CAPPy ²	CAPNy ²	MATy ²	TOGy ²	PWMy ²	ECCFy ²	Module Code
-	0	1	0	0	0	0	1	16-bit capture on positive-edge trigger at CEX[4:0]
-	0	0	1	0	0	0	1	16-bit capture on negative-edge trigger at CEX[4:0]
-	0	1	1	0	0	0	1	16-bit capture on positive/negative-edge trigger at CEX[4:0]
-	1	0	0	1	0	0	1	Compare: software timer
-	1	0	0	1	1	0	1	Compare: high-speed output
-	1	0	0	0	0	1	X ³	Compare: 8-bit PWM
-	1	0	0	1	0 or 1 ⁴	0	X ⁵	Compare: PCA WDT (CCAPM4 only) ⁶

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1. User should not write '1's to reserved bits. The value read from a reserved bit is indeterminate.
2. y = 0, 1, 2, 3, 4
3. No PCA interrupt is needed to generate the PWM.
4. A 0 disables toggle function. A 1 enables toggle function on CEX[4:0] pin.
5. Enabling an interrupt for the Watchdog Timer would defeat the purpose of the Watchdog Timer.
6. For PCA WDT mode, also set the WDTE bit in the CMOD register to enable the reset output signal.

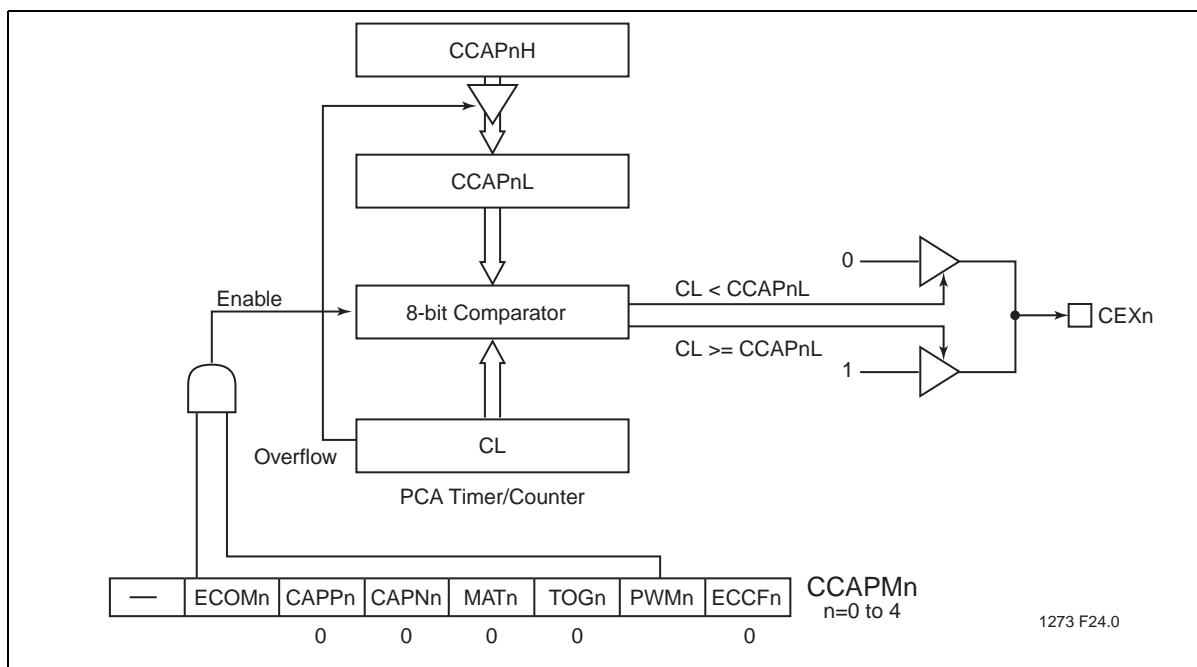


Figure 28:PCA Pulse Width Modulator Mode

Table 24: Pulse Width Modulator Frequencies

PCA Timer Mode	PWM Frequency	
	12 MHz	16 MHz
1/12 Oscillator Frequency	3.9 KHz	5.2 KHz
1/4 Oscillator Frequency	11.8 KHz	15.6 KHz
Timer 0 Overflow:		
8-bit	15.5 Hz	20.3 Hz
16-bit	0.06 Hz	0.08 Hz
8-bit Auto-Reload	3.9 KHz to 15.3 Hz	5.2 KHz to 20.3 Hz
External Input (Max)	5.9 KHz	7.8 KHz

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Watchdog Timer

The Watchdog Timer mode is used to improve reliability in the system without increasing chip count (See Figure 29). Watchdog Timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. It can also be used to prevent a software deadlock. If during the execution of the user's code, there is a deadlock, the Watchdog Timer will time out and an internal reset will occur. Only module 4 can be programmed as a Watchdog Timer (but still can be programmed to other modes if the Watchdog Timer is not used).

To use the Watchdog Timer, the user pre-loads a 16-bit value in the compare register. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven high.

In order to hold off the reset, the user has three options:

1. periodically change the compare value so it will never match the PCA timer,
2. periodically change the PCA timer value so it will never match the compare values, or
3. disable the watchdog timer by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the Watchdog Timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for all modules; changing the time base for other modules would not be a good idea. Thus, in most application the first solution is the best option.

Use the code below to initialize the Watchdog Timer. Module 4 can be configured in either compare mode, and the WDTE bit in CMOD must also be set. The user's software then must periodically change (CCAP4H, CCAP4L) to keep a match from occurring with the PCA timer (CH, CL). This code is given in the Watchdog routine below.

```

;=====
Init_Watchdog:
MOVCCAPM4, #4CH; Module 4 in compare mode
MOVCCAP4L, #0FFH; Write to low byte first
MOVCCAP4H, #0FFH; Before PCA timer counts up
; to FFFF Hex, these compare
; values must be changed.
ORLCMOD, #40H; Set the WDTE bit to enable the
; watchdog timer without
; changing the other bits in
; CMOD
;=====
;Main program goes here, but call WATCHDOG periodically.
;=====
WATCHDOG:

```

Power-Saving Modes

The device provides two power saving modes of operation for applications where power consumption is critical. The two modes are idle and power-down, see Table 28.

Idle Mode

Idle mode is entered setting the IDL bit in the PCON register. In idle mode, the program counter (PC) is stopped. The system clock continues to run and all interrupts and peripherals remain active. The on-chip RAM and the special function registers hold their data during this mode.

The device exits idle mode through either a system interrupt or a hardware reset. Exiting idle mode via system interrupt, the start of the interrupt clears the IDL bit and exits idle mode. After exit the Interrupt Service Routine, the interrupted program resumes execution beginning at the instruction immediately following the instruction which invoked the idle mode. A hardware reset starts the device similar to a power-on reset.

Power-down Mode

The power-down mode is entered by setting the PD bit in the PCON register. In the power-down mode, the clock is stopped and external interrupts are active for level sensitive interrupts only. SRAM contents are retained during power-down, the minimum V_{DD} level is 2.0V.

The device exits power-down mode through either an enabled external level sensitive interrupt or a hardware reset. The start of the interrupt clears the PD bit and exits power-down. Holding the external interrupt pin low restarts the oscillator, the signal must hold low at least 1024 clock cycles before bringing back high to complete the exit. Upon interrupt signal being restored to logic V_{IH} , the first instruction of the interrupt service routine will execute. A hardware reset starts the device similar to power-on reset.

To exit properly out of power-down, the reset or external interrupt should not be executed before the V_{DD} line is restored to its normal operating voltage. Be sure to hold V_{DD} voltage long enough at its normal operating level for the oscillator to restart and stabilize (normally less than 10 ms).

System Clock and Clock Options

Clock Input Options and Recommended Capacitor Values for Oscillator

Shown in Figure 33 are the input and output of an internal inverting amplifier (XTAL1, XTAL2), which can be configured for use as an on-chip oscillator.

When driving the device from an external clock source, XTAL2 should be left disconnected and XTAL1 should be driven.

At start-up, the external oscillator may encounter a higher capacitive load at XTAL1 due to interaction between the amplifier and its feedback capacitance. However, the capacitance will not exceed 15 pF once the external signal meets the V_{IL} and V_{IH} specifications.

Crystal manufacturer, supply voltage, and other factors may cause circuit performance to differ from one application to another. C1 and C2 should be adjusted appropriately for each design. Table 29, shows the typical values for C1 and C2 vs. crystal type for various frequencies

Table 29: Recommended Values for C1 and C2 by Crystal Type

Crystal	C1 = C2
Quartz	20-30pF
Ceramic	40-50pF

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More specific information about on-chip oscillator design can be found in the **FlashFlex Oscillator Circuit Design Considerations** application note.

Clock Doubling Option

By default, the device runs at 12 clocks per machine cycle (x1 mode). The device has a clock doubling option to speed up to 6 clocks per machine cycle. Please refer to Table 30 for detail.

Clock double mode can be enabled either via the external host mode or the IAP mode. Please refer to Table 14 for the IAP mode enabling commands (When set, the EDC# bit in SFST register will indicate 6 clock mode.).

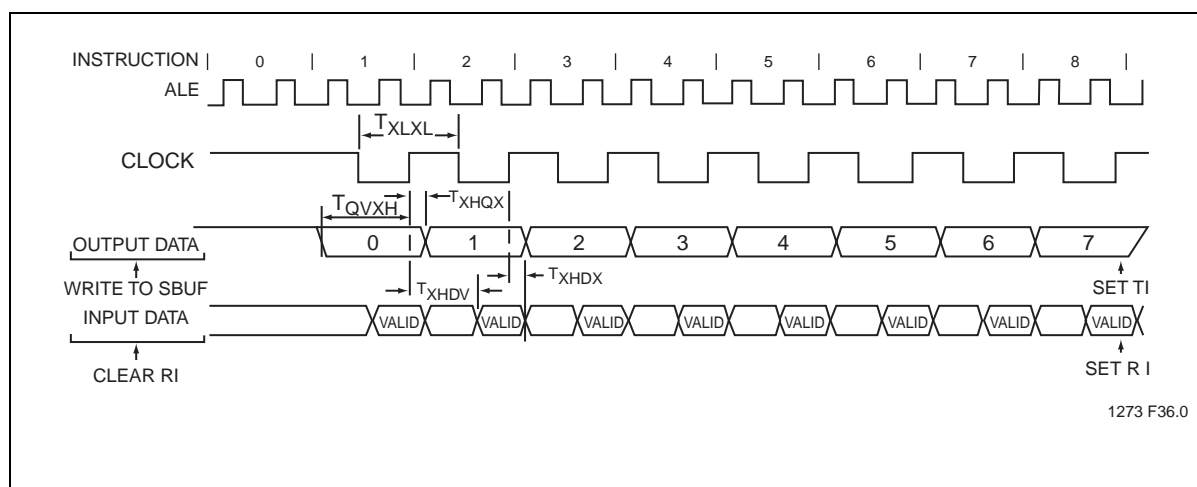
The clock double mode is only for doubling the internal system clock and the internal flash memory, i.e. EA#=1. To access the external memory and the peripheral devices, careful consideration must be taken. Also note that the crystal output (XTAL2) will not be doubled.

1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 15mA
Maximum I_{OL} per 8-bit port: 26mA
Maximum I_{OL} total for all outputs: 71mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Capacitive loading on Ports 0 and 2 may cause spurious noise to be superimposed on the V_{OLS} of ALE and Ports 1 & 3. The noise due to external bus capacitance discharging into the Port 0 & 2 pins when the pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
3. Load capacitance for Port 0, ALE & PSEN# = 100pF, load capacitance for all other outputs = 80pF.
4. Capacitive loading on Ports 0 & 2 may cause the V_{OH} on ALE and PSEN# to momentarily fall below the $V_{DD} - 0.7$ specification when the address bits are stabilizing.
5. Pins of Ports 1, 2, and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
6. Pin capacitance is characterized but not tested. EA# is 25pF (max).

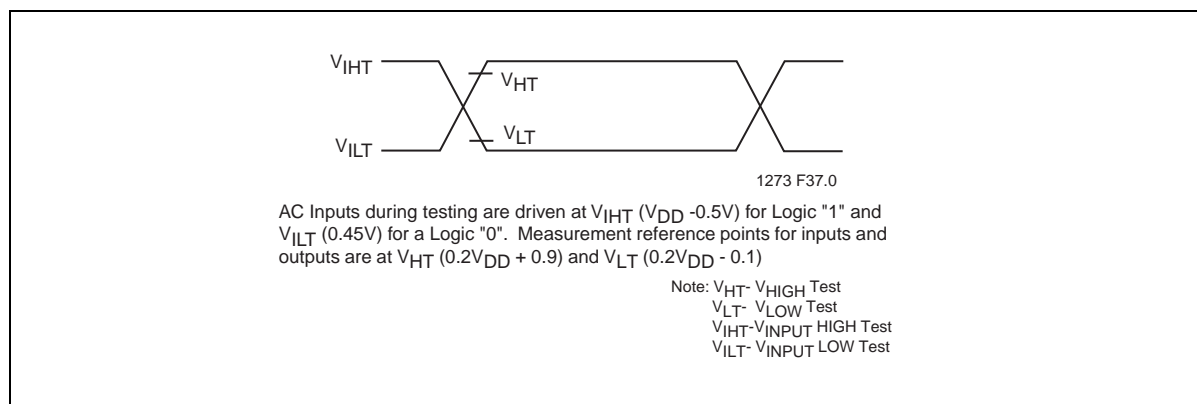
Table 40: Serial Port Timing

Symbol	Parameter	Oscillator						Units
		12MHz		40MHz		Variable		
		Min	Max	Min	Max	Min	Max	
T _{XLXL}	Serial Port Clock Cycle Time	1.0		0.3		12T _{CLCL}		μs
T _{QVXH}	Output Data Setup to Clock Rising Edge	700		117		10T _{CLCL} - 133		ns
T _{XHQX}	Output Data Hold After Clock Rising Edge	50				2T _{CLCL} - 117		ns
				0		2T _{CLCL} - 50		ns
T _{XHDX}	Input Data Hold After Clock Rising Edge	0		0		0		ns
T _{XHDV}	Clock Rising Edge to Input Data Valid		700		117		10T _{CLCL} - 133	ns

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Figure 40: Shift Register Mode Timing Waveforms

Figure 41: AC Testing Input/Output Test Waveform

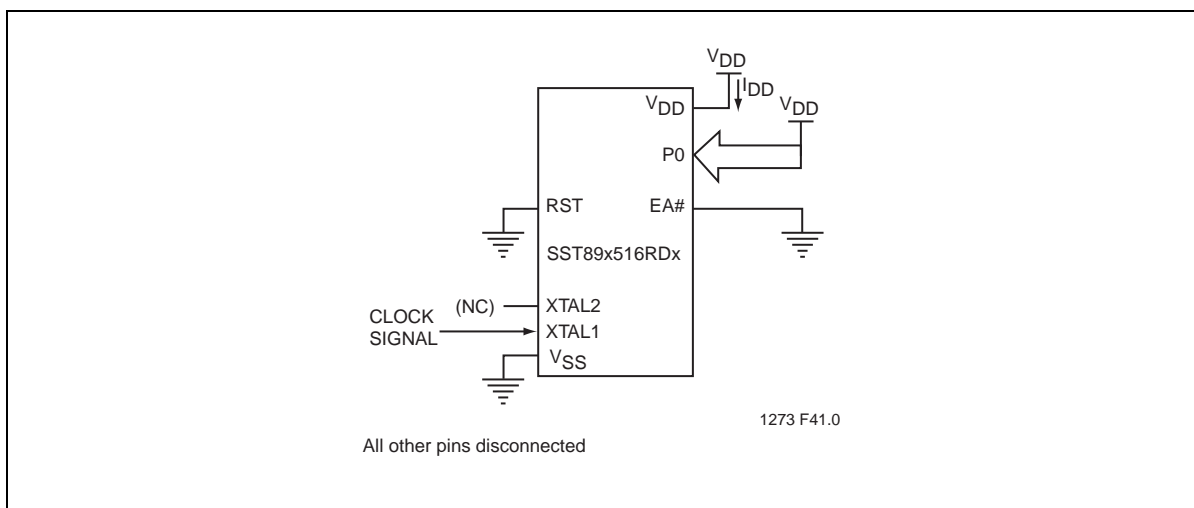


Figure 45: I_{DD} Test Condition, Idle Mode

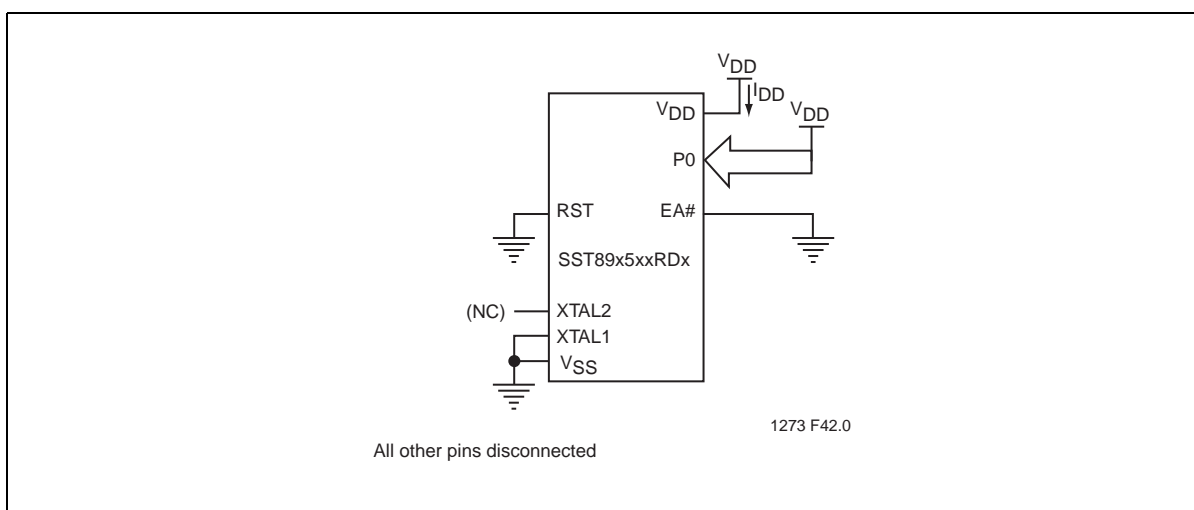


Figure 46: I_{DD} Test Condition, Power-down Mode

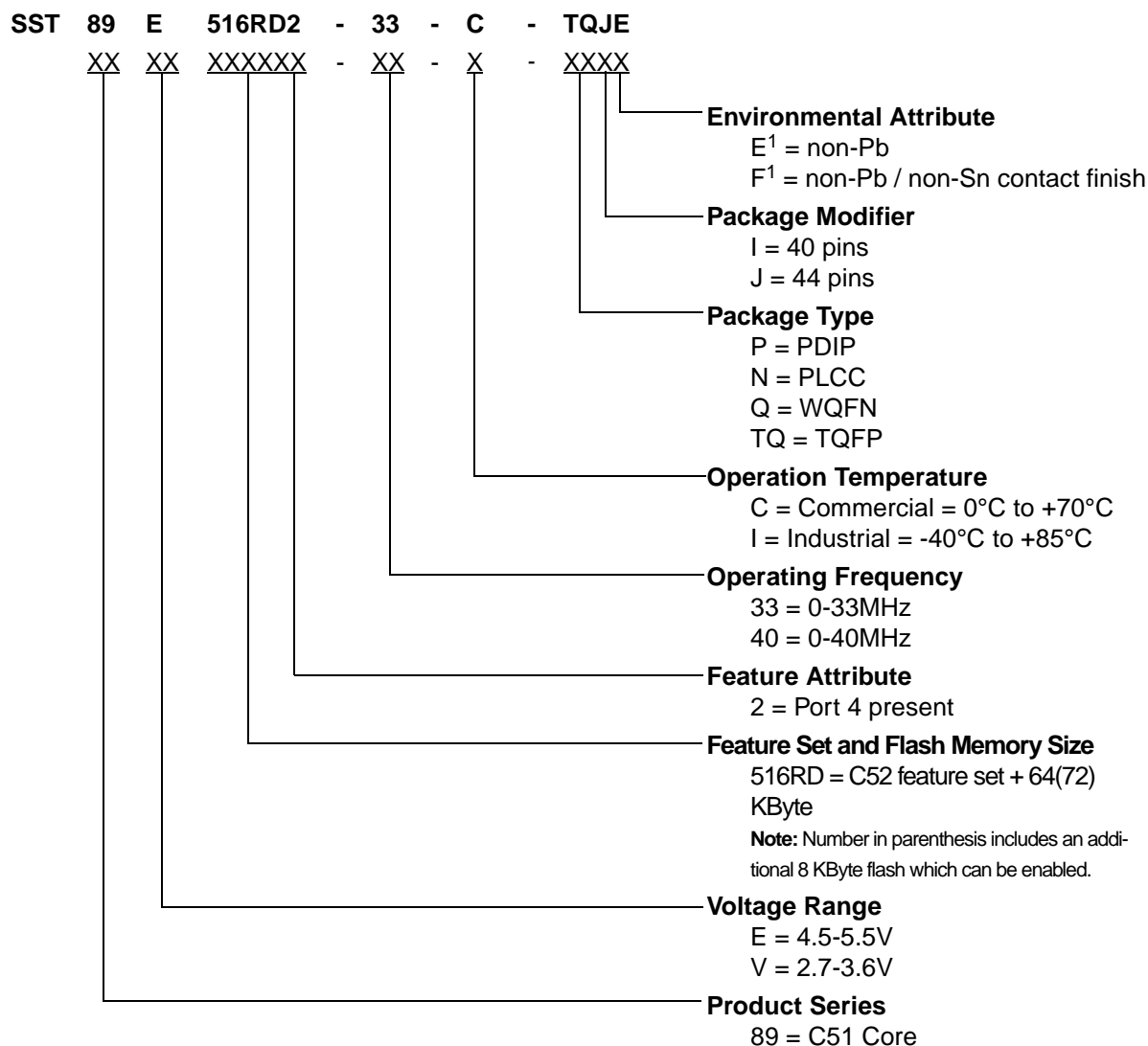
Table 41: Flash Memory Programming/Verification Parameters¹

Parameter ²	Max	Units
Chip-Erase Time	150	ms
Block-Erase Time	100	ms
Sector-Erase Time	30	ms
Byte-Program Time ³	50	μ s
Select-Block Program Time	500	ns
Re-map or Security bit Program Time	80	μ s

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1. For IAP operations, the program execution overhead must be added to the above timing parameters.
2. Program and Erase times will scale inversely proportional to programming clock frequency.
3. Each byte must be erased before programming.

Product Ordering Information



1. Environmental suffix "E" denotes non-Pb solder. Environmental suffix "F" denote non-Pb /non-Sn solder. SST non-Pb / non-Sn solder devices are "RoHS Compliant".

Packaging Diagrams

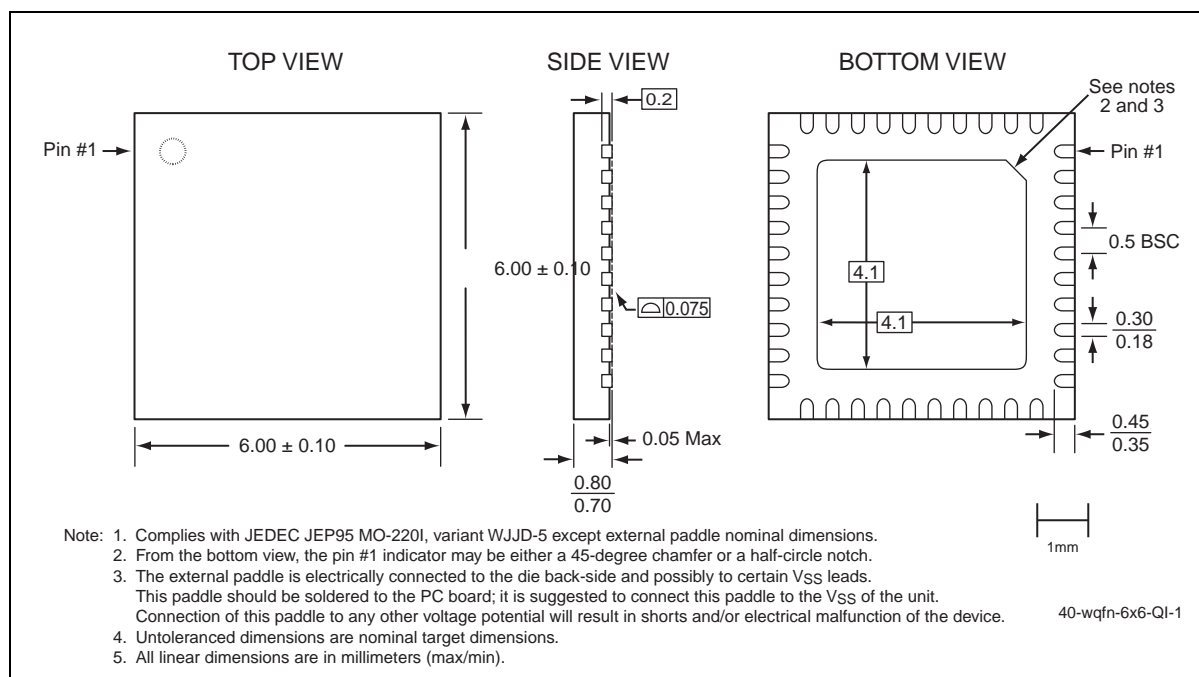


Figure 47:40-contact Very-very-thin Quad Flat No-lead (WQFN)
SST Package Code: QI