Microchip Technology - SST89E516RD2-40-I-NJE-T-NXX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	36
Program Memory Size	72KB (72K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sst89e516rd2-40-i-nje-t-nxx

Table 6: CPU related SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
ACC[1]	Accumulator	E0H	ACC[7:0]								00H
B[1]	B Register	F0H	B[7:0]								00H
PSW[1]	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00H
SP	Stack Pointer	81H	SP[7:0]								07H
DPL	Data Pointer Low	82H	DPL[7:0]								00H
DPH	Data Pointer High	83H	DPH[7:0]								00H
IE[1]	Interrupt Enable	A8H	EA	EC	ET2	ES	ET1	EX1	ET0	EX0	00H
IEA[1]	Interrupt Enable A	E8H	-	-	-	-	EBO	-	-	-	xxxx0xxx b
IP[1]	Interrupt Priority Reg	B8H	-	PPC	PT2	PS	PT1	PX1	PT0	PX0	x0000000 b
IPH	Interrupt Priority Reg High	B7H	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	x0000000 b
IP1[1]	Interrupt Priority Reg A	F8H	-	-	-	-	PBO	PX3	PX2	-	xxxx0xxx b
IP1H	Interrupt Priority Reg A High	F7H	-	-	-	-	PBOH	PX3H	PX2H	-	xxxx0xxx b
PCON	Power Control	87H	SMOD1	SMOD0	BOF	POF	GF1	GF0	PD	IDL	00010000 b
AUXR	Auxiliary Reg	8EH	-	-	-	-	-	-	EXTRAM	AO	xxxxxxx0 0b
AUXR1	Auxiliary Reg 1	A2H	-	-	-	-	GF2	0	-	DPS	xxxx00x0 b
XICON	External Interrupt Control	AEH	-	EX3	IE3	IT3	0	EX2	IE2	IT2	00H

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1. Bit Addressable SFRs

Table 7: Flash Memory Programming SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
SFCF	SuperFlash Configuration	B1H	-	IAPEN	-	-	-	-	SWR	BSEL	x0xxxx00b
SFCM	SuperFlash Command	B2H	FIE	FCM[6:0]							00H
SFAL	SuperFlash Address Low	B3H	SuperFlash Low Order Byte Address Register - A_7 to A_0 (SFAL)								00H
SFAH	SuperFlash Address High	B4H	SuperFlash High Order Byte Address Register - A_{15} to A_8 (SFAH)								00H
SFDT	SuperFlash Data	B5H	SuperFlash Data Register								00H
SFST	SuperFlash Status	B6H	SB1_i	SB2_i	SB3_i	-	EDC_i	FLASH_BUSY	-	-	000x00xxb

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Table 8: Watchdog Timer SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
WDTC [1]	Watchdog Timer Control	C0H	-	-	-	WDOUT	WDRE	WDTS	WDT	SWDT	xxx00x00b
WDTD	Watchdog Timer Data/Reload	85H	Watchdog Timer Data/Reload								00H

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1. Bit Addressable SFRs

Table 9: Timer/Counters SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB LSB								Reset Value
TMOD	Timer/Counter Mode Control	89H	Timer 1				Timer 0				00H
			GATE	C/T#	M1	M0	GATE	C/T#	M1	M0	
TCON[1]	Timer/Counter Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
TH0	Timer 0 MSB	8CH	TH0[7:0]								00H
TL0	Timer 0 LSB	8AH	TL0[7:0]								00H
TH1	Timer 1 MSB	8DH	TH1[7:0]								00H
TL1	Timer 1 LSB	8BH	TL1[7:0]								00H
T2CON[1]	Timer / Counter 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#	00H
T2MOD	Timer2 Mode Control	C9H	-	-	-	-	-	-	T2OE	DCEN	xxxxxx00b
TH2	Timer 2 MSB	CDH	TH2[7:0]								00H
TL2	Timer 2 LSB	CCH	TL2[7:0]								00H
RCAP2H	Timer 2 Capture MSB	CBH	RCAP2H[7:0]								00H
RCAP2L	Timer 2 Capture LSB	CAH	RCAP2L[7:0]								00H

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1. Bit Addressable SFRs

Table 11: PCA SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	RESET Value
CH CL	PCA Timer/Counter	F9H E9H	CH[7:0] CL[7:0]								00H 00H
CCON[1]	PCA Timer/Counter Control Register	D8H	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0	00x0000 0b
CMOD	PCA Timer/Counter Mode Register	D9H	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF	00xxx000 b
CCAP0H	PCA Module 0 Compare/Capture Registers	FAH	CCAP0H[7:0]								00H
CCAP0L		EAH	CCAP0L[7:0]								00H
CCAP1H	PCA Module 1 Compare/Capture Registers	FBH	CCAP1H[7:0]								00H
CCAP1L		EBH	CCAP1L[7:0]								00H
CCAP2H	PCA Module 2 Compare/Capture Registers	FCH	CCAP2H[7:0]								00H
CCAP2L		ECH	CCAP2L[7:0]								00H
CCAP3H	PCA Module 3 Compare/Capture Registers	FDH	CCAP3H[7:0]								00H
CCAP3L		EDH	CCAP3L[7:0]								00H
CCAP4H	PCA Module 4 Compare/Capture Registers	FEH	CCAP4H[7:0]								00H
CCAP4L		EEH	CCAP4L[7:0]								00H
CCAPM0	PCA Compare/Capture Module Mode Registers	DAH	-	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0	x000000 0b
CCAPM1		DBH	-	ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1	x000000 0b
CCAPM2		DCH	-	ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2	x000000 0b
CCAPM3		DDH	-	ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3	x000000 0b
CCAPM4		DEH	-	ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4	x000000 0b

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1. Bit Addressable SFRs

Interrupt Priority (IP)

Location	7	6	5	4	3	2	1	0	Reset Value
B8H	-	PPC	PT2	PS	PT1	PX1	PT0	PX0	x0000000b

Symbol	Function
PPC	PCA interrupt priority bit
PT2	Timer 2 interrupt priority bit
PS	Serial Port interrupt priority bit
PT1	Timer 1 interrupt priority bit
PX1	External interrupt 1 priority bit
PT0	Timer 0 interrupt priority bit
PX0	External interrupt 0 priority bit

Interrupt Priority High (IPH)

Location	7	6	5	4	3	2	1	0	Reset Value
B7H	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	x0000000b

Symbol	Function
PPCH	PCA interrupt priority bit high
PT2H	Timer 2 interrupt priority bit high
PSH	Serial Port interrupt priority bit high
PT1H	Timer 1 interrupt priority bit high
PX1H	External interrupt 1 priority bit high
PT0H	Timer 0 interrupt priority bit high
PX0H	External interrupt 0 priority bit high

Interrupt Priority 1 (IP1)

Location	7	6	5	4	3	2	1	0	Reset Value
F8H	1	-	-	1	PBO	PX3	PX2	1	1xx10001b

Symbol	Function
PBO	Brown-out interrupt priority bit
PX2	External Interrupt 2 priority bit
PX3	External Interrupt 3 priority bit

Interrupt Priority 1 High (IP1H)

Location	7	6	5	4	3	2	1	0	Reset Value
F7H	1	-	-	1	PBOH	PX3H	PX2H	1	1xx10001b

Symbol	Function
PBOH	Brown-out Interrupt priority bit high
PX2H	External Interrupt 2 priority bit high
PX3H	External Interrupt 3 priority bit high

Auxiliary Register (AUXR)

Location	7	6	5	4	3	2	1	0	Reset Value
8EH	-	-	-	-	-	-	EXTRAM	AO	xxxxxx00b

Symbol Function

EXTRAM Internal/External RAM access
0: Internal Expanded RAM access within range of 00H to 2FFH using MOVX @Ri / @DPTR. Beyond 300H, the MCU always accesses external data memory.
For details, refer to Section , “Expanded Data RAM Addressing” .
1: External data memory access.

AO Disable/Enable ALE
0: ALE is emitted at a constant rate of 1/3 the oscillator frequency in 6 clock mode, 1/6 f_{OSC} in 12 clock mode.
1: ALE is active only during a MOVX or MOVC instruction.

Auxiliary Register 1 (AUXR1)

Location	7	6	5	4	3	2	1	0	Reset Value
A2H	-	-	-	-	GF2	0	-	DPS	xxxx00x0b

Symbol Function

GF2 General purpose user-defined flag.

DPS DPTR registers select bit.
0: DPTR0 is selected.
1: DPTR1 is selected.

Watchdog Timer Control Register (WDTC)

Location	7	6	5	4	3	2	1	0	Reset Value
C0H	-	-	-	WDOUT	WDRE	WDTS	WDT	SWDT	xxx00000b

Symbol Function

WDOUT Watchdog output enable.
0: Watchdog reset will not be exported on Reset pin.
1: Watchdog reset if enabled by WDRE, will assert Reset pin for 32 clocks.

WDRE Watchdog timer reset enable.
0: Disable watchdog timer reset.
1: Enable watchdog timer reset.

WDTS Watchdog timer reset flag.
0: External hardware reset or power-on reset clears the flag.
Flag can also be cleared by writing a 1.
Flag survives if chip reset happened because of watchdog timer overflow.
1: Hardware sets the flag on watchdog overflow.

WDT Watchdog timer refresh.
0: Hardware resets the bit when refresh is done.
1: Software sets the bit to force a watchdog timer refresh.

SWDT Start watchdog timer.
0: Stop WDT.
1: Start WDT.

PCA Compare/Capture Module Mode Register[1] (CCAPMn)

Location	7	6	5	4	3	2	1	0	Reset Value
DAH	-	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0	00xxx000b
DBH	-	ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1	00xxx000b
DCH	-	ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2	00xxx000b
DDH	-	ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3	00xxx000b
DEH	-	ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4	00xxx000b

1. Not bit addressable

Symbol **Function**

-
Not implemented, reserved for future use.
Note: User should not write ‘1’s to reserved bits. The value read from a reserved bit is indeterminate.

ECOMn
Enable Comparator
0: Disables the comparator function
1: Enables the comparator function

CAPPn
Capture Positive
0: Disables positive edge capture on CEX[4:0]
1: Enables positive edge capture on CEX[4:0]

CAPNn
Capture Negative
0: Disables negative edge capture on CEX[4:0]
1: Enables negative edge capture on CEX[4:0]

MATn
Match: Set ECOM[4:0] and MAT[4:0] to implement the software timer mode
0: Disables software timer mode
1: A match of the PCA counter with this module’s compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.

TOGn
Toggle
0: Disables toggle function
1: A match of the PCA counter with this module’s compare/capture register causes the CEXn pin to toggle.

PWMn
Pulse Width Modulation mode
0: Disables PWM mode
1: Enables CEXn pin to be used as a pulse width modulated output

ECCFn
Enable CCF Interrupt
0: Disables compare/capture flag CCF[4:0] in the CCON register to generate an interrupt request.
1: Enables compare/capture flag CCF[4:0] in the CCON register to generate an interrupt request.

Timer/Counter 2 Control Register (T2CON)

Location	7	6	5	4	3	2	1	0	Reset Value
C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#	00H

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflow to be used for the transmit clock.
EXEN2	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/stop control for Timer 2. A logic 1 starts the timer.
C/T2#	Timer or counter select (Timer 2) 0: Internal timer (OSC/6 in 6 clock mode, OSC/12 in 12 clock mode) 1: External event counter (falling edge triggered)
CP/RL2#	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Timer/Counter 2 Mode Control (T2MOD)

Location	7	6	5	4	3	2	1	0	Reset Value
C9H	-	-	-	-	-	-	T2OE	DCEN	xxxxxx00b

Symbol	Function
-	Not implemented, reserved for future use. **Note:** User should not write ‘1’s to reserved bits. The value read from a reserved bit is indeterminate.
T2OE	Timer 2 Output Enable bit.
DCEN	Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter.

External Interrupt Control (XICON)

Location	7	6	5	4	3	2	1	0	Reset Value
AEH	-	EX3	IE3	IT3	0	EX2	IE2	IT2	00H

Symbol	Function
EX2	External Interrupt 2 Enable bit if set
IE2	Interrupt Enable If IT2=1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced.
IT2	External Interrupt 2 is falling-edge/low-level triggered when this bit is cleared by software.
EX3	External Interrupt 3 Enable bit if set
IE3	Interrupt Enable If IT3=1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced.
IT3	External Interrupt3 is falling-edge/low-level triggered when this bit is cleared by software.

Prog-SC0

Prog-SC0 command is used to program the SC0 bit. This command only changes the SC0 bit and has no effect on BSEL bit until after a reset cycle.

SC0 bit previously in un-programmed state can be programmed by this command. The Prog-SC0 command should reside only in Block 1 or external code memory.

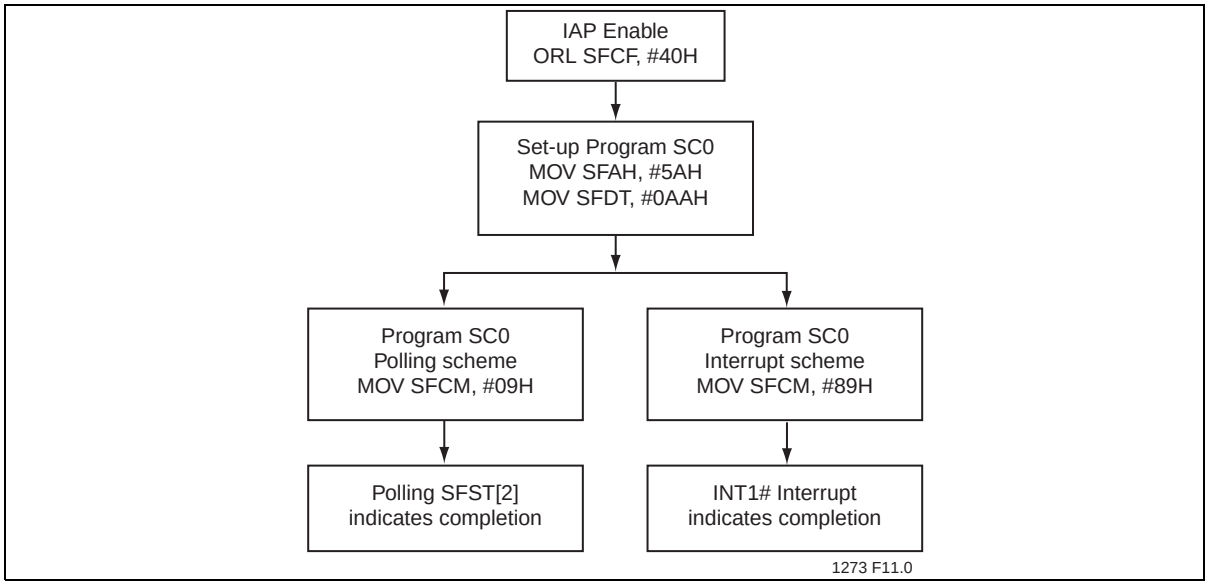

Figure 15: Prog-SC0

Enable-Clock-Double

Enable-Clock-Double command is used to make the MCU run at 6 clocks per machine cycle. The standard (default) is 12 clocks per machine cycle (i.e. clock double command disabled).

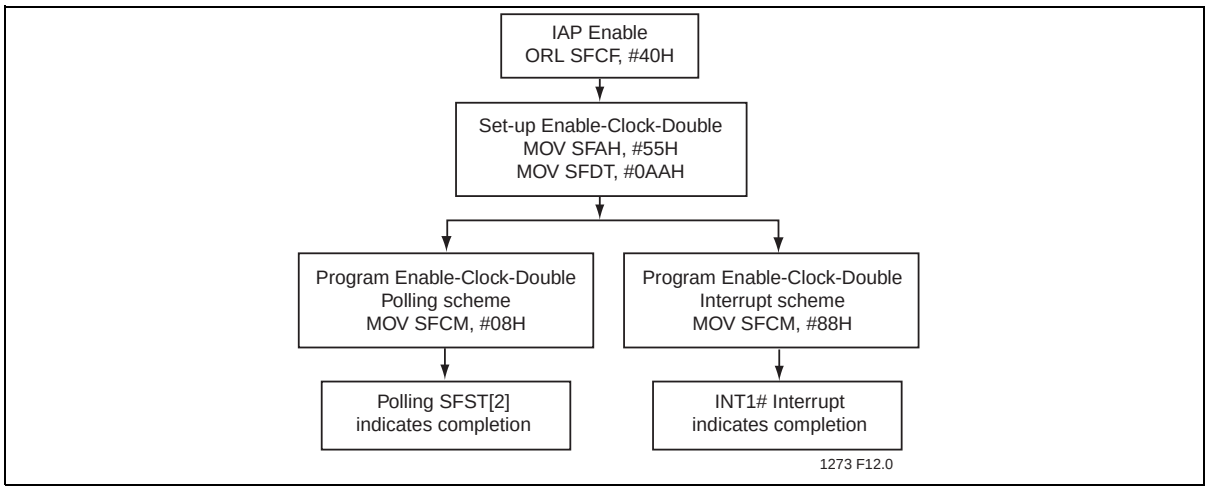

Figure 16: Enable-Clock-Double

There are no IAP counterparts for the external host commands Select-Block0 and Select-Block1.

If mode 1 is used, the stop bit takes the place of the 9th bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit. Note that mode 0 cannot be used. Setting SM2 bit in the SCON register in mode 0 will have no effect.

Each slave's individual address is specified by SFR SADDR. SFR SADEN is a mask byte that defines "don't care" bits to form the given address when combined with SADDR. See the example below:

Slave 1

SADDR	=	1111 0001
SADEN	=	1111 1010
GIVEN	=	1111 0X0X

Slave 2

SADDR	=	1111 0011
SADEN	=	1111 1001
GIVEN	=	1111 0XX1

Using the Given Address to Select Slaves

Any bits masked off by a 0 from SADEN become a "don't care" bit for the given address. Any bit masked off by a 1, becomes ANDED with SADDR. The "don't cares" provide flexibility in the user-defined addresses to address more slaves when using the given address.

Shown in the example above, Slave 1 has been given an address of 1111 0001 (SADDR). The SADEN byte has been used to mask off bits to a given address to allow more combinations of selecting Slave 1 and Slave 2. In this case for the given addresses, the last bit (LSB) of Slave 1 is a "don't care" and the last bit of Slave 2 is a 1. To communicate with Slave 1 and Slave 2, the master would need to send an address with the last bit equal to 1 (e.g. 1111 0001) since Slave 1's last bit is a don't care and Slave 2's last bit has to be a 1. To communicate with Slave 1 alone, the master would send an address with the last bit equal to 0 (e.g. 1111 0000), since Slave 2's last bit is a 1. See the table below for other possible combinations.

Select Slave 1 Only		
Slave 1	**Given Address**	**Possible Addresses**
	1111 0X0X	1111 0000 1111 0100

Select Slave 2 Only		
Slave 2	**Given Address**	**Possible Addresses**
	1111 0XX1	1111 0111 1111 0011

Select Slaves 1 & 2	
Slaves 1 & 2	**Possible Addresses**
	1111 0001 1111 0101

Serial Peripheral Interface

SPI Features

- Master or slave operation
- 10 MHz bit frequency (max)
- LSB first or MSB first data transfer
- Four programmable bit rates
- End of transmission (SPIF)
- Write collision flag protection (WCOL)
- Wake up from idle mode (slave mode only)

SPI Description

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the SST89E/V516RDx and peripheral devices or between several SST89E/V516RDx devices.

Figure 20 shows the correspondence between master and slave SPI devices. The SCK pin is the clock output and input for the master and slave modes, respectively. The SPI clock generator will start following a write to the master devices SPI data register. The written data is then shifted out of the MOSI pin on the master device into the MOSI pin of the slave device. Following a complete transmission of one byte of data, the SPI clock generator is stopped and the SPIF flag is set. An SPI interrupt request will be generated if the SPI Interrupt Enable bit (SPIE) and the Serial Port Interrupt Enable bit (ES) are both set.

An external master drives the Slave Select input pin, SS#/P1[4], low to select the SPI module as a slave. If SS#/P1[4] has not been driven low, then the slave SPI unit is not active and the MOSI/P1[5] port can also be used as an input port pin.

CPHA and CPOL control the phase and polarity of the SPI clock. Figures 21 and 22 show the four possible combinations of these two bits.

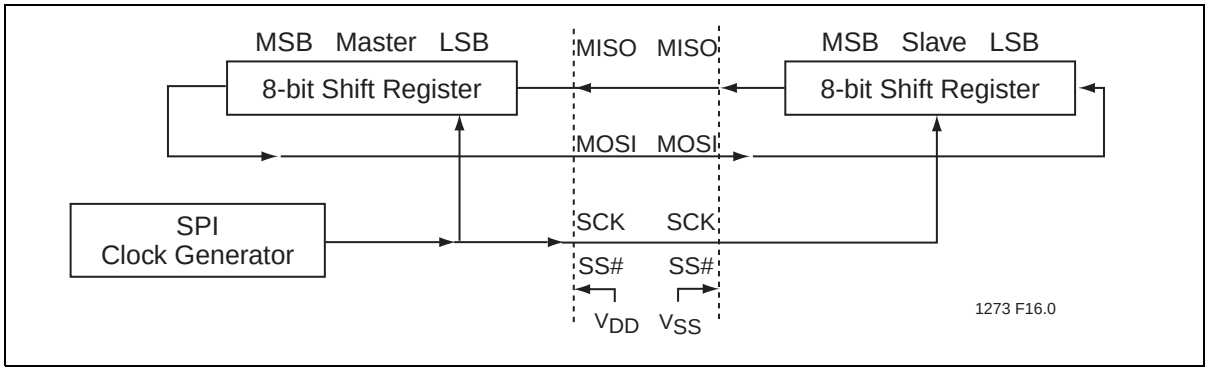

Figure 20: SPI Master-slave Interconnection

SPI Transfer Formats

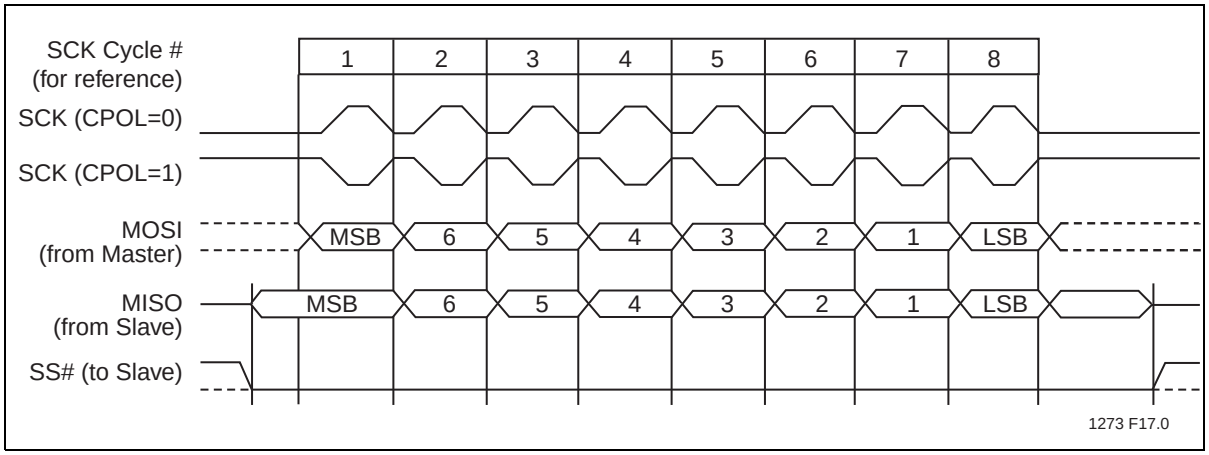

Figure 21: SPI Transfer Format with CPHA = 0

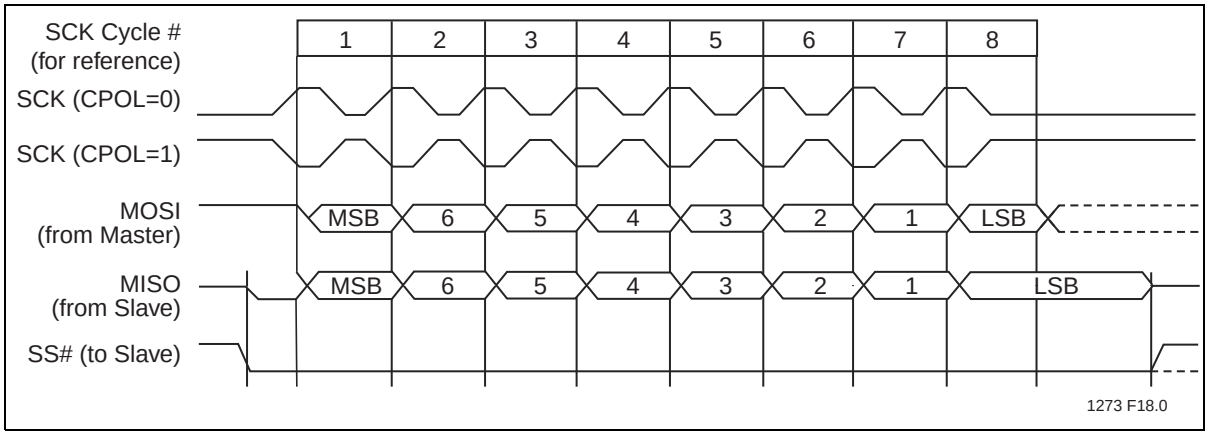

Figure 22: SPI Transfer Format with CPHA = 1

Programmable Counter Array

The Programmable Counter Array (PCA) present on the SST89E/V516RDx is a special 16-bit timer that has five 16-bit capture/compare modules. Each of the modules can be programmed to operate in one of four modes: rising and/or falling edge capture, software timer, high-speed output, or pulse width modulator. The 5th module can be programmed as a Watchdog Timer in addition to the other four modes. Each module has a pin associated with it in port 1. Module 0 is connected to P1.3 (CEX0), module 1 to P1[4] (CEX1), module 2 to P1[5] (CEX2), module 3 to P1[6] (CEX3), and module 4 to P1[7] (CEX4). PCA configuration is shown in Figure 24.

PCA Overview

PCA provides more timing capabilities with less CPU intervention than the standard timer/counter. Its advantages include reduced software overhead and improved accuracy.

The PCA consists of a dedicated timer/counter which serves as the time base for an array of five compare/capture modules. Figure 24 shows a block diagram of the PCA. External events associated with modules are shared with corresponding Port 1 pins. Modules not using the port pins can still be used for standard I/O.

Each of the five modules can be programmed in any of the following modes:

- Rising and/or falling edge capture
- Software timer
- High speed output
- Watchdog Timer (Module 4 only)
- Pulse Width Modulator (PWM)

PCA Timer/Counter

The PCA timer is a free-running 16-bit timer consisting of registers CH and CL (the high and low bytes of the count values). The PCA timer is common time base for all five modules and can be programmed to run at: 1/6 the oscillator frequency, 1/2 the oscillator frequency, Timer 0 overflow, or the input on the ECI pin (P1.2). The timer/counter source is determined from the CPS1 and CPS0 bits in the CMOD SFR as follows (see “PCA Timer/Counter Mode Register (CMOD)” on page 28):

Table 18: PCA Timer/Counter Source

CPS1	CPS0	12 Clock Mode	6 Clock Mode
0	0	f_{OSC} /12	f_{OSC} /6
0	1	f_{OSC} /4	f_{OSC} /2
1	0	Timer 0 overflow	Timer 0 overflow
1	1	External clock at ECI pin (maximum rate = f_{OSC} /8)	External clock at ECI pin (maximum rate = f_{OSC} /4)

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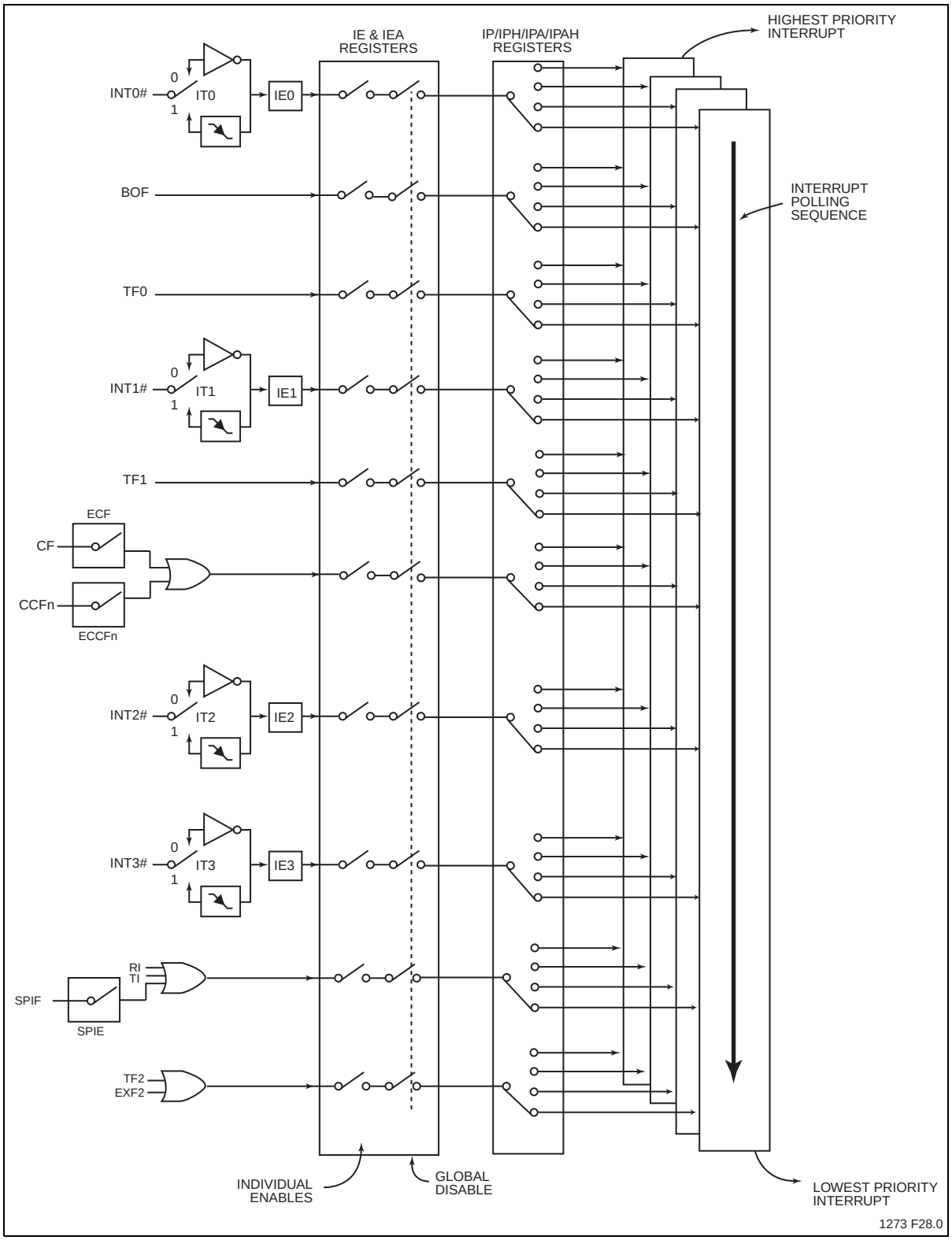

Figure 32: Interrupt Structure

Power-Saving Modes

The device provides two power saving modes of operation for applications where power consumption is critical. The two modes are idle and power-down, see Table 28.

Idle Mode

Idle mode is entered setting the IDL bit in the PCON register. In idle mode, the program counter (PC) is stopped. The system clock continues to run and all interrupts and peripherals remain active. The on-chip RAM and the special function registers hold their data during this mode.

The device exits idle mode through either a system interrupt or a hardware reset. Exiting idle mode via system interrupt, the start of the interrupt clears the IDL bit and exits idle mode. After exit the Interrupt Service Routine, the interrupted program resumes execution beginning at the instruction immediately following the instruction which invoked the idle mode. A hardware reset starts the device similar to a power-on reset.

Power-down Mode

The power-down mode is entered by setting the PD bit in the PCON register. In the power-down mode, the clock is stopped and external interrupts are active for level sensitive interrupts only. SRAM contents are retained during power-down, the minimum V_{DD} level is 2.0V.

The device exits power-down mode through either an enabled external level sensitive interrupt or a hardware reset. The start of the interrupt clears the PD bit and exits power-down. Holding the external interrupt pin low restarts the oscillator, the signal must hold low at least 1024 clock cycles before bringing back high to complete the exit. Upon interrupt signal being restored to logic $V_{IH,}$ the first instruction of the interrupt service routine will execute. A hardware reset starts the device similar to power-on reset.

To exit properly out of power-down, the reset or external interrupt should not be executed before the V_{DD} line is restored to its normal operating voltage. Be sure to hold V_{DD} voltage long enough at its normal operating level for the oscillator to restart and stabilize (normally less than 10 ms).

System Clock and Clock Options

Clock Input Options and Recommended Capacitor Values for Oscillator

Shown in Figure 33 are the input and output of an internal inverting amplifier (XTAL1, XTAL2), which can be configured for use as an on-chip oscillator.

When driving the device from an external clock source, XTAL2 should be left disconnected and XTAL1 should be driven.

At start-up, the external oscillator may encounter a higher capacitive load at XTAL1 due to interaction between the amplifier and its feedback capacitance. However, the capacitance will not exceed 15 pF once the external signal meets the V_{IL} and V_{IH} specifications.

Crystal manufacturer, supply voltage, and other factors may cause circuit performance to differ from one application to another. C1 and C2 should be adjusted appropriately for each design. Table 29, shows the typical values for C1 and C2 vs. crystal type for various frequencies

Table 29: Recommended Values for C1 and C2 by Crystal Type

Crystal	C1 = C2
Quartz	20-30pF
Ceramic	40-50pF

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More specific information about on-chip oscillator design can be found in the ***FlashFlex Oscillator Circuit Design Considerations*** application note.

Clock Doubling Option

By default, the device runs at 12 clocks per machine cycle (x1 mode). The device has a clock doubling option to speed up to 6 clocks per machine cycle. Please refer to Table 30 for detail.

Clock double mode can be enabled either via the external host mode or the IAP mode. Please refer to Table 14 for the IAP mode enabling commands (When set, the EDC# bit in SFST register will indicate 6 clock mode.).

The clock double mode is only for doubling the internal system clock and the internal flash memory, i.e. EA#=1. To access the external memory and the peripheral devices, careful consideration must be taken. Also note that the crystal output (XTAL2) will not be doubled.

Table 40: Serial Port Timing

Symbol	Parameter	Oscillator						Units
		12MHz		40MHz		Variable		
		Min	Max	Min	Max	Min	Max	
T_{XLXL}	Serial Port Clock Cycle Time	1.0		0.3		$12T_{CLCL}$		µs
T_{QVXH}	Output Data Setup to Clock Rising Edge	700		117		$10T_{CLCL}$ - 133		ns
T_{XHQX}	Output Data Hold After Clock Rising Edge	50				$2T_{CLCL}$ - 117		ns
				0		$2T_{CLCL}$ - 50		ns
T_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		700		117		$10T_{CLCL}$ - 133	ns

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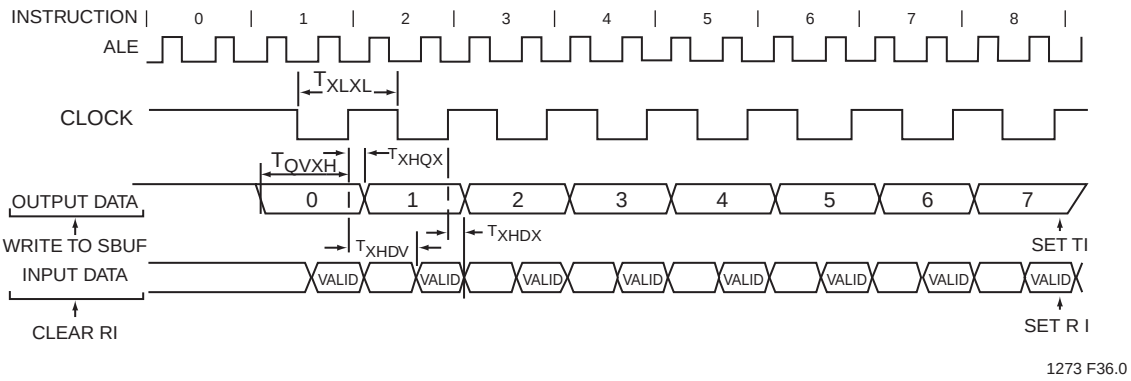
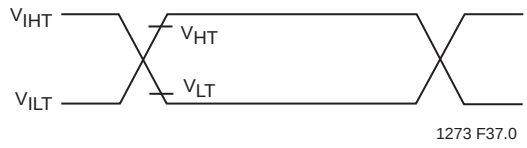


Figure 40: Shift Register Mode Timing Waveforms



AC Inputs during testing are driven at V_{IHT} (V_{DD} -0.5V) for Logic "1" and V_{ILT} (0.45V) for a Logic "0". Measurement reference points for inputs and outputs are at V_{HT} ($0.2V_{DD}$ + 0.9) and V_{LT} ($0.2V_{DD}$ - 0.1)

Note: V_{HT}- V_{HIGH} Test
V_{LT}- V_{LOW} Test
V_{IHT}-V_{INPUT} HIGH Test
V_{ILT}- V_{INPUT} LOW Test

Figure 41: AC Testing Input/Output Test Waveform

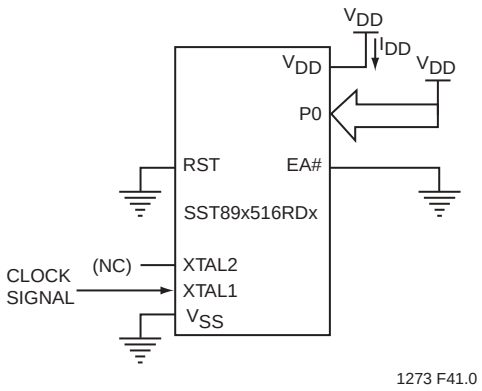


Figure 45: I_{DD} Test Condition, Idle Mode

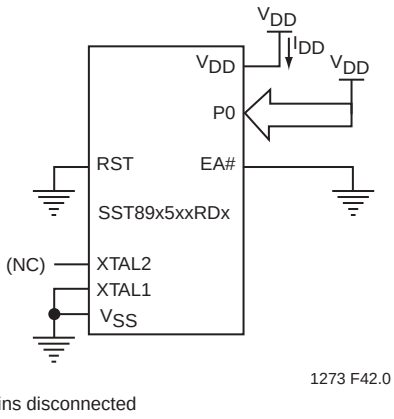


Figure 46: I_{DD} Test Condition, Power-down Mode

Table 41: Flash Memory Programming/Verification Parameters[1]

Parameter[2]	Max	Units
Chip-Erase Time	150	ms
Block-Erase Time	100	ms
Sector-Erase Time	30	ms
Byte-Program Time[3]	50	µs
Select-Block Program Time	500	ns
Re-map or Security bit Program Time	80	µs

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1. For IAP operations, the program execution overhead must be added to the above timing parameters.
2. Program and Erase times will scale inversely proportional to programming clock frequency.
3. Each byte must be erased before programming.

Table 42: Revision History

Revision	Description	Date
00	• Initial Release of S71273 data sheet. SST89E/V516RD2 devices were previously released in S71255-00-000 • S71273 and S71273(01): Added 40-WQFN (QI) package and associated MPNs • Added SST89E/V516RD PDIP devices and associated MPNs • Clarified the solder temperature profile under “Absolute Maximum Stress Ratings” on page 73 • Added RoHS compliance information on page 1 and in the “Product Ordering Information” on page 88 • Removed references to External Host Mode programming • Corrected MPN breakdown definition for “2” to read “Port 4 present” • Corrected the SPI control Register definition for CPHA on page 30	Mar 2005
01	• Status change from Preliminary Specifications to Data sheet	Mar 2005
02	• Removed NJ, TQJ, and PI from Valid Combinations on page 78 • Removed valid combination SST89E516RD-40-I-PIE and SST89V516RD-33-I-PIE on page 78	Oct 2006
03	• Replaced FlashFlex51 with FlashFlex globally	Jan 2007
A	• Applied new document format • Released document under letter revision system • Updated spec number from S71273 to DS25093	Nov 2011
B	• Removed “Not recommended for new designs” statement on page 1.	Feb 2013

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