Microchip Technology - SST89E516RD2-40-I-NJE-ZZ134 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	36
Program Memory Size	72KB (72K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sst89e516rd2-40-i-nje-zz134

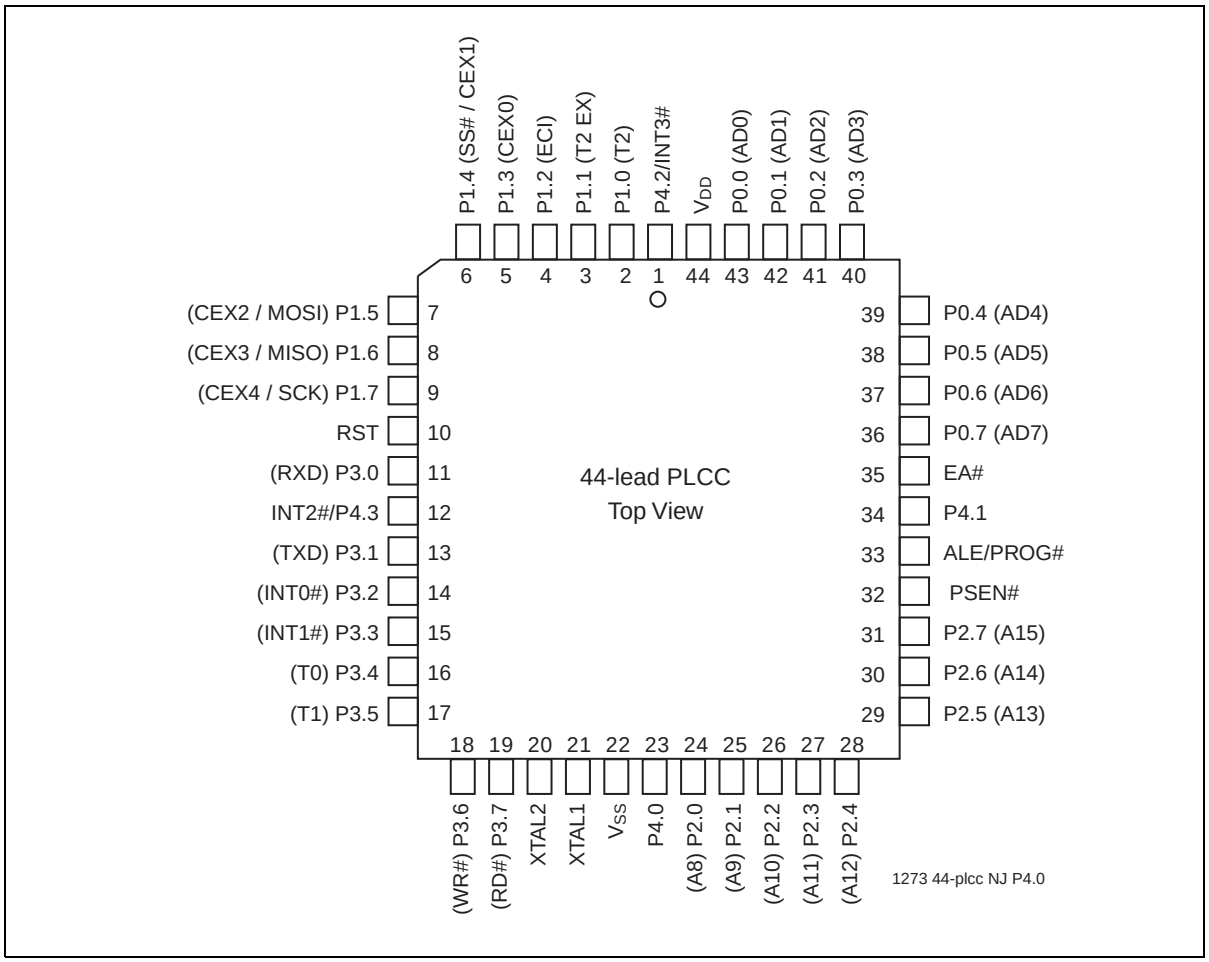

Figure 5: Pin Assignments for 44-lead PLCC

high-order eight address bits (DPH), and Port 0 multiplexes the low order eight address bits (DPL) with data. Both MOVX @Ri and MOVX @DPTR generates the necessary read and write signals (P3.6 - WR# and P3.7 - RD#) for external memory use. Table 4 shows external data memory RD#, WR# operation with EXTRAM bit.

The stack pointer (SP) can be located anywhere within the 256 bytes of internal RAM (lower 128 bytes and upper 128 bytes). The stack pointer may not be located in any part of the expanded RAM.

Table 4: External Data Memory RD#, WR# with EXTRAM bit

	MOVX @DPTR, A or MOVX A, @DPTR		MOVX @Ri, A or MOVX A, @Ri
AUXR	**ADDR < 0300H**	**ADDR >= 0300H**	**ADDR = Any**
EXTRAM = 0	RD# / WR# not asserted	RD# / WR# asserted	RD# / WR# not asserted[1]
EXTRAM = 1	RD# / WR# asserted	RD# / WR# asserted	RD# / WR# asserted

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1. Access limited to ERAM address within 0 to 0FFH; cannot access 100H to 02FFH.

Dual Data Pointers

The device has two 16-bit data pointers. The DPTR Select (DPS) bit in AUXR1 determines which of the two data pointers is accessed. When DPS=0, DPTR0 is selected; when DPS=1, DPTR1 is selected. Quickly switching between the two data pointers can be accomplished by a single INC instruction on AUXR1. (See Figure 8)

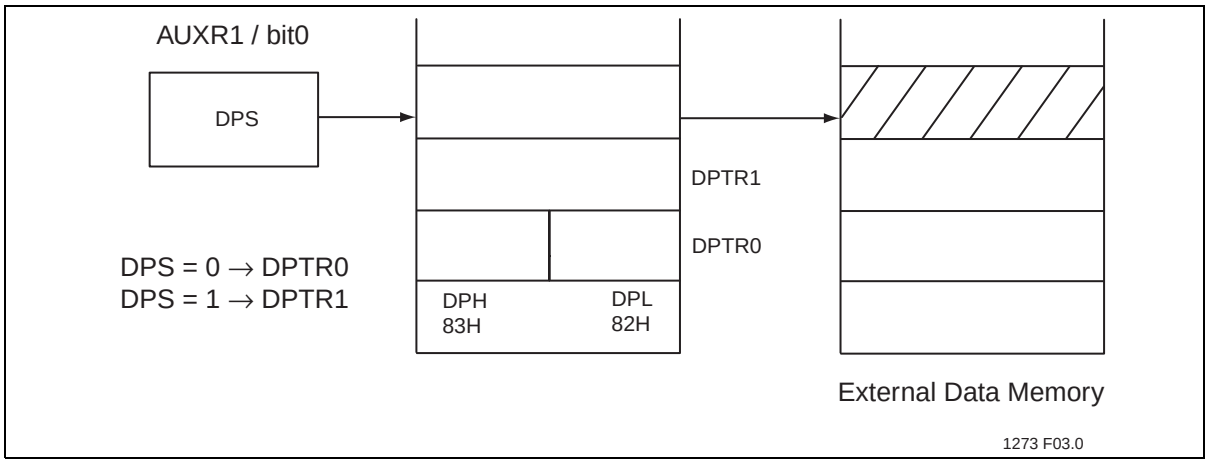

Figure 8: Dual Data Pointer Organization

Special Function Registers

Most of the unique features of the FlashFlex microcontroller family are controlled by bits in special function registers (SFRs) located in the SFR memory map shown in Table 5. Individual descriptions of each SFR are provided and reset values indicated in Tables 6 to 10.

Table 5: FlashFlex SFR Memory Map

	8 BYTES								
F8H	IP1[1]	CH	CCAP0H	CCAP1H	CCAP2H	CCAP3H	CCAP4H		FFH
F0H	B[1]							IP1H	F7H
E8H	IEA[1]	CL	CCAP0L	CCAP1L	CCAP2L	CCAP3L	CCAP4L		EFH
E0H	ACC[1]								E7H
D8H	CCON[1]	CMOD	CCAPM0	CCAPM1	CCAPM2	CCAPM3	CCAPM4		DFH
D0H	PSW[1]					SPCR			D7H
C8H	T2CON[1]	T2MOD	RCAP2L	RCAP2H	TL2	TH2			CFH
C0H	WDTC[1]								C7H
B8H	IP[1]	SADEN							BFH
B0H	P3[1]	SFCF	SFCM	SFAL	SFAH	SFDT	SFST	IPH	B7H
A8H	IE[1]	SADDR	SPSR				XICON		AFH
A0H	P2[1]		AUXR1			P4			A7H
98H	SCON[1]	SBUF							9FH
90H	P1[1]								97H
88H	TCON[1]	TMOD	TL0	TL1	TH0	TH1	AUXR		8FH
80H	P0[1]	SP	DPL	DPH		WDTD	SPDR	PCON	87H

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1. Bit addressable SFRs

Table 10: Interface SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	RESET Value
SBUF	Serial Data Buffer	99H	SBUF[7:0]								Indeterminate
SCON[1]	Serial Port Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SADDR	Slave Address	A9H	SADDR[7:0]								00H
SADEN	Slave Address Mask	B9H	SADEN[7:0]								00H
SPCR	SPI Control Register	D5H	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04H
SPSR	SPI Status Register	AAH	SPIF	WCOL							00H
SPDR	SPI Data Register	86H	SPDR[7:0]								00H
P0[1]	Port 0	80H	P0[7:0]								FFH
P1[1]	Port 1	90H	-	-	-	-	-	-	T2EX	T2	FFH
P2[1]	Port 2	A0H	P2[7:0]								FFH
P3[1]	Port 3	B0H	RD#	WR#	T1	T0	INT1#	INT0#	TXD	RXD	FFH
P4[2]	Port 4	A5H	1	1	1	1	P4.3	P4.2	P4.1	P4.0	FFH

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1. Bit Addressable SFRs
2. P4 is similar to P1 and P3 ports

SuperFlash Address Registers (SFAH)

Location	7	6	5	4	3	2	1	0	Reset Value
B4H	SuperFlash High Order Byte Address Register								00H

Symbol	Function
SFAH	Mailbox register for interfacing with flash memory block. (High order address register).

SuperFlash Data Register (SFDT)

Location	7	6	5	4	3	2	1	0	Reset Value
B5H	SuperFlash Data Register								00H

Symbol	Function
SFDT	Mailbox register for interfacing with flash memory block. (Data register).

SuperFlash Status Register (SFST) (Read Only Register)

Location	7	6	5	4	3	2	1	0	Reset Value
B6H	SB1_i	SB2_i	SB3_i	-	EDC_i	FLASH_BUSY	-	-	xxxxx0xxb

Symbol	Function
SB1_i	Security Bit 1 status (inverse of SB1 bit)
SB2_i	Security Bit 2 status (inverse of SB2 bit)
SB3_i	Security Bit 3 status (inverse of SB3 bit) Please refer to Table 25 for security lock options.
EDC_i	Double Clock Status 0: 12 clocks per machine cycle 1: 6 clocks per machine cycle
FLASH_BUSY	Flash operation completion polling bit. 0: Device has fully completed the last IAP command. 1: Device is busy with flash operation.

PCA Compare/Capture Module Mode Register[1] (CCAPMn)

Location	7	6	5	4	3	2	1	0	Reset Value
DAH	-	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0	00xxx000b
DBH	-	ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1	00xxx000b
DCH	-	ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2	00xxx000b
DDH	-	ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3	00xxx000b
DEH	-	ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4	00xxx000b

1. Not bit addressable

Symbol **Function**

-
Not implemented, reserved for future use.
Note: User should not write ‘1’s to reserved bits. The value read from a reserved bit is indeterminate.

ECOMn
Enable Comparator
0: Disables the comparator function
1: Enables the comparator function

CAPPn
Capture Positive
0: Disables positive edge capture on CEX[4:0]
1: Enables positive edge capture on CEX[4:0]

CAPNn
Capture Negative
0: Disables negative edge capture on CEX[4:0]
1: Enables negative edge capture on CEX[4:0]

MATn
Match: Set ECOM[4:0] and MAT[4:0] to implement the software timer mode
0: Disables software timer mode
1: A match of the PCA counter with this module’s compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.

TOGn
Toggle
0: Disables toggle function
1: A match of the PCA counter with this module’s compare/capture register causes the CEXn pin to toggle.

PWMn
Pulse Width Modulation mode
0: Disables PWM mode
1: Enables CEXn pin to be used as a pulse width modulated output

ECCFn
Enable CCF Interrupt
0: Disables compare/capture flag CCF[4:0] in the CCON register to generate an interrupt request.
1: Enables compare/capture flag CCF[4:0] in the CCON register to generate an interrupt request.

External Interrupt Control (XICON)

Location	7	6	5	4	3	2	1	0	Reset Value
AEH	-	EX3	IE3	IT3	0	EX2	IE2	IT2	00H

Symbol	Function
EX2	External Interrupt 2 Enable bit if set
IE2	Interrupt Enable If IT2=1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced.
IT2	External Interrupt 2 is falling-edge/low-level triggered when this bit is cleared by software.
EX3	External Interrupt 3 Enable bit if set
IE3	Interrupt Enable If IT3=1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced.
IT3	External Interrupt3 is falling-edge/low-level triggered when this bit is cleared by software.

Block 1, then the target address is implicitly defined to be in Block 0. If the IAP operation originates from external program space, then, the target will depend on the address and the state of bank selection.

IAP Enable Bit

The IAP enable bit, SFCF[6], enables in-application programming mode. Until this bit is set, all flash programming IAP commands will be ignored.

Table 13: IAP Address Resolution

EA#	SFCF[1:0]	Address of IAP Inst.	Target Address	Block Being Programmed
1	00	>= 2000H (Block 0)	>= 2000H (Block 0)	None[1]
1	00	>= 2000H (Block 0)	< 2000H (Block 1)	Block 1
1	00	< 2000H (Block 1)	Any (Block 0)	Block 0
1	01, 10, 11	Any (Block 0)	>= 2000H (Block 0)	None[1]
1	01, 10, 11	Any (Block 0)	< 2000H (Block 1)	Block 1
0	00	From external	>= 2000H (Block 0)	Block 0
0	00	From external	< 2000H (Block 1)	Block 1
0	01, 10, 11	From external	Any (Block 0)	Block 0

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1. No operation is performed because code from one block may not program the same originating block

In-Application Programming Mode Commands

All of the following commands can only be initiated in the IAP mode. In all situations, writing the control byte to the SFCM register will initiate all of the operations. All commands will not be enabled if the security locks are enabled on the selected memory block.

The Program command is for programming new data into the memory array. The portion of the memory array to be programmed should be in the erased state, FFH. If the memory is not erased, it should first be erased with an appropriate Erase command. **Warning: Do not attempt to write (program or erase) to a block that the code is currently fetching from. This will cause unpredictable program behavior and may corrupt program data.**

Prog-SC0

Prog-SC0 command is used to program the SC0 bit. This command only changes the SC0 bit and has no effect on BSEL bit until after a reset cycle.

SC0 bit previously in un-programmed state can be programmed by this command. The Prog-SC0 command should reside only in Block 1 or external code memory.

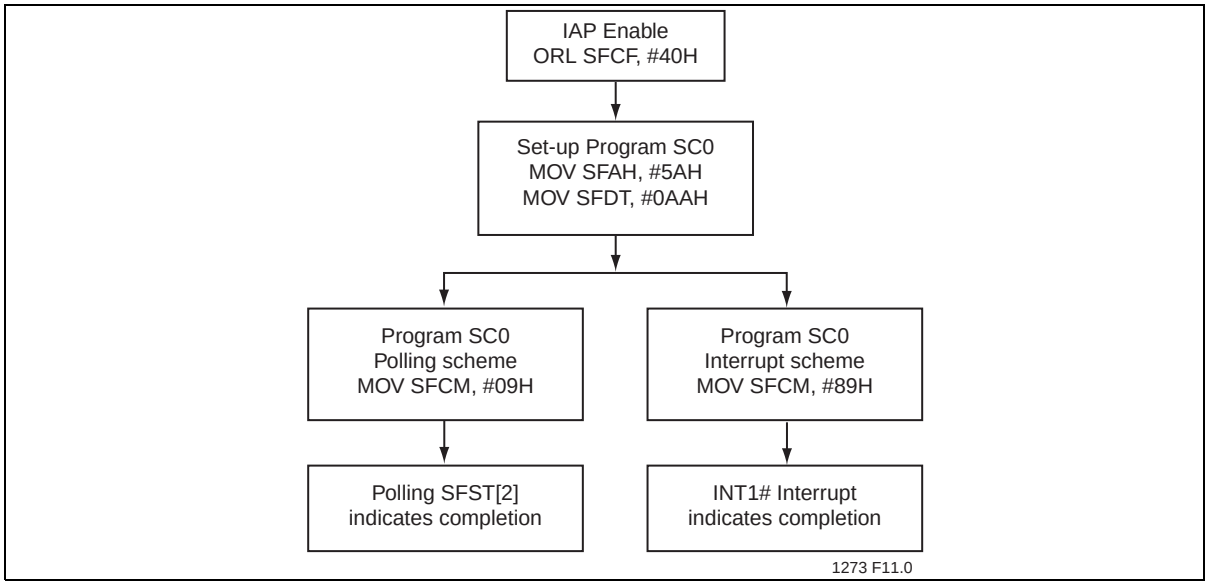

Figure 15: Prog-SC0

Enable-Clock-Double

Enable-Clock-Double command is used to make the MCU run at 6 clocks per machine cycle. The standard (default) is 12 clocks per machine cycle (i.e. clock double command disabled).

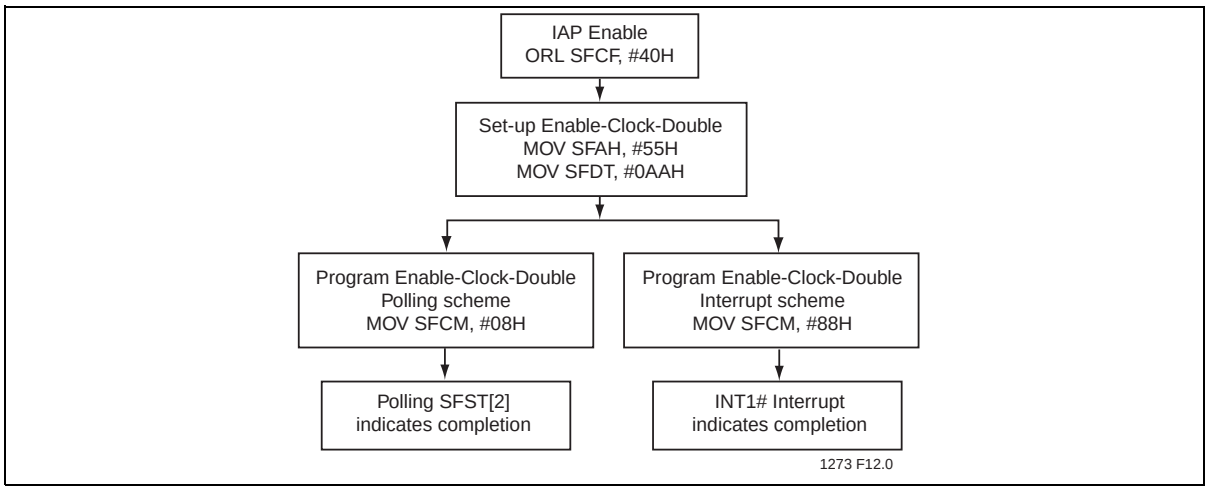

Figure 16: Enable-Clock-Double

There are no IAP counterparts for the external host commands Select-Block0 and Select-Block1.

Polling

A command that uses the polling method to detect flash operation completion should poll on the FLASH_BUSY bit (SFST[2]). When FLASH_BUSY de-asserts (logic 0), the device is ready for the next operation.

MOVC instruction may also be used for verification of the Programming and Erase operation of the flash memory. MOVC instruction will fail if it is directed at a flash block that is still busy.

Interrupt Termination

If interrupt termination is selected, (SFCM[7] is set), then an interrupt (INT1) will be generated to indicate flash operation completion. Under this condition, the INT1 becomes an internal interrupt source. The INT1# pin can now be used as a general purpose port pin and it cannot be the source of External Interrupt 1 during in-application programming.

In order to use an interrupt to signal flash operation termination. EX1 and EA bits of IE register must be set. The IT1 bit of TCON register must also be set for edge trigger detection.

Table 14: IAP Commands[1]

Operation	SFCM [6:0][2]	SFDT [7:0]	SFAH [7:0]	SFAL [7:0]
Chip-Erase[3]	01H	55H	X[4]	X
Block-Erase[5]	0DH	55H	AH	X
Sector-Erase[5]	0BH	X	AH[6]	AL[7]
Byte-Program[5]	0EH	DI[8]	AH	AL
Byte-Verify (Read)[5]	0CH	DO[8]	AH	AL
Prog-SB1[9]	0FH	AAH	X	X
Prog-SB2[9]	03H	AAH	X	X
Prog-SB3[9]	05H	AAH	X	X
Prog-SC0[9]	09H	AAH	5AH	X
Enable-Clock-Double[9]	08H	AAH	55H	X

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1. SFCF[6]=1 enables IAP commands; SFCF[6]=0 disables IAP commands.
2. Interrupt/Polling enable for flash operation completion
   SFCM[7] =1: Interrupt enable for flash operation completion
   0: polling enable for flash operation completion
3. Chip-Erase only functions in IAP mode when EA#=0 (external memory execution) and device is not in level 4 locking.
4. X can be V_{IL} or V_{IH}, but no other value.
5. Refer to Table 13 for address resolution
6. AH = Address high order byte
7. AL = Address low order byte
8. DI = Data Input, DO = Data Output, all other values are in hex.
9. Instruction must be located in Block 1 or external code memory.

Note: DISIAPL pin in PLCC or TQFP will also disable IAP commands if it is externally pulled low when reset.

Timers/Counters

Timers

The device has three 16-bit registers that can be used as either timers or event counters. The three timers/counters are denoted Timer 0 (T0), Timer 1 (T1), and Timer 2 (T2). Each is designated a pair of 8-bit registers in the SFRs. The pair consists of a most significant (high) byte and least significant (low) byte. The respective registers are TL0, TH0, TL1, TH1, TL2, and TH2.

Timer Set-up

Refer to Table 9 for TMOD, TCON, and T2CON registers regarding timers T0, T1, and T2. The following tables provide TMOD values to be used to set up Timers T0, T1, and T2.

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set separately to turn the timer on.

Table 15: Timer/Counter 0

	Mode	Function	TMOD	
			Internal Control[1]	External Control[2]
Used as Timer	0	13-bit Timer	00H	08H
	1	16-bit Timer	01H	09H
	2	8-bit Auto-Reload	02H	0AH
	3	Two 8-bit Timers	03H	0BH
Used as Counter	0	13-bit Timer	04H	0CH
	1	16-bit Timer	05H	0DH
	2	8-bit Auto-Reload	06H	0EH
	3	Two 8-bit Timers	07H	0FH

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1. The Timer is turned ON/OFF by setting/clearing bit TR0 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on INT0# (P3.2) when TR0 = 1 (hardware control).

Table 16: Timer/Counter 1

	Mode	Function	TMOD	
			Internal Control[1]	External Control[2]
Used as Timer	0	13-bit Timer	00H	80H
	1	16-bit Timer	10H	90H
	2	8-bit Auto-Reload	20H	A0H
	3	Does not run	30H	B0H
Used as Counter	0	13-bit Timer	40H	C0H
	1	16-bit Timer	50H	D0H
	2	8-bit Auto-Reload	60H	E0H
	3	Not available	-	-

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1. The Timer is turned ON/OFF by setting/clearing bit TR1 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on INT1# (P3.3) when TR1 = 1 (hardware control).

16-Bit Software Timer Mode

The 16-bit software timer mode is used to trigger interrupt routines, which must occur at periodic intervals. It is setup by setting both the ECOM and MAT bits in the module's CCAPMn register. The PCA timer will be compared to the module's capture registers (CCAPnL and CCAPnH) and when a match occurs, an interrupt will occur, if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set.

If necessary, a new 16-bit compare value can be loaded into CCAPnH and CCAPnL during the interrupt routine. The user should be aware that the hardware temporarily disables the comparator function while these registers are being updated so that an invalid match will not occur. Thus, it is recommended that the user write to the low byte first (CCAPnL) to disable the comparator, then write to the high byte (CCAPnH) to re-enable it. If any updates to the registers are done, the user may want to hold off any interrupts from occurring by clearing the EA bit. (See Figure 26)

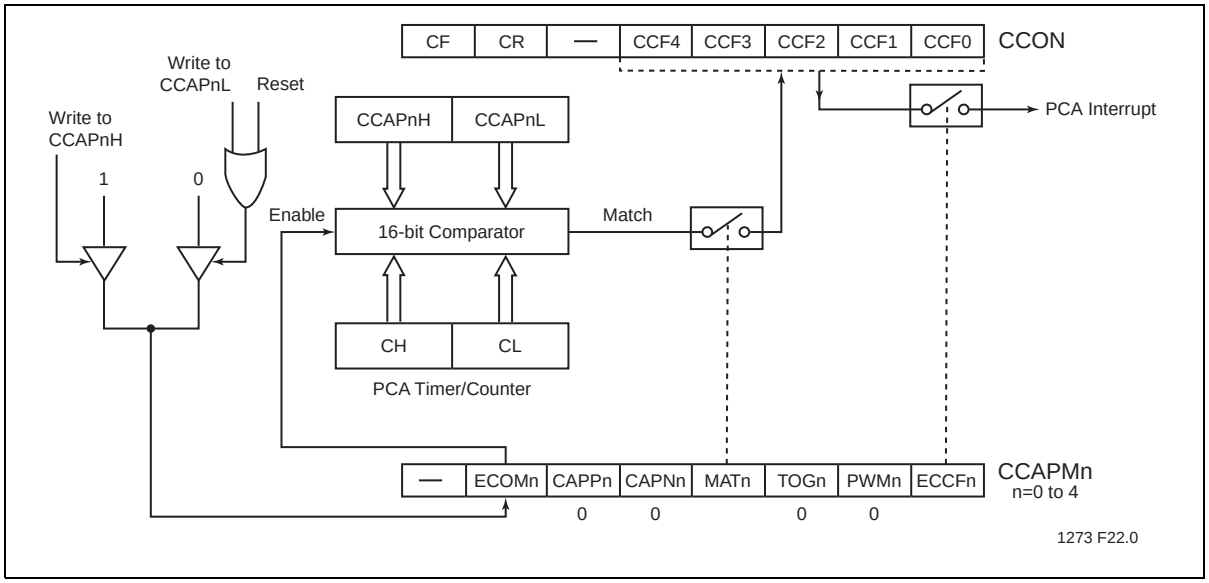

Figure 26: PCA Compare Mode (Software Timer)

High Speed Output Mode

The high speed output mode is used to toggle a port pin when a match occurs between the PCA timer and the preloaded value in the compare registers. In this mode, the CEX output pin (on port 1) associated with the PCA module will toggle every time there is a match between the PCA counter (CH and CL) and the capture registers (CCAPnH and CCAPnL). To activate this mode, the user must set TOG, MAT, and ECOM bits in the module's CCAPMn SFR.

High speed output mode is much more accurate than toggling pins since the toggle occurs before branching to an interrupt. In this case, interrupt latency will not affect the accuracy of the output. When using high speed output, using an interrupt is optional. Only if the user wishes to change the time for the next toggle is it necessary to update the compare registers. Otherwise, the next toggle will occur when the PCA timer rolls over and matches the last compare value. (See Figure 27)

Security Lock

The security lock protects against software piracy and prevents the contents of the flash from being read by unauthorized parties. It also protects against code corruption resulting from accidental erasing and programming to the internal flash memory. There are two different types of security locks in the device security lock system: hard lock and SoftLock.

Hard Lock

When hard lock is activated, MOVC or IAP instructions executed from an unlocked or soft locked program address space, are disabled from reading code bytes in hard locked memory blocks (See Table 26). Hard lock can either lock both flash memory blocks or just lock the 8 KByte flash memory block (Block 1). All external host and IAP commands except for Chip-Erase are ignored for memory blocks that are hard locked.

SoftLock

SoftLock allows flash contents to be altered under a secure environment. This lock option allows the user to update program code in the soft locked memory block through in-application programming mode under a predetermined secure environment. For example, if Block 1 (8K) memory block is locked (hard locked or soft locked), and Block 0 memory block is soft locked, code residing in Block 1 can program Block 0. The following IAP mode commands issued through the command mailbox register, SFCM, executed from a Locked (hard locked or soft locked) block, can be operated on a soft locked block: Block-Erase, Sector-Erase, Byte-Program and Byte-Verify.

In external host mode, SoftLock behaves the same as a hard lock.

Security Lock Status

The three bits that indicate the device security lock status are located in SFST[7:5]. As shown in Figure 30 and Table 25, the three security lock bits control the lock status of the primary and secondary blocks of memory. There are four distinct levels of security lock status. In the first level, none of the security lock bits are programmed and both blocks are unlocked. In the second level, although both blocks are now locked and cannot be programmed, they are available for read operation via Byte-Verify. In the third level, three different options are available: Block 1 hard lock / Block 0 SoftLock, SoftLock on both blocks, and hard lock on both blocks. Locking both blocks is the same as Level 2, Block 1 except read operation isn't available. The fourth level of security is the most secure level. It doesn't allow read/program of internal memory or boot from external memory. For details on how to program the security lock bits refer to the external host mode and in-application programming sections.

Interrupts

Interrupt Priority and Polling Sequence

The device supports eight interrupt sources under a four level priority scheme. Table 27 summarizes the polling sequence of the supported interrupts. Note that the SPI serial interface and the UART share the same interrupt vector. (See Figure 32)

Table 27: Interrupt Polling Sequence

Description	Interrupt Flag	Vector Address	Interrupt Enable	Interrupt Priority	Service Priority	Wake-Up Power-down
Ext. Int0	IE0	0003H	EX0	PX0/H	1(highest)	yes
Brown-out	-	004BH	EBO	PBO/H	2	no
T0	TF0	000BH	ET0	PT0/H	3	no
Ext. Int1	IE1	0013H	EX1	PX1/H	4	yes
T1	TF1	001BH	ET1	PT1/H	5	no
PCA	CF/CCFn	0033H	EC	PPCH	6	no
Ext. Int. 2	IE2	003BH	EX2	PX2/H	7	no
Ext. Int. 3	IE3	0043H	EX3	PX3/H	8	no
UART/SPI	TI/RI/SPIF	0023H	ES	PS/H	9	no
T2	TF2, EXF2	002BH	ET2	PT2/H	10	no

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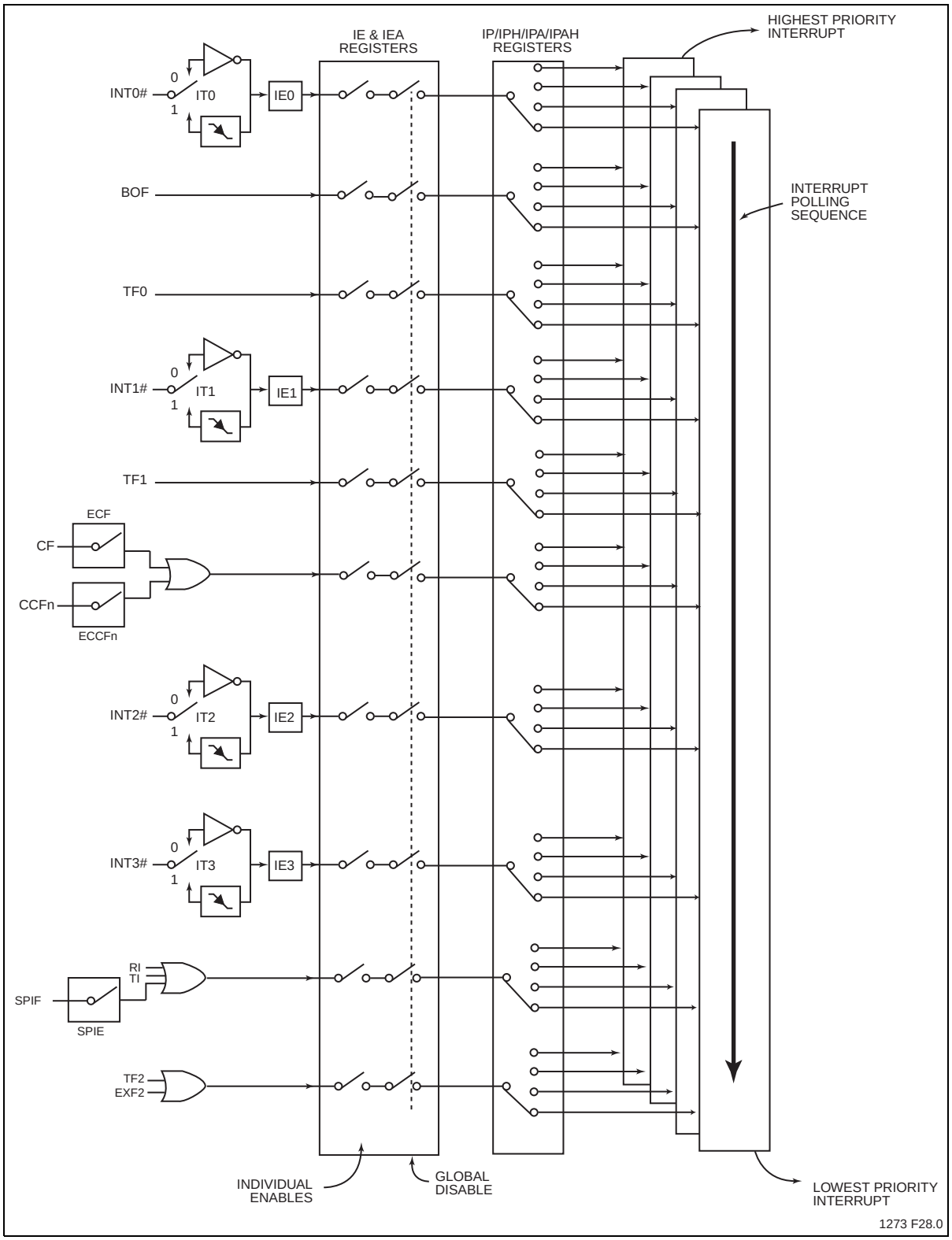


Figure 32: Interrupt Structure

1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 15mA
   Maximum I_{OL} per 8-bit port: 26mA
   Maximum I_{OL} total for all outputs: 71mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification.
   Pins are not guaranteed to sink current greater than the listed test conditions.
2. Capacitive loading on Ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and Ports 1 & 3. The noise due to external bus capacitance discharging into the Port 0 & 2 pins when the pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
3. Load capacitance for Port 0, ALE & PSEN#= 100pF, load capacitance for all other outputs = 80pF.
4. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and PSEN# to momentarily fall below the V_{DD} - 0.7 specification when the address bits are stabilizing.
5. Pins of Ports 1, 2, and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
6. Pin capacitance is characterized but not tested. EA# is 25pF (max).

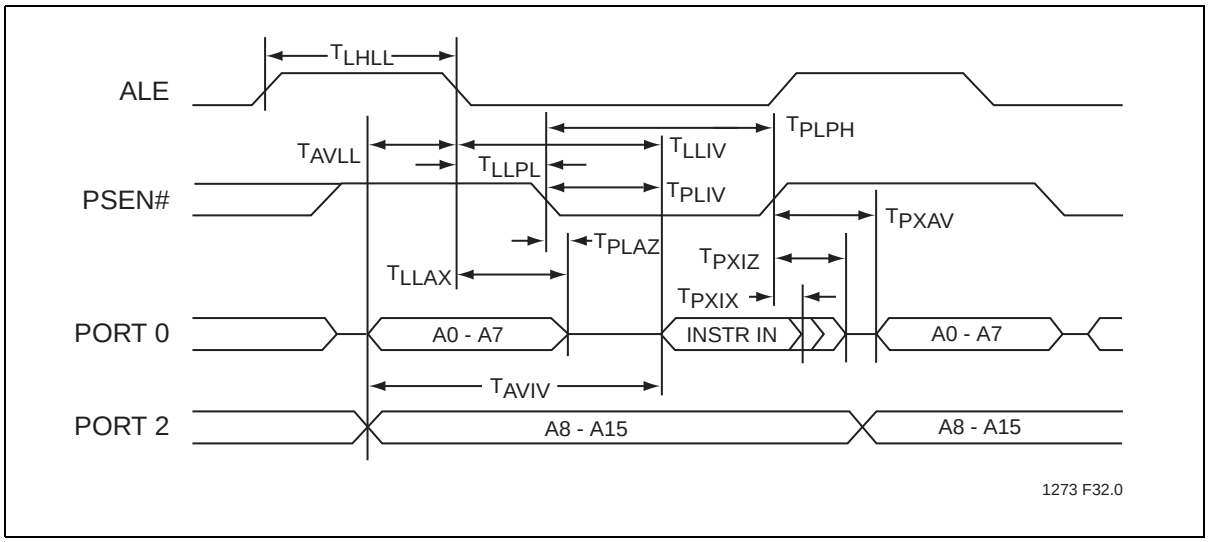


Figure 36: External Program Memory Read Cycle

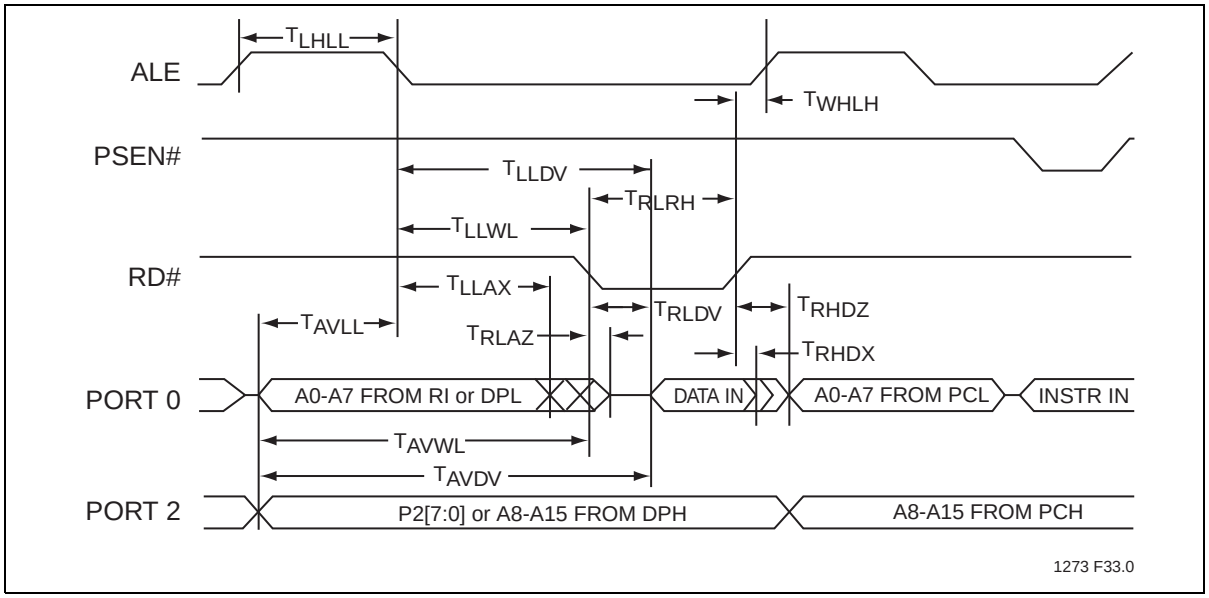
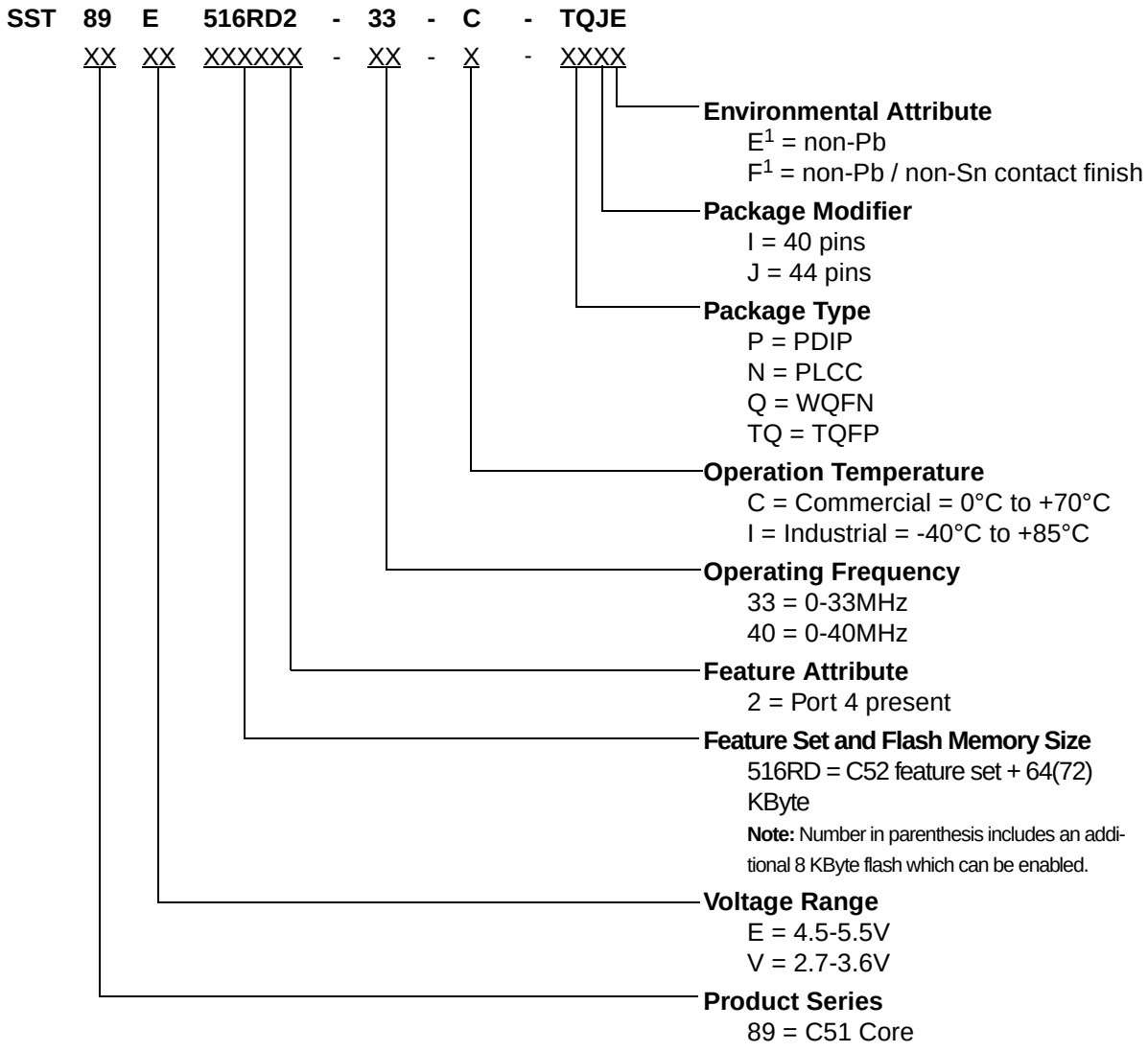


Figure 37: External Data Memory Read Cycle

Product Ordering Information



1. Environmental suffix “E” denotes non-Pb solder. Environmental suffix “F” denote non-Pb /non-Sn solder. SST non-Pb / non-Sn solder devices are “RoHS Compliant”.

Packaging Diagrams

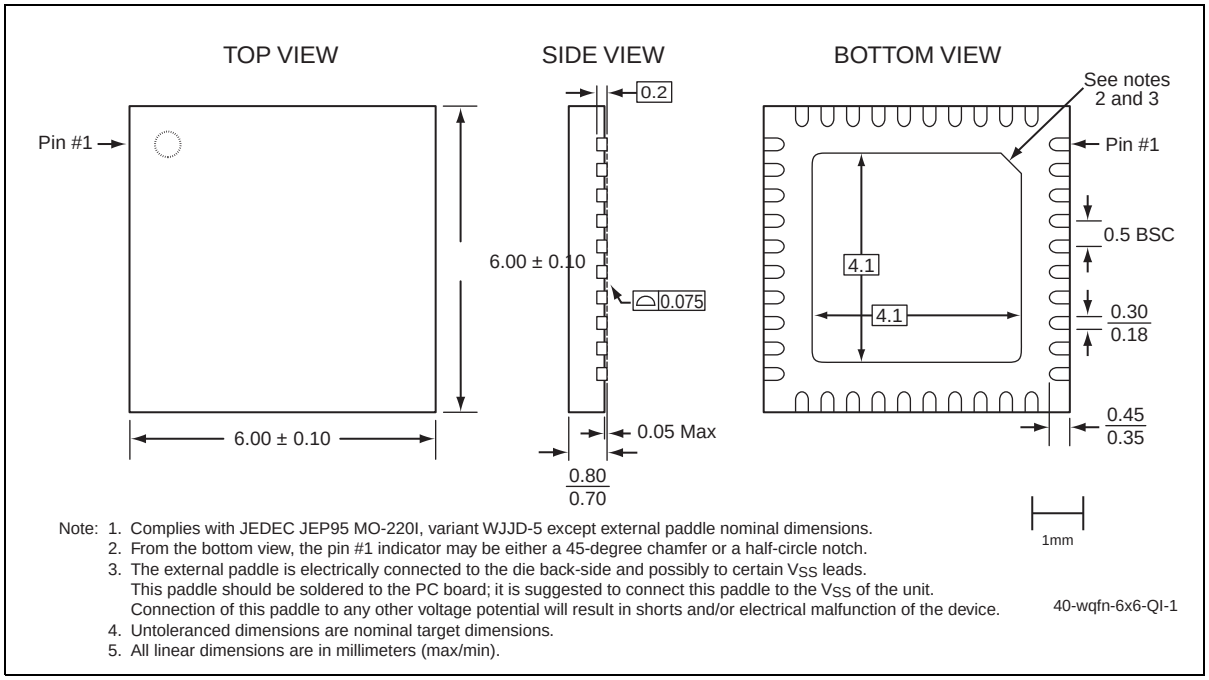
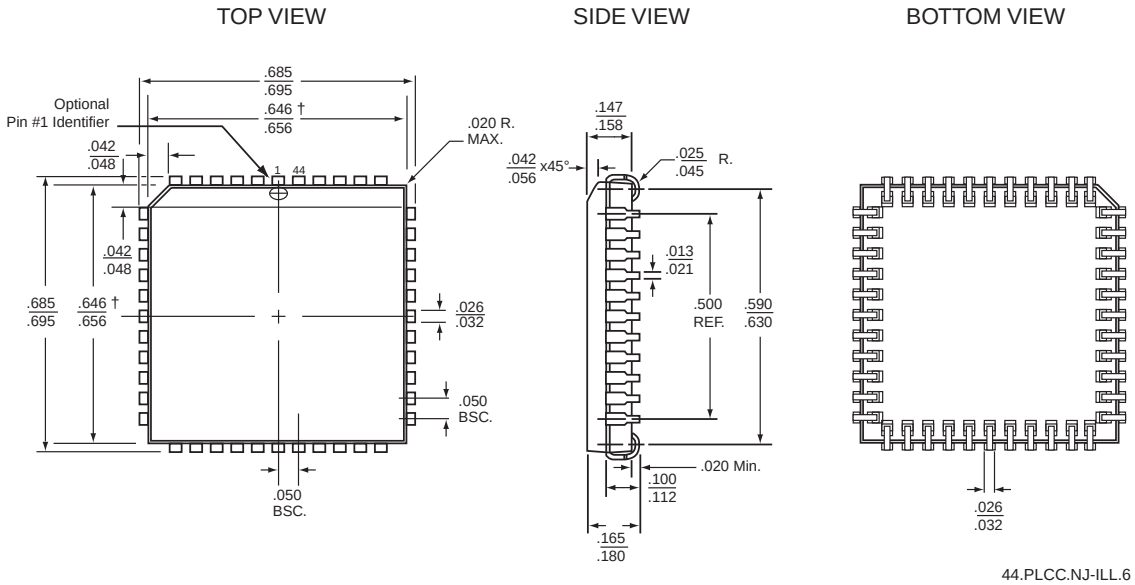


Figure 47: 40-contact Very-very-thin Quad Flat No-lead (WQFN)
SST Package Code: QI



Note:
1. Complies with JEDEC publication 95 MS-018 AC dimensions (except as noted), although some dimensions may be more stringent.
   † = JEDEC min is .650; SST min is *less*stringent
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.
4. Coplanarity: ± 4 mils.

Figure 49: 44-lead Plastic Lead Chip Carrier (PLCC)
SST Package Code: NJ