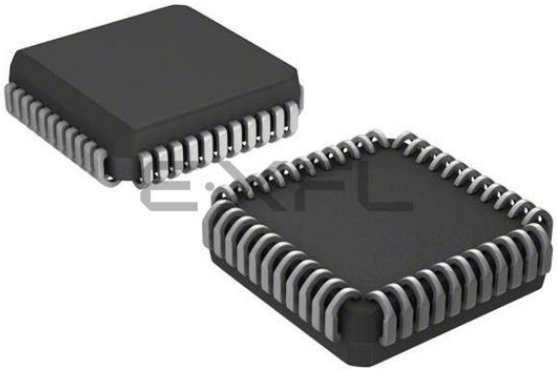

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	36
Program Memory Size	72KB (72K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sst89e516rd2-40-i-nje

Product Description

The SST89E516RDx and SST89V516RDx are members of the FlashFlex family of 8-bit microcontroller products designed and manufactured with SST's patented and proprietary SuperFlash CMOS semiconductor process technology. The split-gate cell design and thick-oxide tunneling injector offer significant cost and reliability benefits for SST's customers. The devices use the 8051 instruction set and are pin-for-pin compatible with standard 8051 microcontroller devices.

The devices come with 72 KByte of on-chip flash EEPROM program memory which is partitioned into 2 independent program memory blocks. The primary Block 0 occupies 64 KByte of internal program memory space and the secondary Block 1 occupies 8 KByte of internal program memory space.

The 8-KByte secondary block can be mapped to the lowest location of the 64 KByte address space; it can also be hidden from the program counter and used as an independent EEPROM-like data memory.

In addition to the 72 KByte of EEPROM program memory on-chip and 1024 x8 bits of on-chip RAM, the devices can address up to 64 KByte of external program memory and up to 64 KByte of external RAM.

The flash memory blocks can be programmed via a standard 87C5x OTP EPROM programmer fitted with a special adapter and the firmware for SST's devices. During power-on reset, the devices can be configured as either a slave to an external host for source code storage or a master to an external host for an in-application programming (IAP) operation. The devices are designed to be programmed in-system and in-application on the printed circuit board for maximum flexibility. The devices are pre-programmed with an example of the bootstrap loader in the memory, demonstrating the initial user program code loading or subsequent user code updating via the IAP operation. The sample bootstrap loader is available for the user's reference and convenience only; SST does not guarantee its functionality or usefulness. Chip-Erase or Block-Erase operations will erase the pre-programmed sample code.

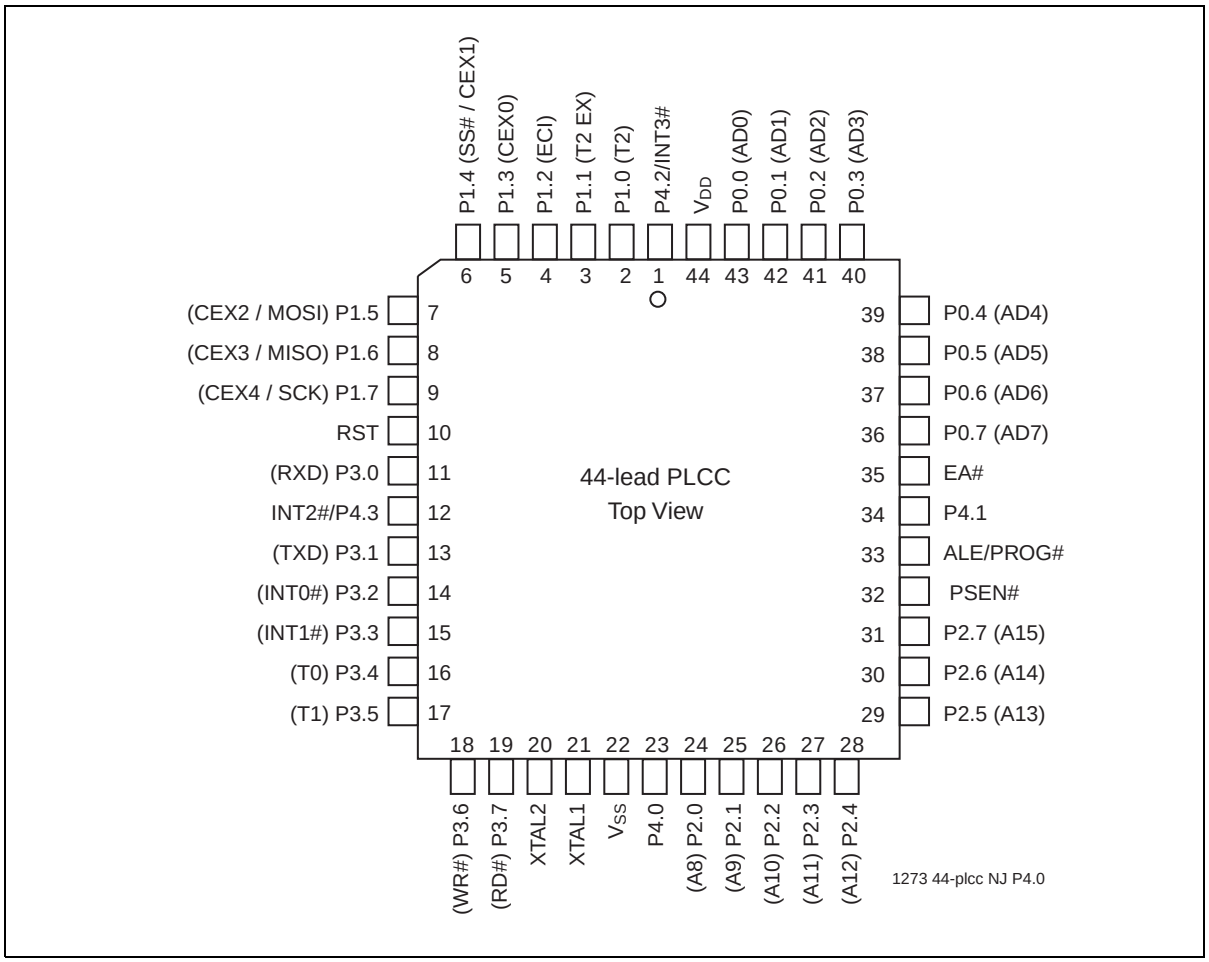

Figure 5: Pin Assignments for 44-lead PLCC

Table 1: Pin Descriptions (Continued) (2 of 3)

Symbol	Type[1]	Name and Functions
P3[7:0]	I/O with internal pull-up	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins are pulled high by the internal pull-ups when "1"s are written to them and can be used as inputs in this state. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Port 3 also receives some control signals and a partial of high-order address bits during the external host mode programming and verification.
P3[0]	I	**RXD:** Universal Asynchronous Receiver/Transmitter (UART) - Receive input
P3[1]	O	**TXD:** UART - Transmit output
P3[2]	I	**INT0#:** External Interrupt 0 Input
P3[3]	I	**INT1#:** External Interrupt 1 Input
P3[4]	I	**T0:** External count input to Timer/Counter 0
P3[5]	I	**T1:** External count input to Timer/Counter 1
P3[6]	O	**WR#:** External Data Memory Write strobe
P3[7]	O	**RD#:** External Data Memory Read strobe
PSEN#	I/O	**Program Store Enable:** PSEN# is the Read strobe to External Program Store. When the device is executing from Internal Program Memory, PSEN# is inactive (V_{OH}). When the device is executing code from External Program Memory, PSEN# is activated twice each machine cycle, except when access to External Data Memory while one PSEN# activation is skipped in each machine cycle. A forced high-to-low input transition on the PSEN# pin while the RST input is continually held high for more than ten machine cycles will cause the device to enter External Host mode for programming.
RST	I	**Reset:** While the oscillator is running, a high logic state on this pin for two machine cycles will reset the device. After a reset, if the PSEN# pin is driven by a high-to-low input transition while the RST input pin is held high, the device will enter the External Host mode, otherwise the device will enter the Normal operation mode.
EA#	I	**External Access Enable:** EA# must be driven to V_{IL} in order to enable the device to fetch code from the External Program Memory. EA# must be driven to V_{IH} for internal program execution. However, Security lock level 4 will disable EA#, and program execution is only possible from internal program memory. The EA# pin can tolerate a high voltage[2] of 12V.
ALE/ PROG#	I/O	**Address Latch Enable:** ALE is the output signal for latching the low byte of the address during an access to external memory. This pin is also the programming pulse input (PROG#) for flash programming. Normally the ALE[3] is emitted at a constant rate of 1/6 the crystal frequency[4] and can be used for external timing and clocking. One ALE pulse is skipped during each access to external data memory. However, if AO is set to 1, ALE is disabled.
P4[3:0][5]	I/O with internal pull-ups	**Port 4:** Port 4 is an 4-bit bi-directional I/O port with internal pull-ups. The port 4 output buffers can drive LS TTL inputs. Port 4 pins are pulled high by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, port 4 pins that are externally pulled low will source current because of the internal pull-ups.
P4[0]	I/O	Bit 0 of port 4
P4[1]	I/O	Bit 1 of port 4
P4[2] / INT3#	I/O	Bit 2 of port 4 / INT3# External interrupt 3 input

high-order eight address bits (DPH), and Port 0 multiplexes the low order eight address bits (DPL) with data. Both MOVX @Ri and MOVX @DPTR generates the necessary read and write signals (P3.6 - WR# and P3.7 - RD#) for external memory use. Table 4 shows external data memory RD#, WR# operation with EXTRAM bit.

The stack pointer (SP) can be located anywhere within the 256 bytes of internal RAM (lower 128 bytes and upper 128 bytes). The stack pointer may not be located in any part of the expanded RAM.

Table 4: External Data Memory RD#, WR# with EXTRAM bit

	MOVX @DPTR, A or MOVX A, @DPTR		MOVX @Ri, A or MOVX A, @Ri
AUXR	**ADDR < 0300H**	**ADDR >= 0300H**	**ADDR = Any**
EXTRAM = 0	RD# / WR# not asserted	RD# / WR# asserted	RD# / WR# not asserted[1]
EXTRAM = 1	RD# / WR# asserted	RD# / WR# asserted	RD# / WR# asserted

T0-0.0 25093

1. Access limited to ERAM address within 0 to 0FFH; cannot access 100H to 02FFH.

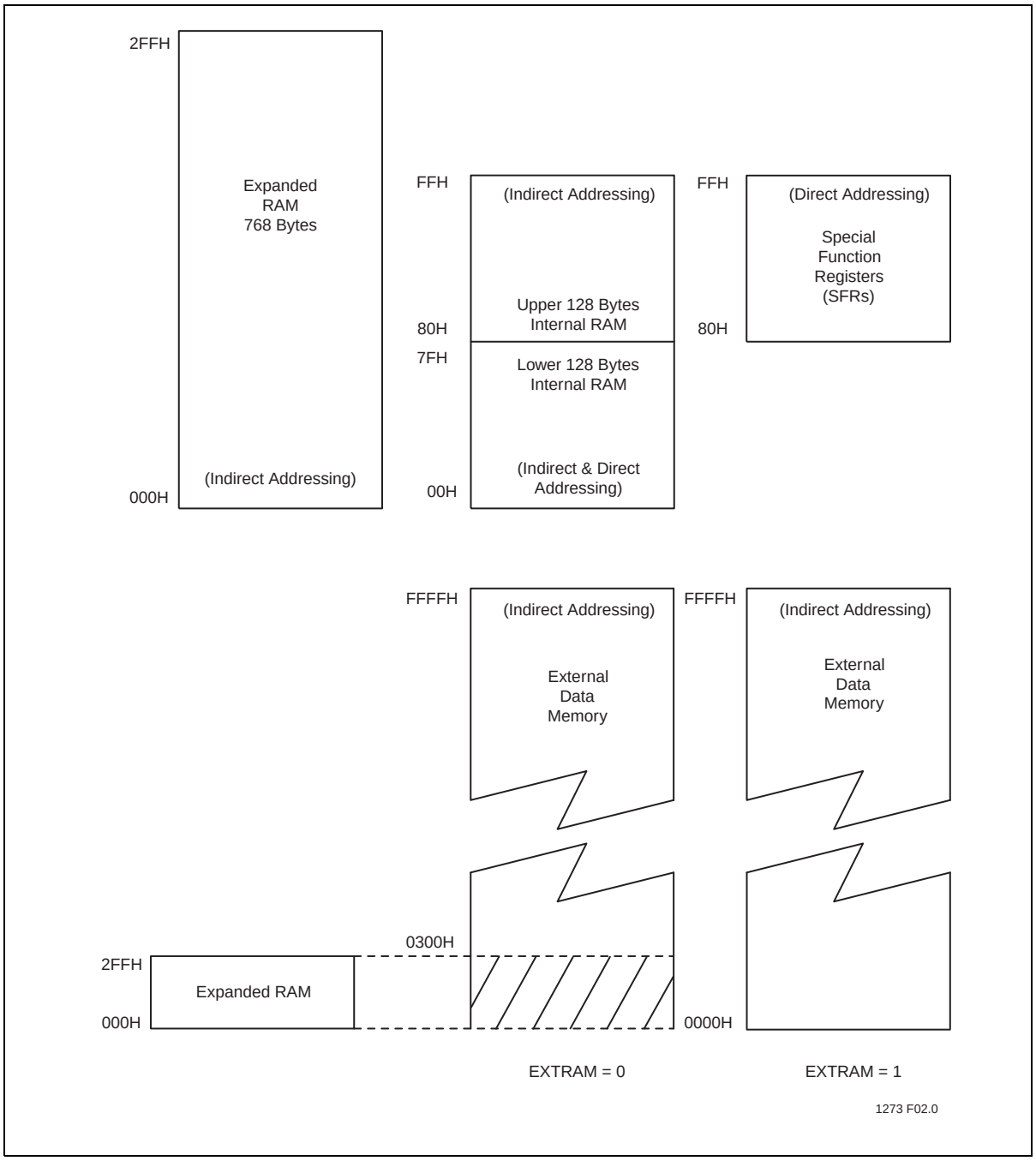

Figure 7: Internal and External Data Memory Structure

Table 6: CPU related SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
ACC[1]	Accumulator	E0H	ACC[7:0]								00H
B[1]	B Register	F0H	B[7:0]								00H
PSW[1]	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00H
SP	Stack Pointer	81H	SP[7:0]								07H
DPL	Data Pointer Low	82H	DPL[7:0]								00H
DPH	Data Pointer High	83H	DPH[7:0]								00H
IE[1]	Interrupt Enable	A8H	EA	EC	ET2	ES	ET1	EX1	ET0	EX0	00H
IEA[1]	Interrupt Enable A	E8H	-	-	-	-	EBO	-	-	-	xxxx0xxx b
IP[1]	Interrupt Priority Reg	B8H	-	PPC	PT2	PS	PT1	PX1	PT0	PX0	x0000000 b
IPH	Interrupt Priority Reg High	B7H	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	x0000000 b
IP1[1]	Interrupt Priority Reg A	F8H	-	-	-	-	PBO	PX3	PX2	-	xxxx0xxx b
IP1H	Interrupt Priority Reg A High	F7H	-	-	-	-	PBOH	PX3H	PX2H	-	xxxx0xxx b
PCON	Power Control	87H	SMOD1	SMOD0	BOF	POF	GF1	GF0	PD	IDL	00010000 b
AUXR	Auxiliary Reg	8EH	-	-	-	-	-	-	EXTRAM	AO	xxxxxxx0 0b
AUXR1	Auxiliary Reg 1	A2H	-	-	-	-	GF2	0	-	DPS	xxxx00x0 b
XICON	External Interrupt Control	AEH	-	EX3	IE3	IT3	0	EX2	IE2	IT2	00H

T0-0.0 25093

1. Bit Addressable SFRs

Table 7: Flash Memory Programming SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
SFCF	SuperFlash Configuration	B1H	-	IAPEN	-	-	-	-	SWR	BSEL	x0xxxx00b
SFCM	SuperFlash Command	B2H	FIE	FCM[6:0]							00H
SFAL	SuperFlash Address Low	B3H	SuperFlash Low Order Byte Address Register - A_7 to A_0 (SFAL)								00H
SFAH	SuperFlash Address High	B4H	SuperFlash High Order Byte Address Register - A_{15} to A_8 (SFAH)								00H
SFDT	SuperFlash Data	B5H	SuperFlash Data Register								00H
SFST	SuperFlash Status	B6H	SB1_i	SB2_i	SB3_i	-	EDC_i	FLASH_BUSY	-	-	000x00xxb

T0-0.0 25093

Table 8: Watchdog Timer SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
WDTC [1]	Watchdog Timer Control	C0H	-	-	-	WDOUT	WDRE	WDTS	WDT	SWDT	xxx00x00b
WDTD	Watchdog Timer Data/Reload	85H	Watchdog Timer Data/Reload								00H

T0-0.0 25093

1. Bit Addressable SFRs

Interrupt Priority (IP)

Location	7	6	5	4	3	2	1	0	Reset Value
B8H	-	PPC	PT2	PS	PT1	PX1	PT0	PX0	x0000000b

Symbol	Function
PPC	PCA interrupt priority bit
PT2	Timer 2 interrupt priority bit
PS	Serial Port interrupt priority bit
PT1	Timer 1 interrupt priority bit
PX1	External interrupt 1 priority bit
PT0	Timer 0 interrupt priority bit
PX0	External interrupt 0 priority bit

Interrupt Priority High (IPH)

Location	7	6	5	4	3	2	1	0	Reset Value
B7H	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	x0000000b

Symbol	Function
PPCH	PCA interrupt priority bit high
PT2H	Timer 2 interrupt priority bit high
PSH	Serial Port interrupt priority bit high
PT1H	Timer 1 interrupt priority bit high
PX1H	External interrupt 1 priority bit high
PT0H	Timer 0 interrupt priority bit high
PX0H	External interrupt 0 priority bit high

Interrupt Priority 1 (IP1)

Location	7	6	5	4	3	2	1	0	Reset Value
F8H	1	-	-	1	PBO	PX3	PX2	1	1xx10001b

Symbol	Function
PBO	Brown-out interrupt priority bit
PX2	External Interrupt 2 priority bit
PX3	External Interrupt 3 priority bit

Interrupt Priority 1 High (IP1H)

Location	7	6	5	4	3	2	1	0	Reset Value
F7H	1	-	-	1	PBOH	PX3H	PX2H	1	1xx10001b

Symbol	Function
PBOH	Brown-out Interrupt priority bit high
PX2H	External Interrupt 2 priority bit high
PX3H	External Interrupt 3 priority bit high

Timer/Counter 2 Control Register (T2CON)

Location	7	6	5	4	3	2	1	0	Reset Value
C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#	00H

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflow to be used for the transmit clock.
EXEN2	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/stop control for Timer 2. A logic 1 starts the timer.
C/T2#	Timer or counter select (Timer 2) 0: Internal timer (OSC/6 in 6 clock mode, OSC/12 in 12 clock mode) 1: External event counter (falling edge triggered)
CP/RL2#	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Timer/Counter 2 Mode Control (T2MOD)

Location	7	6	5	4	3	2	1	0	Reset Value
C9H	-	-	-	-	-	-	T2OE	DCEN	xxxxxx00b

Symbol	Function
-	Not implemented, reserved for future use. **Note:** User should not write ‘1’s to reserved bits. The value read from a reserved bit is indeterminate.
T2OE	Timer 2 Output Enable bit.
DCEN	Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter.

External Interrupt Control (XICON)

Location	7	6	5	4	3	2	1	0	Reset Value
AEH	-	EX3	IE3	IT3	0	EX2	IE2	IT2	00H

Symbol	Function
EX2	External Interrupt 2 Enable bit if set
IE2	Interrupt Enable If IT2=1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced.
IT2	External Interrupt 2 is falling-edge/low-level triggered when this bit is cleared by software.
EX3	External Interrupt 3 Enable bit if set
IE3	Interrupt Enable If IT3=1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced.
IT3	External Interrupt3 is falling-edge/low-level triggered when this bit is cleared by software.

SPI Transfer Formats

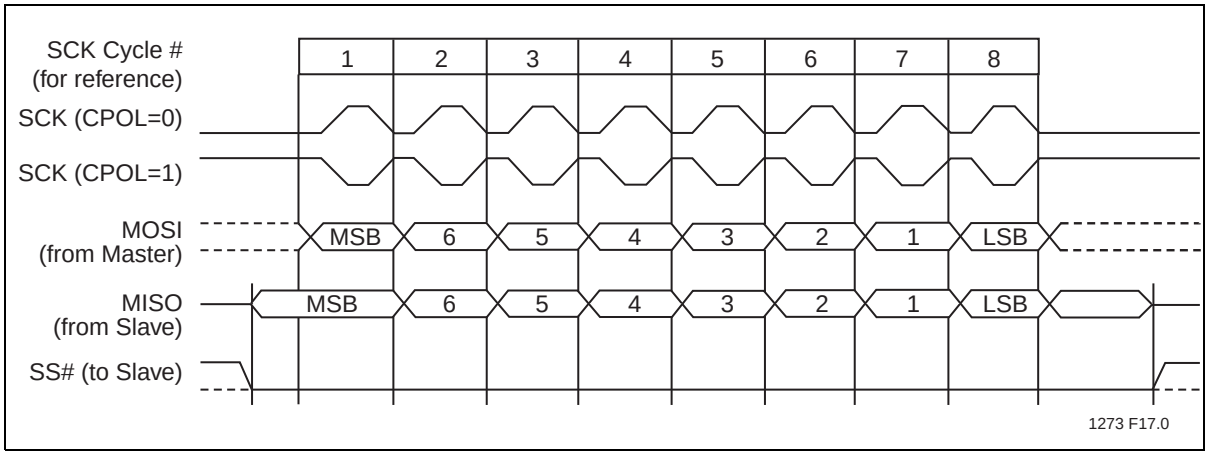

Figure 21: SPI Transfer Format with CPHA = 0

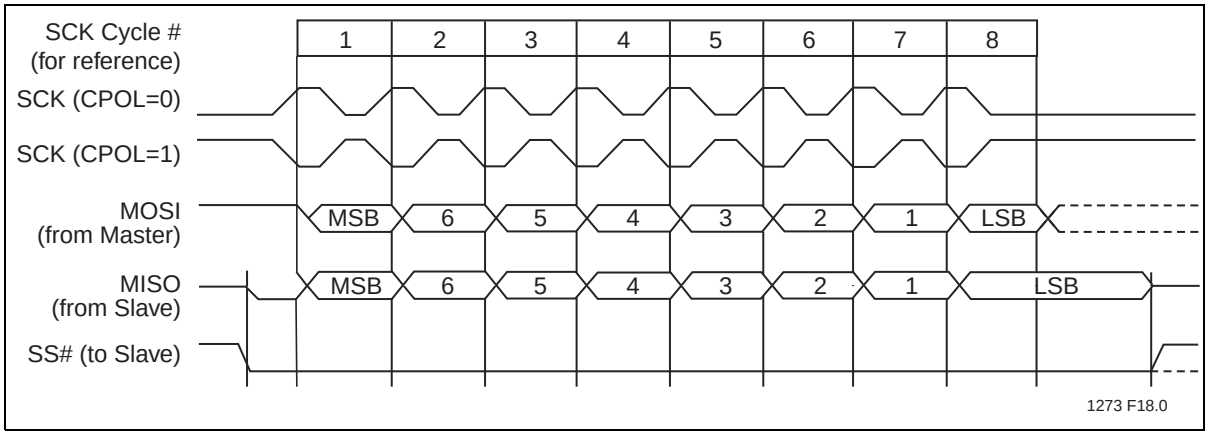

Figure 22: SPI Transfer Format with CPHA = 1

Software Reset

The software reset is executed by changing SFCF[1] (SWR) from “0” to “1”. A software reset will reset the program counter to address 0000H. All SFR registers will be set to their reset values, except SFCF[1] (SWR), WDTC[2] (WDTS), and RAM data will not be altered.

Brown-out Detection Reset

The device includes a brown-out detection circuit to protect the system from severed supplied voltage V_{DD} fluctuations. SST89E516RDx internal brown-out detection threshold is 3.85V, SST89V516RDx brown-out detection threshold is 2.35V. For brown-out voltage parameters, please refer to Table 36.

When V_{DD} drops below this voltage threshold, the brown-out detector triggers the circuit to generate a brown-out interrupt but the CPU still runs until the supplied voltage returns to the brown-out detection voltage V_{BOD}. The default operation for a brown-out detection is to cause a processor reset.

V_{DD} must stay below V_{BOD} at least four oscillator clock periods before the brown-out detection circuit will respond.

Brown-out interrupt can be enabled by setting the EBO bit in IEA register (address E8H, bit 3). If EBO bit is set and a brown-out condition occurs, a brown-out interrupt will be generated to execute the program at location 004BH. It is required that the EBO bit be cleared by software after the brown-out interrupt is serviced. Clearing EBO bit when the brown-out condition is active will properly reset the device. If brown-out interrupt is not enabled, a brown-out condition will reset the program to resume execution at location 0000H.

Interrupts

Interrupt Priority and Polling Sequence

The device supports eight interrupt sources under a four level priority scheme. Table 27 summarizes the polling sequence of the supported interrupts. Note that the SPI serial interface and the UART share the same interrupt vector. (See Figure 32)

Table 27: Interrupt Polling Sequence

Description	Interrupt Flag	Vector Address	Interrupt Enable	Interrupt Priority	Service Priority	Wake-Up Power-down
Ext. Int0	IE0	0003H	EX0	PX0/H	1(highest)	yes
Brown-out	-	004BH	EBO	PBO/H	2	no
T0	TF0	000BH	ET0	PT0/H	3	no
Ext. Int1	IE1	0013H	EX1	PX1/H	4	yes
T1	TF1	001BH	ET1	PT1/H	5	no
PCA	CF/CCFn	0033H	EC	PPCH	6	no
Ext. Int. 2	IE2	003BH	EX2	PX2/H	7	no
Ext. Int. 3	IE3	0043H	EX3	PX3/H	8	no
UART/SPI	TI/RI/SPIF	0023H	ES	PS/H	9	no
T2	TF2, EXF2	002BH	ET2	PT2/H	10	no

T0-0.0 25093

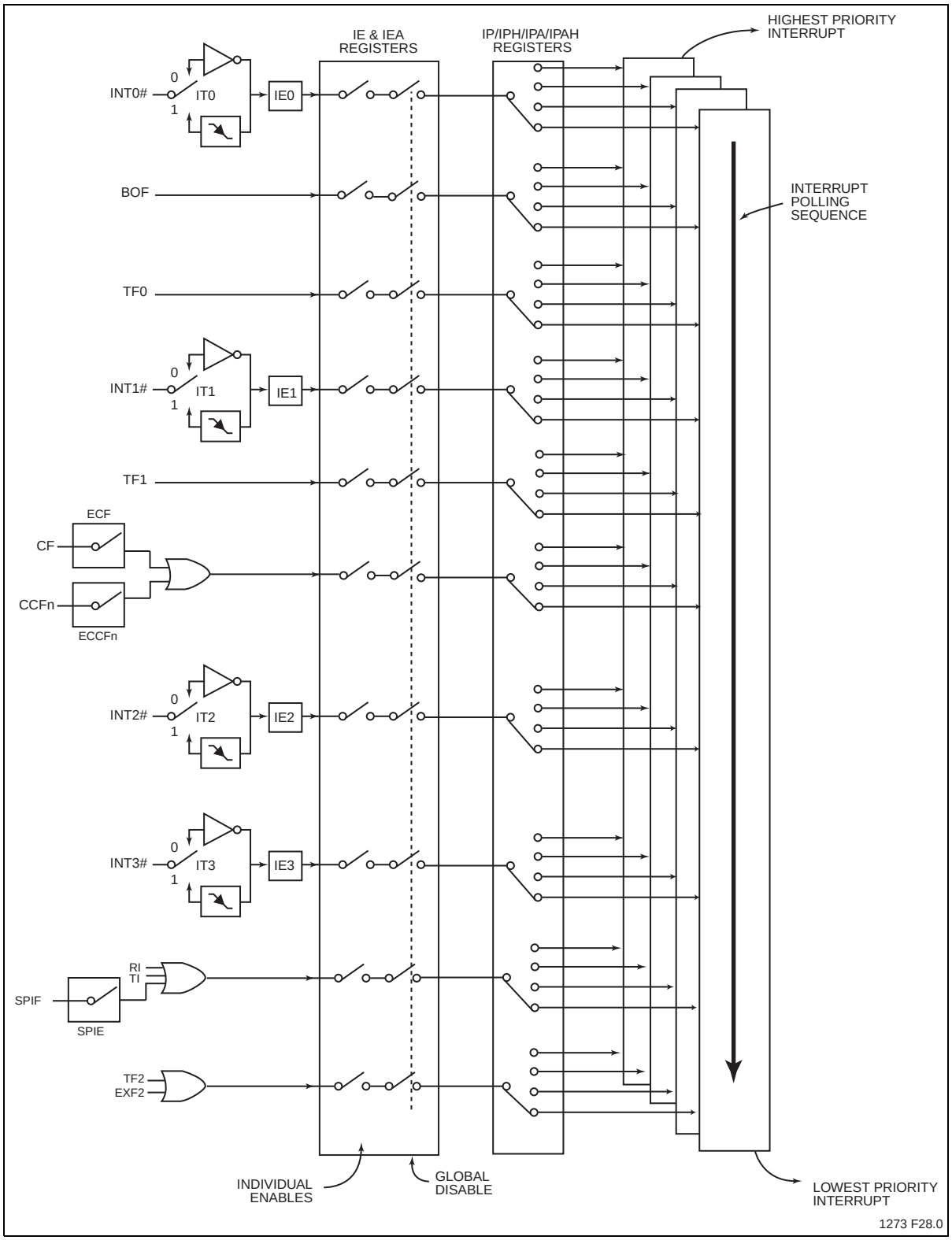

Figure 32: Interrupt Structure

Table 32: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

T0-0.0 25093

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 33: AC Conditions of Test[1]

Input Rise/Fall Time	Output Load
10 ns	C_L = 100 pF

T33.1 25093

1. See Figures 41 and 43

Table 34: Recommended System Power-up Timings

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	100	µs

T0-0.0 25093

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter

Table 35: Pin Impedance **(V_{DD}=3.3V, T_A=25°C, f=1 Mhz, other pins open)**

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	15 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	12 pF
L_{PIN}[2]	Pin Inductance		20 nH

T0-0.0 25093

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. Refer to PCI spec.

DC Electrical Characteristics

Table 36: DC Electrical Characteristics for SST89E516RDx
T_A = -40°C to +85°C; V_{DD} = 4.5-5.5V; V_{SS} = 0V

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Voltage	4.5 < V_{DD} < 5.5	-0.5	0.2V_{DD} - 0.1	V
V_{IH}	Input High Voltage	4.5 < V_{DD} < 5.5	0.2V_{DD} + 0.9	V_{DD} + 0.5	V
V_{IH1}	Input High Voltage (XTAL1, RST)	4.5 < V_{DD} < 5.5	0.7V_{DD}	V_{DD} + 0.5	V
V_{OL}	Output Low Voltage (Ports 1.5, 1.6, 1.7)	V_{DD} = 4.5V			
		I_{OL} = 16mA		1.0	V
V_{OL}	Output Low Voltage (Ports 1, 2, 3)[1]	V_{DD} = 4.5V			
		I_{OL} = 100µA[2]		0.3	V
		I_{OL} = 1.6mA[2]		0.45	V
		I_{OL} = 3.5mA[2]		1.0	V
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#)[1,3]	V_{DD} = 4.5V			
		I_{OL} = 200µA[2]		0.3	V
		I_{OL} = 3.2mA[2]		0.45	V
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, PSEN#)[4]	V_{DD} = 4.5V			
		I_{OH} = -10µA	V_{DD} - 0.3		V
		I_{OH} = -30µA	V_{DD} - 0.7		V
		I_{OH} = -60µA	V_{DD} - 1.5		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)[4]	V_{DD} = 4.5V			
		I_{OH} = -200µA	V_{DD} - 0.3		V
		I_{OH} = -3.2mA	V_{DD} - 0.7		V
V_{BOD}	Brown-out Detection Voltage		3.85	4.15	V
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V_{IN} = 0.4V		-75	µA
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3)[5]	V_{IN} = 2V		-650	µA
I_{LI}	Input Leakage Current (Port 0)	0.45 < V_{IN} < V_{DD}-0.3		±10	µA
R_{RST}	RST Pull-down Resistor		40	225	KΩ
C_{IO}	Pin Capacitance[6]	@ 1 MHz, 25°C		15	pF
I_{DD}	Power Supply Current IAP Mode @ 40 MHz			88	mA
	Active Mode @ 40 MHz			50	mA
	Idle Mode @ 40 MHz			42	mA
	Power-down Mode (min. V_{DD} = 2V)	T_A = 0°C to +70°C		80	µA
		T_A = -40°C to +85°C		90	µA

T0-0.1 25093

Explanation of Symbols

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW or ALE
P: PSEN#
Q: Output data
R: RD# signal
T: Time
V: Valid
W: WR# signal
X: No longer a valid logic level
Z: High Impedance (Float)

For example:

T_{AVLL} = Time from Address Valid to ALE Low

T_{LLPL} = Time from ALE Low to PSEN# Low

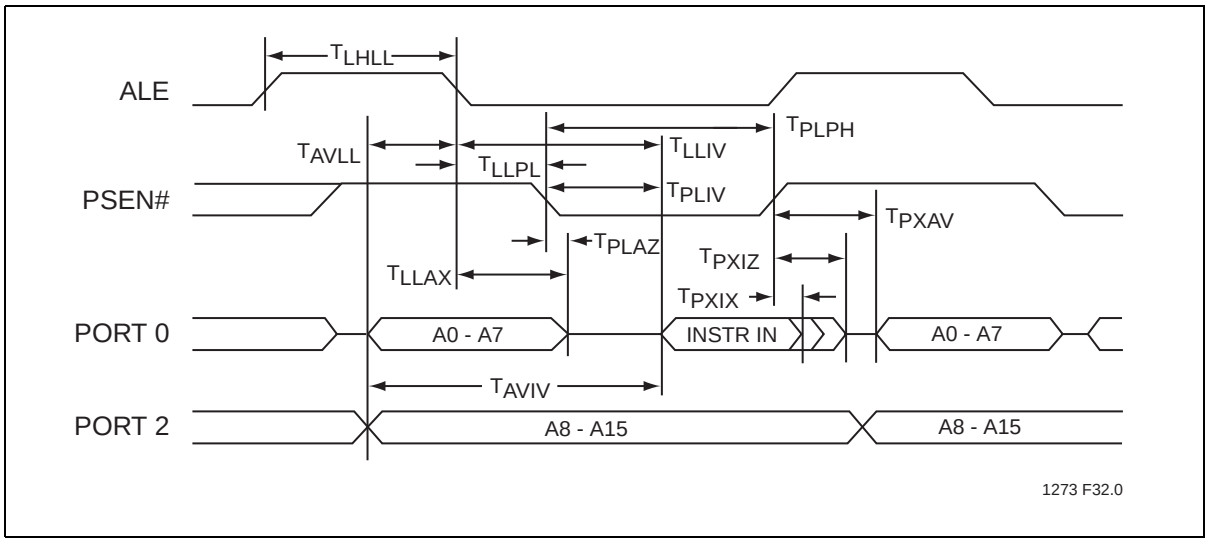

Figure 36: External Program Memory Read Cycle

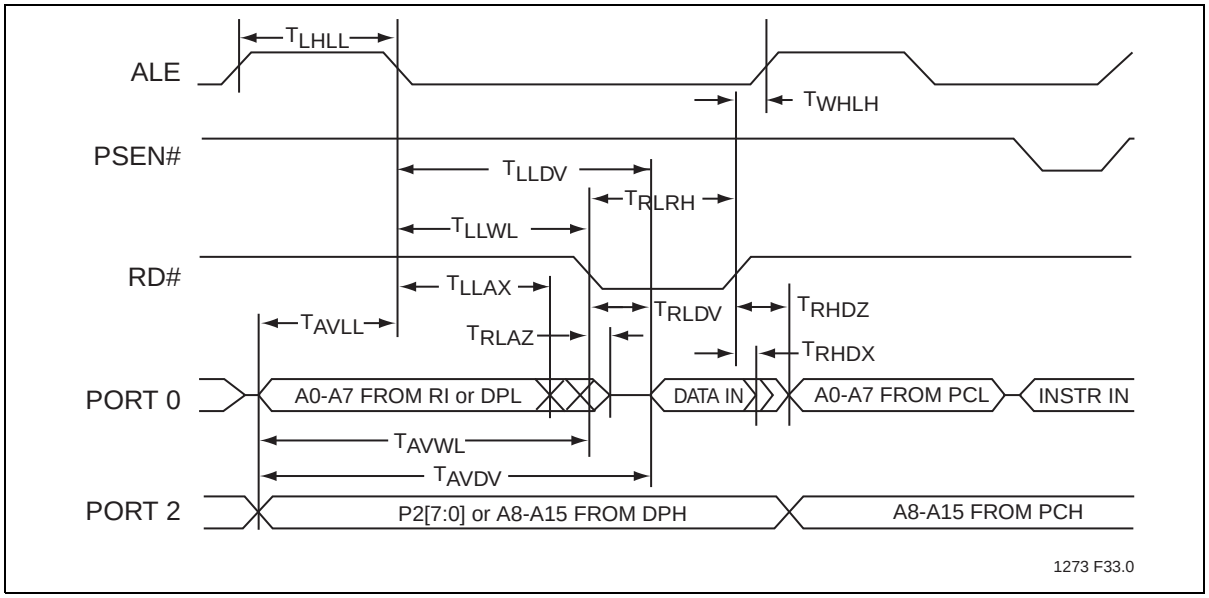

Figure 37: External Data Memory Read Cycle

Valid Combinations

Valid combinations for SST89E516RD2

SST89E516RD2-40-C-NJE	SST89E516RD2-40-C-TQJE
SST89E516RD2-40-I-NJE	SST89E516RD2-40-I-TQJE

Valid combinations for SST89V516RD2

SST89V516RD2-33-C-NJE	SST89V516RD2-33-C-TQJE
SST89V516RD2-33-I-NJE	SST89V516RD2-33-I-TQJE

Valid combinations for SST89E516RD

SST89E516RD-40-C-PIE	SST89E516RD-40-C-QIF
	SST89E516RD-40-I-QIF

Valid combinations for SST89V516RD

SST89V516RD-33-C-PIE	SST89V516RD-33-C-QIF
	SST89V516RD-33-I-QIF

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Packaging Diagrams

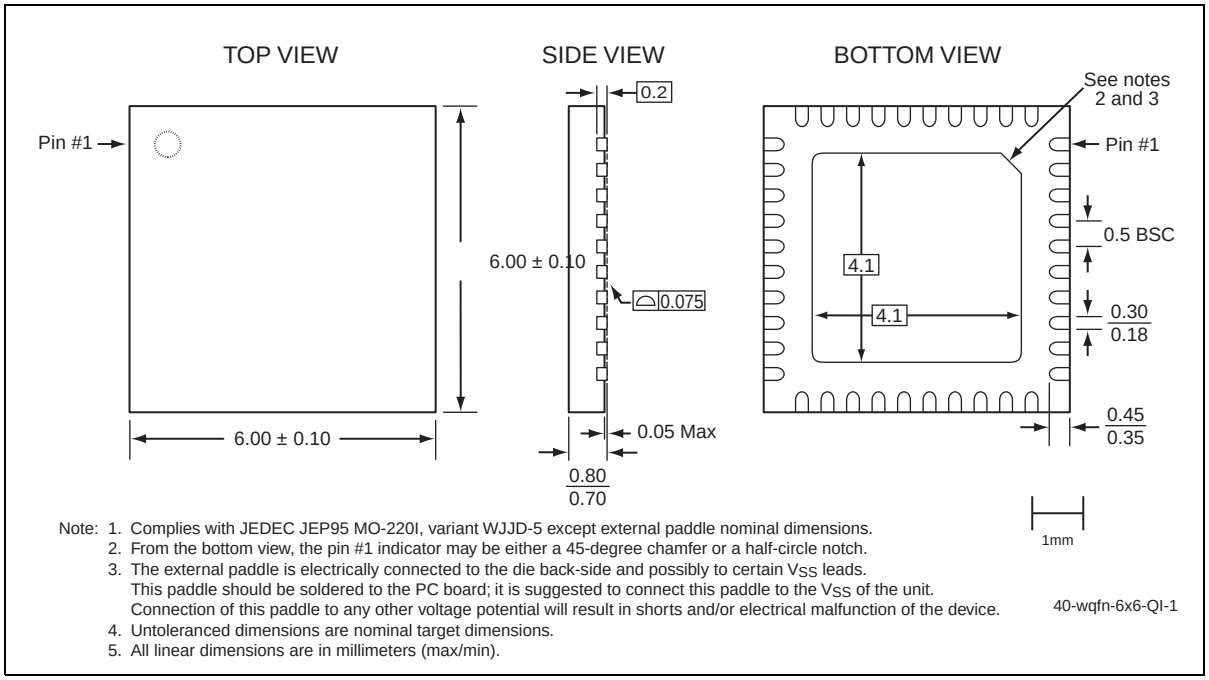

Figure 47: 40-contact Very-very-thin Quad Flat No-lead (WQFN)
SST Package Code: QI