Microchip Technology - SST89E516RD2-40-I-TQJE-T-NXX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	36
Program Memory Size	72KB (72K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sst89e516rd2-40-i-tqje-t-nxx

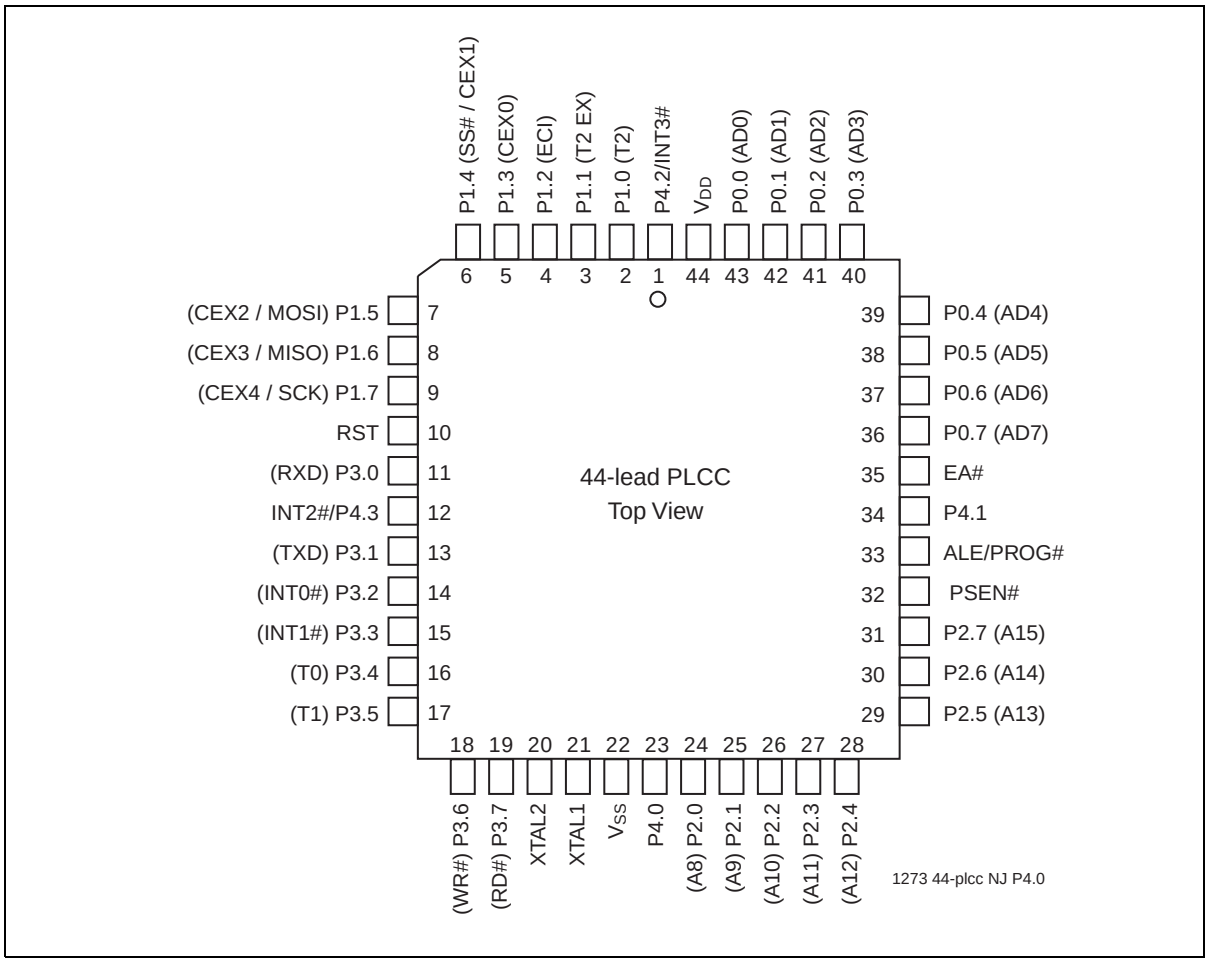

Figure 5: Pin Assignments for 44-lead PLCC

Program Memory Block Switching

The program memory block switching feature of the device allows either Block 1 or the lowest 8 KByte of Block 0 to be used for the lowest 8 KByte of the program address space. SFCF[1:0] controls program memory block switching.

Table 2: SFCF Values for Program Memory Block Switching

SFCF[1:0]	Program Memory Block Switching
01, 10, 11	Block 1 is not visible to the program counter (PC). Block 1 is reachable only via in-application programming from 0000H - 1FFFH.
00	Block 1 is overlaid onto the low 8K of the program address space; occupying address locations 0000H - 1FFFH. When the PC falls within 0000H - 1FFFH, the instruction will be fetched from Block 1 instead of Block 0. Outside of 0000H - 1FFFH, Block 0 is used. Locations 0000H - 1FFFH of Block 0 are reachable through in-application programming.

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Reset Configuration of Program Memory Block Switching

Program memory block switching is initialized after reset according to the state of the Start-up Configuration bit SC0. The SC0 bit is programmed via an external host mode command or an IAP Mode command. See Table 14.

Once out of reset, the SFCF[0] bit can be changed dynamically by the program for desired effects. Changing SFCF[0] will not change the SC0 bit.

Caution must be taken when dynamically changing the SFCF[0] bit. Since this will cause different physical memory to be mapped to the logical program address space. The user must avoid executing block switching instructions within the address range 0000H to 1FFFH.

Table 3: SFCF Values Under Different Reset Conditions

	State of SFCF[1:0] after:		
SC0[1]	Power-on or External Reset	WDT Reset or Brown-out Reset	Software Reset
U (1)	00 (default)	x0	10
P (0)	01	x1	11

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1. P = Programmed (Bit logic state = 0),
   U = Unprogrammed (Bit logic state = 1)

Data RAM Memory

The data RAM has 1024 bytes of internal memory. The RAM can be addressed up to 64KB for external data memory.

high-order eight address bits (DPH), and Port 0 multiplexes the low order eight address bits (DPL) with data. Both MOVX @Ri and MOVX @DPTR generates the necessary read and write signals (P3.6 - WR# and P3.7 - RD#) for external memory use. Table 4 shows external data memory RD#, WR# operation with EXTRAM bit.

The stack pointer (SP) can be located anywhere within the 256 bytes of internal RAM (lower 128 bytes and upper 128 bytes). The stack pointer may not be located in any part of the expanded RAM.

Table 4: External Data Memory RD#, WR# with EXTRAM bit

	MOVX @DPTR, A or MOVX A, @DPTR		MOVX @Ri, A or MOVX A, @Ri
AUXR	**ADDR < 0300H**	**ADDR >= 0300H**	**ADDR = Any**
EXTRAM = 0	RD# / WR# not asserted	RD# / WR# asserted	RD# / WR# not asserted[1]
EXTRAM = 1	RD# / WR# asserted	RD# / WR# asserted	RD# / WR# asserted

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1. Access limited to ERAM address within 0 to 0FFH; cannot access 100H to 02FFH.

Table 7: Flash Memory Programming SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
SFCF	SuperFlash Configuration	B1H	-	IAPEN	-	-	-	-	SWR	BSEL	x0xxxx00b
SFCM	SuperFlash Command	B2H	FIE	FCM[6:0]							00H
SFAL	SuperFlash Address Low	B3H	SuperFlash Low Order Byte Address Register - A_7 to A_0 (SFAL)								00H
SFAH	SuperFlash Address High	B4H	SuperFlash High Order Byte Address Register - A_{15} to A_8 (SFAH)								00H
SFDT	SuperFlash Data	B5H	SuperFlash Data Register								00H
SFST	SuperFlash Status	B6H	SB1_i	SB2_i	SB3_i	-	EDC_i	FLASH_BUSY	-	-	000x00xxb

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Table 8: Watchdog Timer SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
WDTC [1]	Watchdog Timer Control	C0H	-	-	-	WDOUT	WDRE	WDTS	WDT	SWDT	xxx00x00b
WDTD	Watchdog Timer Data/Reload	85H	Watchdog Timer Data/Reload								00H

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1. Bit Addressable SFRs

Table 10: Interface SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	RESET Value
SBUF	Serial Data Buffer	99H	SBUF[7:0]								Indeterminate
SCON[1]	Serial Port Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SADDR	Slave Address	A9H	SADDR[7:0]								00H
SADEN	Slave Address Mask	B9H	SADEN[7:0]								00H
SPCR	SPI Control Register	D5H	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04H
SPSR	SPI Status Register	AAH	SPIF	WCOL							00H
SPDR	SPI Data Register	86H	SPDR[7:0]								00H
P0[1]	Port 0	80H	P0[7:0]								FFH
P1[1]	Port 1	90H	-	-	-	-	-	-	T2EX	T2	FFH
P2[1]	Port 2	A0H	P2[7:0]								FFH
P3[1]	Port 3	B0H	RD#	WR#	T1	T0	INT1#	INT0#	TXD	RXD	FFH
P4[2]	Port 4	A5H	1	1	1	1	P4.3	P4.2	P4.1	P4.0	FFH

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1. Bit Addressable SFRs
2. P4 is similar to P1 and P3 ports

SPI Control Register (SPCR)

Location	7	6	5	4	3	2	1	0	Reset Value
D5H	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	00H

Symbol **Function**

SPIE If both SPIE and ES are set to one, SPI interrupts are enabled.

SPE SPI enable bit.
0: Disables SPI.
1: Enables SPI and connects SS#, MOSI, MISO, and SCK to pins P1.4, P1.5, P1.6, P1.7.

DORD Data Transmission Order.
0: MSB first in data transmission.
1: LSB first in data transmission.

MSTR Master/Slave select.
0: Selects Slave mode.
1: Selects Master mode.

CPOL Clock Polarity
0: SCK is low when idle (Active High).
1: SCK is high when idle (Active Low).

CPHA Clock Phase control bit. The CPHA bit with the CPOL bit control the clock and data relationship between master and slave. See Figures 21 and 22.
0: Shift triggered on the leading edge of the clock.
1: Shift triggered on the trailing edge of the clock.

SPR1, SPR0SPI Clock Rate Select bits. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, f_{OSC}, is as follows:

SPR1	SPR0	SCK = f_{OSC} divided by
0	0	4
0	1	16
1	0	64
1	1	128

SPI Status Register (SPSR)

Location	7	6	5	4	3	2	1	0	Reset Value
AAH	SPIF	WCOL	-	-	-	-	-	-	00xxxxxxb

Symbol **Function**

SPIF SPI Interrupt Flag.
Upon completion of data transfer, this bit is set to 1.
If SPIE =1 and ES =1, an interrupt is then generated.
This bit is cleared by software.

WCOL Write Collision Flag.
Set if the SPI data register is written to during data transfer.
This bit is cleared by software.

External Interrupt Control (XICON)

Location	7	6	5	4	3	2	1	0	Reset Value
AEH	-	EX3	IE3	IT3	0	EX2	IE2	IT2	00H

Symbol	Function
EX2	External Interrupt 2 Enable bit if set
IE2	Interrupt Enable If IT2=1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced.
IT2	External Interrupt 2 is falling-edge/low-level triggered when this bit is cleared by software.
EX3	External Interrupt 3 Enable bit if set
IE3	Interrupt Enable If IT3=1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced.
IT3	External Interrupt3 is falling-edge/low-level triggered when this bit is cleared by software.

Flash Memory Programming

The device internal flash memory can be programmed or erased using In-Application Programming (IAP) mode

Product Identification

The Read-ID command accesses the Signature Bytes that identify the device and the manufacturer as SST. External programmers primarily use these Signature Bytes in the selection of programming algorithms.

Table 12: Product Identification

	Address	Data
Manufacturer's ID	30H	BFH
Device ID		
SST89E516RD2/RD	31H	93H
SST89V516RD2/RD	31H	92H

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In-Application Programming Mode

The device offers either 72 KByte of in-application programmable flash memory. During in-application programming, the CPU of the microcontroller enters IAP mode. The two blocks of flash memory allow the CPU to execute user code from one block, while the other is being erased or reprogrammed concurrently. The CPU may also fetch code from an external memory while all internal flash is being reprogrammed. The mailbox registers (SFST, SFCM, SFAL, SFAH, SFDT and SFCF) located in the special function register (SFR), control and monitor the device's erase and program process.

Table 14 outline the commands and their associated mailbox register settings.

In-Application Programming Mode Clock Source

During IAP mode, both the CPU core and the flash controller unit are driven off the external clock. However, an internal oscillator will provide timing references for Program and Erase operations. The internal oscillator is only turned on when required, and is turned off as soon as the flash operation is completed.

Memory Bank Selection for In-Application Programming Mode

With the addressing range limited to 16 bit, only 64 KByte of program address space is "visible" at any one time. As shown in Table 13, the bank selection (the configuration of EA# and SFCF[1:0]), allows Block 1 memory to be overlaid on the lowest 8 KByte of Block 0 memory, making Block 1 reachable. The same concept is employed to allow both Block 0 and Block 1 flash to be accessible to IAP operations. Code from a block that is not visible may not be used as a source to program another address. However, a block that is not "visible" may be programmed by code from the other block through mailbox registers.

The device allows IAP code in one block of memory to program the other block of memory, but may not program any location in the same block. If an IAP operation originates physically from Block 0, the target of this operation is implicitly defined to be in Block 1. If the IAP operation originates physically from

Block 1, then the target address is implicitly defined to be in Block 0. If the IAP operation originates from external program space, then, the target will depend on the address and the state of bank selection.

IAP Enable Bit

The IAP enable bit, SFCF[6], enables in-application programming mode. Until this bit is set, all flash programming IAP commands will be ignored.

Table 13: IAP Address Resolution

EA#	SFCF[1:0]	Address of IAP Inst.	Target Address	Block Being Programmed
1	00	>= 2000H (Block 0)	>= 2000H (Block 0)	None[1]
1	00	>= 2000H (Block 0)	< 2000H (Block 1)	Block 1
1	00	< 2000H (Block 1)	Any (Block 0)	Block 0
1	01, 10, 11	Any (Block 0)	>= 2000H (Block 0)	None[1]
1	01, 10, 11	Any (Block 0)	< 2000H (Block 1)	Block 1
0	00	From external	>= 2000H (Block 0)	Block 0
0	00	From external	< 2000H (Block 1)	Block 1
0	01, 10, 11	From external	Any (Block 0)	Block 0

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1. No operation is performed because code from one block may not program the same originating block

In-Application Programming Mode Commands

All of the following commands can only be initiated in the IAP mode. In all situations, writing the control byte to the SFCM register will initiate all of the operations. All commands will not be enabled if the security locks are enabled on the selected memory block.

The Program command is for programming new data into the memory array. The portion of the memory array to be programmed should be in the erased state, FFH. If the memory is not erased, it should first be erased with an appropriate Erase command. **Warning: Do not attempt to write (program or erase) to a block that the code is currently fetching from. This will cause unpredictable program behavior and may corrupt program data.**

Timers/Counters

Timers

The device has three 16-bit registers that can be used as either timers or event counters. The three timers/counters are denoted Timer 0 (T0), Timer 1 (T1), and Timer 2 (T2). Each is designated a pair of 8-bit registers in the SFRs. The pair consists of a most significant (high) byte and least significant (low) byte. The respective registers are TL0, TH0, TL1, TH1, TL2, and TH2.

Timer Set-up

Refer to Table 9 for TMOD, TCON, and T2CON registers regarding timers T0, T1, and T2. The following tables provide TMOD values to be used to set up Timers T0, T1, and T2.

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set separately to turn the timer on.

Table 15: Timer/Counter 0

	Mode	Function	TMOD	
			Internal Control[1]	External Control[2]
Used as Timer	0	13-bit Timer	00H	08H
	1	16-bit Timer	01H	09H
	2	8-bit Auto-Reload	02H	0AH
	3	Two 8-bit Timers	03H	0BH
Used as Counter	0	13-bit Timer	04H	0CH
	1	16-bit Timer	05H	0DH
	2	8-bit Auto-Reload	06H	0EH
	3	Two 8-bit Timers	07H	0FH

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1. The Timer is turned ON/OFF by setting/clearing bit TR0 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on INT0# (P3.2) when TR0 = 1 (hardware control).

Table 16: Timer/Counter 1

	Mode	Function	TMOD	
			Internal Control[1]	External Control[2]
Used as Timer	0	13-bit Timer	00H	80H
	1	16-bit Timer	10H	90H
	2	8-bit Auto-Reload	20H	A0H
	3	Does not run	30H	B0H
Used as Counter	0	13-bit Timer	40H	C0H
	1	16-bit Timer	50H	D0H
	2	8-bit Auto-Reload	60H	E0H
	3	Not available	-	-

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1. The Timer is turned ON/OFF by setting/clearing bit TR1 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on INT1# (P3.3) when TR1 = 1 (hardware control).

Programmable Counter Array

The Programmable Counter Array (PCA) present on the SST89E/V516RDx is a special 16-bit timer that has five 16-bit capture/compare modules. Each of the modules can be programmed to operate in one of four modes: rising and/or falling edge capture, software timer, high-speed output, or pulse width modulator. The 5th module can be programmed as a Watchdog Timer in addition to the other four modes. Each module has a pin associated with it in port 1. Module 0 is connected to P1.3 (CEX0), module 1 to P1[4] (CEX1), module 2 to P1[5] (CEX2), module 3 to P1[6] (CEX3), and module 4 to P1[7] (CEX4). PCA configuration is shown in Figure 24.

PCA Overview

PCA provides more timing capabilities with less CPU intervention than the standard timer/counter. Its advantages include reduced software overhead and improved accuracy.

The PCA consists of a dedicated timer/counter which serves as the time base for an array of five compare/capture modules. Figure 24 shows a block diagram of the PCA. External events associated with modules are shared with corresponding Port 1 pins. Modules not using the port pins can still be used for standard I/O.

Each of the five modules can be programmed in any of the following modes:

- Rising and/or falling edge capture
- Software timer
- High speed output
- Watchdog Timer (Module 4 only)
- Pulse Width Modulator (PWM)

PCA Timer/Counter

The PCA timer is a free-running 16-bit timer consisting of registers CH and CL (the high and low bytes of the count values). The PCA timer is common time base for all five modules and can be programmed to run at: 1/6 the oscillator frequency, 1/2 the oscillator frequency, Timer 0 overflow, or the input on the ECI pin (P1.2). The timer/counter source is determined from the CPS1 and CPS0 bits in the CMOD SFR as follows (see “PCA Timer/Counter Mode Register (CMOD)” on page 28):

Table 18: PCA Timer/Counter Source

CPS1	CPS0	12 Clock Mode	6 Clock Mode
0	0	f_{OSC} /12	f_{OSC} /6
0	1	f_{OSC} /4	f_{OSC} /2
1	0	Timer 0 overflow	Timer 0 overflow
1	1	External clock at ECI pin (maximum rate = f_{OSC} /8)	External clock at ECI pin (maximum rate = f_{OSC} /4)

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Table 22: PCA Module Modes

Without Interrupt enabled								
-[1]	ECOMy[2]	CAPPy[2]	CAPNy[2]	MATy[2]	TOGy[2]	PWMy[2]	ECCFy[2]	Module Code
-	0	0	0	0	0	0	0	No Operation
-	0	1	0	0	0	0	0	16-bit capture on positive-edge trigger at CEX[4:0]
-	0	0	1	0	0	0	0	16-bit capture on negative-edge trigger at CEX[4:0]
-	0	1	1	0	0	0	0	16-bit capture on positive/negative-edge trigger at CEX[4:0]
-	1	0	0	1	0	0	0	Compare: software timer
-	1	0	0	1	1	0	0	Compare: high-speed output
-	1	0	0	0	0	1	0	Compare: 8-bit PWM
-	1	0	0	1	0 or 1[3]	0	0	Compare: PCA WDT (CCAPM4 only)[4]

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1. User should not write ‘1’s to reserved bits. The value read from a reserved bit is indeterminate.
2. y = 0, 1, 2, 3, 4
3. A 0 disables toggle function. A 1 enables toggle function on CEX[4:0] pin.
4. For PCA WDT mode, also set the WDTE bit in the CMOD register to enable the reset output signal.

Table 23: PCA Module Modes

With Interrupt enabled								
-[1]	ECOMy[2]	CAPPy[2]	CAPNy[2]	MATy[2]	TOGy[2]	PWMy[2]	ECCFy[2]	Module Code
-	0	1	0	0	0	0	1	16-bit capture on positive-edge trigger at CEX[4:0]
-	0	0	1	0	0	0	1	16-bit capture on negative-edge trigger at CEX[4:0]
-	0	1	1	0	0	0	1	16-bit capture on positive/negative-edge trigger at CEX[4:0]
-	1	0	0	1	0	0	1	Compare: software timer
-	1	0	0	1	1	0	1	Compare: high-speed output
-	1	0	0	0	0	1	X[3]	Compare: 8-bit PWM
-	1	0	0	1	0 or 1[4]	0	X[5]	Compare: PCA WDT (CCAPM4 only)[6]

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1. User should not write ‘1’s to reserved bits. The value read from a reserved bit is indeterminate.
2. y = 0, 1, 2, 3, 4
3. No PCA interrupt is needed to generate the PWM.
4. A 0 disables toggle function. A 1 enables toggle function on CEX[4:0] pin.
5. Enabling an interrupt for the Watchdog Timer would defeat the purpose of the Watchdog Timer.
6. For PCA WDT mode, also set the WDTE bit in the CMOD register to enable the reset output signal.

16-Bit Software Timer Mode

The 16-bit software timer mode is used to trigger interrupt routines, which must occur at periodic intervals. It is setup by setting both the ECOM and MAT bits in the module's CCAPMn register. The PCA timer will be compared to the module's capture registers (CCAPnL and CCAPnH) and when a match occurs, an interrupt will occur, if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set.

If necessary, a new 16-bit compare value can be loaded into CCAPnH and CCAPnL during the interrupt routine. The user should be aware that the hardware temporarily disables the comparator function while these registers are being updated so that an invalid match will not occur. Thus, it is recommended that the user write to the low byte first (CCAPnL) to disable the comparator, then write to the high byte (CCAPnH) to re-enable it. If any updates to the registers are done, the user may want to hold off any interrupts from occurring by clearing the EA bit. (See Figure 26)

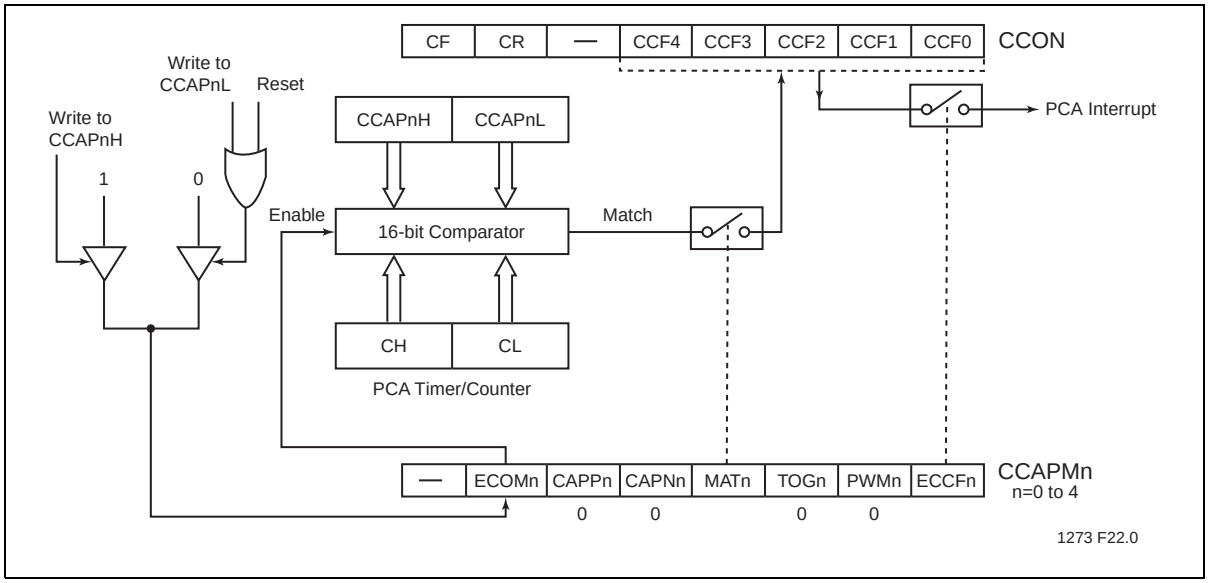

Figure 26: PCA Compare Mode (Software Timer)

High Speed Output Mode

The high speed output mode is used to toggle a port pin when a match occurs between the PCA timer and the preloaded value in the compare registers. In this mode, the CEX output pin (on port 1) associated with the PCA module will toggle every time there is a match between the PCA counter (CH and CL) and the capture registers (CCAPnH and CCAPnL). To activate this mode, the user must set TOG, MAT, and ECOM bits in the module's CCAPMn SFR.

High speed output mode is much more accurate than toggling pins since the toggle occurs before branching to an interrupt. In this case, interrupt latency will not affect the accuracy of the output. When using high speed output, using an interrupt is optional. Only if the user wishes to change the time for the next toggle is it necessary to update the compare registers. Otherwise, the next toggle will occur when the PCA timer rolls over and matches the last compare value. (See Figure 27)

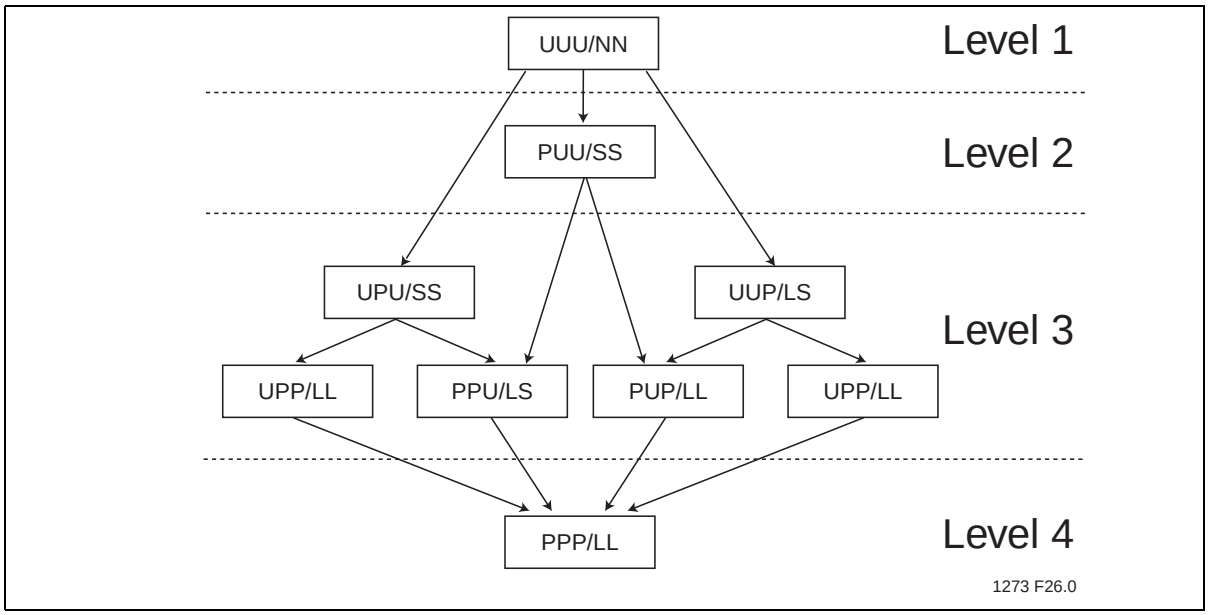

Figure 30: Security Lock Levels

Note: P = Programmed (Bit logic state = 0), U = Unprogrammed (Bit logic state = 1), N = Not Locked, L = Hard locked, S = Soft locked

Table 25: Security Lock Options

Level	Security Lock Bits[1,2]				Security Status of:		Security Type
	SFST[7:5]	SB1	SB2[1]	SB3[1]	Block 1	Block 0	
1	000	U	U	U	Unlock	Unlock	No Security Features are Enabled.
2	100	P	U	U	SoftLock	SoftLock	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA# is sampled and latched on Reset, and further programming of the flash is disabled.
3	011 101	U P	P U	P P	Hard Lock	Hard Lock	Level 2 plus Verify disabled, both blocks locked.
	010	U	P	U	SoftLock	SoftLock	Level 2 plus Verify disabled. Code in Block 1 may program Block 0 and vice versa.
	110 001	P U	P U	U P	Hard Lock	SoftLock	Level 2 plus Verify disabled. Code in Block 1 may program Block 0.
4	111	P	P	P	Hard Lock	Hard Lock	Same as Level 3 hard lock/hard lock, but MCU will start code execution from the internal memory regardless of EA#.

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1. P = Programmed (Bit logic state = 0), U = Unprogrammed (Bit logic state = 1).
2. SFST[7:5] = Security Lock Status Bits (SB1_i, SB2_i, SB3_i)

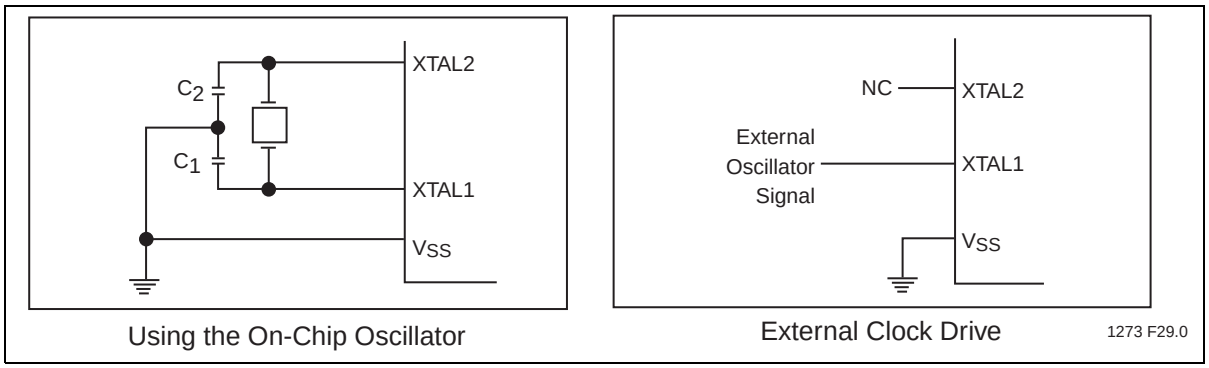

Figure 33: Oscillator Characteristics

Table 30: Clock Doubling Features

Device	Standard Mode (x1)		Clock Double Mode (x2)	
	Clocks per Machine Cycle	Max. External Clock Frequency (MHz)	Clocks per Machine Cycle	Max. External Clock Frequency (MHz)
SST89E516RDx	12	40	6	20
SST89V516RDx	12	33	6	16

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DC Electrical Characteristics

Table 36: DC Electrical Characteristics for SST89E516RDx
T_A = -40°C to +85°C; V_{DD} = 4.5-5.5V; V_{SS} = 0V

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Voltage	4.5 < V_{DD} < 5.5	-0.5	0.2V_{DD} - 0.1	V
V_{IH}	Input High Voltage	4.5 < V_{DD} < 5.5	0.2V_{DD} + 0.9	V_{DD} + 0.5	V
V_{IH1}	Input High Voltage (XTAL1, RST)	4.5 < V_{DD} < 5.5	0.7V_{DD}	V_{DD} + 0.5	V
V_{OL}	Output Low Voltage (Ports 1.5, 1.6, 1.7)	V_{DD} = 4.5V			
		I_{OL} = 16mA		1.0	V
V_{OL}	Output Low Voltage (Ports 1, 2, 3)[1]	V_{DD} = 4.5V			
		I_{OL} = 100µA[2]		0.3	V
		I_{OL} = 1.6mA[2]		0.45	V
		I_{OL} = 3.5mA[2]		1.0	V
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#)[1,3]	V_{DD} = 4.5V			
		I_{OL} = 200µA[2]		0.3	V
		I_{OL} = 3.2mA[2]		0.45	V
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, PSEN#)[4]	V_{DD} = 4.5V			
		I_{OH} = -10µA	V_{DD} - 0.3		V
		I_{OH} = -30µA	V_{DD} - 0.7		V
		I_{OH} = -60µA	V_{DD} - 1.5		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)[4]	V_{DD} = 4.5V			
		I_{OH} = -200µA	V_{DD} - 0.3		V
		I_{OH} = -3.2mA	V_{DD} - 0.7		V
V_{BOD}	Brown-out Detection Voltage		3.85	4.15	V
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V_{IN} = 0.4V		-75	µA
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3)[5]	V_{IN} = 2V		-650	µA
I_{LI}	Input Leakage Current (Port 0)	0.45 < V_{IN} < V_{DD}-0.3		±10	µA
R_{RST}	RST Pull-down Resistor		40	225	KΩ
C_{IO}	Pin Capacitance[6]	@ 1 MHz, 25°C		15	pF
I_{DD}	Power Supply Current IAP Mode @ 40 MHz			88	mA
	Active Mode @ 40 MHz			50	mA
	Idle Mode @ 40 MHz			42	mA
	Power-down Mode (min. V_{DD} = 2V)	T_A = 0°C to +70°C		80	µA
		T_A = -40°C to +85°C		90	µA

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Table 37: DC Electrical Characteristics for SST89V516RDx
T_A = -40°C to +85°C; V_{DD} = 2.7-3.6V; V_{SS} = 0V

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Voltage	2.7 < V_{DD} < 3.6	-0.5	0.7	V
V_{IH}	Input High Voltage	2.7 < V_{DD} < 3.6	0.2V_{DD} + 0.9	V_{DD} + 0.5	V
V_{IH1}	Input High Voltage (XTAL1, RST)	2.7 < V_{DD} < 3.6	0.7V_{DD}	V_{DD} + 0.5	V
V_{OL}	Output Low Voltage (Ports 1.5, 1.6, 1.7)	V_{DD} = 2.7V			
		I_{OL} = 16mA		1.0	V
V_{OL}	Output Low Voltage (Ports 1, 2, 3)[1]	V_{DD} = 2.7V			
		I_{OL} = 100µA[2]		0.3	V
		I_{OL} = 1.6mA[2]		0.45	V
		I_{OL} = 3.5mA[2]		1.0	V
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#)[1,3]	V_{DD} = 2.7V			
		I_{OL} = 200µA[2]		0.3	V
		I_{OL} = 3.2mA[2]		0.45	V
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, PSEN#)[4]	V_{DD} = 2.7V			
		I_{OH} = -10µA	V_{DD} - 0.3		V
		I_{OH} = -30µA	V_{DD} - 0.7		V
		I_{OH} = -60µA	V_{DD} - 1.5		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)[4]	V_{DD} = 2.7V			
		I_{OH} = -200µA	V_{DD} - 0.3		V
		I_{OH} = -3.2mA	V_{DD} - 0.7		V
V_{BOD}	Brown-out Detection Voltage		2.35	2.55	V
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V_{IN} = 0.4V		-75	µA
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3)[5]	V_{IN} = 2V		-650	µA
I_{LI}	Input Leakage Current (Port 0)	0.45 < V_{IN} < V_{DD}-0.3		±10	µA
R_{RST}	RST Pull-down Resistor			225	KΩ
C_{IO}	Pin Capacitance[6]	@ 1 MHz, 25°C		15	pF
I_{DD}	Power Supply Current IAP Mode @ 33 MHz			47	mA
	Active Mode @ 33 MHz			30	mA
	Idle Mode @ 33 MHz			21	mA
	Power-down Mode (min. V_{DD} = 2V)	T_A = 0°C to +70°C		45	µA
		T_A = -40°C to +85°C		55	µA

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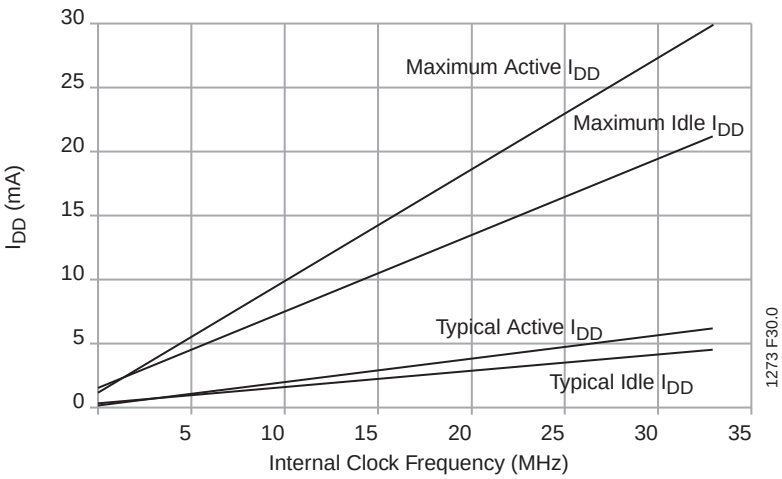

Figure 34: I_{DD} vs. Frequency for 3V SST89V516RDx

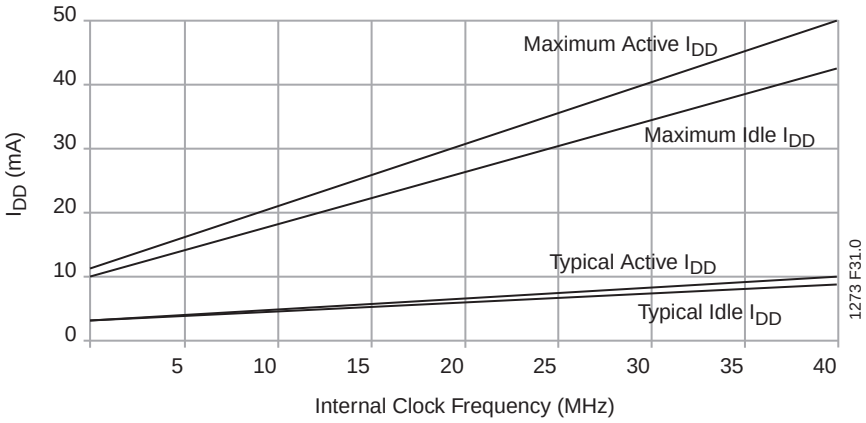

Figure 35: I_{DD} vs. Frequency for 5V SST89E516RDx

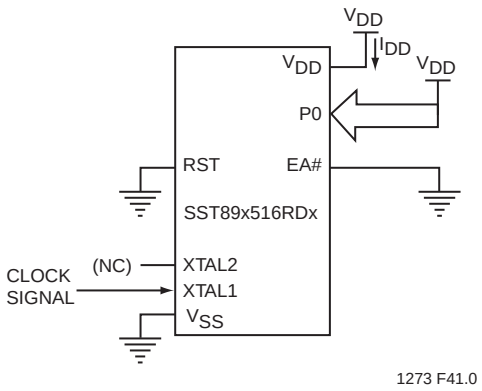

Figure 45: I_{DD} Test Condition, Idle Mode

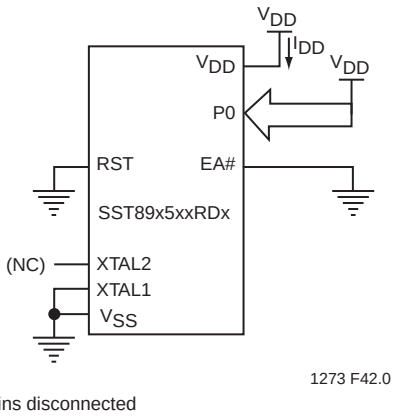

Figure 46: I_{DD} Test Condition, Power-down Mode

Table 41: Flash Memory Programming/Verification Parameters[1]

Parameter[2]	Max	Units
Chip-Erase Time	150	ms
Block-Erase Time	100	ms
Sector-Erase Time	30	ms
Byte-Program Time[3]	50	µs
Select-Block Program Time	500	ns
Re-map or Security bit Program Time	80	µs

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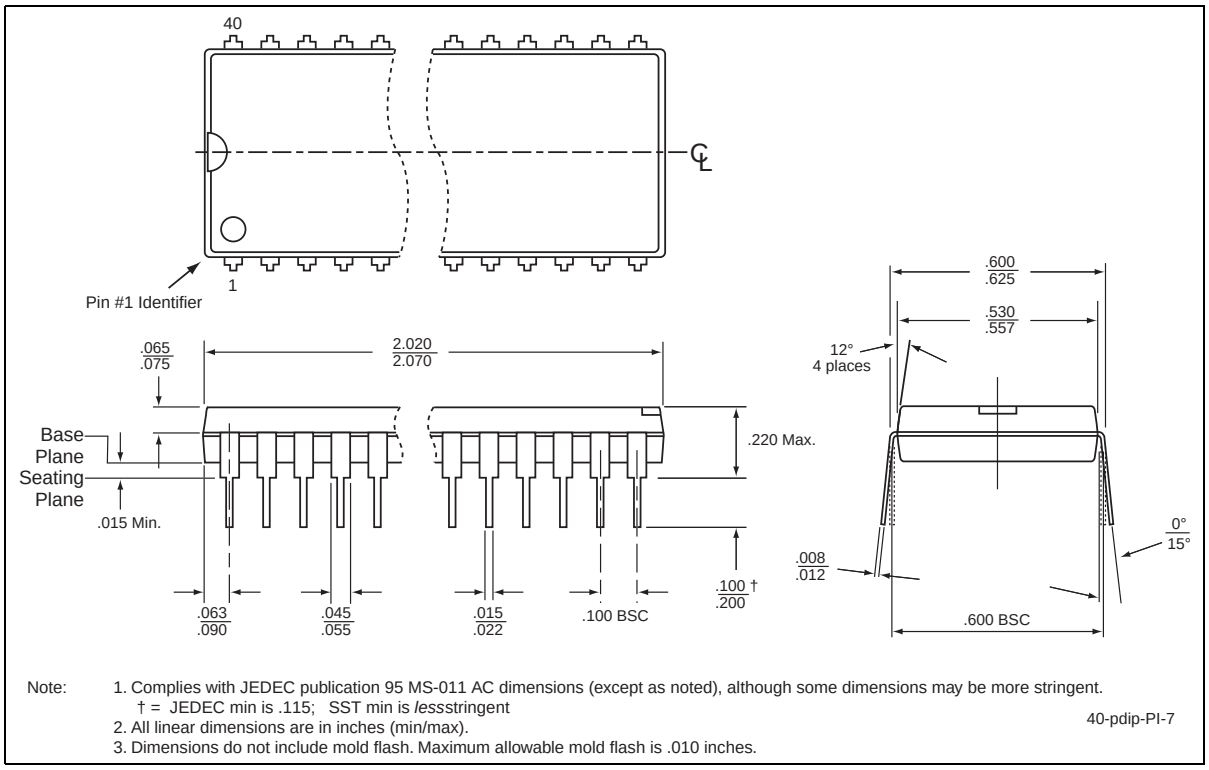
1. For IAP operations, the program execution overhead must be added to the above timing parameters.
2. Program and Erase times will scale inversely proportional to programming clock frequency.
3. Each byte must be erased before programming.



Note: 1. Complies with JEDEC publication 95 MS-011 AC dimensions (except as noted), although some dimensions may be more stringent.
† = JEDEC min is .115; SST min is *less*stringent
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .010 inches.

Figure 48: 40-pin Plastic Dual In-line Pins (PDIP)
SST Package Code: PI