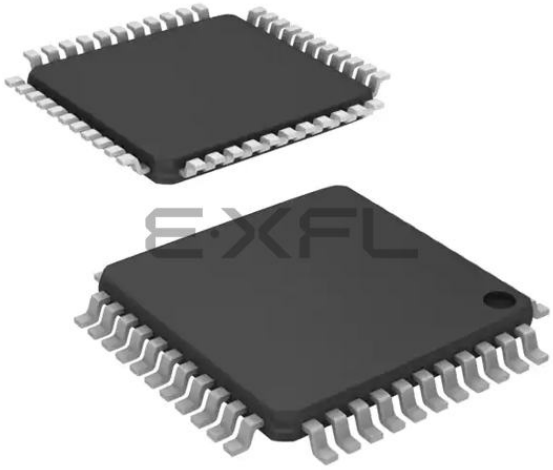

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	36
Program Memory Size	72KB (72K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sst89e516rd2-40-i-tqje

Product Description

The SST89E516RDx and SST89V516RDx are members of the FlashFlex family of 8-bit microcontroller products designed and manufactured with SST's patented and proprietary SuperFlash CMOS semiconductor process technology. The split-gate cell design and thick-oxide tunneling injector offer significant cost and reliability benefits for SST's customers. The devices use the 8051 instruction set and are pin-for-pin compatible with standard 8051 microcontroller devices.

The devices come with 72 KByte of on-chip flash EEPROM program memory which is partitioned into 2 independent program memory blocks. The primary Block 0 occupies 64 KByte of internal program memory space and the secondary Block 1 occupies 8 KByte of internal program memory space.

The 8-KByte secondary block can be mapped to the lowest location of the 64 KByte address space; it can also be hidden from the program counter and used as an independent EEPROM-like data memory.

In addition to the 72 KByte of EEPROM program memory on-chip and 1024 x8 bits of on-chip RAM, the devices can address up to 64 KByte of external program memory and up to 64 KByte of external RAM.

The flash memory blocks can be programmed via a standard 87C5x OTP EPROM programmer fitted with a special adapter and the firmware for SST's devices. During power-on reset, the devices can be configured as either a slave to an external host for source code storage or a master to an external host for an in-application programming (IAP) operation. The devices are designed to be programmed in-system and in-application on the printed circuit board for maximum flexibility. The devices are pre-programmed with an example of the bootstrap loader in the memory, demonstrating the initial user program code loading or subsequent user code updating via the IAP operation. The sample bootstrap loader is available for the user's reference and convenience only; SST does not guarantee its functionality or usefulness. Chip-Erase or Block-Erase operations will erase the pre-programmed sample code.

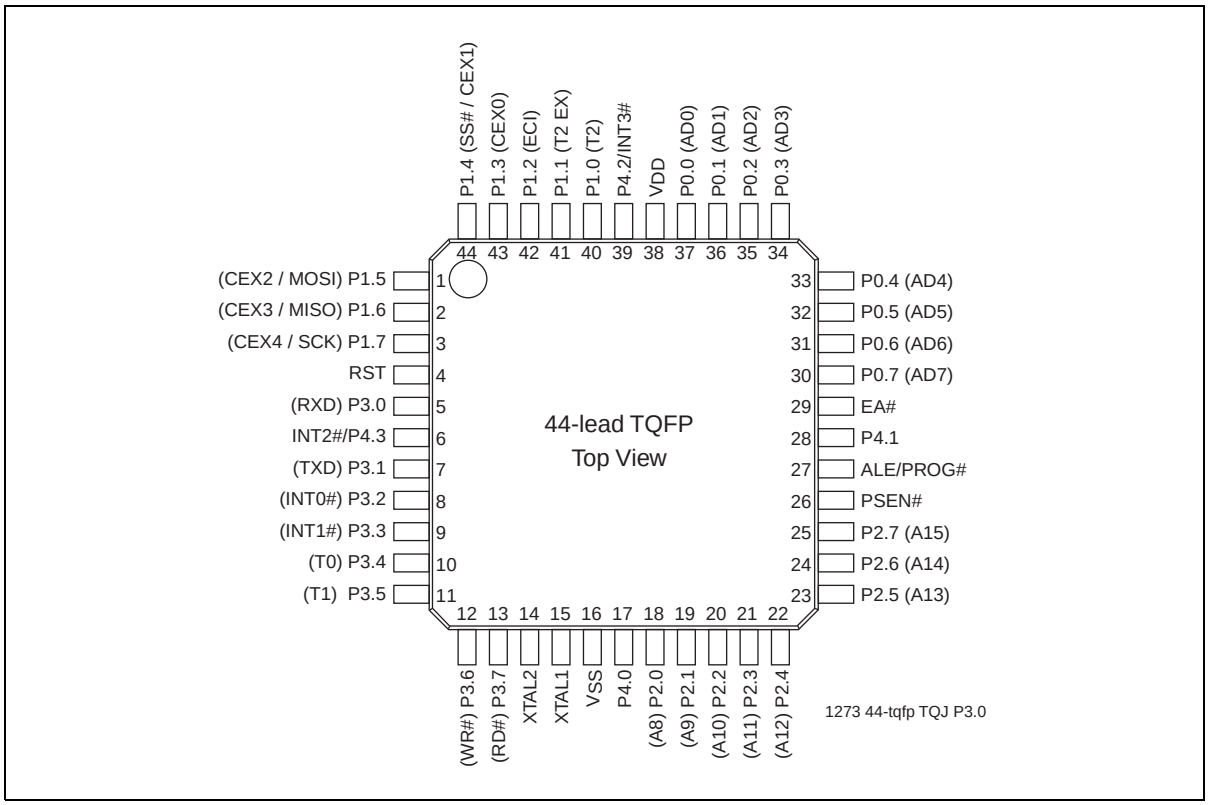

Figure 4: Pin Assignments for 44-lead TQFP

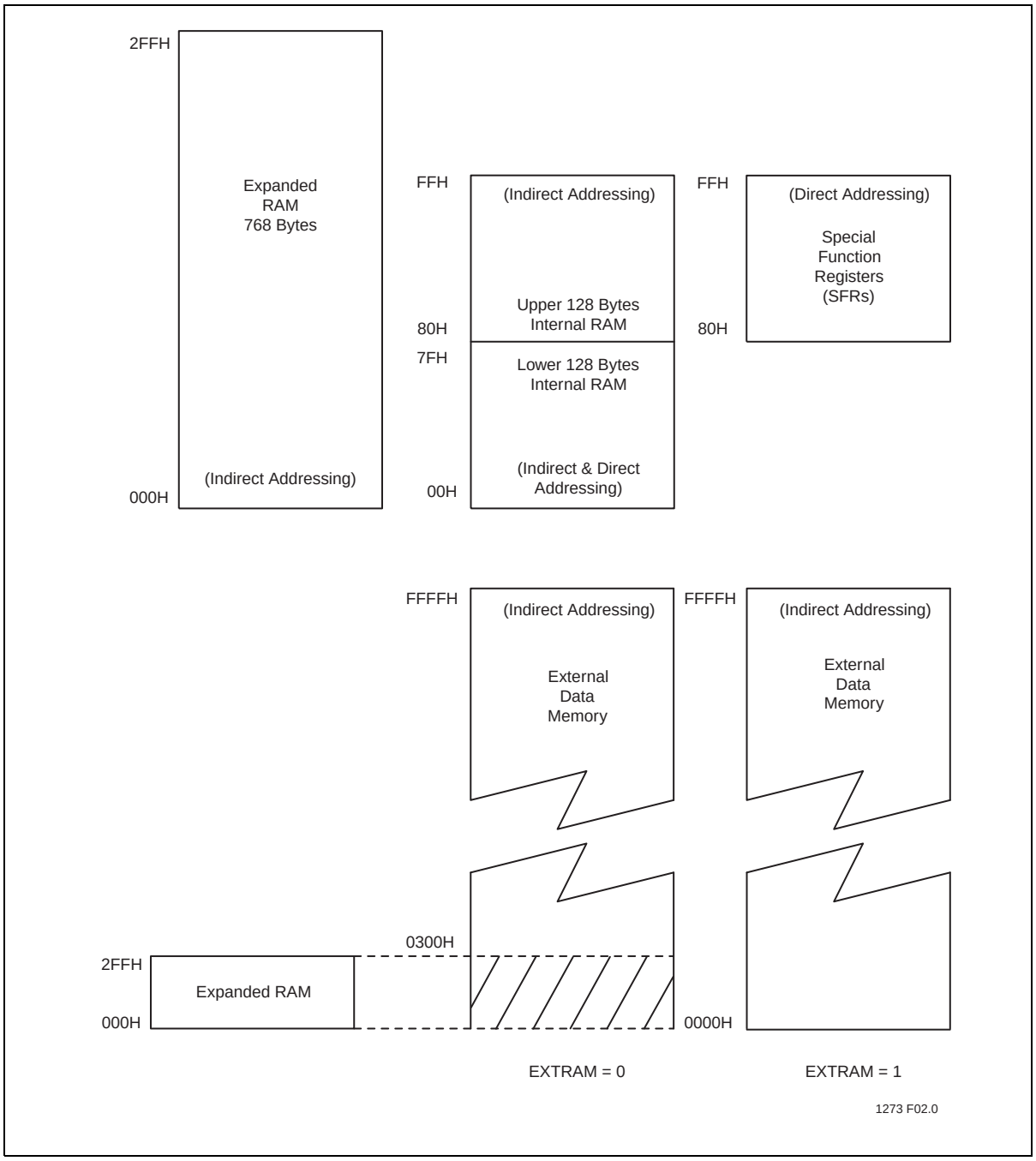

Figure 7: Internal and External Data Memory Structure

Table 6: CPU related SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
ACC[1]	Accumulator	E0H	ACC[7:0]								00H
B[1]	B Register	F0H	B[7:0]								00H
PSW[1]	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00H
SP	Stack Pointer	81H	SP[7:0]								07H
DPL	Data Pointer Low	82H	DPL[7:0]								00H
DPH	Data Pointer High	83H	DPH[7:0]								00H
IE[1]	Interrupt Enable	A8H	EA	EC	ET2	ES	ET1	EX1	ET0	EX0	00H
IEA[1]	Interrupt Enable A	E8H	-	-	-	-	EBO	-	-	-	xxxx0xxx b
IP[1]	Interrupt Priority Reg	B8H	-	PPC	PT2	PS	PT1	PX1	PT0	PX0	x0000000 b
IPH	Interrupt Priority Reg High	B7H	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	x0000000 b
IP1[1]	Interrupt Priority Reg A	F8H	-	-	-	-	PBO	PX3	PX2	-	xxxx0xxx b
IP1H	Interrupt Priority Reg A High	F7H	-	-	-	-	PBOH	PX3H	PX2H	-	xxxx0xxx b
PCON	Power Control	87H	SMOD1	SMOD0	BOF	POF	GF1	GF0	PD	IDL	00010000 b
AUXR	Auxiliary Reg	8EH	-	-	-	-	-	-	EXTRAM	AO	xxxxxxx0 0b
AUXR1	Auxiliary Reg 1	A2H	-	-	-	-	GF2	0	-	DPS	xxxx00x0 b
XICON	External Interrupt Control	AEH	-	EX3	IE3	IT3	0	EX2	IE2	IT2	00H

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1. Bit Addressable SFRs

Table 7: Flash Memory Programming SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
SFCF	SuperFlash Configuration	B1H	-	IAPEN	-	-	-	-	SWR	BSEL	x0xxxx00b
SFCM	SuperFlash Command	B2H	FIE	FCM[6:0]							00H
SFAL	SuperFlash Address Low	B3H	SuperFlash Low Order Byte Address Register - A_7 to A_0 (SFAL)								00H
SFAH	SuperFlash Address High	B4H	SuperFlash High Order Byte Address Register - A_{15} to A_8 (SFAH)								00H
SFDT	SuperFlash Data	B5H	SuperFlash Data Register								00H
SFST	SuperFlash Status	B6H	SB1_i	SB2_i	SB3_i	-	EDC_i	FLASH_BUSY	-	-	000x00xxb

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Table 8: Watchdog Timer SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
WDTC [1]	Watchdog Timer Control	C0H	-	-	-	WDOUT	WDRE	WDTS	WDT	SWDT	xxx00x00b
WDTD	Watchdog Timer Data/Reload	85H	Watchdog Timer Data/Reload								00H

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1. Bit Addressable SFRs

PCA Timer/Counter Mode Register[1] (CMOD)

Location	7	6	5	4	3	2	1	0	Reset Value
D9H	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF	00xxx000b

1. Not bit addressable

Symbol **Function**

CIDL Counter Idle Control:
0: Programs the PCA Counter to continue functioning during idle mode
1: Programs the PCA Counter to be gated off during idle

WDTE Watchdog Timer Enable:
0: Disables Watchdog Timer function on PCA module 4
1: Enables Watchdog Timer function on PCA module 4

- Not implemented, reserved for future use.
Note: User should not write '1's to reserved bits. The value read from a reserved bit is indeterminate.

CPS1 PCA Count Pulse Select bit 1

CPS0 PCA Count Pulse Select bit 2

CPS1	CPS0	Selected PCA Input[1]	
0	0	0	Internal clock, f_{OSC}/6 in 6 clock mode (f_{OSC}/12 in 12 clock mode)
0	1	1	Internal clock, f_{OSC}/2 in 6 clock mode (f_{OSC}/4 in 12 clock mode)
1	0	2	Timer 0 overflow
1	1	3	External clock at ECI/P1.2 pin
			(max. rate = f_{OSC}/4 in 6 clock mode, f_{OSC}/8 in 12 clock mode)

1. f_{OSC} = oscillator frequency

ECF PCA Enable Counter Overflow interrupt:
0: Disables the CF bit in CCON
1: Enables CF bit in CCON to generate an interrupt

SPI Control Register (SPCR)

Location	7	6	5	4	3	2	1	0	Reset Value
D5H	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	00H

Symbol **Function**

SPIE If both SPIE and ES are set to one, SPI interrupts are enabled.

SPE SPI enable bit.
0: Disables SPI.
1: Enables SPI and connects SS#, MOSI, MISO, and SCK to pins P1.4, P1.5, P1.6, P1.7.

DORD Data Transmission Order.
0: MSB first in data transmission.
1: LSB first in data transmission.

MSTR Master/Slave select.
0: Selects Slave mode.
1: Selects Master mode.

CPOL Clock Polarity
0: SCK is low when idle (Active High).
1: SCK is high when idle (Active Low).

CPHA Clock Phase control bit. The CPHA bit with the CPOL bit control the clock and data relationship between master and slave. See Figures 21 and 22.
0: Shift triggered on the leading edge of the clock.
1: Shift triggered on the trailing edge of the clock.

SPR1, SPR0SPI Clock Rate Select bits. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, f_{OSC}, is as follows:

SPR1	SPR0	SCK = f_{OSC} divided by
0	0	4
0	1	16
1	0	64
1	1	128

SPI Status Register (SPSR)

Location	7	6	5	4	3	2	1	0	Reset Value
AAH	SPIF	WCOL	-	-	-	-	-	-	00xxxxxxb

Symbol **Function**

SPIF SPI Interrupt Flag.
Upon completion of data transfer, this bit is set to 1.
If SPIE =1 and ES =1, an interrupt is then generated.
This bit is cleared by software.

WCOL Write Collision Flag.
Set if the SPI data register is written to during data transfer.
This bit is cleared by software.

Block 1, then the target address is implicitly defined to be in Block 0. If the IAP operation originates from external program space, then, the target will depend on the address and the state of bank selection.

IAP Enable Bit

The IAP enable bit, SFCF[6], enables in-application programming mode. Until this bit is set, all flash programming IAP commands will be ignored.

Table 13: IAP Address Resolution

EA#	SFCF[1:0]	Address of IAP Inst.	Target Address	Block Being Programmed
1	00	>= 2000H (Block 0)	>= 2000H (Block 0)	None[1]
1	00	>= 2000H (Block 0)	< 2000H (Block 1)	Block 1
1	00	< 2000H (Block 1)	Any (Block 0)	Block 0
1	01, 10, 11	Any (Block 0)	>= 2000H (Block 0)	None[1]
1	01, 10, 11	Any (Block 0)	< 2000H (Block 1)	Block 1
0	00	From external	>= 2000H (Block 0)	Block 0
0	00	From external	< 2000H (Block 1)	Block 1
0	01, 10, 11	From external	Any (Block 0)	Block 0

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1. No operation is performed because code from one block may not program the same originating block

In-Application Programming Mode Commands

All of the following commands can only be initiated in the IAP mode. In all situations, writing the control byte to the SFCM register will initiate all of the operations. All commands will not be enabled if the security locks are enabled on the selected memory block.

The Program command is for programming new data into the memory array. The portion of the memory array to be programmed should be in the erased state, FFH. If the memory is not erased, it should first be erased with an appropriate Erase command. **Warning: Do not attempt to write (program or erase) to a block that the code is currently fetching from. This will cause unpredictable program behavior and may corrupt program data.**

Byte-Verify

The Byte-Verify command allows the user to verify that the device has correctly performed an Erase or Program command. Byte-Verify command returns the data byte in SFDT if the command is successful. The user is required to check that the previous flash operation has fully completed before issuing a Byte-Verify. Byte-Verify command execution time is short enough that there is no need to poll for command completion and no interrupt is generated.

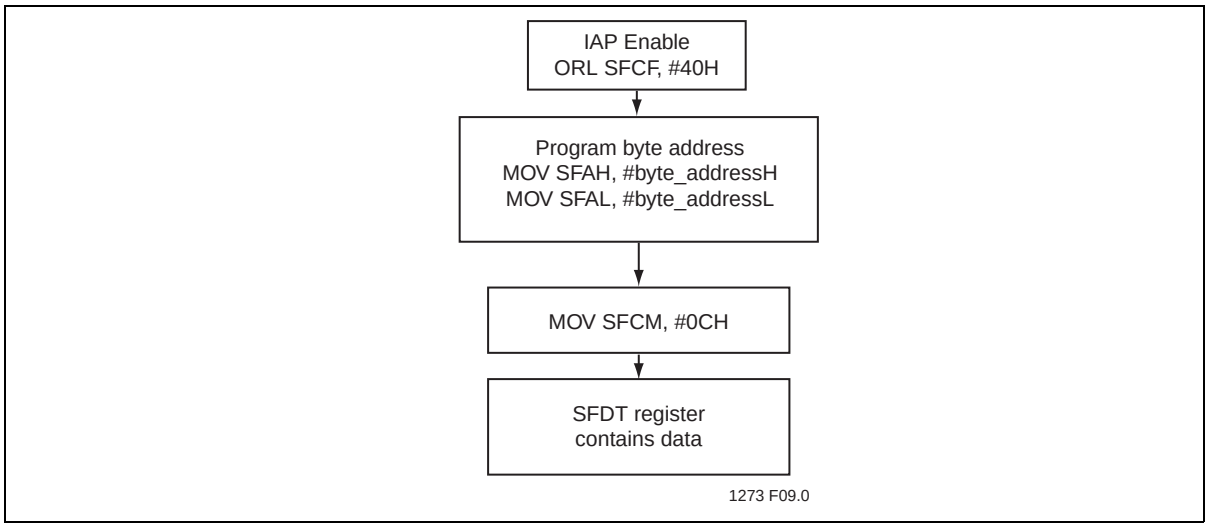

Figure 13: Byte Verify

Prog-SB3, Prog-SB2, Prog-SB1

Prog-SB3, Prog-SB2, Prog-SB1 commands are used to program the security bits (see Table 25). Completion of any of these commands, the security options will be updated immediately.

Security bits previously in un-programmed state can be programmed by these commands. Prog-SB3, Prog-SB2 and Prog-SB1 commands should only reside in Block 1 or external code memory.

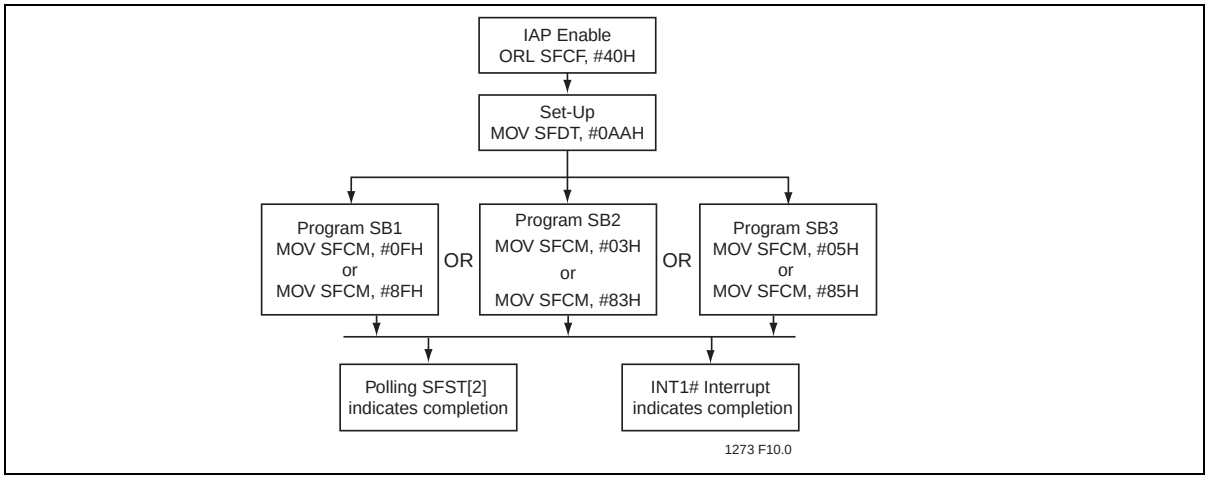

Figure 14: Prog-SB3, Prog-SB2, Prog-SB1

Polling

A command that uses the polling method to detect flash operation completion should poll on the FLASH_BUSY bit (SFST[2]). When FLASH_BUSY de-asserts (logic 0), the device is ready for the next operation.

MOVC instruction may also be used for verification of the Programming and Erase operation of the flash memory. MOVC instruction will fail if it is directed at a flash block that is still busy.

Interrupt Termination

If interrupt termination is selected, (SFCM[7] is set), then an interrupt (INT1) will be generated to indicate flash operation completion. Under this condition, the INT1 becomes an internal interrupt source. The INT1# pin can now be used as a general purpose port pin and it cannot be the source of External Interrupt 1 during in-application programming.

In order to use an interrupt to signal flash operation termination. EX1 and EA bits of IE register must be set. The IT1 bit of TCON register must also be set for edge trigger detection.

Table 14: IAP Commands[1]

Operation	SFCM [6:0][2]	SFDT [7:0]	SFAH [7:0]	SFAL [7:0]
Chip-Erase[3]	01H	55H	X[4]	X
Block-Erase[5]	0DH	55H	AH	X
Sector-Erase[5]	0BH	X	AH[6]	AL[7]
Byte-Program[5]	0EH	DI[8]	AH	AL
Byte-Verify (Read)[5]	0CH	DO[8]	AH	AL
Prog-SB1[9]	0FH	AAH	X	X
Prog-SB2[9]	03H	AAH	X	X
Prog-SB3[9]	05H	AAH	X	X
Prog-SC0[9]	09H	AAH	5AH	X
Enable-Clock-Double[9]	08H	AAH	55H	X

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1. SFCF[6]=1 enables IAP commands; SFCF[6]=0 disables IAP commands.
2. Interrupt/Polling enable for flash operation completion
   SFCM[7] =1: Interrupt enable for flash operation completion
   0: polling enable for flash operation completion
3. Chip-Erase only functions in IAP mode when EA#=0 (external memory execution) and device is not in level 4 locking.
4. X can be V_{IL} or V_{IH}, but no other value.
5. Refer to Table 13 for address resolution
6. AH = Address high order byte
7. AL = Address low order byte
8. DI = Data Input, DO = Data Output, all other values are in hex.
9. Instruction must be located in Block 1 or external code memory.

Note: DISIAPL pin in PLCC or TQFP will also disable IAP commands if it is externally pulled low when reset.

Timers/Counters

Timers

The device has three 16-bit registers that can be used as either timers or event counters. The three timers/counters are denoted Timer 0 (T0), Timer 1 (T1), and Timer 2 (T2). Each is designated a pair of 8-bit registers in the SFRs. The pair consists of a most significant (high) byte and least significant (low) byte. The respective registers are TL0, TH0, TL1, TH1, TL2, and TH2.

Timer Set-up

Refer to Table 9 for TMOD, TCON, and T2CON registers regarding timers T0, T1, and T2. The following tables provide TMOD values to be used to set up Timers T0, T1, and T2.

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set separately to turn the timer on.

Table 15: Timer/Counter 0

	Mode	Function	TMOD	
			Internal Control[1]	External Control[2]
Used as Timer	0	13-bit Timer	00H	08H
	1	16-bit Timer	01H	09H
	2	8-bit Auto-Reload	02H	0AH
	3	Two 8-bit Timers	03H	0BH
Used as Counter	0	13-bit Timer	04H	0CH
	1	16-bit Timer	05H	0DH
	2	8-bit Auto-Reload	06H	0EH
	3	Two 8-bit Timers	07H	0FH

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1. The Timer is turned ON/OFF by setting/clearing bit TR0 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on INT0# (P3.2) when TR0 = 1 (hardware control).

Table 16: Timer/Counter 1

	Mode	Function	TMOD	
			Internal Control[1]	External Control[2]
Used as Timer	0	13-bit Timer	00H	80H
	1	16-bit Timer	10H	90H
	2	8-bit Auto-Reload	20H	A0H
	3	Does not run	30H	B0H
Used as Counter	0	13-bit Timer	40H	C0H
	1	16-bit Timer	50H	D0H
	2	8-bit Auto-Reload	60H	E0H
	3	Not available	-	-

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1. The Timer is turned ON/OFF by setting/clearing bit TR1 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on INT1# (P3.3) when TR1 = 1 (hardware control).

SPI Transfer Formats

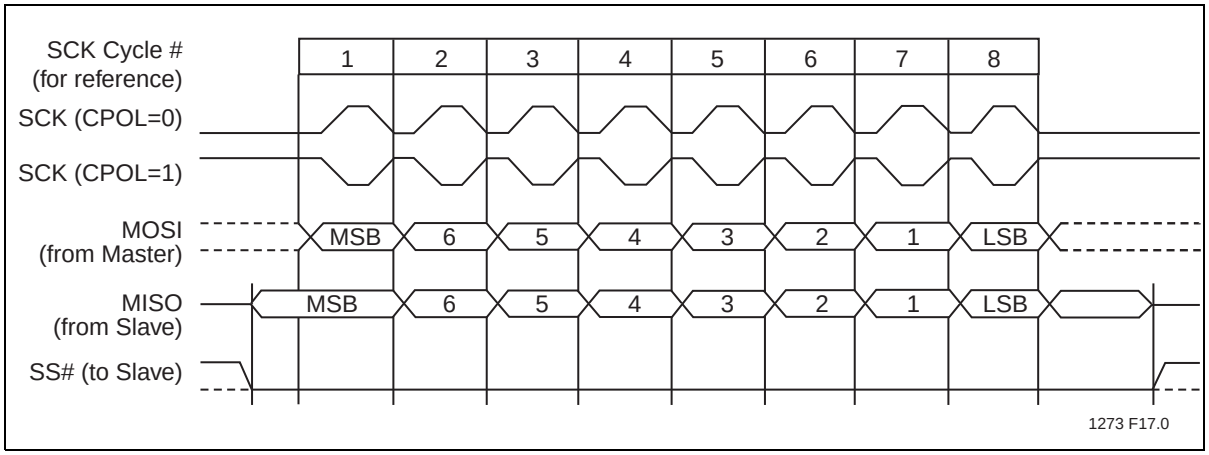

Figure 21: SPI Transfer Format with CPHA = 0

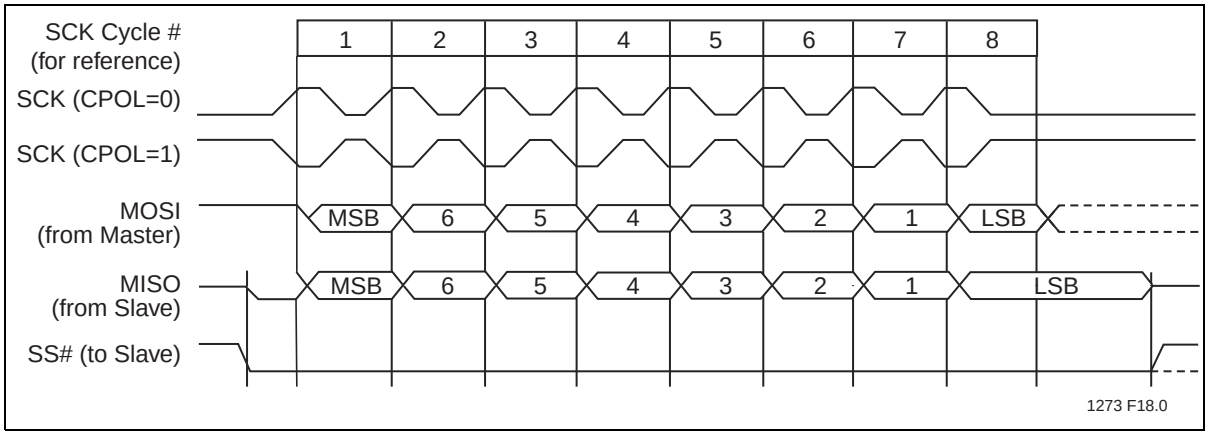

Figure 22: SPI Transfer Format with CPHA = 1

Security Lock

The security lock protects against software piracy and prevents the contents of the flash from being read by unauthorized parties. It also protects against code corruption resulting from accidental erasing and programming to the internal flash memory. There are two different types of security locks in the device security lock system: hard lock and SoftLock.

Hard Lock

When hard lock is activated, MOVC or IAP instructions executed from an unlocked or soft locked program address space, are disabled from reading code bytes in hard locked memory blocks (See Table 26). Hard lock can either lock both flash memory blocks or just lock the 8 KByte flash memory block (Block 1). All external host and IAP commands except for Chip-Erase are ignored for memory blocks that are hard locked.

SoftLock

SoftLock allows flash contents to be altered under a secure environment. This lock option allows the user to update program code in the soft locked memory block through in-application programming mode under a predetermined secure environment. For example, if Block 1 (8K) memory block is locked (hard locked or soft locked), and Block 0 memory block is soft locked, code residing in Block 1 can program Block 0. The following IAP mode commands issued through the command mailbox register, SFCM, executed from a Locked (hard locked or soft locked) block, can be operated on a soft locked block: Block-Erase, Sector-Erase, Byte-Program and Byte-Verify.

In external host mode, SoftLock behaves the same as a hard lock.

Security Lock Status

The three bits that indicate the device security lock status are located in SFST[7:5]. As shown in Figure 30 and Table 25, the three security lock bits control the lock status of the primary and secondary blocks of memory. There are four distinct levels of security lock status. In the first level, none of the security lock bits are programmed and both blocks are unlocked. In the second level, although both blocks are now locked and cannot be programmed, they are available for read operation via Byte-Verify. In the third level, three different options are available: Block 1 hard lock / Block 0 SoftLock, SoftLock on both blocks, and hard lock on both blocks. Locking both blocks is the same as Level 2, Block 1 except read operation isn't available. The fourth level of security is the most secure level. It doesn't allow read/program of internal memory or boot from external memory. For details on how to program the security lock bits refer to the external host mode and in-application programming sections.

Software Reset

The software reset is executed by changing SFCF[1] (SWR) from “0” to “1”. A software reset will reset the program counter to address 0000H. All SFR registers will be set to their reset values, except SFCF[1] (SWR), WDTC[2] (WDTS), and RAM data will not be altered.

Brown-out Detection Reset

The device includes a brown-out detection circuit to protect the system from severed supplied voltage V_{DD} fluctuations. SST89E516RDx internal brown-out detection threshold is 3.85V, SST89V516RDx brown-out detection threshold is 2.35V. For brown-out voltage parameters, please refer to Table 36.

When V_{DD} drops below this voltage threshold, the brown-out detector triggers the circuit to generate a brown-out interrupt but the CPU still runs until the supplied voltage returns to the brown-out detection voltage V_{BOD}. The default operation for a brown-out detection is to cause a processor reset.

V_{DD} must stay below V_{BOD} at least four oscillator clock periods before the brown-out detection circuit will respond.

Brown-out interrupt can be enabled by setting the EBO bit in IEA register (address E8H, bit 3). If EBO bit is set and a brown-out condition occurs, a brown-out interrupt will be generated to execute the program at location 004BH. It is required that the EBO bit be cleared by software after the brown-out interrupt is serviced. Clearing EBO bit when the brown-out condition is active will properly reset the device. If brown-out interrupt is not enabled, a brown-out condition will reset the program to resume execution at location 0000H.

Table 28: Power Saving Modes

Mode	Initiated by	State of MCU	Exited by
Idle Mode	Software (Set IDL bit in PCON) MOV PCON, #01H;	CLK is running. Interrupts, serial port and timers/counters are active. Program Counter is stopped. ALE and PSEN# signals at a HIGH level during Idle. All registers remain unchanged.	Enabled interrupt or hardware reset. Start of interrupt clears IDL bit and exits idle mode, after the ISR RETI instruction, program resumes execution beginning at the instruction following the one that invoked idle mode. A user could consider placing two or three NOP instructions after the instruction that invokes idle mode to eliminate any problems. A hardware reset restarts the device similar to a power-on reset.
Power-down Mode	Software (Set PD bit in PCON) MOV PCON, #02H;	CLK is stopped. On-chip SRAM and SFR data is maintained. ALE and PSEN# signals at a LOW level during power -down. External Interrupts are only active for level sensitive interrupts, if enabled.	Enabled external level sensitive interrupt or hardware reset. Start of interrupt clears PD bit and exits power-down mode, after the ISR RETI instruction program resumes execution beginning at the instruction following the one that invoked power-down mode. A user could consider placing two or three NOP instructions after the instruction that invokes power-down mode to eliminate any problems. A hardware reset restarts the device similar to a power-on reset.

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Electrical Specification

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Ambient Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on EA# Pin to V_{SS} . . . . . -0.5V to +14.0V
D.C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20ns) on Any Other Pin to V_{SS} . . . . . -1.0V to V_{DD}+1.0V
Maximum I_{OL} per I/O Pins P1.5, P1.6, P1.7 . . . . . 20mA
Maximum I_{OL} per I/O for All Other Pins 15mA
Package Power Dissipation Capability (T_A = 25°C) 1.5W
Through Hole Lead Soldering Temperature (10 Seconds) . . . . . 300°C
Surface Mount Solder Reflow Temperature[1] . . . . . 260°C for 10 seconds
Output Short Circuit Current[2] . . . . . 50 mA

1. Excluding certain with-Pb 32-PLCC units, all packages are 260°C capable in both non-Pb and with-Pb solder versions. Certain with-Pb 32-PLCC package types are capable of 240°C for 10 seconds; please consult the factory for the latest information.
2. Outputs shorted for no more than one second. No more than one output shorted at a time.
(Based on package heat transfer limitations, not device power consumption.

Note: This specification contains preliminary information on new products in production.
The specifications are subject to change without notice.

Table 31: Operating Range

Symbol	Description	Min.	Max	Unit
T_A	Ambient Temperature Under Bias			
	Standard	0	+70	°C
	Industrial	-40	+85	°C
V_{DD}	Supply Voltage			
	SST89E516RDx	4.5	5.5	V
	SST89V516RDx	2.7	3.6	V
f_{OSC}	Oscillator Frequency			
	SST89E516RDx	0	40	MHz
	SST89V516RDx	0	33	MHz
	Oscillator Frequency for IAP			
	SST89E516RDx	.25	40	MHz
	SST89V516RDx	.25	33	MHz

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AC Electrical Characteristics

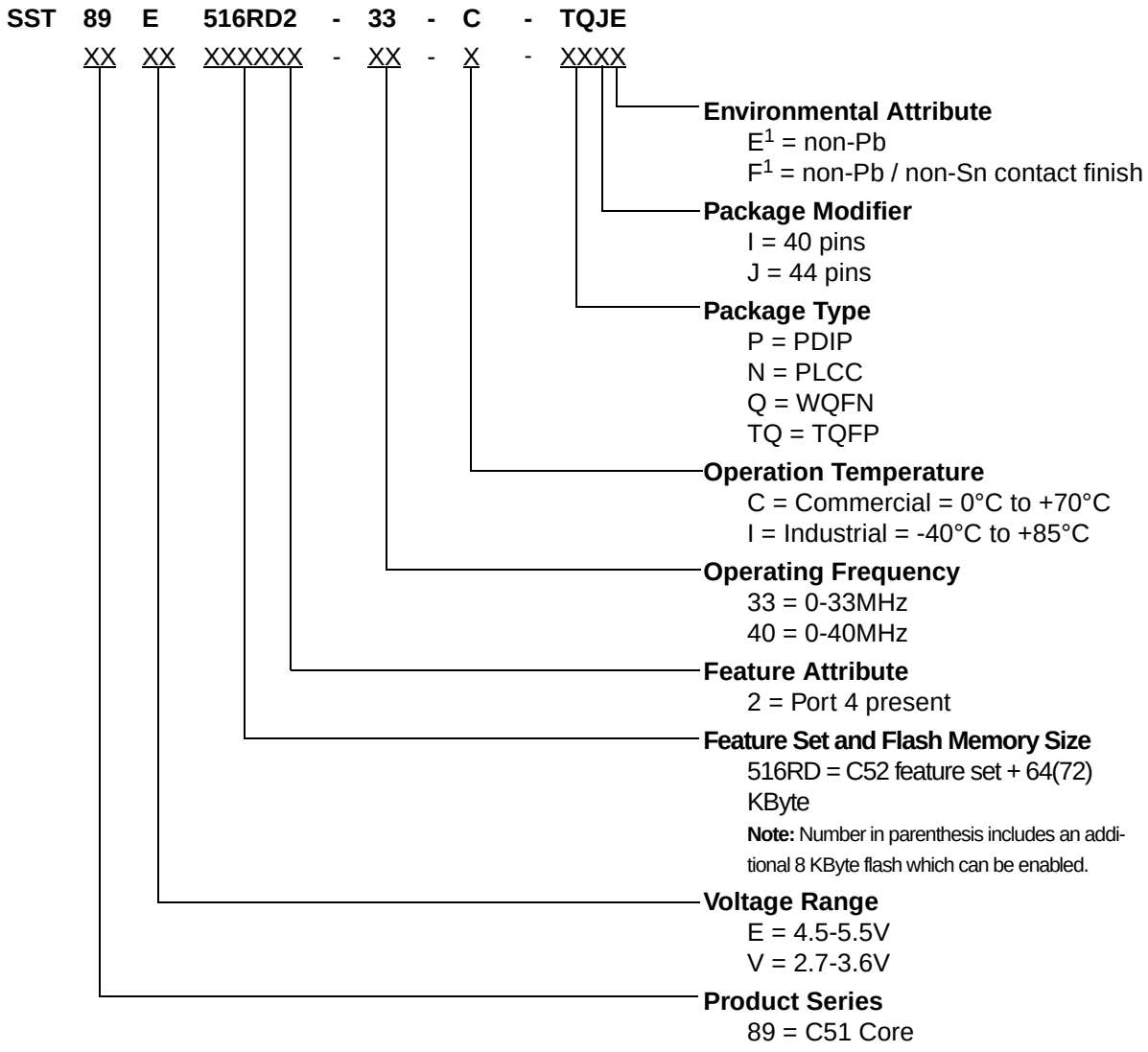
AC Characteristics:

(Over Operating Conditions: Load Capacitance for Port 0, ALE#, and PSEN# = 100pF; Load Capacitance for All Other Outputs = 80pF)

Table 38: AC Electrical Characteristics (1 of 2)
T_A = -40°C to +85°C, V_{DD} = 2.7-3.6V@33MHz, 4.5-5.5V@40MHz, V_{SS} = 0V

		Oscillator						
		33 MHz (x1 Mode) 16 MHz (x2 Mode)[1]		40 MHz (x1 Mode) 20 MHz (x2 Mode)[1]		Variable		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units
$1/T_{CLCL}$	x1 Mode Oscillator Frequency	0	33	0	40	0	40	MHz
$1/2T_{CLCL}$	x2 Mode Oscillator Frequency	0	16	0	20	0	20	MHz
T_{LHLL}	ALE Pulse Width	46		35		$2T_{CLCL}$ - 15		ns
T_{AVLL}	Address Valid to ALE Low	5				T_{CLCL} - 25 (3V)		ns
				10		T_{CLCL} - 15 (5V)		ns
T_{LLAX}	Address Hold After ALE Low	5				T_{CLCL} - 25 (3V)		ns
				10		T_{CLCL} - 15 (5V)		ns
T_{LLIV}	ALE Low to Valid Instr In		56				$4T_{CLCL}$ - 65 (3V)	ns
					55		$4T_{CLCL}$ - 45 (5V)	ns
T_{LLPL}	ALE Low to PSEN# Low	5				T_{CLCL} - 25 (3V)		ns
				10		T_{CLCL} - 15 (5V)		ns
T_{PLPH}	PSEN# Pulse Width	66		60		$3T_{CLCL}$ - 25 (3V) $3T_{CLCL}$ - 15 (5V)		ns
T_{PLIV}	PSEN# Low to Valid Instr In		35				$3T_{CLCL}$ - 55 (3V)	ns
					25		$3T_{CLCL}$ - 50 (5V)	ns
T_{PXIX}	Input Instr Hold After PSEN#					0		ns
T_{PXIZ}	Input Instr Float After PSEN#		25				T_{CLCL} - 5 (3V)	ns
					10		T_{CLCL} - 15 (5V)	ns
T_{PXAV}	PSEN# to Address valid	22		17		T_{CLCL} - 8		ns
T_{AVIV}	Address to Valid Instr In		72				$5T_{CLCL}$ - 80 (3V)	ns
					65		$5T_{CLCL}$ - 60 (5V)	ns
T_{PLAZ}	PSEN# Low to Address Float		10		10		10	ns
T_{RLRH}	RD# Pulse Width	142		120		$6T_{CLCL}$ - 40 (3V) $6T_{CLCL}$ - 30 (5V)		ns
T_{WLWH}	Write Pulse Width (WE#)	142		120		$6T_{CLCL}$ - 40 (3V) $6T_{CLCL}$ - 30 (5V)		ns
T_{RLDV}	RD# Low to Valid Data In		62				$5T_{CLCL}$ - 90 (3V)	ns

Product Ordering Information



1. Environmental suffix “E” denotes non-Pb solder. Environmental suffix “F” denote non-Pb /non-Sn solder. SST non-Pb / non-Sn solder devices are “RoHS Compliant”.

Valid Combinations

Valid combinations for SST89E516RD2

SST89E516RD2-40-C-NJE	SST89E516RD2-40-C-TQJE
SST89E516RD2-40-I-NJE	SST89E516RD2-40-I-TQJE

Valid combinations for SST89V516RD2

SST89V516RD2-33-C-NJE	SST89V516RD2-33-C-TQJE
SST89V516RD2-33-I-NJE	SST89V516RD2-33-I-TQJE

Valid combinations for SST89E516RD

SST89E516RD-40-C-PIE	SST89E516RD-40-C-QIF
	SST89E516RD-40-I-QIF

Valid combinations for SST89V516RD

SST89V516RD-33-C-PIE	SST89V516RD-33-C-QIF
	SST89V516RD-33-I-QIF

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Packaging Diagrams

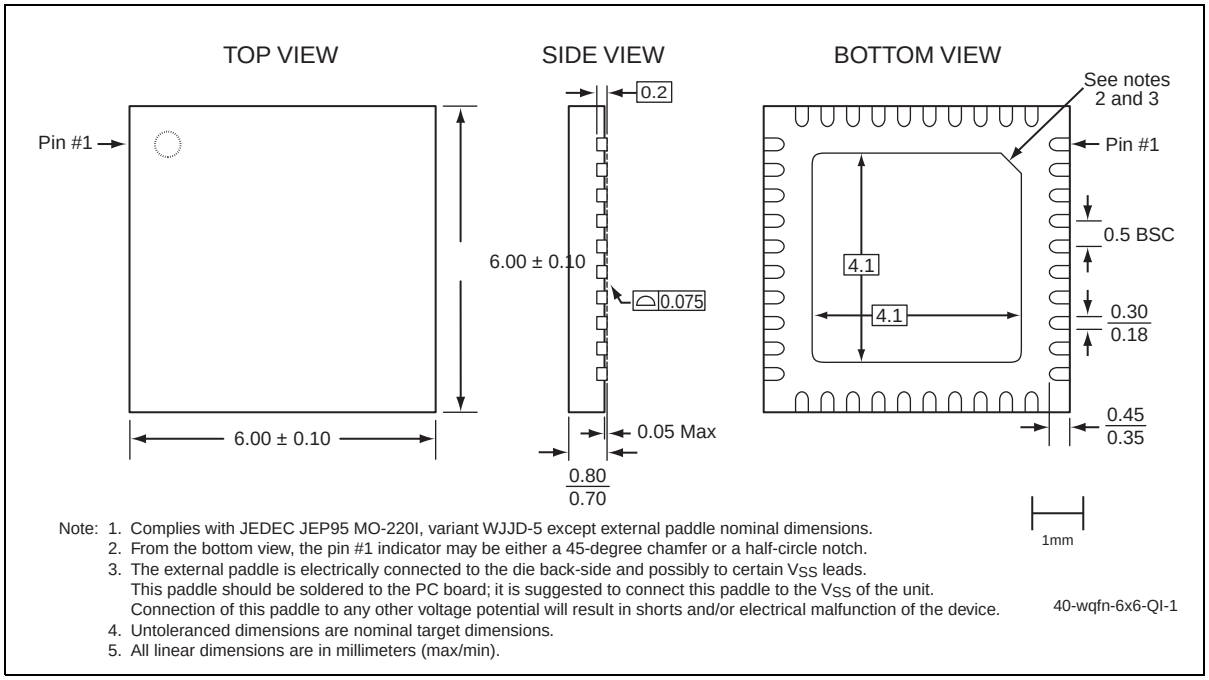


Figure 47: 40-contact Very-very-thin Quad Flat No-lead (WQFN)
SST Package Code: QI