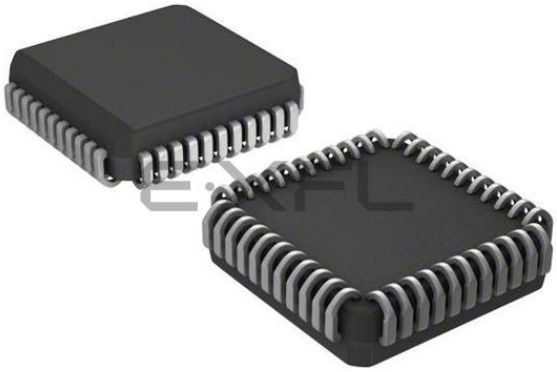

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	36
Program Memory Size	72KB (72K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sst89v516rd2-33-c-nje

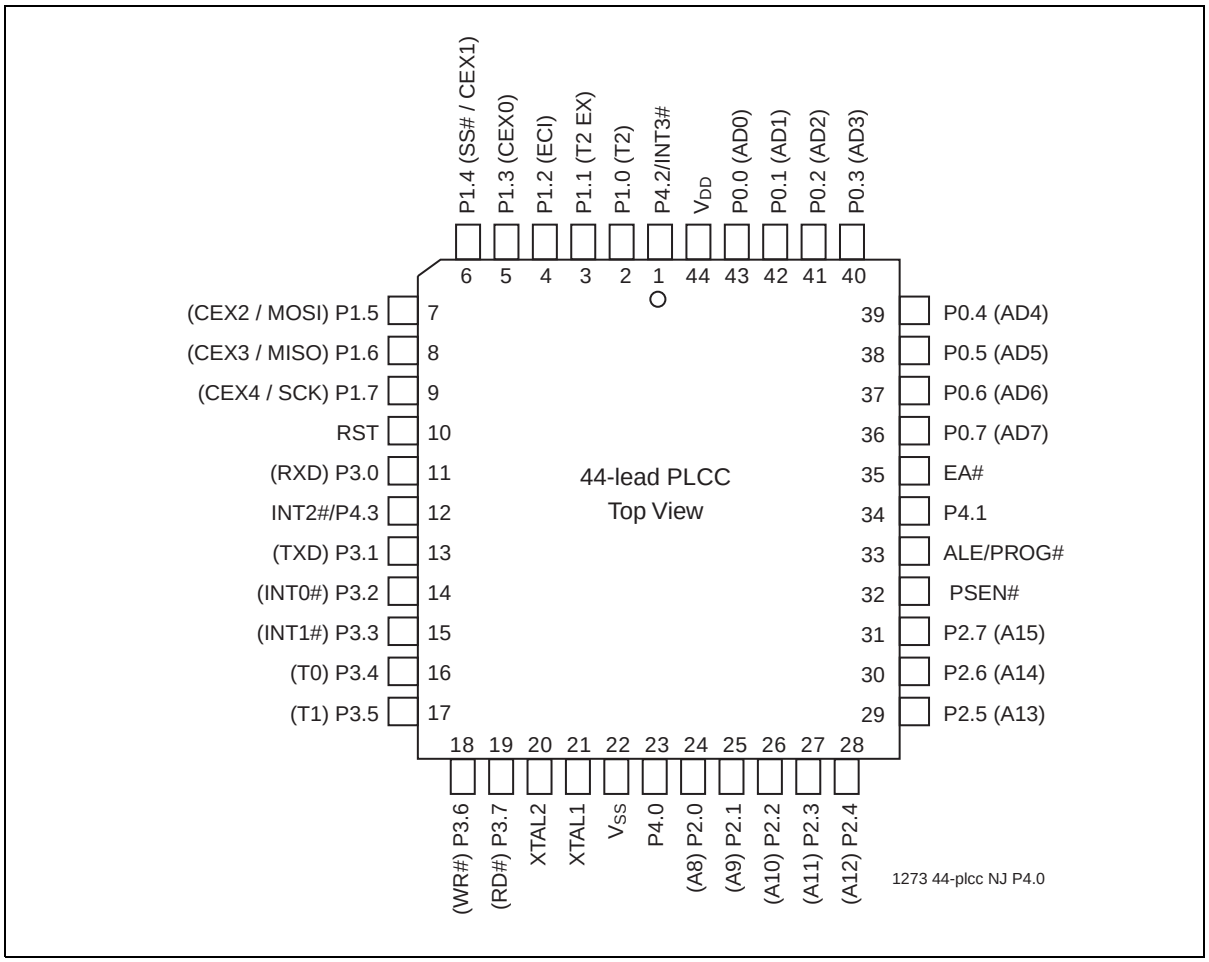

Figure 5: Pin Assignments for 44-lead PLCC

Table 1: Pin Descriptions (Continued) (3 of 3)

Symbol	Type[1]	Name and Functions
P4[3] / INT2#	I/O	Bit 3 of port 4 / INT2# External interrupt 2 input
XTAL1	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	O	**Crystal 2:** Output from the inverting oscillator amplifier
V_{DD}	I	**Power Supply**
V_{SS}	I	**Ground**

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1. I = Input; O = Output
2. It is not necessary to receive a 12V programming supply voltage during flash programming.
3. ALE loading issue: When ALE pin experiences higher loading (>30pf) during the reset, the MCU may accidentally enter into modes other than normal working mode. The solution is to add a pull-up resistor of 3-50 KΩ to V_{DD}, e.g. for ALE pin.
4. For 6 clock mode, ALE is emitted at 1/3 of crystal frequency.
5. Port 4 is not present on the PDIP and WQFN packages.

Program Memory Block Switching

The program memory block switching feature of the device allows either Block 1 or the lowest 8 KByte of Block 0 to be used for the lowest 8 KByte of the program address space. SFCF[1:0] controls program memory block switching.

Table 2: SFCF Values for Program Memory Block Switching

SFCF[1:0]	Program Memory Block Switching
01, 10, 11	Block 1 is not visible to the program counter (PC). Block 1 is reachable only via in-application programming from 0000H - 1FFFH.
00	Block 1 is overlaid onto the low 8K of the program address space; occupying address locations 0000H - 1FFFH. When the PC falls within 0000H - 1FFFH, the instruction will be fetched from Block 1 instead of Block 0. Outside of 0000H - 1FFFH, Block 0 is used. Locations 0000H - 1FFFH of Block 0 are reachable through in-application programming.

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Reset Configuration of Program Memory Block Switching

Program memory block switching is initialized after reset according to the state of the Start-up Configuration bit SC0. The SC0 bit is programmed via an external host mode command or an IAP Mode command. See Table 14.

Once out of reset, the SFCF[0] bit can be changed dynamically by the program for desired effects. Changing SFCF[0] will not change the SC0 bit.

Caution must be taken when dynamically changing the SFCF[0] bit. Since this will cause different physical memory to be mapped to the logical program address space. The user must avoid executing block switching instructions within the address range 0000H to 1FFFH.

Table 3: SFCF Values Under Different Reset Conditions

	State of SFCF[1:0] after:		
SC0[1]	Power-on or External Reset	WDT Reset or Brown-out Reset	Software Reset
U (1)	00 (default)	x0	10
P (0)	01	x1	11

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1. P = Programmed (Bit logic state = 0),
   U = Unprogrammed (Bit logic state = 1)

Data RAM Memory

The data RAM has 1024 bytes of internal memory. The RAM can be addressed up to 64KB for external data memory.

Expanded Data RAM Addressing

The SST89E/V516RDx have the capability of 1 KByte RAM. See Figure 7.

The device has four sections of internal data memory:

1. The lower 128 Bytes of RAM (00H to 7FH) are directly and indirectly addressable.
2. The higher 128 Bytes of RAM (80H to FFH) are indirectly addressable.
3. The special function registers (80H to FFH) are directly addressable only.
4. The expanded RAM of 768 Bytes (00H to 2FFH) is indirectly addressable by the move external instruction (MOVX) and clearing the EXTRAM bit. (See “Auxiliary Register (AUXR)” in Section , “Special Function Registers”)

Since the upper 128 Bytes occupy the same addresses as the SFRs, the RAM must be accessed indirectly. The RAM and SFRs space are physically separate even though they have the same addresses.

When instructions access addresses in the upper 128 Bytes (above 7FH), the MCU determines whether to access the SFRs or RAM by the type of instruction given. If it is indirect, then RAM is accessed. If it is direct, then an SFR is accessed. See the examples below.

Indirect Access:

MOV@R0, #data; R0 contains 90H

Register R0 points to 90H which is located in the upper address range. Data in “#data” is written to RAM location 90H rather than port 1.

Direct Access:

MOV90H, #data; write data to P1

Data in “#data” is written to port 1. Instructions that write directly to the address write to the SFRs.

To access the expanded RAM, the EXTRAM bit must be cleared and MOVX instructions must be used. The extra 768 bytes of memory is physically located on the chip and logically occupies the first 768 bytes of external memory (addresses 000H to 2FFH).

When EXTRAM = 0, the expanded RAM is indirectly addressed using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. Accessing the expanded RAM does not affect ports P0, P3.6 (WR#), P3.7 (RD#), or P2. With EXTRAM = 0, the expanded RAM can be accessed as in the following example.

Expanded RAM Access (Indirect Addressing only):

MOVX@DPTR, A; DPTR contains 0A0H

DPTR points to 0A0H and data in “A” is written to address 0A0H of the expanded RAM rather than external memory. Access to external memory higher than 2FFH using the MOVX instruction will access external memory (0300H to FFFFH) and will perform in the same way as the standard 8051, with P0 and P2 as data/address bus, and P3.6 and P3.7 as write and read timing signals.

When EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 8051. Using MOVX @Ri provides an 8-bit address with multiplexed data on Port 0. Other output port pins can be used to output higher order address bits. This provides external paging capabilities. Using MOVX @DPTR generates a 16-bit address. This allows external addressing up the 64K. Port 2 provides the

Table 7: Flash Memory Programming SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
SFCF	SuperFlash Configuration	B1H	-	IAPEN	-	-	-	-	SWR	BSEL	x0xxxx00b
SFCM	SuperFlash Command	B2H	FIE	FCM[6:0]							00H
SFAL	SuperFlash Address Low	B3H	SuperFlash Low Order Byte Address Register - A_7 to A_0 (SFAL)								00H
SFAH	SuperFlash Address High	B4H	SuperFlash High Order Byte Address Register - A_{15} to A_8 (SFAH)								00H
SFDT	SuperFlash Data	B5H	SuperFlash Data Register								00H
SFST	SuperFlash Status	B6H	SB1_i	SB2_i	SB3_i	-	EDC_i	FLASH_BUSY	-	-	000x00xxb

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Table 8: Watchdog Timer SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
WDTC [1]	Watchdog Timer Control	C0H	-	-	-	WDOUT	WDRE	WDTS	WDT	SWDT	xxx00x00b
WDTD	Watchdog Timer Data/Reload	85H	Watchdog Timer Data/Reload								00H

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1. Bit Addressable SFRs

Interrupt Enable (IE)

Location	7	6	5	4	3	2	1	0	Reset Value
A8H	EA	EC	ET2	ES	ET1	EX1	ET0	EX0	00H

Symbol	Function
EA	Global Interrupt Enable. 0 = Disable 1 = Enable
EC	PCA Interrupt Enable.
ET2	Timer 2 Interrupt Enable.
ES	Serial Interrupt Enable.
ET1	Timer 1 Interrupt Enable.
EX1	External 1 Interrupt Enable.
ET0	Timer 0 Interrupt Enable.
EX0	External 0 Interrupt Enable.

Interrupt Enable A (IEA)

Location	7	6	5	4	3	2	1	0	Reset Value
E8H	-	-	-	-	EBO	-	-	-	xxxx0xxxb

Symbol	Function
EBO	Brown-out Interrupt Enable. 1 = Enable the interrupt 0 = Disable the interrupt

Watchdog Timer Data/Reload Register (WDTD)

Location	7	6	5	4	3	2	1	0	Reset Value
85H	Watchdog Timer Data/Reload								00H

Symbol	Function
WDTD	Initial/Reload value in Watchdog Timer. New value won't be effective until WDT is set.

PCA Timer/Counter Control Register[1] (CCON)

Location	7	6	5	4	3	2	1	0	Reset Value
D8H	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0	00x00000b

1. Bit addressable

Symbol	Function
CF	PCA Counter Overflow Flag Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software, but can only cleared by software.
CR	PCA Counter Run control bit Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.
-	Not implemented, reserved for future use. **Note:** User should not write '1's to reserved bits. The value read from a reserved bit is indeterminate.
CCF4	PCA Module 4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF3	PCA Module 3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF2	PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF1	PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF0	PCA Module 0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.

PCA Compare/Capture Module Mode Register[1] (CCAPMn)

Location	7	6	5	4	3	2	1	0	Reset Value
DAH	-	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0	00xxx000b
DBH	-	ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1	00xxx000b
DCH	-	ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2	00xxx000b
DDH	-	ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3	00xxx000b
DEH	-	ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4	00xxx000b

1. Not bit addressable

Symbol **Function**

-
Not implemented, reserved for future use.
Note: User should not write ‘1’s to reserved bits. The value read from a reserved bit is indeterminate.

ECOMn
Enable Comparator
0: Disables the comparator function
1: Enables the comparator function

CAPPn
Capture Positive
0: Disables positive edge capture on CEX[4:0]
1: Enables positive edge capture on CEX[4:0]

CAPNn
Capture Negative
0: Disables negative edge capture on CEX[4:0]
1: Enables negative edge capture on CEX[4:0]

MATn
Match: Set ECOM[4:0] and MAT[4:0] to implement the software timer mode
0: Disables software timer mode
1: A match of the PCA counter with this module’s compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.

TOGn
Toggle
0: Disables toggle function
1: A match of the PCA counter with this module’s compare/capture register causes the CEXn pin to toggle.

PWMn
Pulse Width Modulation mode
0: Disables PWM mode
1: Enables CEXn pin to be used as a pulse width modulated output

ECCFn
Enable CCF Interrupt
0: Disables compare/capture flag CCF[4:0] in the CCON register to generate an interrupt request.
1: Enables compare/capture flag CCF[4:0] in the CCON register to generate an interrupt request.

Serial Port Control Register (SCON)

Location	7	6	5	4	3	2	1	0	Reset Value
98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00000000b

Symbol **Function**

FE — Set SMOD0 = 1 to access FE bit.
0: No framing error
1: Framing Error. Set by receiver when an invalid stop bit is detected. This bit needs to be cleared by software.

SM0 — SMOD0 = 0 to access SM0 bit.
Serial Port Mode Bit 0

SM1 — Serial Port Mode Bit 1

SM0	SM1	Mode	Description	Baud Rate[1]
0	0	0	Shift Register	f_{OSC}/6 (6 clock mode) or f_{OSC}/12 (12 clock mode)
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	f_{OSC}/32 or f_{OSC}/16 (6 clock mode) or f_{OSC}/64 or f_{OSC}/32 (12 clock mode)
1	1	3	9-bit UART	Variable

1. f_{OSC} = oscillator frequency

SM2 — Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a given or broadcast address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received. In Mode 0, SM2 should be 0.

REN — Enables serial reception.
0: to disable reception.
1: to enable reception.

TB8 — The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.

RB8 — In Modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.

TI — Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission, Must be cleared by software.

RI — Receive interrupt flag. Set by hardware at the end of the8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

Timers/Counters

Timers

The device has three 16-bit registers that can be used as either timers or event counters. The three timers/counters are denoted Timer 0 (T0), Timer 1 (T1), and Timer 2 (T2). Each is designated a pair of 8-bit registers in the SFRs. The pair consists of a most significant (high) byte and least significant (low) byte. The respective registers are TL0, TH0, TL1, TH1, TL2, and TH2.

Timer Set-up

Refer to Table 9 for TMOD, TCON, and T2CON registers regarding timers T0, T1, and T2. The following tables provide TMOD values to be used to set up Timers T0, T1, and T2.

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set separately to turn the timer on.

Table 15: Timer/Counter 0

	Mode	Function	TMOD	
			Internal Control[1]	External Control[2]
Used as Timer	0	13-bit Timer	00H	08H
	1	16-bit Timer	01H	09H
	2	8-bit Auto-Reload	02H	0AH
	3	Two 8-bit Timers	03H	0BH
Used as Counter	0	13-bit Timer	04H	0CH
	1	16-bit Timer	05H	0DH
	2	8-bit Auto-Reload	06H	0EH
	3	Two 8-bit Timers	07H	0FH

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1. The Timer is turned ON/OFF by setting/clearing bit TR0 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on INT0# (P3.2) when TR0 = 1 (hardware control).

Table 16: Timer/Counter 1

	Mode	Function	TMOD	
			Internal Control[1]	External Control[2]
Used as Timer	0	13-bit Timer	00H	80H
	1	16-bit Timer	10H	90H
	2	8-bit Auto-Reload	20H	A0H
	3	Does not run	30H	B0H
Used as Counter	0	13-bit Timer	40H	C0H
	1	16-bit Timer	50H	D0H
	2	8-bit Auto-Reload	60H	E0H
	3	Not available	-	-

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1. The Timer is turned ON/OFF by setting/clearing bit TR1 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on INT1# (P3.3) when TR1 = 1 (hardware control).

If mode 1 is used, the stop bit takes the place of the 9th bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit. Note that mode 0 cannot be used. Setting SM2 bit in the SCON register in mode 0 will have no effect.

Each slave's individual address is specified by SFR SADDR. SFR SADEN is a mask byte that defines "don't care" bits to form the given address when combined with SADDR. See the example below:

Slave 1

SADDR	=	1111 0001
SADEN	=	1111 1010
GIVEN	=	1111 0X0X

Slave 2

SADDR	=	1111 0011
SADEN	=	1111 1001
GIVEN	=	1111 0XX1

Using the Given Address to Select Slaves

Any bits masked off by a 0 from SADEN become a "don't care" bit for the given address. Any bit masked off by a 1, becomes ANDED with SADDR. The "don't cares" provide flexibility in the user-defined addresses to address more slaves when using the given address.

Shown in the example above, Slave 1 has been given an address of 1111 0001 (SADDR). The SADEN byte has been used to mask off bits to a given address to allow more combinations of selecting Slave 1 and Slave 2. In this case for the given addresses, the last bit (LSB) of Slave 1 is a "don't care" and the last bit of Slave 2 is a 1. To communicate with Slave 1 and Slave 2, the master would need to send an address with the last bit equal to 1 (e.g. 1111 0001) since Slave 1's last bit is a don't care and Slave 2's last bit has to be a 1. To communicate with Slave 1 alone, the master would send an address with the last bit equal to 0 (e.g. 1111 0000), since Slave 2's last bit is a 1. See the table below for other possible combinations.

Select Slave 1 Only		
Slave 1	**Given Address**	**Possible Addresses**
	1111 0X0X	1111 0000 1111 0100

Select Slave 2 Only		
Slave 2	**Given Address**	**Possible Addresses**
	1111 0XX1	1111 0111 1111 0011

Select Slaves 1 & 2	
Slaves 1 & 2	**Possible Addresses**
	1111 0001 1111 0101

If the user added a third slave such as the example below:

Slave 3

SADDR	=	1111	1001
SADEN	=	1111	0101
GIVEN	=	1111	X0X1

Select Slave 3 Only		
Slave 2	**Given Address**	**Possible Addresses**
	1111 X0X1	1111 1011 1111 1001

The user could use the possible addresses above to select slave 3 only. Another combination could be to select slave 2 and 3 only as shown below.

Select Slaves 2 & 3 Only	
Slaves 2 & 3	**Possible Addresses**
	1111 0011

More than one slave may have the same SADDR address as well, and a given address could be used to modify the address so that it is unique.

Using the Broadcast Address to Select Slaves

Using the broadcast address, the master can communicate with all the slaves at once. It is formed by performing a logical OR of SADDR and SADEN with ‘0’s in the result treated as “don’t cares”.

Slave 1

1111 0001	=	SADDR
+1111 1010	=	SADEN
1111 1X11	=	Broadcast

“Don’t cares” allow for a wider range in defining the broadcast address, but in most cases, the broadcast address will be FFH.

On reset, SADDR and SADEN are “0”. This produces an given address of all “don’t cares” as well as a broadcast address of all “don’t cares.” This effectively disables Automatic Addressing mode and allows the microcontroller to function as a standard 8051, which does not make use of this feature.

SPI Transfer Formats

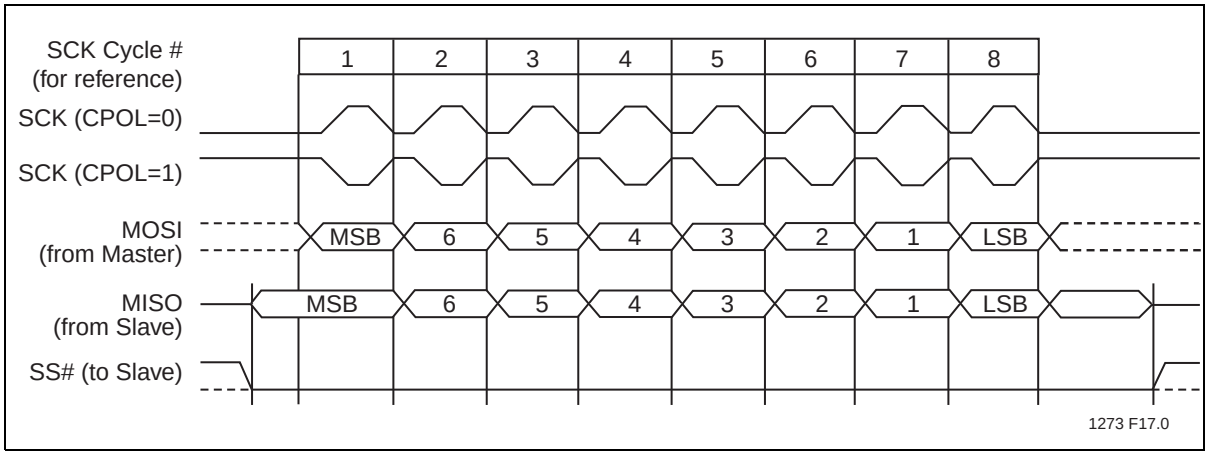

Figure 21: SPI Transfer Format with CPHA = 0

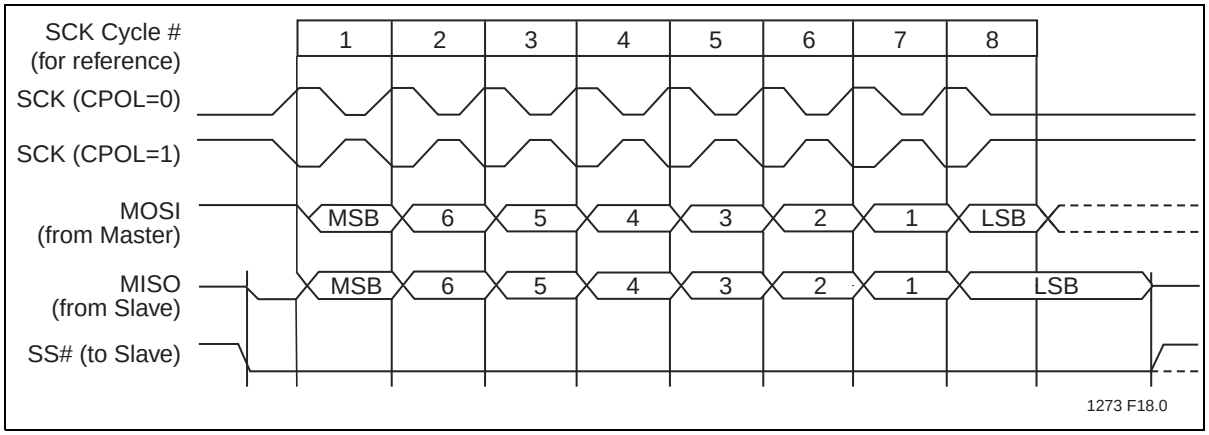

Figure 22: SPI Transfer Format with CPHA = 1

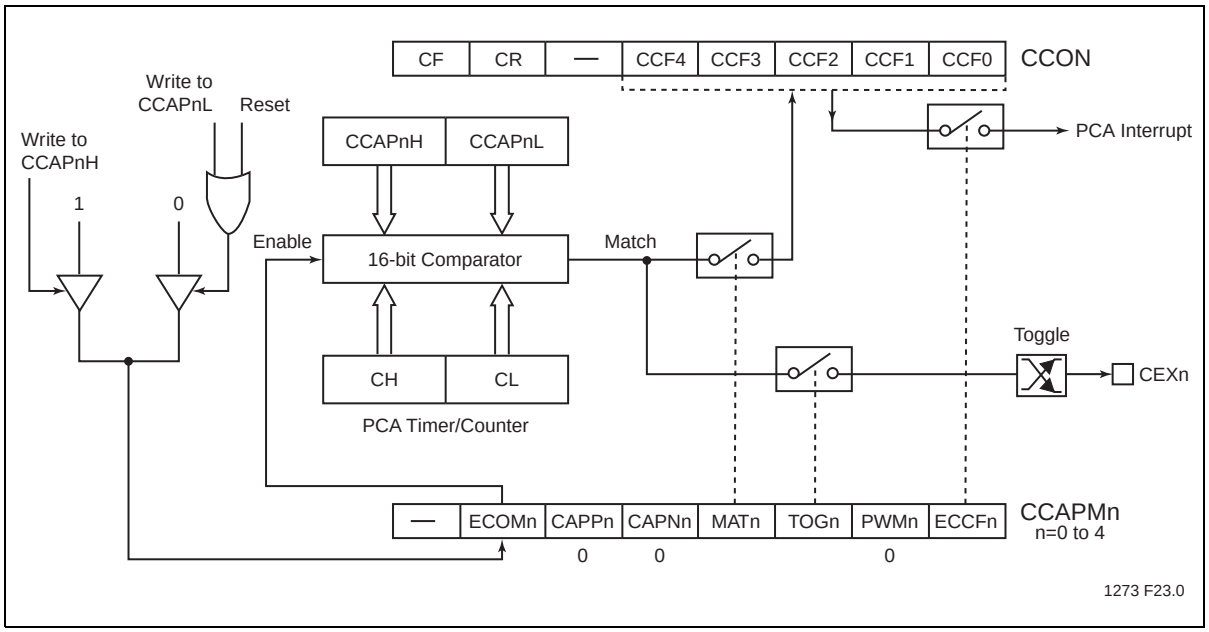

Figure 27: PCA High Speed Output Mode

Pulse Width Modulator

The Pulse Width Modulator (PWM) mode is used to generate 8-bit PWMs by comparing the low byte of the PCA timer (CL) with the low byte of the compare register (CCAPnL). When CL < CCAPnL the output is low. When CL ≥ CCAPnL the output is high. To activate this mode, the user must set the PWM and ECOM bits in the module's CCAPMn SFR. (See Figure 28 and Table 24)

In PWM mode, the frequency of the output depends on the source for the PCA timer. Since there is only one set of CH and CL registers, all modules share the PCA timer and frequency. Duty cycle of the output is controlled by the value loaded into the high byte (CCAPnH). Since writes to the CCAPnH register are asynchronous, a new value written to the high byte will not be shifted into CCAPnL for comparison until the next period of the output (when CL rolls over from 255 to 00).

To calculate values for CCAPnH for any duty cycle, use the following equation:

CCAPnH = 256(1 - Duty Cycle)

where CCAPnH is an 8-bit integer and Duty Cycle is a fraction.

Read Operation Under Lock Condition

The status of security bits SB1, SB2, and SB3 can be read when the read command is disabled by security lock. There are three ways to read the status.

1. External host mode: Read-back = 00H (locked)
2. IAP command: Read-back = previous SFDT data
3. MOVC: Read-back = FFH (blank)

Table 26: Security Lock Access Table

Level	SFST[7:5]	Source Address[1]	Target Address[2]	Byte-Verify Allowed		MOVC Allowed
				External Host[3]	IAP	516RDx
4	111b (hard lock on both blocks)	Block 0/1	Block 0/1	N	N	Y
			External	N/A	N/A	N
		External	Block 0/1	N	N	N
			External	N/A	N/A	N
3	011b/101b (hard lock on both blocks)	Block 0/1	Block 0/1	N	N	Y
			External	N/A	N/A	N
		External	Block 0/1	N	N	N
			External	N/A	N/A	Y
	001b/110b (Block 0 = SoftLock, Block 1 = hard lock)	Block 0	Block 0	N	N	Y
			Block 1	N	N	N
			External	N/A	N/A	N
		Block 1	Block 0	N	Y	Y
			Block 1	N	N	Y
			External	N/A	N/A	N
		External	Block 0/1	N	N	N
			External	N/A	N/A	Y
	010b (SoftLock on both blocks)	Block 0	Block 0	N	N	Y
			Block 1	N	Y	Y
			External	N/A	N/A	N
		Block 1	Block 0	N	Y	Y
			Block 1	N	N	Y
			External	N/A	N/A	N
		External	Block 0/1	N	N	N
			External	N/A	N/A	Y
2	100b (SoftLock on both blocks)	Block 0	Block 0	Y	N	Y
			Block 1	Y	Y	Y
			External	N/A	N/A	N
		Block 1	Block 0	Y	Y	Y
			Block 1	Y	N	Y
			External	N/A	N/A	N
		External	Block 0/1	Y	N	N
			External	N/A	N/A	Y

Table 26: Security Lock Access Table

Level	SFST[7:5]	Source Address[1]	Target Address[2]	Byte-Verify Allowed		MOVC Allowed
				External Host[3]	IAP	516RDx
1	000b (unlock)	Block 0	Block 0	Y	N	Y
			Block 1	Y	Y	Y
			External	N/A	N/A	N
		Block 1	Block 0	Y	Y	Y
			Block 1	Y	N	Y
			External	N/A	N/A	N
		External	Block 0/1	Y	Y	N
			External	N/A	N/A	Y

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1. Location of MOVC or IAP instruction
2. Target address is the location of the byte being read
3. External host Byte-Verify access does not depend on a source address.

Power-Saving Modes

The device provides two power saving modes of operation for applications where power consumption is critical. The two modes are idle and power-down, see Table 28.

Idle Mode

Idle mode is entered setting the IDL bit in the PCON register. In idle mode, the program counter (PC) is stopped. The system clock continues to run and all interrupts and peripherals remain active. The on-chip RAM and the special function registers hold their data during this mode.

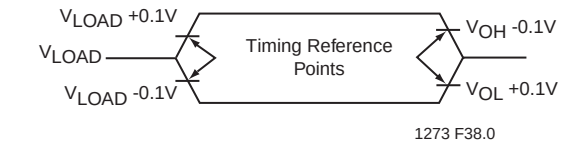
The device exits idle mode through either a system interrupt or a hardware reset. Exiting idle mode via system interrupt, the start of the interrupt clears the IDL bit and exits idle mode. After exit the Interrupt Service Routine, the interrupted program resumes execution beginning at the instruction immediately following the instruction which invoked the idle mode. A hardware reset starts the device similar to a power-on reset.

Power-down Mode

The power-down mode is entered by setting the PD bit in the PCON register. In the power-down mode, the clock is stopped and external interrupts are active for level sensitive interrupts only. SRAM contents are retained during power-down, the minimum V_{DD} level is 2.0V.

The device exits power-down mode through either an enabled external level sensitive interrupt or a hardware reset. The start of the interrupt clears the PD bit and exits power-down. Holding the external interrupt pin low restarts the oscillator, the signal must hold low at least 1024 clock cycles before bringing back high to complete the exit. Upon interrupt signal being restored to logic $V_{IH,}$ the first instruction of the interrupt service routine will execute. A hardware reset starts the device similar to power-on reset.

To exit properly out of power-down, the reset or external interrupt should not be executed before the V_{DD} line is restored to its normal operating voltage. Be sure to hold V_{DD} voltage long enough at its normal operating level for the oscillator to restart and stabilize (normally less than 10 ms).



For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. I_{OL}/I_{OH} = ± 20mA.

Figure 42: Float Waveform

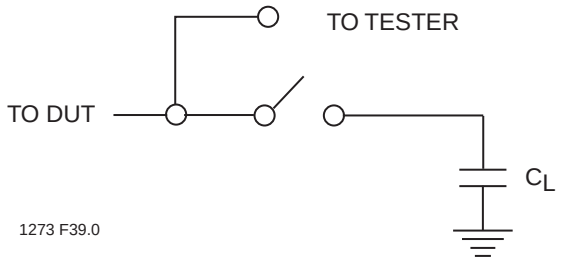
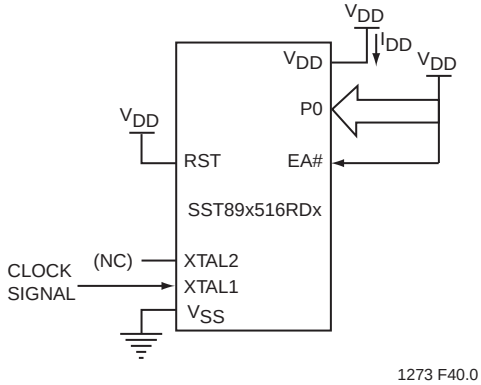
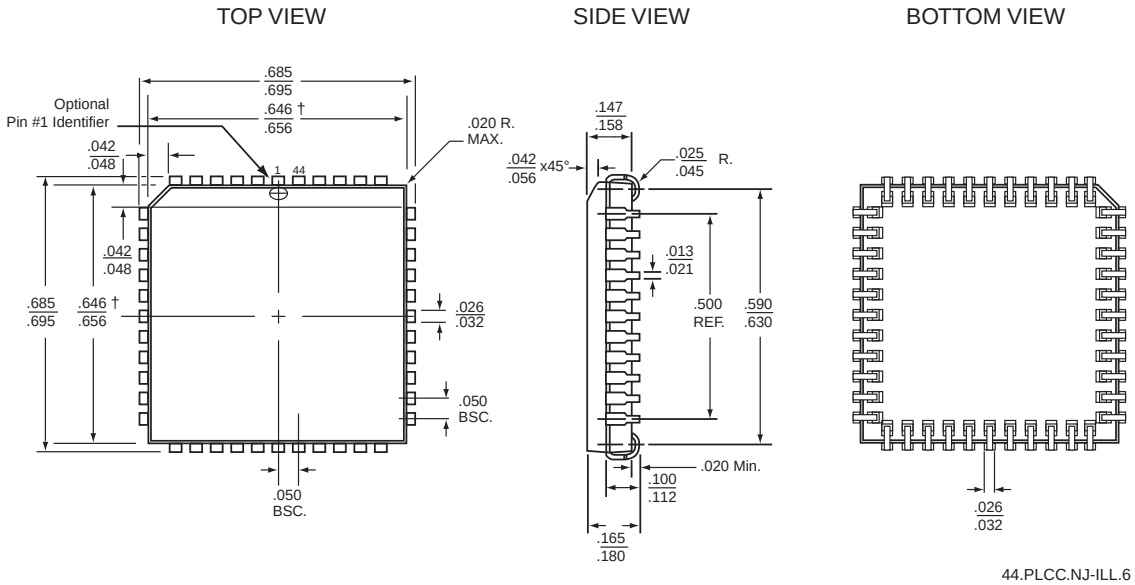


Figure 43: A Test Load Example



All other pins disconnected

Figure 44: I_{DD} Test Condition, Active Mode



Note:
1. Complies with JEDEC publication 95 MS-018 AC dimensions (except as noted), although some dimensions may be more stringent.
   † = JEDEC min is .650; SST min is *less*stringent
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.
4. Coplanarity: ± 4 mils.

Figure 49: 44-lead Plastic Lead Chip Carrier (PLCC)
SST Package Code: NJ

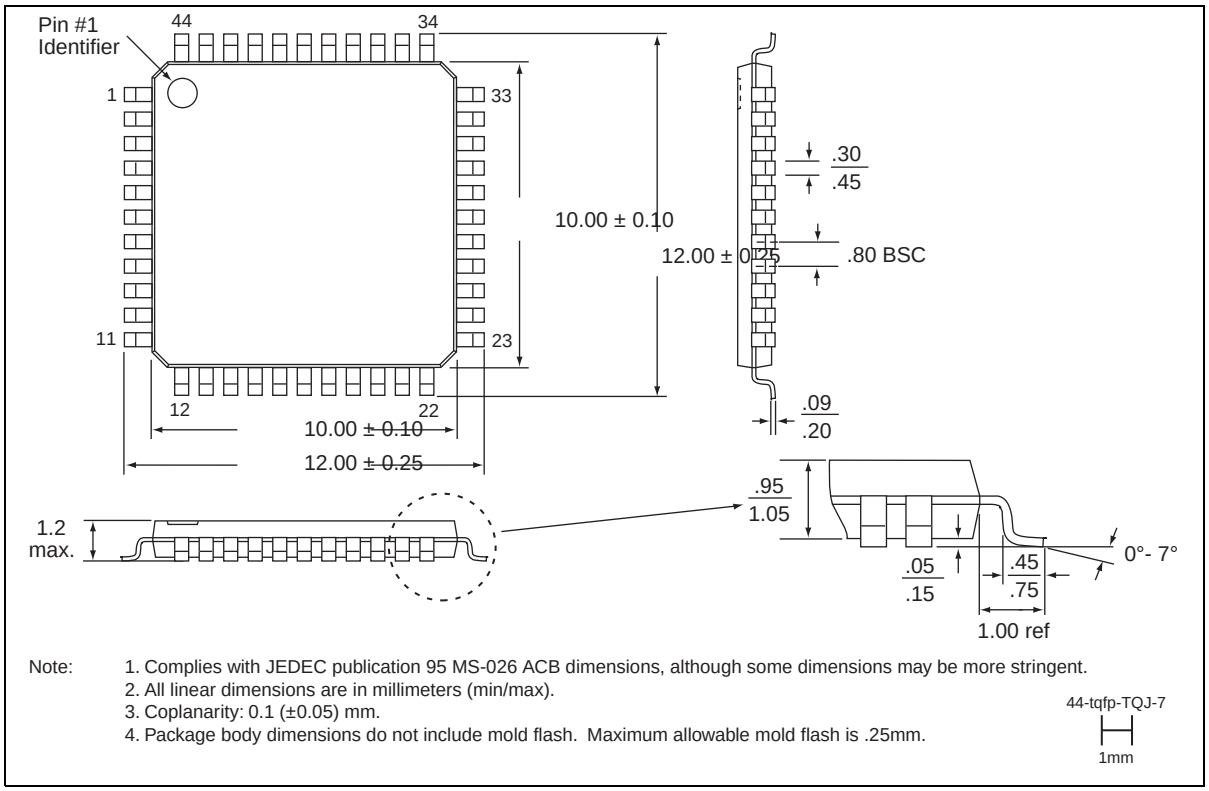


Figure 50: 44-lead Thin Quad Flat Pack (TQFP)
SST Package Code: TQJ