Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	36
Program Memory Size	72KB (72K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sst89v516rd2-33-i-nje-nxx

Functional Blocks

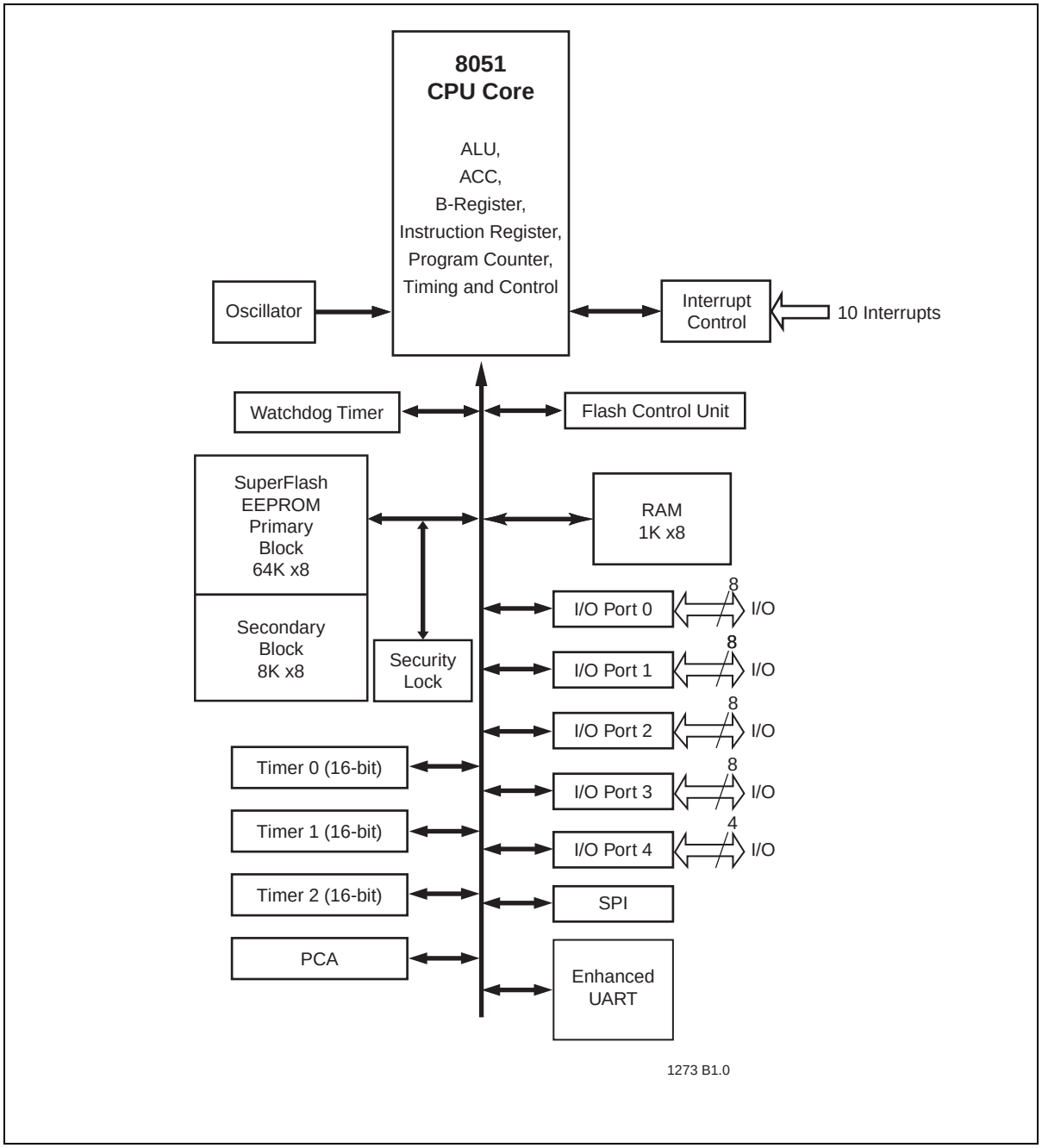


Figure 1: Functional Block Diagram

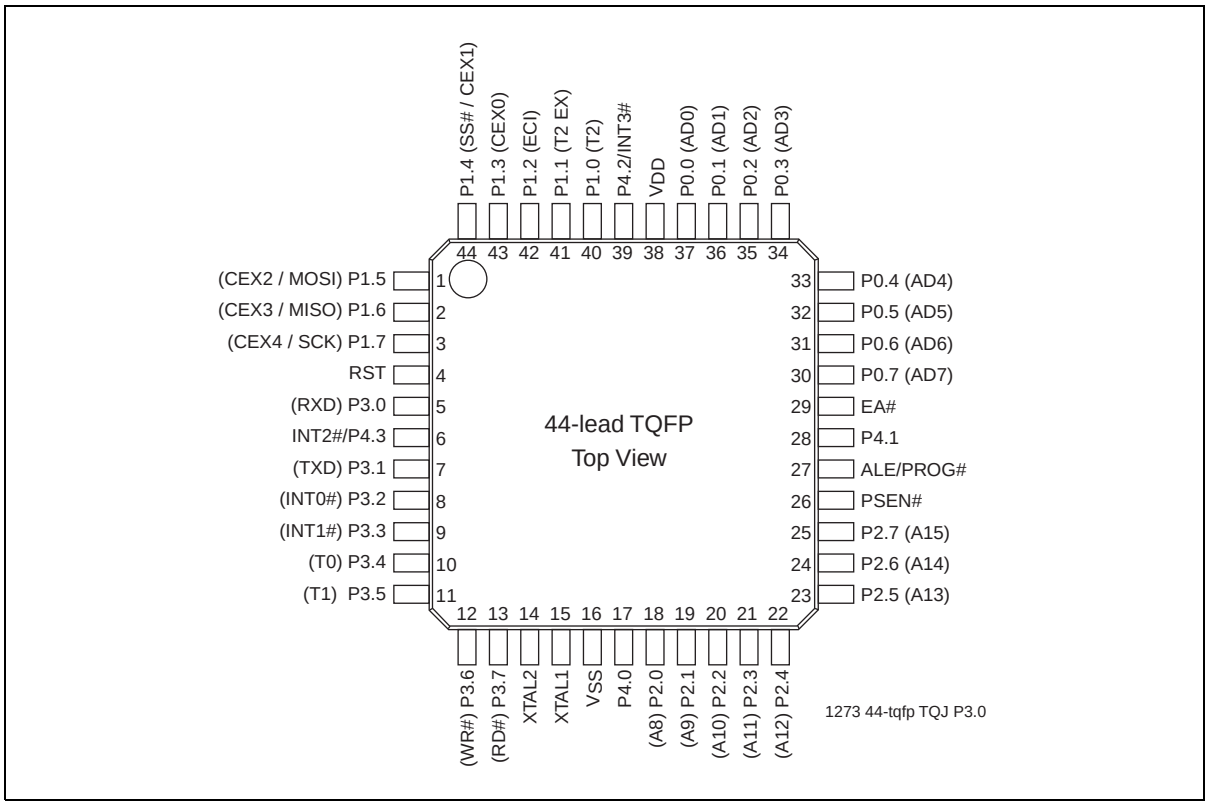


Figure 4: Pin Assignments for 44-lead TQFP

Table 6: CPU related SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	Reset Value
ACC[1]	Accumulator	E0H	ACC[7:0]								00H
B[1]	B Register	F0H	B[7:0]								00H
PSW[1]	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00H
SP	Stack Pointer	81H	SP[7:0]								07H
DPL	Data Pointer Low	82H	DPL[7:0]								00H
DPH	Data Pointer High	83H	DPH[7:0]								00H
IE[1]	Interrupt Enable	A8H	EA	EC	ET2	ES	ET1	EX1	ET0	EX0	00H
IEA[1]	Interrupt Enable A	E8H	-	-	-	-	EBO	-	-	-	xxxx0xxx b
IP[1]	Interrupt Priority Reg	B8H	-	PPC	PT2	PS	PT1	PX1	PT0	PX0	x0000000 b
IPH	Interrupt Priority Reg High	B7H	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	x0000000 b
IP1[1]	Interrupt Priority Reg A	F8H	-	-	-	-	PBO	PX3	PX2	-	xxxx0xxx b
IP1H	Interrupt Priority Reg A High	F7H	-	-	-	-	PBOH	PX3H	PX2H	-	xxxx0xxx b
PCON	Power Control	87H	SMOD1	SMOD0	BOF	POF	GF1	GF0	PD	IDL	00010000 b
AUXR	Auxiliary Reg	8EH	-	-	-	-	-	-	EXTRAM	AO	xxxxxxx0 0b
AUXR1	Auxiliary Reg 1	A2H	-	-	-	-	GF2	0	-	DPS	xxxx00x0 b
XICON	External Interrupt Control	AEH	-	EX3	IE3	IT3	0	EX2	IE2	IT2	00H

T0-0.0 25093

1. Bit Addressable SFRs

Table 9: Timer/Counters SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB LSB								Reset Value
TMOD	Timer/Counter Mode Control	89H	Timer 1				Timer 0				00H
			GATE	C/T#	M1	M0	GATE	C/T#	M1	M0	
TCON[1]	Timer/Counter Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
TH0	Timer 0 MSB	8CH	TH0[7:0]								00H
TL0	Timer 0 LSB	8AH	TL0[7:0]								00H
TH1	Timer 1 MSB	8DH	TH1[7:0]								00H
TL1	Timer 1 LSB	8BH	TL1[7:0]								00H
T2CON[1]	Timer / Counter 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#	00H
T2MOD	Timer2 Mode Control	C9H	-	-	-	-	-	-	T2OE	DCEN	xxxxxx00b
TH2	Timer 2 MSB	CDH	TH2[7:0]								00H
TL2	Timer 2 LSB	CCH	TL2[7:0]								00H
RCAP2H	Timer 2 Capture MSB	CBH	RCAP2H[7:0]								00H
RCAP2L	Timer 2 Capture LSB	CAH	RCAP2L[7:0]								00H

T0-0.0 25093

1. Bit Addressable SFRs

Table 10: Interface SFRs

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB							LSB	RESET Value
SBUF	Serial Data Buffer	99H	SBUF[7:0]								Indeterminate
SCON[1]	Serial Port Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SADDR	Slave Address	A9H	SADDR[7:0]								00H
SADEN	Slave Address Mask	B9H	SADEN[7:0]								00H
SPCR	SPI Control Register	D5H	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04H
SPSR	SPI Status Register	AAH	SPIF	WCOL							00H
SPDR	SPI Data Register	86H	SPDR[7:0]								00H
P0[1]	Port 0	80H	P0[7:0]								FFH
P1[1]	Port 1	90H	-	-	-	-	-	-	T2EX	T2	FFH
P2[1]	Port 2	A0H	P2[7:0]								FFH
P3[1]	Port 3	B0H	RD#	WR#	T1	T0	INT1#	INT0#	TXD	RXD	FFH
P4[2]	Port 4	A5H	1	1	1	1	P4.3	P4.2	P4.1	P4.0	FFH

T0-0.0 25093

1. Bit Addressable SFRs
2. P4 is similar to P1 and P3 ports

SuperFlash Address Registers (SFAH)

Location	7	6	5	4	3	2	1	0	Reset Value
B4H	SuperFlash High Order Byte Address Register								00H

Symbol	Function
SFAH	Mailbox register for interfacing with flash memory block. (High order address register).

SuperFlash Data Register (SFDT)

Location	7	6	5	4	3	2	1	0	Reset Value
B5H	SuperFlash Data Register								00H

Symbol	Function
SFDT	Mailbox register for interfacing with flash memory block. (Data register).

SuperFlash Status Register (SFST) (Read Only Register)

Location	7	6	5	4	3	2	1	0	Reset Value
B6H	SB1_i	SB2_i	SB3_i	-	EDC_i	FLASH_BUSY	-	-	xxxxx0xxb

Symbol	Function
SB1_i	Security Bit 1 status (inverse of SB1 bit)
SB2_i	Security Bit 2 status (inverse of SB2 bit)
SB3_i	Security Bit 3 status (inverse of SB3 bit) Please refer to Table 25 for security lock options.
EDC_i	Double Clock Status 0: 12 clocks per machine cycle 1: 6 clocks per machine cycle
FLASH_BUSY	Flash operation completion polling bit. 0: Device has fully completed the last IAP command. 1: Device is busy with flash operation.

Byte-Verify

The Byte-Verify command allows the user to verify that the device has correctly performed an Erase or Program command. Byte-Verify command returns the data byte in SFDT if the command is successful. The user is required to check that the previous flash operation has fully completed before issuing a Byte-Verify. Byte-Verify command execution time is short enough that there is no need to poll for command completion and no interrupt is generated.

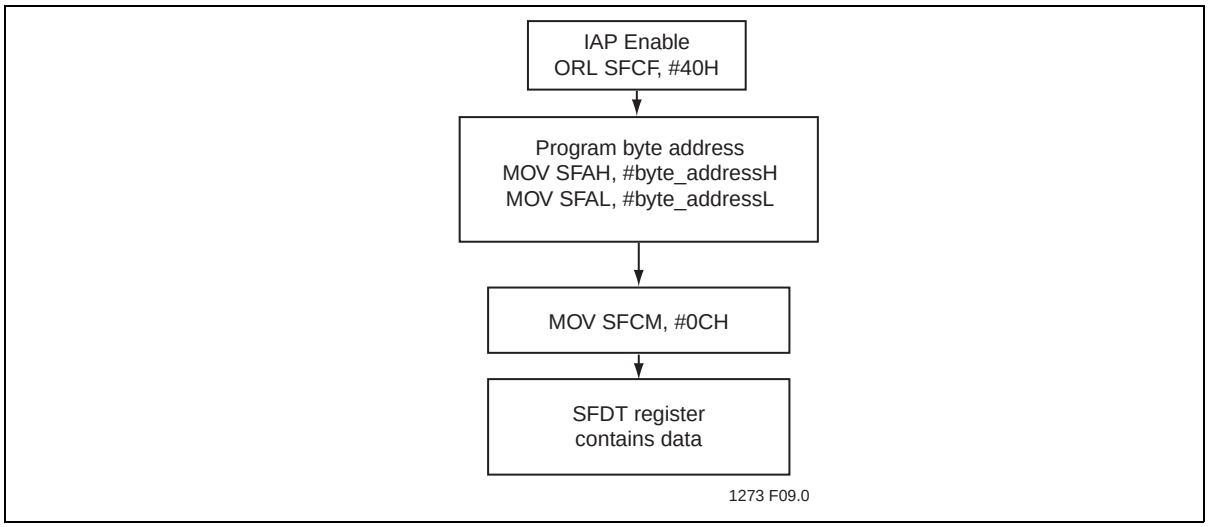


Figure 13: Byte Verify

Prog-SB3, Prog-SB2, Prog-SB1

Prog-SB3, Prog-SB2, Prog-SB1 commands are used to program the security bits (see Table 25). Completion of any of these commands, the security options will be updated immediately.

Security bits previously in un-programmed state can be programmed by these commands. Prog-SB3, Prog-SB2 and Prog-SB1 commands should only reside in Block 1 or external code memory.

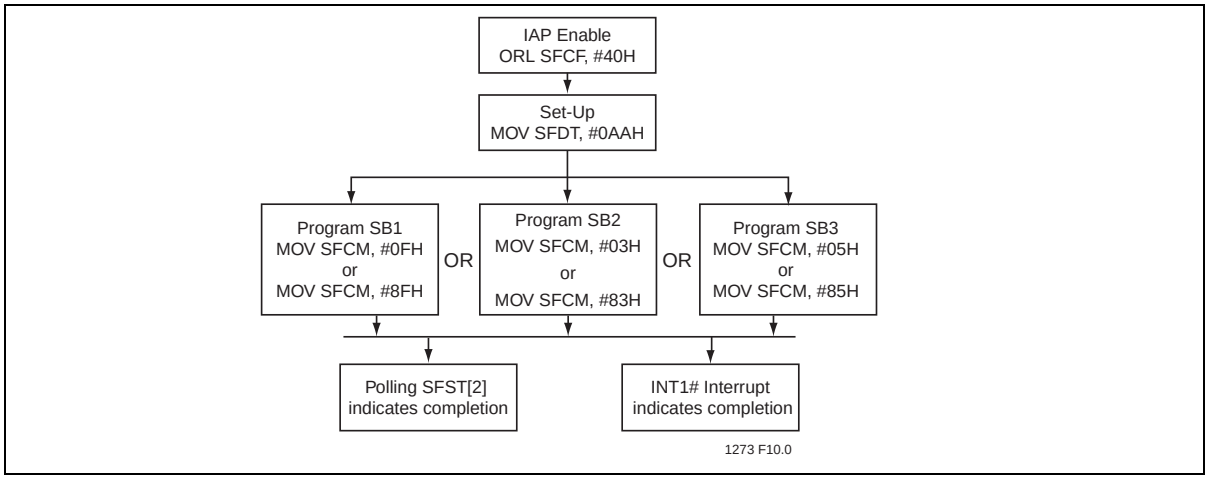


Figure 14: Prog-SB3, Prog-SB2, Prog-SB1

Timers/Counters

Timers

The device has three 16-bit registers that can be used as either timers or event counters. The three timers/counters are denoted Timer 0 (T0), Timer 1 (T1), and Timer 2 (T2). Each is designated a pair of 8-bit registers in the SFRs. The pair consists of a most significant (high) byte and least significant (low) byte. The respective registers are TL0, TH0, TL1, TH1, TL2, and TH2.

Timer Set-up

Refer to Table 9 for TMOD, TCON, and T2CON registers regarding timers T0, T1, and T2. The following tables provide TMOD values to be used to set up Timers T0, T1, and T2.

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set separately to turn the timer on.

Table 15: Timer/Counter 0

	Mode	Function	TMOD	
			Internal Control[1]	External Control[2]
Used as Timer	0	13-bit Timer	00H	08H
	1	16-bit Timer	01H	09H
	2	8-bit Auto-Reload	02H	0AH
	3	Two 8-bit Timers	03H	0BH
Used as Counter	0	13-bit Timer	04H	0CH
	1	16-bit Timer	05H	0DH
	2	8-bit Auto-Reload	06H	0EH
	3	Two 8-bit Timers	07H	0FH

T0-0.0 25093

1. The Timer is turned ON/OFF by setting/clearing bit TR0 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on INT0# (P3.2) when TR0 = 1 (hardware control).

Table 16: Timer/Counter 1

	Mode	Function	TMOD	
			Internal Control[1]	External Control[2]
Used as Timer	0	13-bit Timer	00H	80H
	1	16-bit Timer	10H	90H
	2	8-bit Auto-Reload	20H	A0H
	3	Does not run	30H	B0H
Used as Counter	0	13-bit Timer	40H	C0H
	1	16-bit Timer	50H	D0H
	2	8-bit Auto-Reload	60H	E0H
	3	Not available	-	-

T0-0.0 25093

1. The Timer is turned ON/OFF by setting/clearing bit TR1 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on INT1# (P3.3) when TR1 = 1 (hardware control).

Serial I/O

Full-Duplex, Enhanced UART

The device serial I/O port is a full-duplex port that allows data to be transmitted and received simultaneously in hardware by the transmit and receive registers, respectively, while the software is performing other tasks. The transmit and receive registers are both located in the Serial Data Buffer (SBUF) special function register. Writing to the SBUF register loads the transmit register, and reading from the SBUF register obtains the contents of the receive register.

The UART has four modes of operation which are selected by the Serial Port Mode Specifier (SM0 and SM1) bits of the Serial Port Control (SCON) special function register. In all four modes, transmission is initiated by any instruction that uses the SBUF register as a destination register. Reception is initiated in mode 0 when the Receive Interrupt (RI) flag bit of the Serial Port Control (SCON) SFR is cleared and the Reception Enable/ Disable (REN) bit of the SCON register is set. Reception is initiated in the other modes by the incoming start bit if the REN bit of the SCON register is set.

Framing Error Detection

Framing Error Detection is a feature, which allows the receiving controller to check for valid stop bits in modes 1, 2, or 3. Missing stops bits can be caused by noise in serial lines or from simultaneous transmission by two CPUs.

Framing Error Detection is selected by going to the PCON register and changing SMOD0 = 1 (see Figure 17). If a stop bit is missing, the Framing Error bit (FE) will be set. Software may examine the FE bit after each reception to check for data errors. After the FE bit has been set, it can only be cleared by software. Valid stop bits do not clear FE. When FE is enabled, RI rises on the stop bit, instead of the last data bit (see Figure 18 and Figure 19).

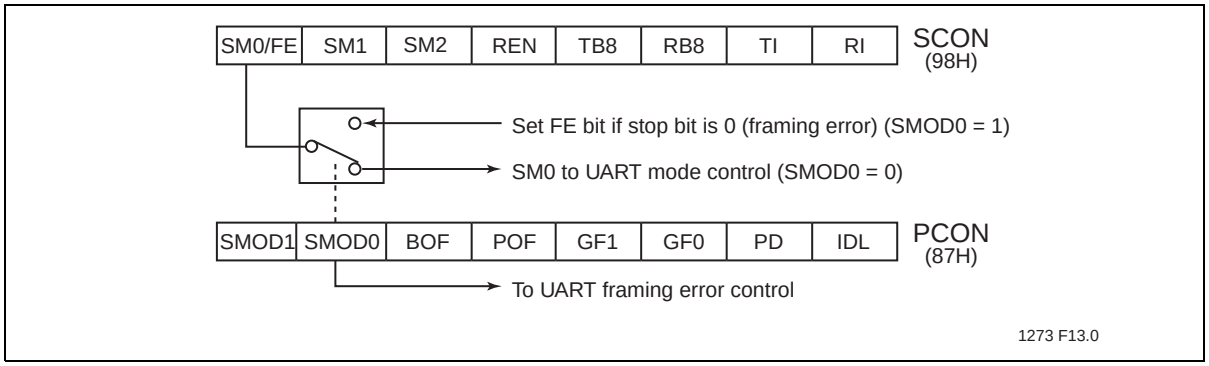


Figure 17: Framing Error Block Diagram

SPI Transfer Formats

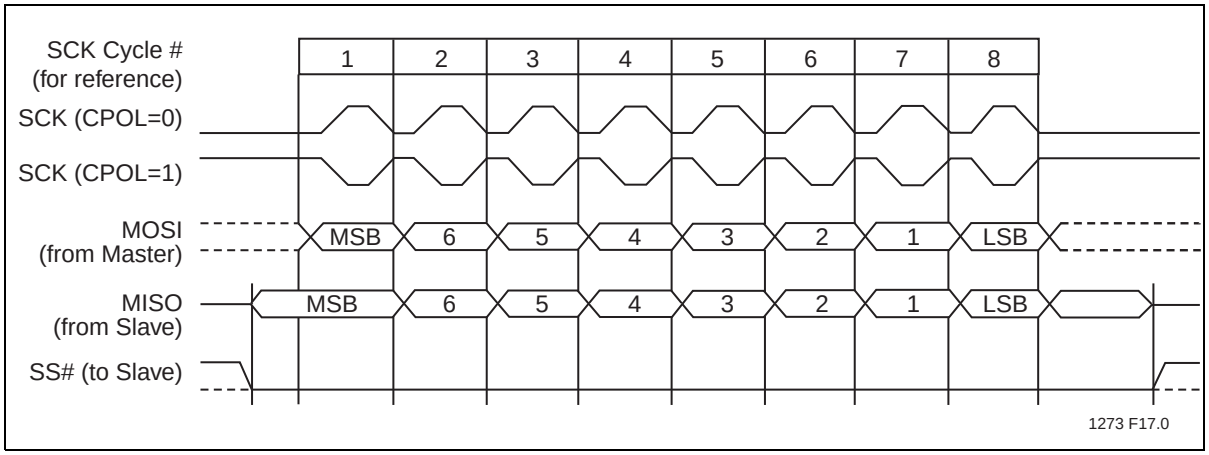


Figure 21: SPI Transfer Format with CPHA = 0

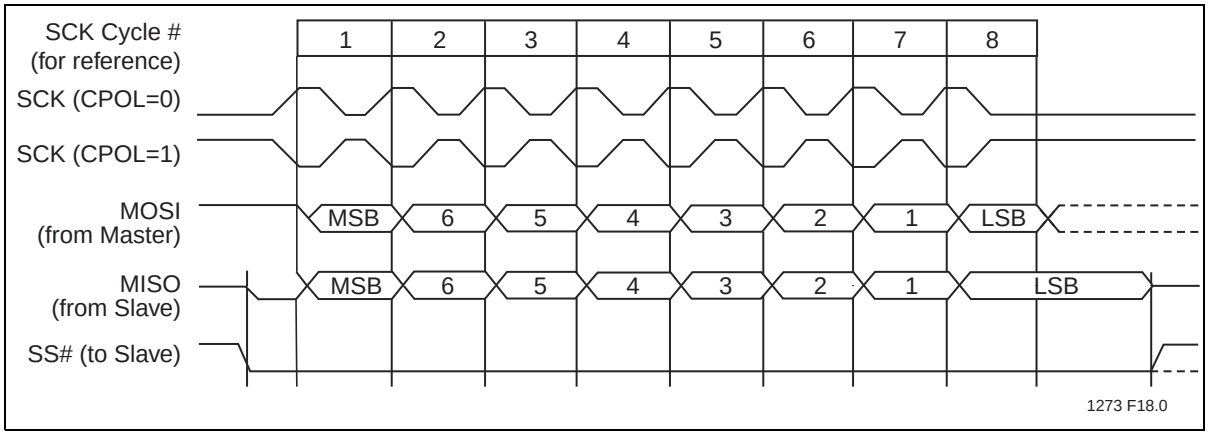


Figure 22: SPI Transfer Format with CPHA = 1

Capture Mode

Capture mode is used to capture the PCA timer/counter value into a module's capture registers (CCAPnH and CCAPnL). The capture will occur on a positive edge, negative edge, or both on the corresponding module's pin. To use one of the PCA modules in the capture mode, either one or both the CCAPM bits CAPN and CAPP for that module must be set. When a valid transition occurs on the CEX pin corresponding to the module used, the PCA hardware loads the 16-bit value of the PCA counter register (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set, then an interrupt will be generated. In the interrupt service routine, the 16-bit capture value must be saved in RAM before the next event capture occurs. If a subsequent capture occurred, the original capture values would be lost. After flag event flag has been set by hardware, the user must clear the flag in software. (See Figure 25)

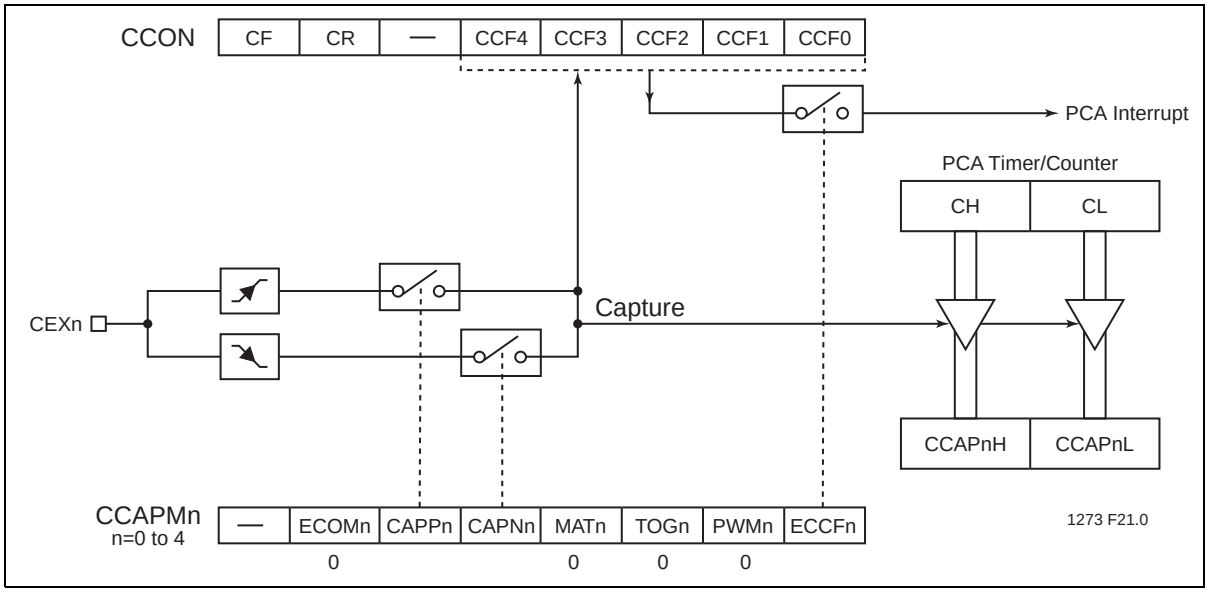


Figure 25: PCA Capture Mode

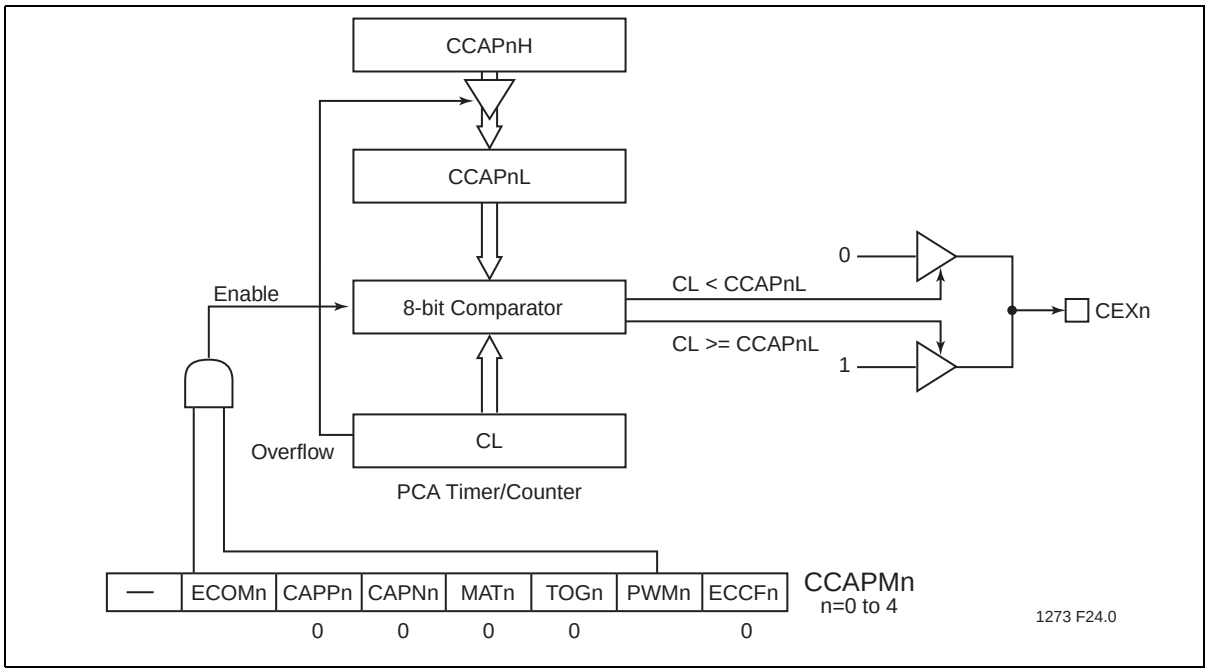


Figure 28: PCA Pulse Width Modulator Mode

Table 24: Pulse Width Modulator Frequencies

PCA Timer Mode	PWM Frequency	
	12 MHz	**16 MHz**
1/12 Oscillator Frequency	3.9 KHz	5.2 KHz
1/4 Oscillator Frequency	11.8 KHz	15.6 KHz
Timer 0 Overflow:		
8-bit	15.5 Hz	20.3 Hz
16-bit	0.06 Hz	0.08 Hz
8-bit Auto-Reload	3.9 KHz to 15.3 Hz	5.2 KHz to 20.3 Hz
External Input (Max)	5.9 KHz	7.8 KHz

T0-0.0 25093

Table 26: Security Lock Access Table

Level	SFST[7:5]	Source Address[1]	Target Address[2]	Byte-Verify Allowed		MOVC Allowed
				External Host[3]	IAP	516RDx
1	000b (unlock)	Block 0	Block 0	Y	N	Y
			Block 1	Y	Y	Y
			External	N/A	N/A	N
		Block 1	Block 0	Y	Y	Y
			Block 1	Y	N	Y
			External	N/A	N/A	N
		External	Block 0/1	Y	Y	N
			External	N/A	N/A	Y

T0-0.0 25093

1. Location of MOVC or IAP instruction
2. Target address is the location of the byte being read
3. External host Byte-Verify access does not depend on a source address.

Table 28: Power Saving Modes

Mode	Initiated by	State of MCU	Exited by
Idle Mode	Software (Set IDL bit in PCON) MOV PCON, #01H;	CLK is running. Interrupts, serial port and timers/counters are active. Program Counter is stopped. ALE and PSEN# signals at a HIGH level during Idle. All registers remain unchanged.	Enabled interrupt or hardware reset. Start of interrupt clears IDL bit and exits idle mode, after the ISR RETI instruction, program resumes execution beginning at the instruction following the one that invoked idle mode. A user could consider placing two or three NOP instructions after the instruction that invokes idle mode to eliminate any problems. A hardware reset restarts the device similar to a power-on reset.
Power-down Mode	Software (Set PD bit in PCON) MOV PCON, #02H;	CLK is stopped. On-chip SRAM and SFR data is maintained. ALE and PSEN# signals at a LOW level during power -down. External Interrupts are only active for level sensitive interrupts, if enabled.	Enabled external level sensitive interrupt or hardware reset. Start of interrupt clears PD bit and exits power-down mode, after the ISR RETI instruction program resumes execution beginning at the instruction following the one that invoked power-down mode. A user could consider placing two or three NOP instructions after the instruction that invokes power-down mode to eliminate any problems. A hardware reset restarts the device similar to a power-on reset.

T0-0.0 25093

System Clock and Clock Options

Clock Input Options and Recommended Capacitor Values for Oscillator

Shown in Figure 33 are the input and output of an internal inverting amplifier (XTAL1, XTAL2), which can be configured for use as an on-chip oscillator.

When driving the device from an external clock source, XTAL2 should be left disconnected and XTAL1 should be driven.

At start-up, the external oscillator may encounter a higher capacitive load at XTAL1 due to interaction between the amplifier and its feedback capacitance. However, the capacitance will not exceed 15 pF once the external signal meets the V_{IL} and V_{IH} specifications.

Crystal manufacturer, supply voltage, and other factors may cause circuit performance to differ from one application to another. C1 and C2 should be adjusted appropriately for each design. Table 29, shows the typical values for C1 and C2 vs. crystal type for various frequencies

Table 29: Recommended Values for C1 and C2 by Crystal Type

Crystal	C1 = C2
Quartz	20-30pF
Ceramic	40-50pF

T0-0.0 25093

More specific information about on-chip oscillator design can be found in the ***FlashFlex Oscillator Circuit Design Considerations*** application note.

Clock Doubling Option

By default, the device runs at 12 clocks per machine cycle (x1 mode). The device has a clock doubling option to speed up to 6 clocks per machine cycle. Please refer to Table 30 for detail.

Clock double mode can be enabled either via the external host mode or the IAP mode. Please refer to Table 14 for the IAP mode enabling commands (When set, the EDC# bit in SFST register will indicate 6 clock mode.).

The clock double mode is only for doubling the internal system clock and the internal flash memory, i.e. EA#=1. To access the external memory and the peripheral devices, careful consideration must be taken. Also note that the crystal output (XTAL2) will not be doubled.

Table 37: DC Electrical Characteristics for SST89V516RDx
T_A = -40°C to +85°C; V_{DD} = 2.7-3.6V; V_{SS} = 0V

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Voltage	2.7 < V_{DD} < 3.6	-0.5	0.7	V
V_{IH}	Input High Voltage	2.7 < V_{DD} < 3.6	0.2V_{DD} + 0.9	V_{DD} + 0.5	V
V_{IH1}	Input High Voltage (XTAL1, RST)	2.7 < V_{DD} < 3.6	0.7V_{DD}	V_{DD} + 0.5	V
V_{OL}	Output Low Voltage (Ports 1.5, 1.6, 1.7)	V_{DD} = 2.7V			
		I_{OL} = 16mA		1.0	V
V_{OL}	Output Low Voltage (Ports 1, 2, 3)[1]	V_{DD} = 2.7V			
		I_{OL} = 100µA[2]		0.3	V
		I_{OL} = 1.6mA[2]		0.45	V
		I_{OL} = 3.5mA[2]		1.0	V
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#)[1,3]	V_{DD} = 2.7V			
		I_{OL} = 200µA[2]		0.3	V
		I_{OL} = 3.2mA[2]		0.45	V
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, PSEN#)[4]	V_{DD} = 2.7V			
		I_{OH} = -10µA	V_{DD} - 0.3		V
		I_{OH} = -30µA	V_{DD} - 0.7		V
		I_{OH} = -60µA	V_{DD} - 1.5		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)[4]	V_{DD} = 2.7V			
		I_{OH} = -200µA	V_{DD} - 0.3		V
		I_{OH} = -3.2mA	V_{DD} - 0.7		V
V_{BOD}	Brown-out Detection Voltage		2.35	2.55	V
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V_{IN} = 0.4V		-75	µA
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3)[5]	V_{IN} = 2V		-650	µA
I_{LI}	Input Leakage Current (Port 0)	0.45 < V_{IN} < V_{DD}-0.3		±10	µA
R_{RST}	RST Pull-down Resistor			225	KΩ
C_{IO}	Pin Capacitance[6]	@ 1 MHz, 25°C		15	pF
I_{DD}	Power Supply Current IAP Mode @ 33 MHz			47	mA
	Active Mode @ 33 MHz			30	mA
	Idle Mode @ 33 MHz			21	mA
	Power-down Mode (min. V_{DD} = 2V)	T_A = 0°C to +70°C		45	µA
		T_A = -40°C to +85°C		55	µA

T0-0.1 25093

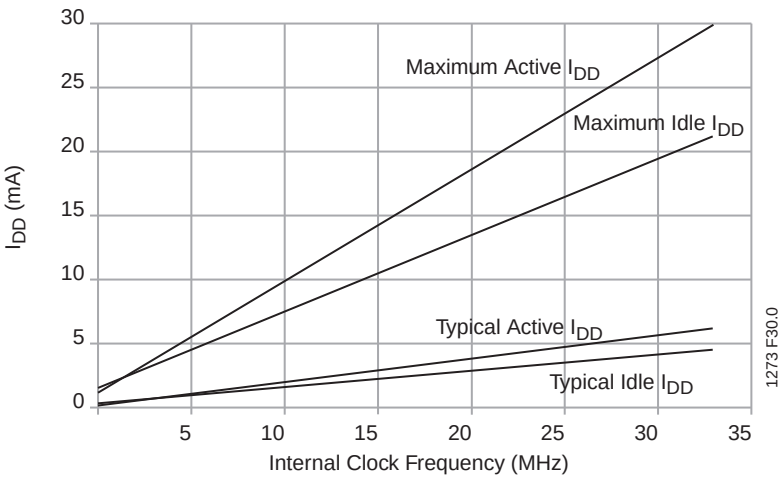


Figure 34: I_{DD} vs. Frequency for 3V SST89V516RDx

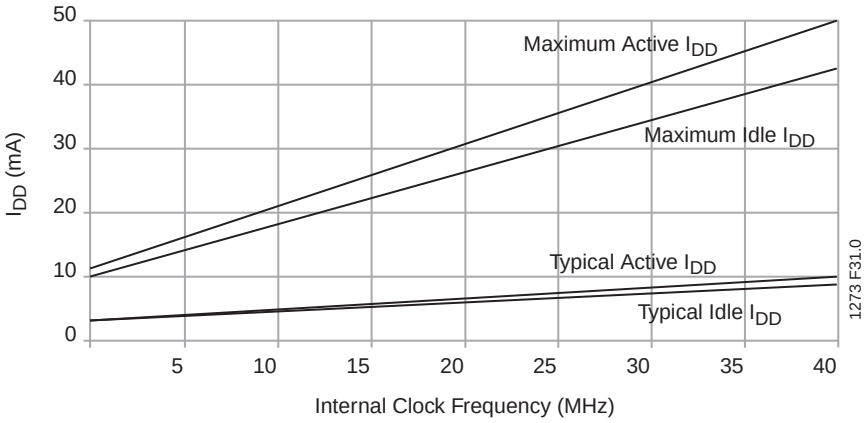


Figure 35: I_{DD} vs. Frequency for 5V SST89E516RDx

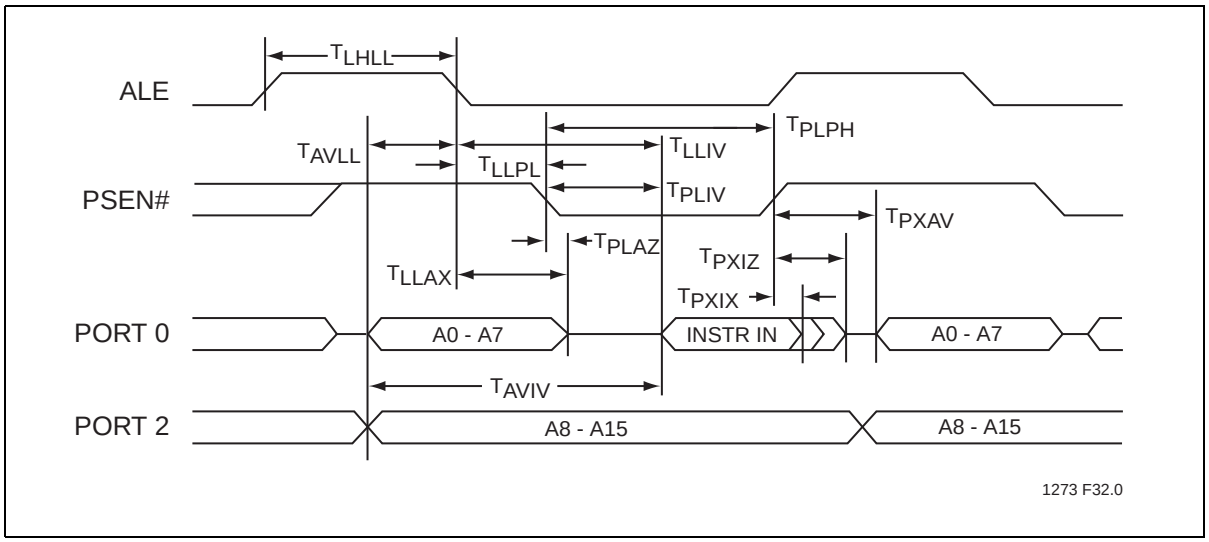


Figure 36: External Program Memory Read Cycle

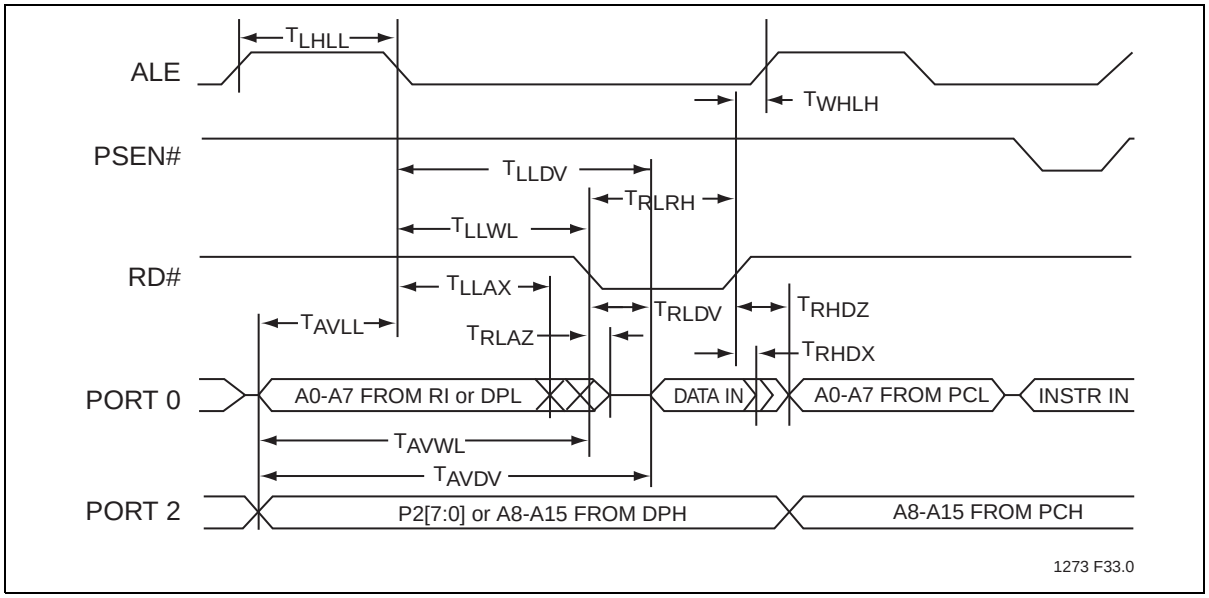


Figure 37: External Data Memory Read Cycle

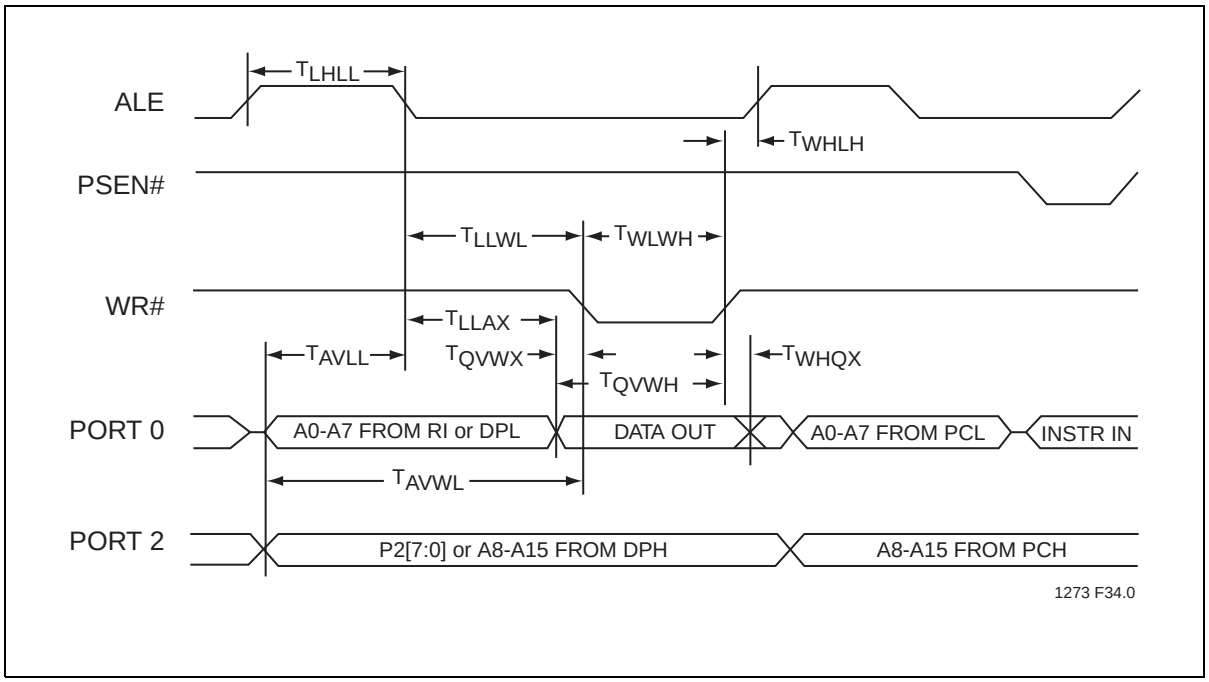


Figure 38: External Data Memory Write Cycle

Table 39: External Clock Drive

Symbol	Parameter	Oscillator						Units
		12MHz		40MHz		Variable		
		Min	Max	Min	Max	Min	Max	
$1/T_{CLCL}$	Oscillator Frequency					0	40	MHz
T_{CLCL}		83		25				ns
T_{CHCX}	High Time			8.75		$0.35T_{CLCL}$	$0.65T_{CLCL}$	ns
T_{CLCX}	Low Time			8.75		$0.35T_{CLCL}$	$0.65T_{CLCL}$	ns
T_{CLCH}	Rise Time		20		10			ns
T_{CHCL}	Fall Time		20		10			ns

T0-0.0 25093

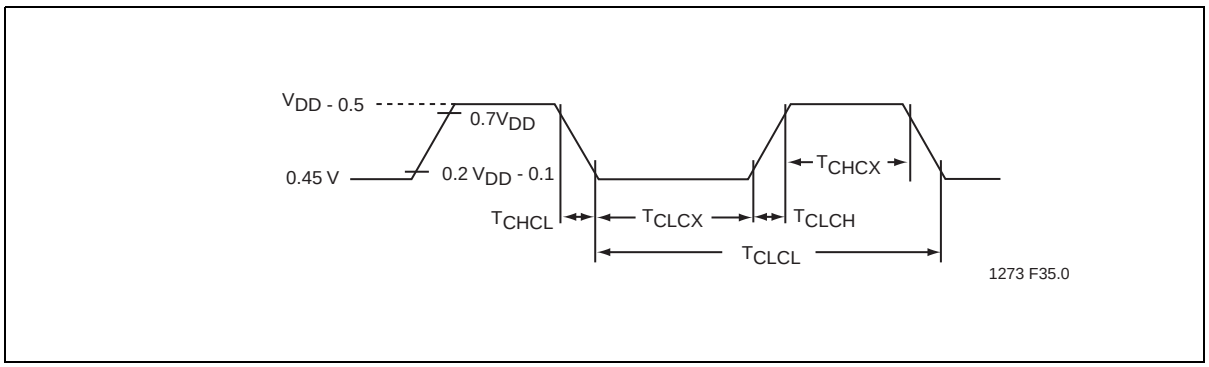
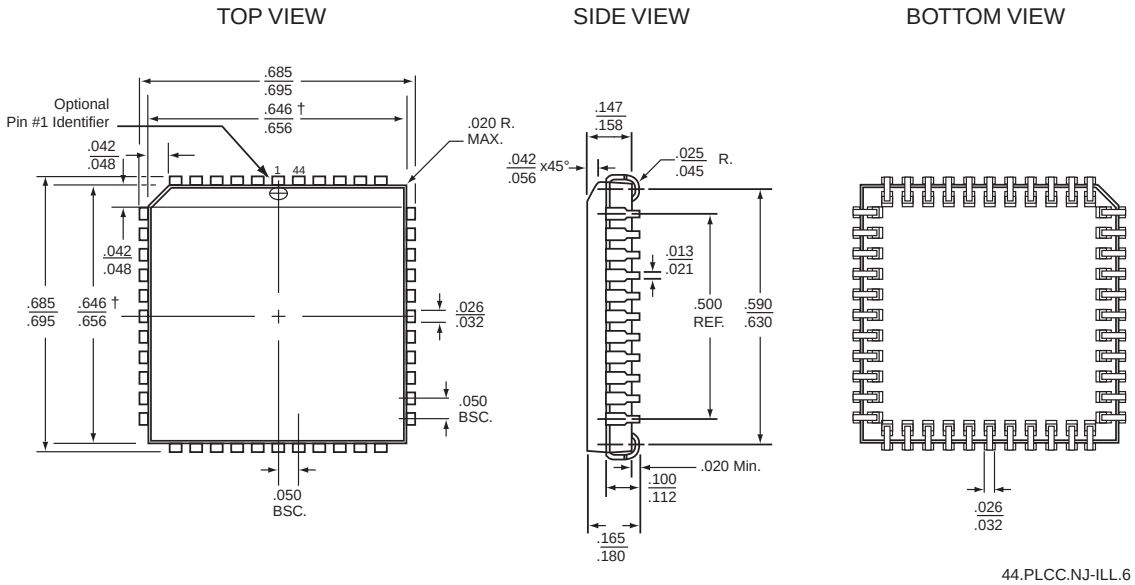


Figure 39: External Clock Drive Waveform



Note:
1. Complies with JEDEC publication 95 MS-018 AC dimensions (except as noted), although some dimensions may be more stringent.
   † = JEDEC min is .650; SST min is *less*stringent
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.
4. Coplanarity: ± 4 mils.

Figure 49: 44-lead Plastic Lead Chip Carrier (PLCC)
SST Package Code: NJ