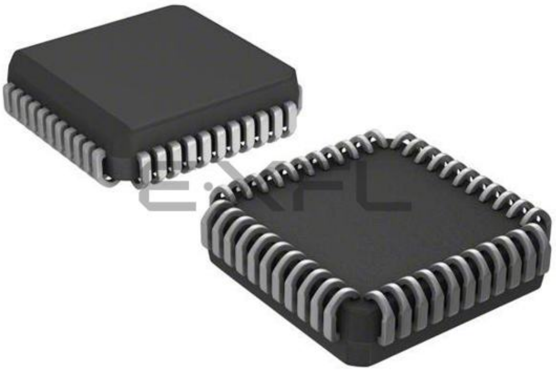
Microchip Technology - SST89V516RD2-33-I-NJE Datasheet



What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	36
Program Memory Size	72KB (72K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sst89v516rd2-33-i-nje

Product Description

The SST89E516RDx and SST89V516RDx are members of the FlashFlex family of 8-bit microcontroller products designed and manufactured with SST's patented and proprietary SuperFlash CMOS semiconductor process technology. The split-gate cell design and thick-oxide tunneling injector offer significant cost and reliability benefits for SST's customers. The devices use the 8051 instruction set and are pin-for-pin compatible with standard 8051 microcontroller devices.

The devices come with 72 KByte of on-chip flash EEPROM program memory which is partitioned into 2 independent program memory blocks. The primary Block 0 occupies 64 KByte of internal program memory space and the secondary Block 1 occupies 8 KByte of internal program memory space.

The 8-KByte secondary block can be mapped to the lowest location of the 64 KByte address space; it can also be hidden from the program counter and used as an independent EEPROM-like data memory.

In addition to the 72 KByte of EEPROM program memory on-chip and 1024 x8 bits of on-chip RAM, the devices can address up to 64 KByte of external program memory and up to 64 KByte of external RAM.

The flash memory blocks can be programmed via a standard 87C5x OTP EPROM programmer fitted with a special adapter and the firmware for SST's devices. During power-on reset, the devices can be configured as either a slave to an external host for source code storage or a master to an external host for an in-application programming (IAP) operation. The devices are designed to be programmed in-system and in-application on the printed circuit board for maximum flexibility. The devices are pre-programmed with an example of the bootstrap loader in the memory, demonstrating the initial user program code loading or subsequent user code updating via the IAP operation. The sample bootstrap loader is available for the user's reference and convenience only; SST does not guarantee its functionality or usefulness. Chip-Erase or Block-Erase operations will erase the pre-programmed sample code.

Functional Blocks

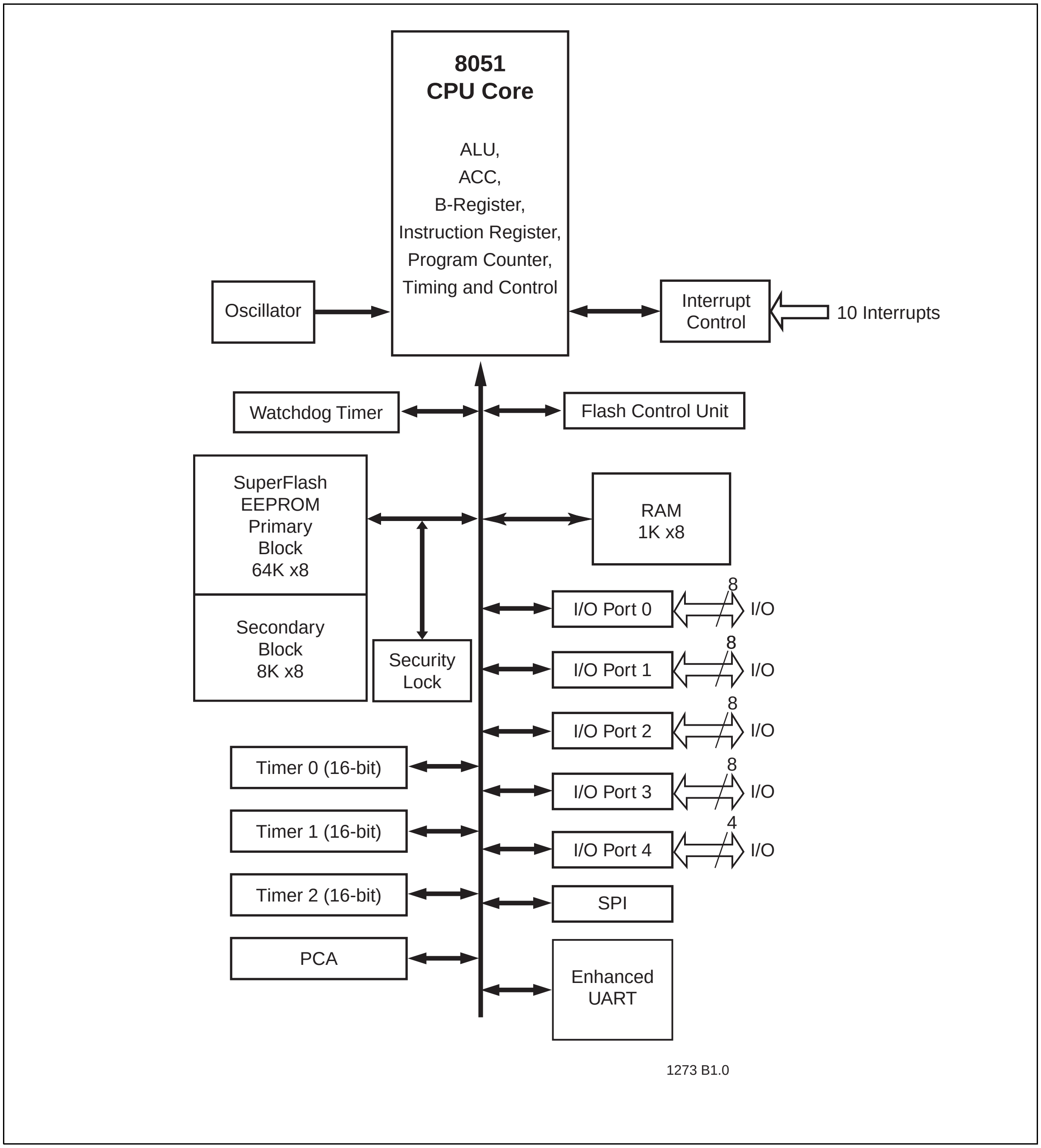


Figure 1: Functional Block Diagram

Pin Assignments

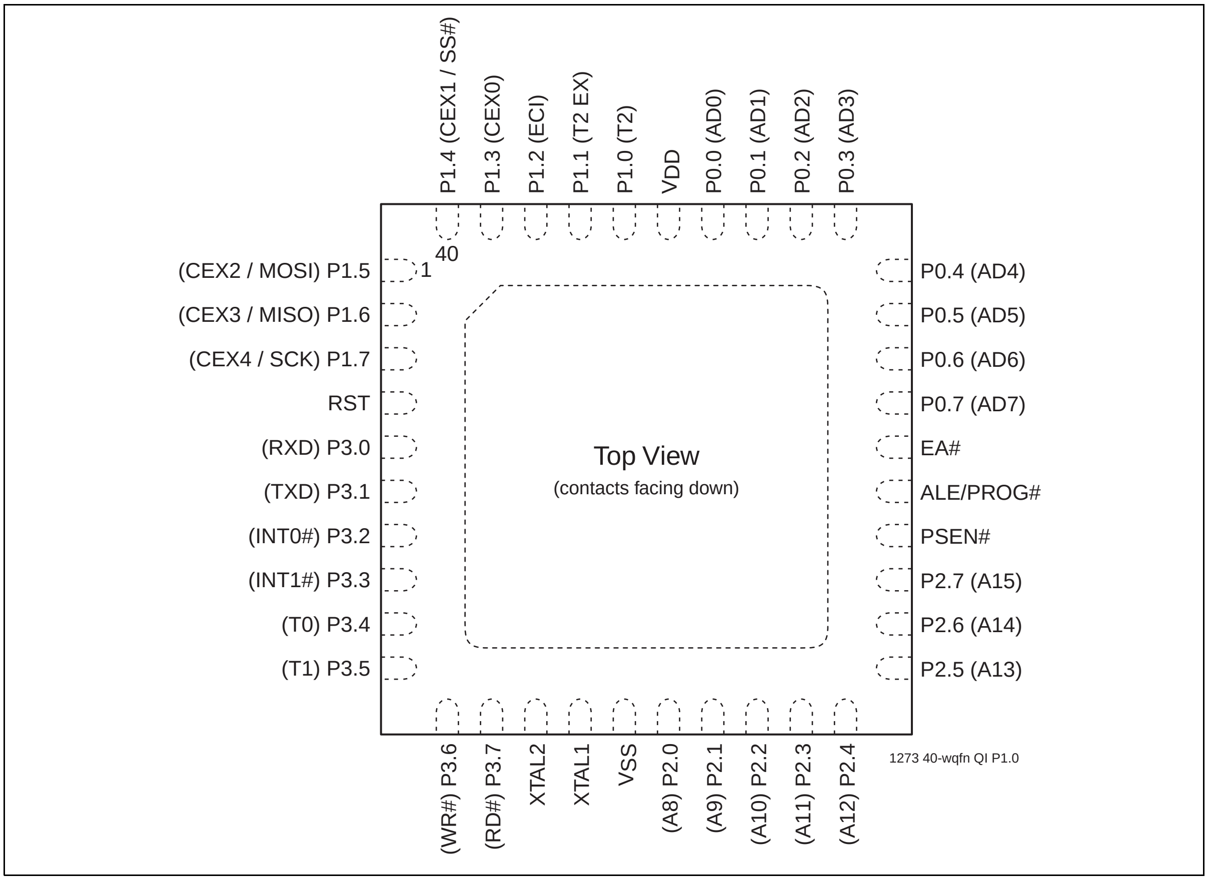


Figure 2: Pin Assignments for 40-Contact WQFN

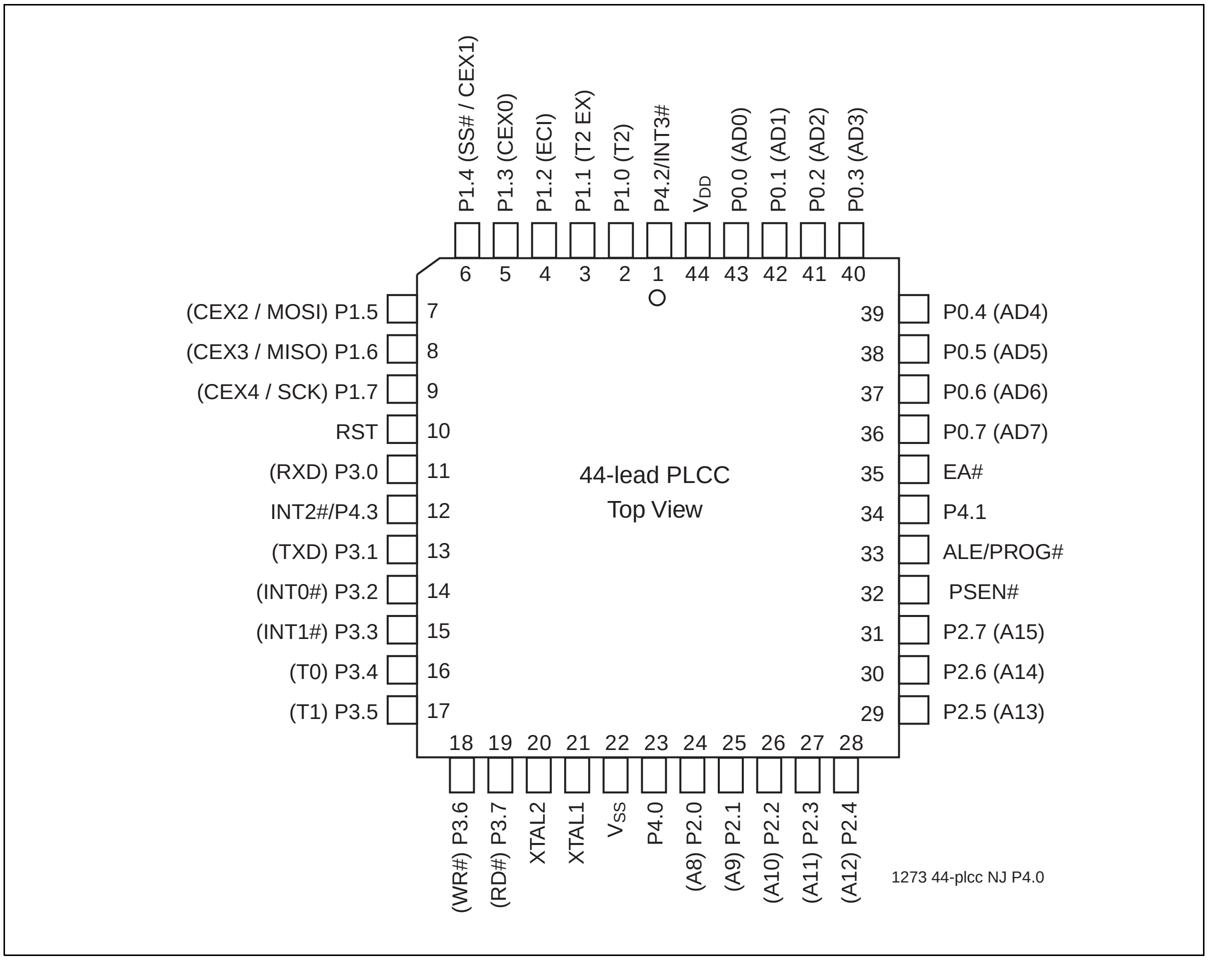


Figure 5: Pin Assignments for 44-lead PLCC

Pin Descriptions

Table 1: Pin Descriptions (1 of 3)

Symbol	Type[1]	Name and Functions
P0[7:0]	I/O	**Port 0:** Port 0 is an 8-bit open drain bi-directional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins float that have ‘1’s written to them, and in this state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external memory. In this application, it uses strong internal pull-ups when transitioning to $V_{OH.}$ Port 0 also receives the code bytes during the external host mode programming, and outputs the code bytes during the external host mode verification. External pull-ups are required during program verification.
P1[7:0]	I/O with internal pull-ups	**Port 1:** Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins are pulled high by the internal pull-ups when “1”s are written to them and can be used as inputs in this state. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. P1[5, 6, 7] have high current drive of 16 mA. Port 1 also receives the low-order address bytes during the external host mode programming and verification.
P1[0]	I/O	**T2:** External count input to Timer/Counter 2 or Clock-out from Timer/Counter 2
P1[1]	I	**T2EX:** Timer/Counter 2 capture/reload trigger and direction control
P1[2]	I	**ECI:** PCA Timer/Counter External Input: This signal is the external clock input for the PCA timer/counter.
P1[3]	I/O	**CEX0:** Compare/Capture Module External I/O Each compare/capture module connects to a Port 1 pin for external I/O. When not used by the PCA, this pin can handle standard I/O.
P1[4]	I/O	**SS#:** Master Input or Slave Output for SPI. **OR** **CEX1:** Compare/Capture Module External I/O
P1[5]	I/O	**MOSI:** Master Output line, Slave Input line for SPI **OR** **CEX2:** Compare/Capture Module External I/O
P1[6]	I/O	**MISO:** Master Input line, Slave Output line for SPI **OR** **CEX3:** Compare/Capture Module External I/O
P1[7]	I/O	**SCK:** Master clock output, slave clock input line for SPI **OR** **CEX4:** Compare/Capture Module External I/O
P2[7:0]	I/O with internal pull-up	**Port 2:** Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. Port 2 pins are pulled high by the internal pull-ups when “1”s are written to them and can be used as inputs in this state. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 sends the high-order address byte during fetches from external Program memory and during accesses to external Data Memory that use 16-bit address (MOVX@DPTR). In this application, it uses strong internal pull-ups when transitioning to V_{OH}. Port 2 also receives some control signals and high-order address bits during the external host mode programming and verification.

Program Memory Block Switching

The program memory block switching feature of the device allows either Block 1 or the lowest 8 KByte of Block 0 to be used for the lowest 8 KByte of the program address space. SFCF[1:0] controls program memory block switching.

Table 2: SFCF Values for Program Memory Block Switching

SFCF[1:0]	Program Memory Block Switching
01, 10, 11	Block 1 is not visible to the program counter (PC). Block 1 is reachable only via in-application programming from 0000H - 1FFFH.
00	Block 1 is overlaid onto the low 8K of the program address space; occupying address locations 0000H - 1FFFH. When the PC falls within 0000H - 1FFFH, the instruction will be fetched from Block 1 instead of Block 0. Outside of 0000H - 1FFFH, Block 0 is used. Locations 0000H - 1FFFH of Block 0 are reachable through in-application programming.

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Reset Configuration of Program Memory Block Switching

Program memory block switching is initialized after reset according to the state of the Start-up Configuration bit SC0. The SC0 bit is programmed via an external host mode command or an IAP Mode command. See Table 14.

Once out of reset, the SFCF[0] bit can be changed dynamically by the program for desired effects. Changing SFCF[0] will not change the SC0 bit.

Caution must be taken when dynamically changing the SFCF[0] bit. Since this will cause different physical memory to be mapped to the logical program address space. The user must avoid executing block switching instructions within the address range 0000H to 1FFFH.

Table 3: SFCF Values Under Different Reset Conditions

	State of SFCF[1:0] after:		
SC0[1]	Power-on or External Reset	WDT Reset or Brown-out Reset	Software Reset
U (1)	00 (default)	x0	10
P (0)	01	x1	11

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1. P = Programmed (Bit logic state = 0),
U = Unprogrammed (Bit logic state = 1)

Data RAM Memory

The data RAM has 1024 bytes of internal memory. The RAM can be addressed up to 64KB for external data memory.

high-order eight address bits (DPH), and Port 0 multiplexes the low order eight address bits (DPL) with data. Both MOVX @Ri and MOVX @DPTR generates the necessary read and write signals (P3.6 - WR# and P3.7 - RD#) for external memory use. Table 4 shows external data memory RD#, WR# operation with EXTRAM bit.

The stack pointer (SP) can be located anywhere within the 256 bytes of internal RAM (lower 128 bytes and upper 128 bytes). The stack pointer may not be located in any part of the expanded RAM.

Table 4: External Data Memory RD#, WR# with EXTRAM bit

	MOVX @DPTR, A or MOVX A, @DPTR		**MOVX @Ri, A or MOVX A, @Ri**
AUXR	**ADDR < 0300H**	**ADDR >= 0300H**	**ADDR = Any**
EXTRAM = 0	RD# / WR# not asserted	RD# / WR# asserted	RD# / WR# not asserted[1]
EXTRAM = 1	RD# / WR# asserted	RD# / WR# asserted	RD# / WR# asserted

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1. Access limited to ERAM address within 0 to 0FFH; cannot access 100H to 02FFH.

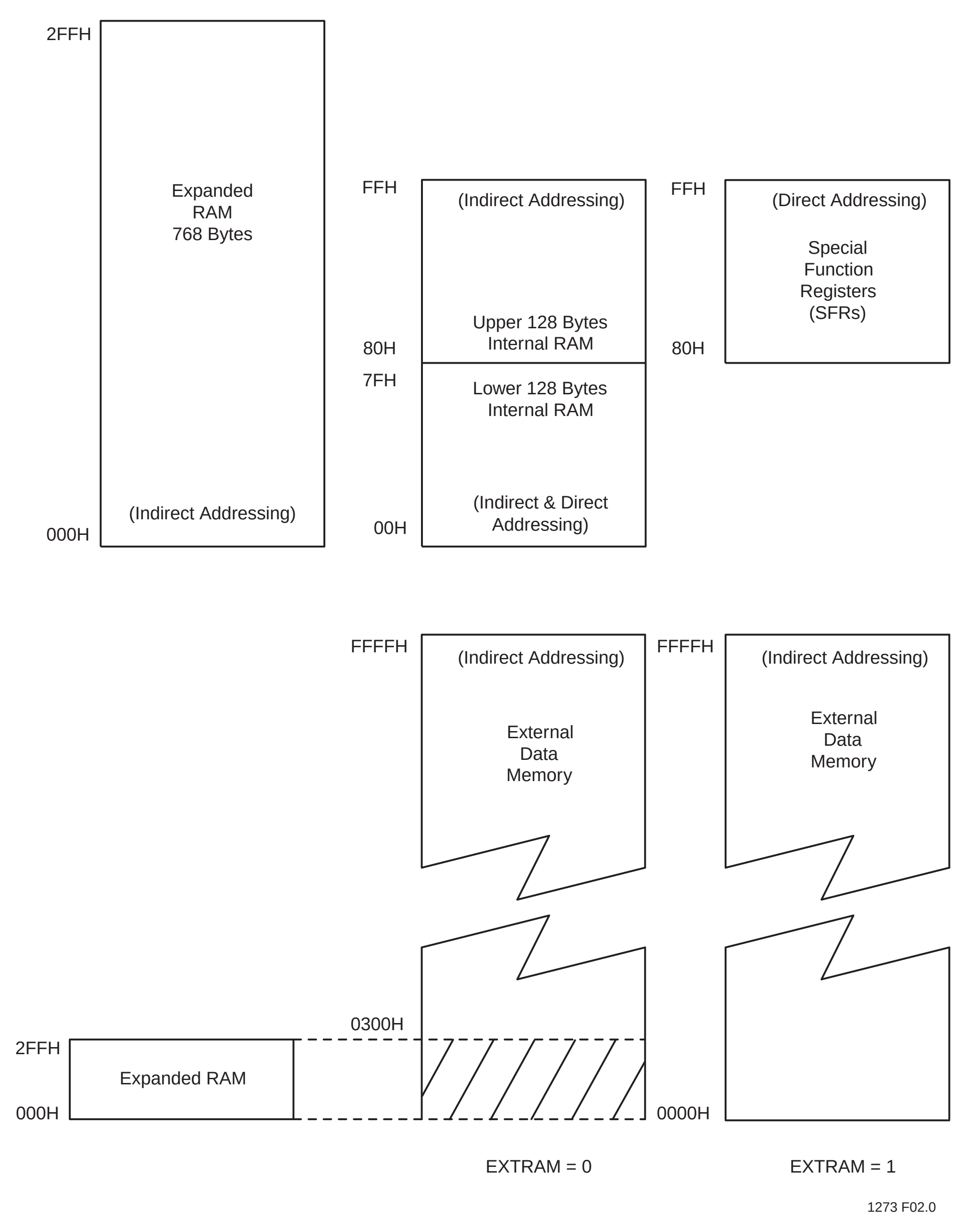

Figure 7: Internal and External Data Memory Structure

SuperFlash Address Registers (SFAH)

Location	7	6	5	4	3	2	1	0	Reset Value
B4H	SuperFlash High Order Byte Address Register								00H

Symbol	Function
SFAH	Mailbox register for interfacing with flash memory block. (High order address register).

SuperFlash Data Register (SFDT)

Location	7	6	5	4	3	2	1	0	Reset Value
B5H	SuperFlash Data Register								00H

Symbol	Function
SFDT	Mailbox register for interfacing with flash memory block. (Data register).

SuperFlash Status Register (SFST) (Read Only Register)

Location	7	6	5	4	3	2	1	0	Reset Value
B6H	SB1_i	SB2_i	SB3_i	-	EDC_i	FLASH_BUSY	-	-	xxxxx0xxb

Symbol	Function
SB1_i	Security Bit 1 status (inverse of SB1 bit)
SB2_i	Security Bit 2 status (inverse of SB2 bit)
SB3_i	Security Bit 3 status (inverse of SB3 bit) Please refer to Table 25 for security lock options.
EDC_i	Double Clock Status 0: 12 clocks per machine cycle 1: 6 clocks per machine cycle
FLASH_BUSY	Flash operation completion polling bit. 0: Device has fully completed the last IAP command. 1: Device is busy with flash operation.

Interrupt Priority (IP)

Location	7	6	5	4	3	2	1	0	Reset Value
B8H	-	PPC	PT2	PS	PT1	PX1	PT0	PX0	x0000000b

Symbol	Function
PPC	PCA interrupt priority bit
PT2	Timer 2 interrupt priority bit
PS	Serial Port interrupt priority bit
PT1	Timer 1 interrupt priority bit
PX1	External interrupt 1 priority bit
PT0	Timer 0 interrupt priority bit
PX0	External interrupt 0 priority bit

Interrupt Priority High (IPH)

Location	7	6	5	4	3	2	1	0	Reset Value
B7H	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	x0000000b

Symbol	Function
PPCH	PCA interrupt priority bit high
PT2H	Timer 2 interrupt priority bit high
PSH	Serial Port interrupt priority bit high
PT1H	Timer 1 interrupt priority bit high
PX1H	External interrupt 1 priority bit high
PT0H	Timer 0 interrupt priority bit high
PX0H	External interrupt 0 priority bit high

Interrupt Priority 1 (IP1)

Location	7	6	5	4	3	2	1	0	Reset Value
F8H	1	-	-	1	PBO	PX3	PX2	1	1xx10001b

Symbol	Function
PBO	Brown-out interrupt priority bit
PX2	External Interrupt 2 priority bit
PX3	External Interrupt 3 priority bit

Interrupt Priority 1 High (IP1H)

Location	7	6	5	4	3	2	1	0	Reset Value
F7H	1	-	-	1	PBOH	PX3H	PX2H	1	1xx10001b

Symbol	Function
PBOH	Brown-out Interrupt priority bit high
PX2H	External Interrupt 2 priority bit high
PX3H	External Interrupt 3 priority bit high

Flash Memory Programming

The device internal flash memory can be programmed or erased using In-Application Programming (IAP) mode

Product Identification

The Read-ID command accesses the Signature Bytes that identify the device and the manufacturer as SST. External programmers primarily use these Signature Bytes in the selection of programming algorithms.

Table 12: Product Identification

	Address	Data
Manufacturer’s ID	30H	BFH
Device ID		
SST89E516RD2/RD	31H	93H
SST89V516RD2/RD	31H	92H

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In-Application Programming Mode

The device offers either 72 KByte of in-application programmable flash memory. During in-application programming, the CPU of the microcontroller enters IAP mode. The two blocks of flash memory allow the CPU to execute user code from one block, while the other is being erased or reprogrammed concurrently. The CPU may also fetch code from an external memory while all internal flash is being reprogrammed. The mailbox registers (SFST, SFCM, SFAL, SFAH, SFDT and SFCF) located in the special function register (SFR), control and monitor the device’s erase and program process.

Table 14 outline the commands and their associated mailbox register settings.

In-Application Programming Mode Clock Source

During IAP mode, both the CPU core and the flash controller unit are driven off the external clock. However, an internal oscillator will provide timing references for Program and Erase operations. The internal oscillator is only turned on when required, and is turned off as soon as the flash operation is completed.

Memory Bank Selection for In-Application Programming Mode

With the addressing range limited to 16 bit, only 64 KByte of program address space is “visible” at any one time. As shown in Table 13, the bank selection (the configuration of EA# and SFCF[1:0]), allows Block 1 memory to be overlaid on the lowest 8 KByte of Block 0 memory, making Block 1 reachable. The same concept is employed to allow both Block 0 and Block 1 flash to be accessible to IAP operations. Code from a block that is not visible may not be used as a source to program another address. However, a block that is not “visible” may be programmed by code from the other block through mailbox registers.

The device allows IAP code in one block of memory to program the other block of memory, but may not program any location in the same block. If an IAP operation originates physically from Block 0, the target of this operation is implicitly defined to be in Block 1. If the IAP operation originates physically from

Sector-Erase

The Sector-Erase command erases all of the bytes in a sector. The sector size for the flash memory blocks is 128 Bytes. The selection of the sector to be erased is determined by the contents of SFAH and SFAL.

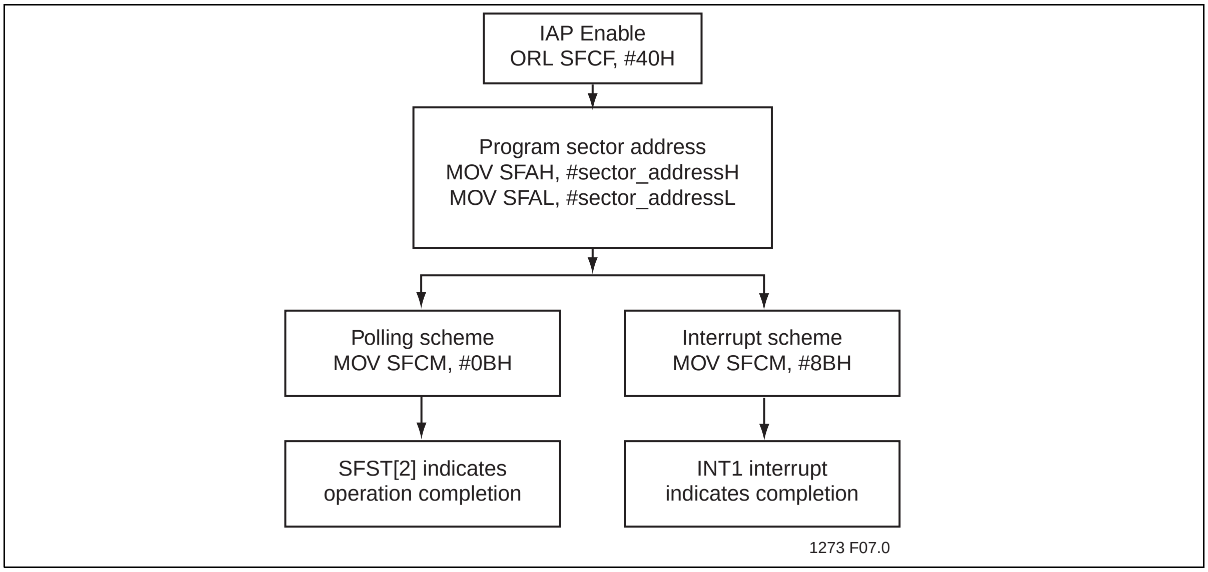

Figure 11: Sector Erase

Byte-Program

The Byte-Program command programs data into a single byte. The address is determined by the contents of SFAH and SFAL. The data byte is in SFDT.

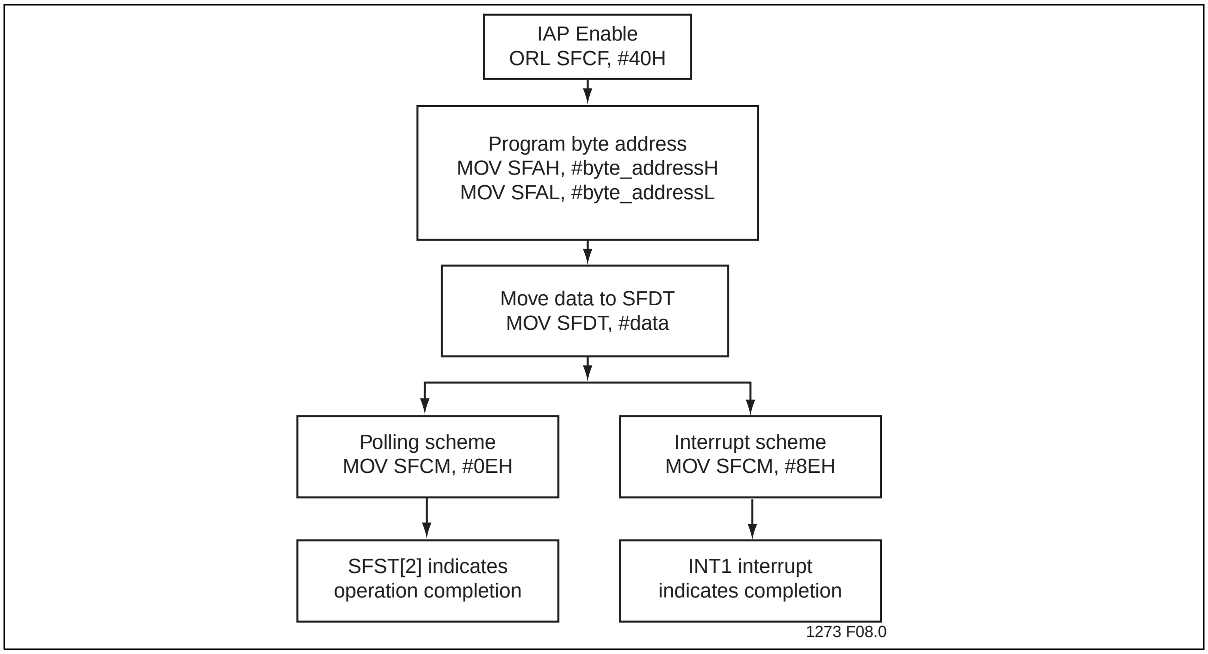

Figure 12: Byte Program

Byte-Verify

The Byte-Verify command allows the user to verify that the device has correctly performed an Erase or Program command. Byte-Verify command returns the data byte in SFDT if the command is successful. The user is required to check that the previous flash operation has fully completed before issuing a Byte-Verify. Byte-Verify command execution time is short enough that there is no need to poll for command completion and no interrupt is generated.

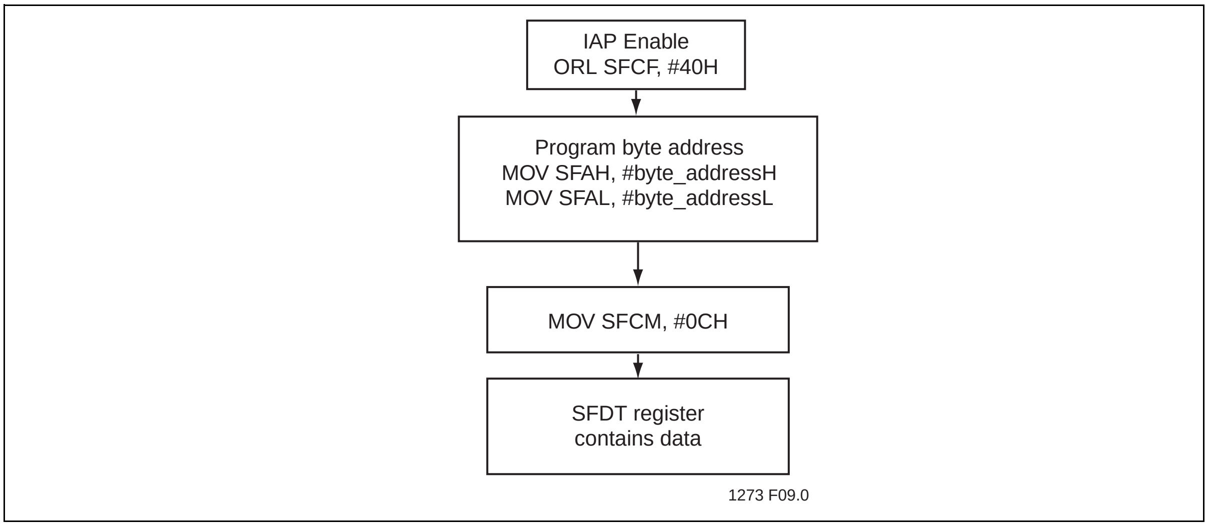

Figure 13: Byte Verify

Prog-SB3, Prog-SB2, Prog-SB1

Prog-SB3, Prog-SB2, Prog-SB1 commands are used to program the security bits (see Table 25). Completion of any of these commands, the security options will be updated immediately.

Security bits previously in un-programmed state can be programmed by these commands. Prog-SB3, Prog-SB2 and Prog-SB1 commands should only reside in Block 1 or external code memory.

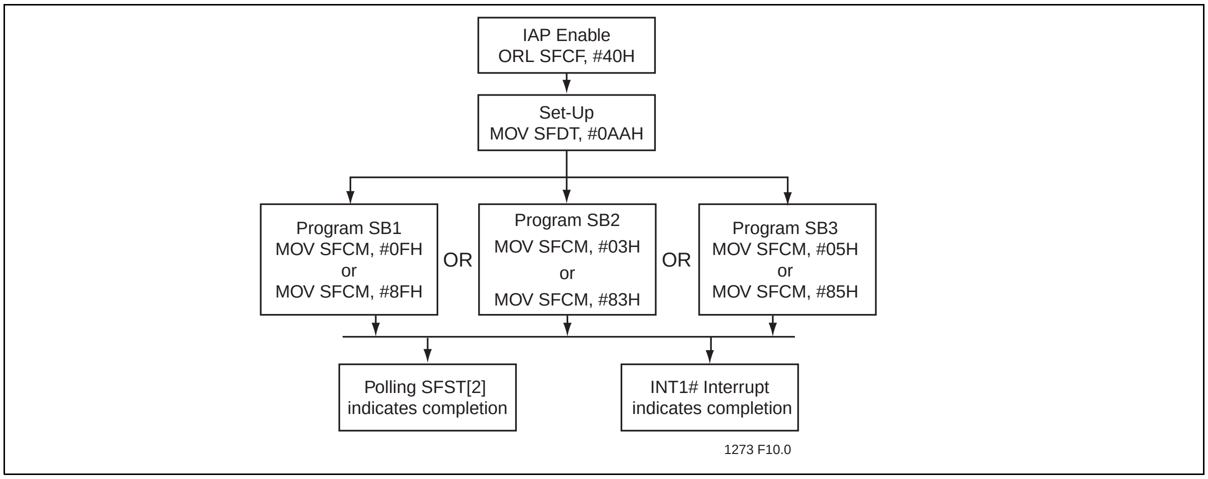

Figure 14: Prog-SB3, Prog-SB2, Prog-SB1

an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software. Each module has its own timer interrupt or capture interrupt flag (CCF0 for module 0, CCF4 for module 4, etc.). They are set when either a match or capture occurs. These flags can only be cleared by software. (See “PCA Timer/Counter Control Register (CCON)” on page 27.)

Compare/Capture Modules

Each PCA module has an associated SFR with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. Refer to “PCA Compare/Capture Module Mode Register (CCAPMn)” on page 29 for details. The registers each contain 7 bits which are used to control the mode each module will operate in. The ECCF bit (CCAPMn.0 where n = 0, 1, 2, 3, or 4 depending on module) will enable the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs. PWM (CCAPMn.1) enables the pulse width modulation mode. The TOG bit (CCAPMn.2) when set, causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module’s capture/compare register. When there is a match between the PCA counter and the module’s capture/compare register, the MATn (CCAPMn.3) and the CCFn bit in the CCON register to be set.

Bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine whether the capture input will be active on a positive edge or negative edge. The CAPN bit enables the negative edge that a capture input will be active on, and the CAPP bit enables the positive edge. When both bits are set, both edges will be enabled and a capture will occur for either transition. The last bit in the register ECOM (CCAPMn.6) when set, enables the comparator function. Table 22 shows the CCAPMn settings for the various PCA functions.

There are two additional register associated with each of the PCA modules: CCAPnH and CCAPnL. They are registers that hold the 16-bit count value when a capture occurs or a compare occurs. When a module is used in PWM mode, these registers are used to control the duty cycle of the output. See Figure 24.

Table 21: PCA High and Low Register Compare/Capture Modules

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB LSB	RESET Value
CCAP0H	PCA Module 0 Compare/Capture Registers	FAH	CCAP0H[7:0]	00H
CCAP0L		EAH	CCAP0L[7:0]	00H
CCAP1H	PCA Module 1 Compare/Capture Registers	FBH	CCAP1H[7:0]	00H
CCAP1L		EBH	CCAP1L[7:0]	00H
CCAP2H	PCA Module 2 Compare/Capture Registers	FCH	CCAP2H[7:0]	00H
CCAP2L		ECH	CCAP2L[7:0]	00H
CCAP3H	PCA Module 3 Compare/Capture Registers	FDH	CCAP3H[7:0]	00H
CCAP3L		EDH	CCAP3L[7:0]	00H
CCAP4H	PCA Module 4 Compare/Capture Registers	FEH	CCAP4H[7:0]	00H
CCAP4L		EEH	CCAP4L[7:0]	00H

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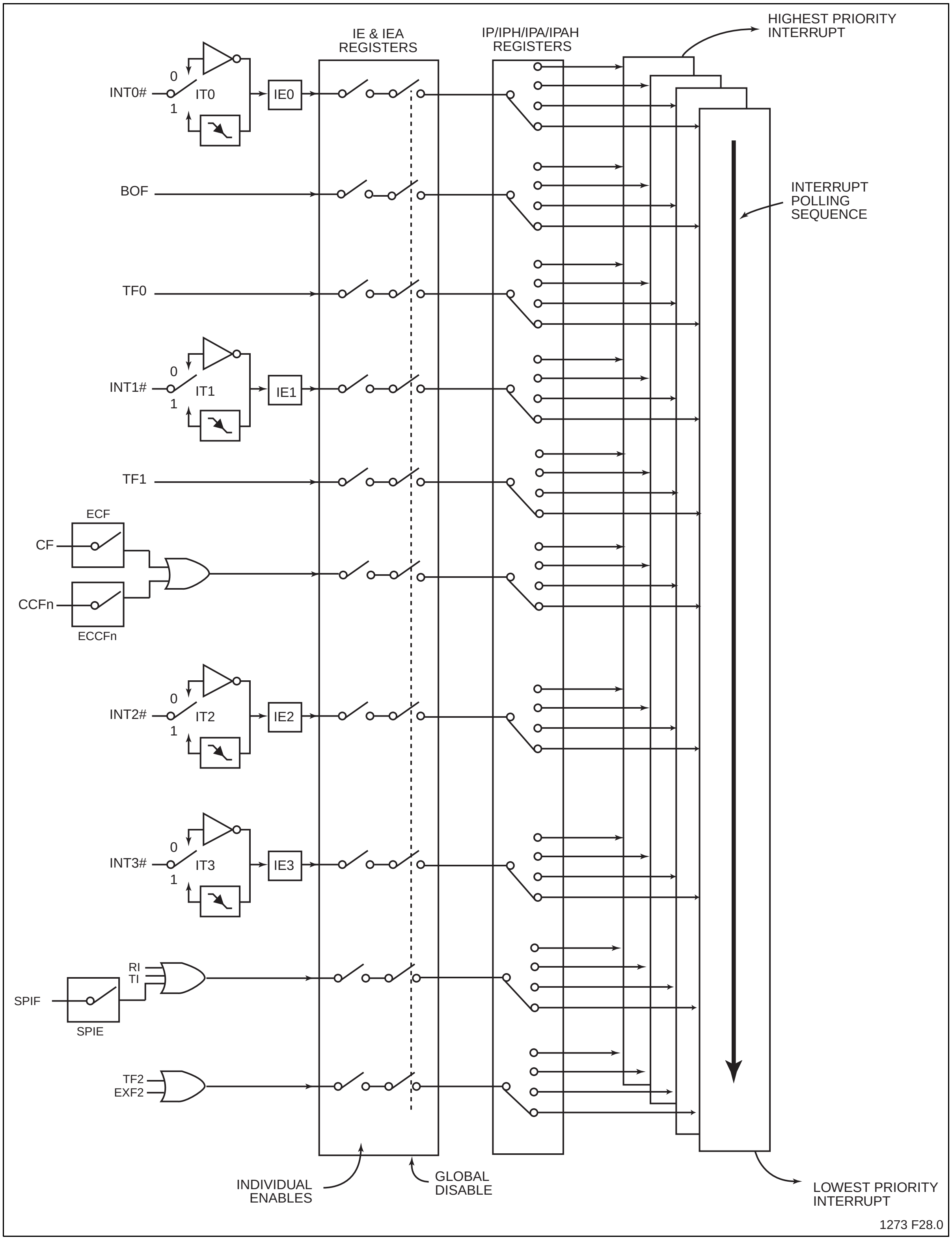

Figure 32: Interrupt Structure

System Clock and Clock Options

Clock Input Options and Recommended Capacitor Values for Oscillator

Shown in Figure 33 are the input and output of an internal inverting amplifier (XTAL1, XTAL2), which can be configured for use as an on-chip oscillator.

When driving the device from an external clock source, XTAL2 should be left disconnected and XTAL1 should be driven.

At start-up, the external oscillator may encounter a higher capacitive load at XTAL1 due to interaction between the amplifier and its feedback capacitance. However, the capacitance will not exceed 15 pF once the external signal meets the V_{IL} and V_{IH} specifications.

Crystal manufacturer, supply voltage, and other factors may cause circuit performance to differ from one application to another. C1 and C2 should be adjusted appropriately for each design. Table 29, shows the typical values for C1 and C2 vs. crystal type for various frequencies

Table 29: Recommended Values for C1 and C2 by Crystal Type

Crystal	C1 = C2
Quartz	20-30pF
Ceramic	40-50pF

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More specific information about on-chip oscillator design can be found in the ***FlashFlex Oscillator Circuit Design Considerations*** application note.

Clock Doubling Option

By default, the device runs at 12 clocks per machine cycle (x1 mode). The device has a clock doubling option to speed up to 6 clocks per machine cycle. Please refer to Table 30 for detail.

Clock double mode can be enabled either via the external host mode or the IAP mode. Please refer to Table 14 for the IAP mode enabling commands (When set, the EDC# bit in SFST register will indicate 6 clock mode.).

The clock double mode is only for doubling the internal system clock and the internal flash memory, i.e. EA#=1. To access the external memory and the peripheral devices, careful consideration must be taken. Also note that the crystal output (XTAL2) will not be doubled.

DC Electrical Characteristics

Table 36: DC Electrical Characteristics for SST89E516RDx
T_A = -40°C to +85°C; V_{DD} = 4.5-5.5V; V_{SS} = 0V

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Voltage	$4.5 < V_{DD} < 5.5$	-0.5	$0.2V_{DD}$ - 0.1	V
V_{IH}	Input High Voltage	$4.5 < V_{DD} < 5.5$	$0.2V_{DD}$ + 0.9	V_{DD} + 0.5	V
V_{IH1}	Input High Voltage (XTAL1, RST)	$4.5 < V_{DD} < 5.5$	$0.7V_{DD}$	V_{DD} + 0.5	V
V_{OL}	Output Low Voltage (Ports 1.5, 1.6, 1.7)	V_{DD} = 4.5V			
		I_{OL} = 16mA		1.0	V
V_{OL}	Output Low Voltage (Ports 1, 2, 3)[1]	V_{DD} = 4.5V			
		I_{OL} = 100µA[2]		0.3	V
		I_{OL} = 1.6mA[2]		0.45	V
		I_{OL} = 3.5mA[2]		1.0	V
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#)[1,3]	V_{DD} = 4.5V			
		I_{OL} = 200µA[2]		0.3	V
		I_{OL} = 3.2mA[2]		0.45	V
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, PSEN#)[4]	V_{DD} = 4.5V			
		I_{OH} = -10µA	V_{DD} - 0.3		V
		I_{OH} = -30µA	V_{DD} - 0.7		V
		I_{OH} = -60µA	V_{DD} - 1.5		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)[4]	V_{DD} = 4.5V			
		I_{OH} = -200µA	V_{DD} - 0.3		V
		I_{OH} = -3.2mA	V_{DD} - 0.7		V
V_{BOD}	Brown-out Detection Voltage		3.85	4.15	V
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V_{IN} = 0.4V		-75	µA
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3)[5]	V_{IN} = 2V		-650	µA
I_{LI}	Input Leakage Current (Port 0)	$0.45 < V_{IN} < V_{DD}-0.3$		±10	µA
R_{RST}	RST Pull-down Resistor		40	225	KΩ
C_{IO}	Pin Capacitance[6]	@ 1 MHz, 25°C		15	pF
I_{DD}	Power Supply Current IAP Mode @ 40 MHz			88	mA
	Active Mode @ 40 MHz			50	mA
	Idle Mode @ 40 MHz			42	mA
	Power-down Mode (min. V_{DD} = 2V)	T_A = 0°C to +70°C		80	µA
		T_A = -40°C to +85°C		90	µA

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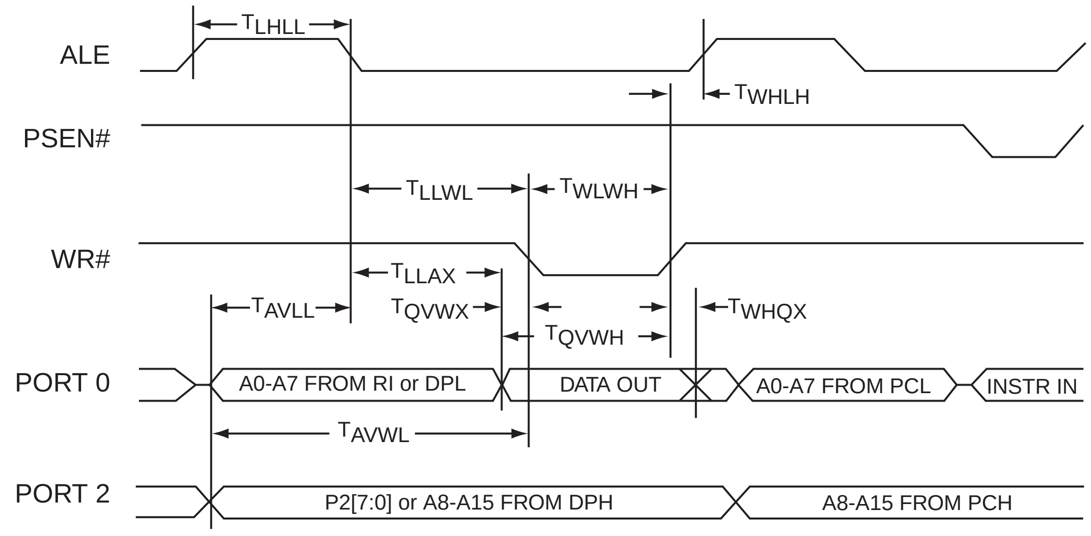


Figure 38: External Data Memory Write Cycle

Table 39: External Clock Drive

		Oscillator						
		12MHz		**40MHz**		**Variable**		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
$1/T_{CLCL}$	Oscillator Frequency					0	40	MHz
T_{CLCL}		83		25				ns
T_{CHCX}	High Time			8.75		$0.35T_{CLCL}$	$0.65T_{CLCL}$	ns
T_{CLCX}	Low Time			8.75		$0.35T_{CLCL}$	$0.65T_{CLCL}$	ns
T_{CLCH}	Rise Time		20		10			ns
T_{CHCL}	Fall Time		20		10			ns

T0-0.0 25093

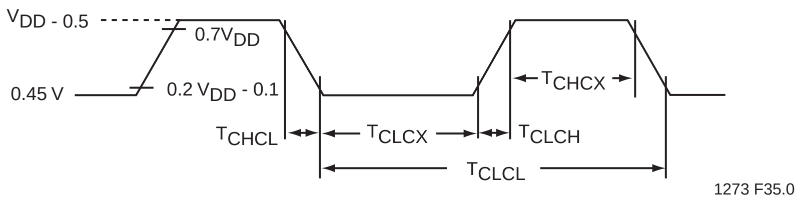
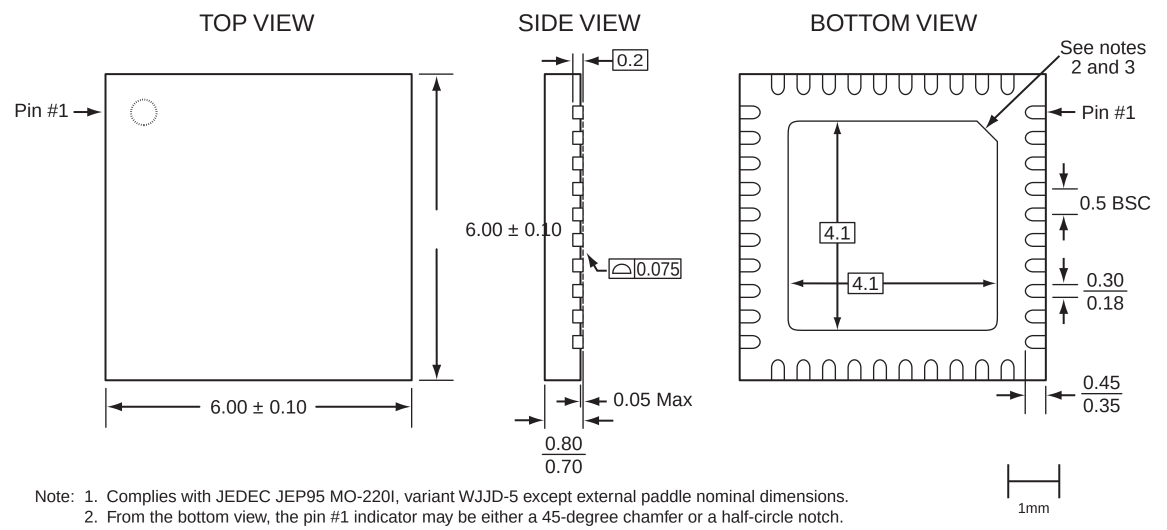


Figure 39: External Clock Drive Waveform

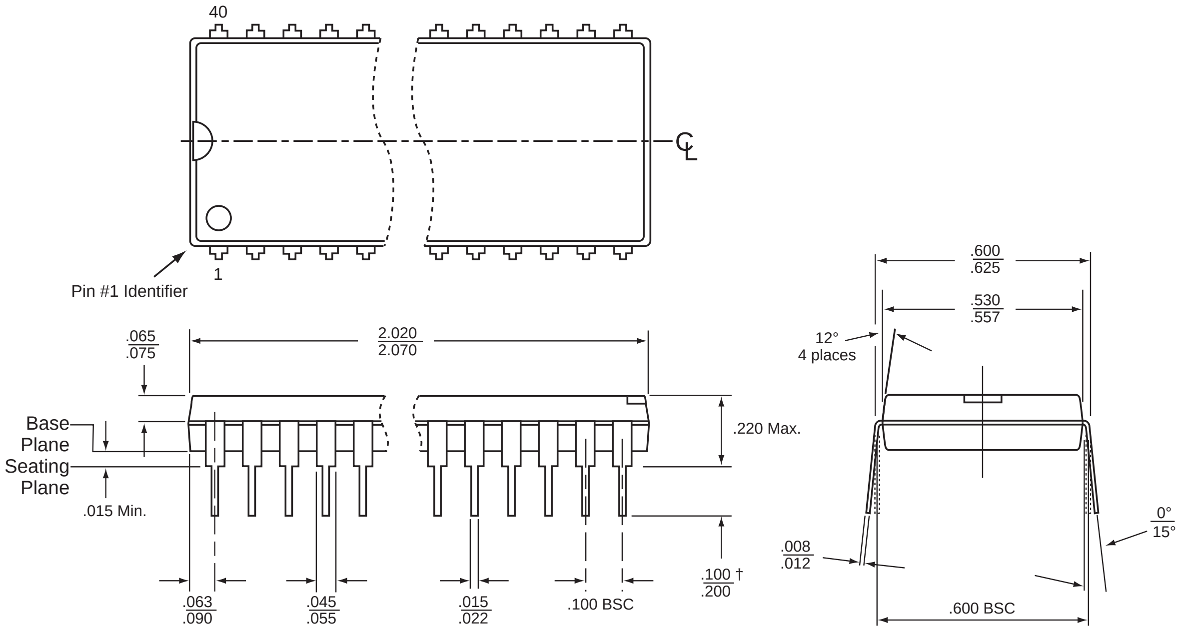
Packaging Diagrams



Note:
1. Complies with JEDEC JEP95 MO-220I, variant WJJD-5 except external paddle nominal dimensions.
2. From the bottom view, the pin #1 indicator may be either a 45-degree chamfer or a half-circle notch.
3. The external paddle is electrically connected to the die back-side and possibly to certain V_{SS} leads. This paddle should be soldered to the PC board; it is suggested to connect this paddle to the V_{SS} of the unit. Connection of this paddle to any other voltage potential will result in shorts and/or electrical malfunction of the device.
4. Untoleranced dimensions are nominal target dimensions.
5. All linear dimensions are in millimeters (max/min).

40-wqfn-6x6-QI-1

Figure 47: 40-contact Very-very-thin Quad Flat No-lead (WQFN)
SST Package Code: QI



Note: 1. Complies with JEDEC publication 95 MS-011 AC dimensions (except as noted), although some dimensions may be more stringent.
† = JEDEC min is .115; SST min is *less*stringent
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .010 inches.

40-pdip-PI-7

Figure 48: 40-pin Plastic Dual In-line Pins (PDIP)
SST Package Code: PI