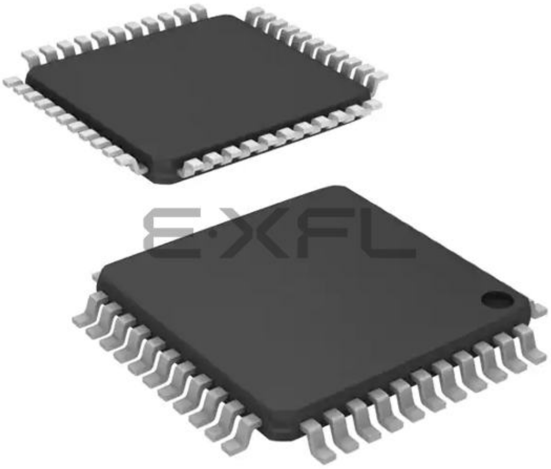
Microchip Technology - SST89V516RD2-33-I-TQJE Datasheet



What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	36
Program Memory Size	72KB (72K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/sst89v516rd2-33-i-tqje

Program Memory Block Switching

The program memory block switching feature of the device allows either Block 1 or the lowest 8 KByte of Block 0 to be used for the lowest 8 KByte of the program address space. SFCF[1:0] controls program memory block switching.

Table 2: SFCF Values for Program Memory Block Switching

SFCF[1:0]	Program Memory Block Switching
01, 10, 11	Block 1 is not visible to the program counter (PC). Block 1 is reachable only via in-application programming from 0000H - 1FFFH.
00	Block 1 is overlaid onto the low 8K of the program address space; occupying address locations 0000H - 1FFFH. When the PC falls within 0000H - 1FFFH, the instruction will be fetched from Block 1 instead of Block 0. Outside of 0000H - 1FFFH, Block 0 is used. Locations 0000H - 1FFFH of Block 0 are reachable through in-application programming.

T0-0.0 25093

Reset Configuration of Program Memory Block Switching

Program memory block switching is initialized after reset according to the state of the Start-up Configuration bit SC0. The SC0 bit is programmed via an external host mode command or an IAP Mode command. See Table 14.

Once out of reset, the SFCF[0] bit can be changed dynamically by the program for desired effects. Changing SFCF[0] will not change the SC0 bit.

Caution must be taken when dynamically changing the SFCF[0] bit. Since this will cause different physical memory to be mapped to the logical program address space. The user must avoid executing block switching instructions within the address range 0000H to 1FFFH.

Table 3: SFCF Values Under Different Reset Conditions

	State of SFCF[1:0] after:		
SC0[1]	Power-on or External Reset	WDT Reset or Brown-out Reset	Software Reset
U (1)	00 (default)	x0	10
P (0)	01	x1	11

T0-0.0 25093

[1] P = Programmed (Bit logic state = 0),
U = Unprogrammed (Bit logic state = 1)

Data RAM Memory

The data RAM has 1024 bytes of internal memory. The RAM can be addressed up to 64KB for external data memory.

Dual Data Pointers

The device has two 16-bit data pointers. The DPTR Select (DPS) bit in AUXR1 determines which of the two data pointers is accessed. When DPS=0, DPTR0 is selected; when DPS=1, DPTR1 is selected. Quickly switching between the two data pointers can be accomplished by a single INC instruction on AUXR1. (See Figure 8)

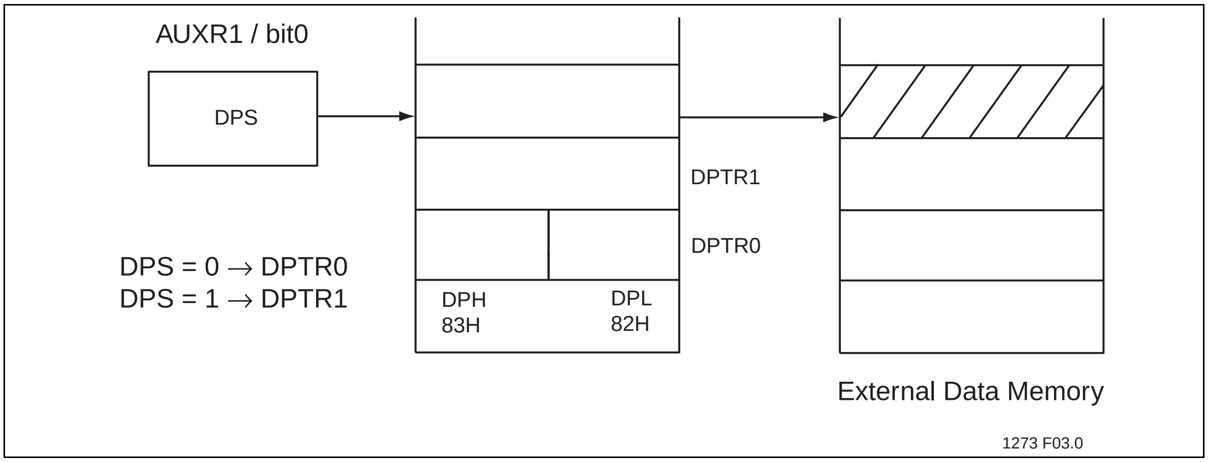


Figure 8: Dual Data Pointer Organization

Special Function Registers

Most of the unique features of the FlashFlex microcontroller family are controlled by bits in special function registers (SFRs) located in the SFR memory map shown in Table 5. Individual descriptions of each SFR are provided and reset values indicated in Tables 6 to 10.

Table 5: FlashFlex SFR Memory Map

	8 BYTES								
F8H	IP1[1]	CH	CCAP0H	CCAP1H	CCAP2H	CCAP3H	CCAP4H		FFH
F0H	B[1]							IP1H	F7H
E8H	IEA[1]	CL	CCAP0L	CCAP1L	CCAP2L	CCAP3L	CCAP4L		EFH
E0H	ACC[1]								E7H
D8H	CCON[1]	CMOD	CCAPM0	CCAPM1	CCAPM2	CCAPM3	CCAPM4		DFH
D0H	PSW[1]					SPCR			D7H
C8H	T2CON[1]	T2MOD	RCAP2L	RCAP2H	TL2	TH2			CFH
C0H	WDTC[1]								C7H
B8H	IP[1]	SADEN							BFH
B0H	P3[1]	SFCF	SFCM	SFAL	SFAH	SFDT	SFST	IPH	B7H
A8H	IE[1]	SADDR	SPSR				XICON		AFH
A0H	P2[1]		AUXR1			P4			A7H
98H	SCON[1]	SBUF							9FH
90H	P1[1]								97H
88H	TCON[1]	TMOD	TL0	TL1	TH0	TH1	AUXR		8FH
80H	P0[1]	SP	DPL	DPH		WDTD	SPDR	PCON	87H

T0-0.0 25093

[1] Bit addressable SFRs

Table 11: PCA SFRs

		Direct	Bit Address, Symbol, or Alternative Port Function								RESET
Symbol	Description	Address	MSB							LSB	Value
CH CL	PCA Timer/Counter	F9H E9H	CH[7:0] CL[7:0]								00H 00H
CCON[1]	PCA Timer/Counter Control Register	D8H	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0	00x00000b
CMOD	PCA Timer/Counter Mode Register	D9H	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF	00xxx000b
CCAP0H	PCA Module 0 Compare/Capture Registers	FAH	CCAP0H[7:0]								00H
CCAP0L		EAH	CCAP0L[7:0]								00H
CCAP1H	PCA Module 1 Compare/Capture Registers	FBH	CCAP1H[7:0]								00H
CCAP1L		EBH	CCAP1L[7:0]								00H
CCAP2H	PCA Module 2 Compare/Capture Registers	FCH	CCAP2H[7:0]								00H
CCAP2L		ECH	CCAP2L[7:0]								00H
CCAP3H	PCA Module 3 Compare/Capture Registers	FDH	CCAP3H[7:0]								00H
CCAP3L		EDH	CCAP3L[7:0]								00H
CCAP4H	PCA Module 4 Compare/Capture Registers	FEH	CCAP4H[7:0]								00H
CCAP4L		EEH	CCAP4L[7:0]								00H
CCAPM0	PCA Compare/Capture Module Mode Registers	DAH	-	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0	x0000000b
CCAPM1		DBH	-	ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1	x0000000b
CCAPM2		DCH	-	ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2	x0000000b
CCAPM3		DDH	-	ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3	x0000000b
CCAPM4		DEH	-	ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4	x0000000b

T0-0.0 25093

1. Bit Addressable SFRs

PCA Timer/Counter Mode Register[1] (CMOD)

Location	7	6	5	4	3	2	1	0	Reset Value
D9H	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF	00xxx000b

[1] Not bit addressable

Symbol	Function
CIDL	Counter Idle Control: 0: Programs the PCA Counter to continue functioning during idle mode 1: Programs the PCA Counter to be gated off during idle
WDTE	Watchdog Timer Enable: 0: Disables Watchdog Timer function on PCA module 4 1: Enables Watchdog Timer function on PCA module 4
-	Not implemented, reserved for future use. **Note:** User should not write ‘1’s to reserved bits. The value read from a reserved bit is indeterminate.
CPS1	PCA Count Pulse Select bit 1
CPS0	PCA Count Pulse Select bit 2

CPS1	CPS0	Selected PCA Input[1]	
0	0	0	Internal clock, f_{OSC}/6 in 6 clock mode (f_{OSC}/12 in 12 clock mode)
0	1	1	Internal clock, f_{OSC}/2 in 6 clock mode (f_{OSC}/4 in 12 clock mode)
1	0	2	Timer 0 overflow
1	1	3	External clock at ECI/P1.2 pin
			(max. rate = f_{OSC}/4 in 6 clock mode, f_{OSC}/8 in 12 clock mode)

[1] f_{OSC} = oscillator frequency

Symbol	Function
ECF	PCA Enable Counter Overflow interrupt: 0: Disables the CF bit in CCON 1: Enables CF bit in CCON to generate an interrupt

Flash Memory Programming

The device internal flash memory can be programmed or erased using In-Application Programming (IAP) mode

Product Identification

The Read-ID command accesses the Signature Bytes that identify the device and the manufacturer as SST. External programmers primarily use these Signature Bytes in the selection of programming algorithms.

Table 12: Product Identification

	Address	Data
Manufacturer's ID	30H	BFH
Device ID		
SST89E516RD2/RD	31H	93H
SST89V516RD2/RD	31H	92H

T0-0.0 25093

In-Application Programming Mode

The device offers either 72 KByte of in-application programmable flash memory. During in-application programming, the CPU of the microcontroller enters IAP mode. The two blocks of flash memory allow the CPU to execute user code from one block, while the other is being erased or reprogrammed concurrently. The CPU may also fetch code from an external memory while all internal flash is being reprogrammed. The mailbox registers (SFST, SFCM, SFAL, SFAH, SFDT and SFCF) located in the special function register (SFR), control and monitor the device's erase and program process.

Table 14 outline the commands and their associated mailbox register settings.

In-Application Programming Mode Clock Source

During IAP mode, both the CPU core and the flash controller unit are driven off the external clock. However, an internal oscillator will provide timing references for Program and Erase operations. The internal oscillator is only turned on when required, and is turned off as soon as the flash operation is completed.

Memory Bank Selection for In-Application Programming Mode

With the addressing range limited to 16 bit, only 64 KByte of program address space is "visible" at any one time. As shown in Table 13, the bank selection (the configuration of EA# and SFCF[1:0]), allows Block 1 memory to be overlaid on the lowest 8 KByte of Block 0 memory, making Block 1 reachable. The same concept is employed to allow both Block 0 and Block 1 flash to be accessible to IAP operations. Code from a block that is not visible may not be used as a source to program another address. However, a block that is not "visible" may be programmed by code from the other block through mailbox registers.

The device allows IAP code in one block of memory to program the other block of memory, but may not program any location in the same block. If an IAP operation originates physically from Block 0, the target of this operation is implicitly defined to be in Block 1. If the IAP operation originates physically from

Block 1, then the target address is implicitly defined to be in Block 0. If the IAP operation originates from external program space, then, the target will depend on the address and the state of bank selection.

IAP Enable Bit

The IAP enable bit, SFCF[6], enables in-application programming mode. Until this bit is set, all flash programming IAP commands will be ignored.

Table 13: IAP Address Resolution

EA#	SFCF[1:0]	Address of IAP Inst.	Target Address	Block Being Programmed
1	00	>= 2000H (Block 0)	>= 2000H (Block 0)	None[1]
1	00	>= 2000H (Block 0)	< 2000H (Block 1)	Block 1
1	00	< 2000H (Block 1)	Any (Block 0)	Block 0
1	01, 10, 11	Any (Block 0)	>= 2000H (Block 0)	None[1]
1	01, 10, 11	Any (Block 0)	< 2000H (Block 1)	Block 1
0	00	From external	>= 2000H (Block 0)	Block 0
0	00	From external	< 2000H (Block 1)	Block 1
0	01, 10, 11	From external	Any (Block 0)	Block 0

T0-0.0 25093

[1] No operation is performed because code from one block may not program the same originating block

In-Application Programming Mode Commands

All of the following commands can only be initiated in the IAP mode. In all situations, writing the control byte to the SFCM register will initiate all of the operations. All commands will not be enabled if the security locks are enabled on the selected memory block.

The Program command is for programming new data into the memory array. The portion of the memory array to be programmed should be in the erased state, FFH. If the memory is not erased, it should first be erased with an appropriate Erase command. **Warning: Do not attempt to write (program or erase) to a block that the code is currently fetching from. This will cause unpredictable program behavior and may corrupt program data.**

Prog-SC0

Prog-SC0 command is used to program the SC0 bit. This command only changes the SC0 bit and has no effect on BSEL bit until after a reset cycle.

SC0 bit previously in un-programmed state can be programmed by this command. The Prog-SC0 command should reside only in Block 1 or external code memory.

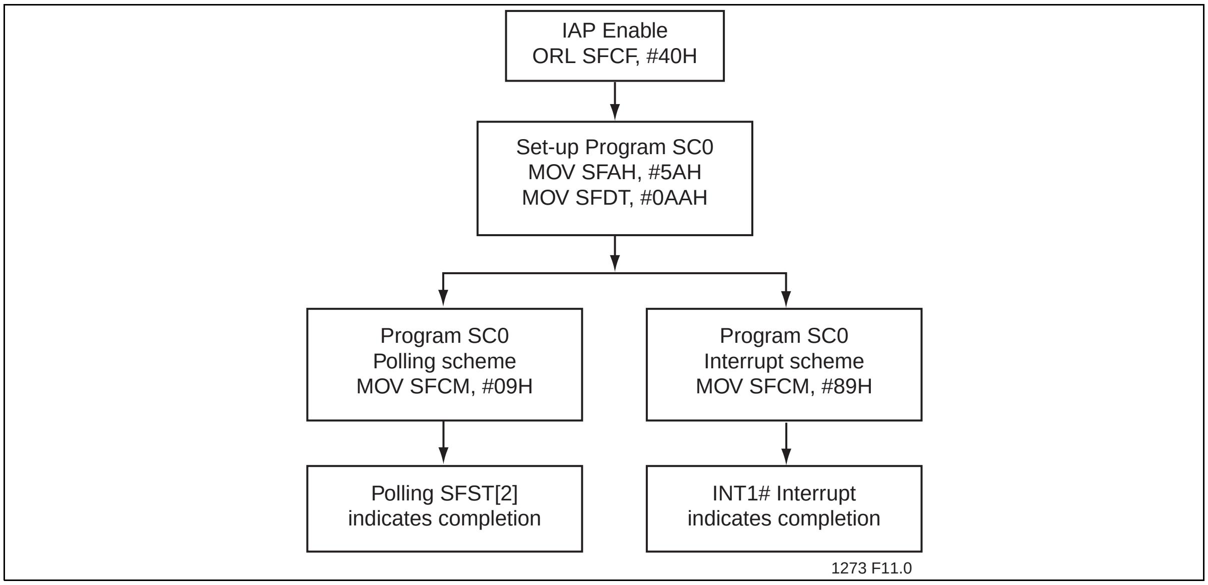


Figure 15: Prog-SC0

Enable-Clock-Double

Enable-Clock-Double command is used to make the MCU run at 6 clocks per machine cycle. The standard (default) is 12 clocks per machine cycle (i.e. clock double command disabled).

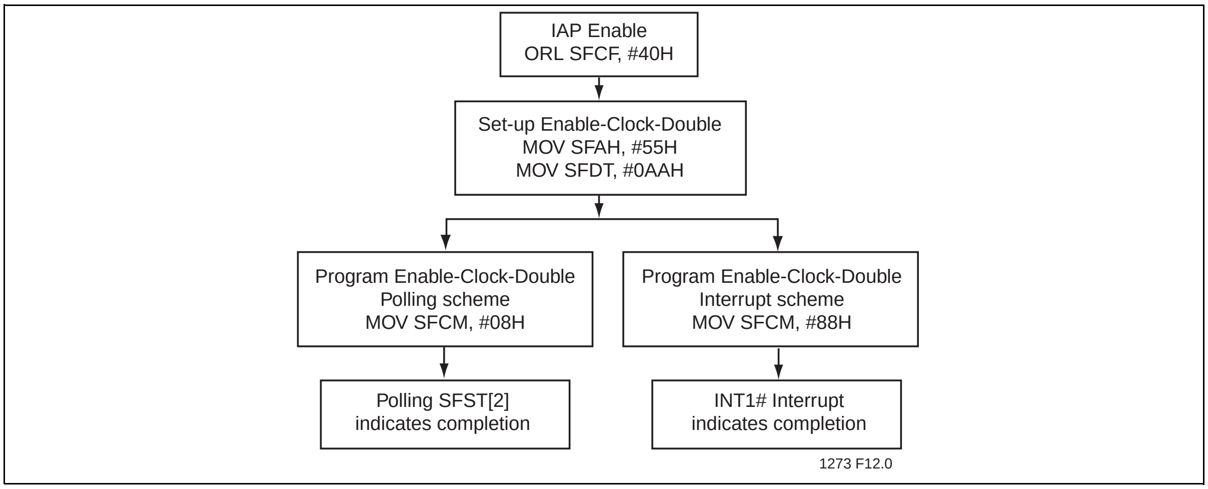


Figure 16: Enable-Clock-Double

There are no IAP counterparts for the external host commands Select-Block0 and Select-Block1.

Timers/Counters

Timers

The device has three 16-bit registers that can be used as either timers or event counters. The three timers/counters are denoted Timer 0 (T0), Timer 1 (T1), and Timer 2 (T2). Each is designated a pair of 8-bit registers in the SFRs. The pair consists of a most significant (high) byte and least significant (low) byte. The respective registers are TL0, TH0, TL1, TH1, TL2, and TH2.

Timer Set-up

Refer to Table 9 for TMOD, TCON, and T2CON registers regarding timers T0, T1, and T2. The following tables provide TMOD values to be used to set up Timers T0, T1, and T2.

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set separately to turn the timer on.

Table 15: Timer/Counter 0

			TMOD	
	Mode	**Function**	**Internal Control[1]**	**External Control[2]**
Used as Timer	0	13-bit Timer	00H	08H
	1	16-bit Timer	01H	09H
	2	8-bit Auto-Reload	02H	0AH
	3	Two 8-bit Timers	03H	0BH
Used as Counter	0	13-bit Timer	04H	0CH
	1	16-bit Timer	05H	0DH
	2	8-bit Auto-Reload	06H	0EH
	3	Two 8-bit Timers	07H	0FH

T0-0.0 25093

1. The Timer is turned ON/OFF by setting/clearing bit TR0 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on INT0# (P3.2) when TR0 = 1 (hardware control).

Table 16: Timer/Counter 1

			TMOD	
	Mode	**Function**	**Internal Control[1]**	**External Control[2]**
Used as Timer	0	13-bit Timer	00H	80H
	1	16-bit Timer	10H	90H
	2	8-bit Auto-Reload	20H	A0H
	3	Does not run	30H	B0H
Used as Counter	0	13-bit Timer	40H	C0H
	1	16-bit Timer	50H	D0H
	2	8-bit Auto-Reload	60H	E0H
	3	Not available	-	-

T0-0.0 25093

1. The Timer is turned ON/OFF by setting/clearing bit TR1 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on INT1# (P3.3) when TR1 = 1 (hardware control).

Table 17: Timer/Counter 2

		T2CON	
	Mode	**Internal Control**[1]	**External Control**[2]
Used as Timer	16-bit Auto-Reload	00H	08H
	16-bit Capture	01H	09H
	Baud rate generator receive and transmit same baud rate	34H	36H
	Receive only	24H	26H
	Transmit only	14H	16H
Used as Counter	16-bit Auto-Reload	02H	0AH
	16-bit Capture	03H	0BH

T0-0.0 25093

1. Capture/Reload occurs only on timer/counter overflow.
2. Capture/Reload occurs on timer/counter overflow and a 1 to 0 transition on T2EX (P1.1) pin except when Timer 2 is used in the baud rate generating mode.

Programmable Clock-Out

A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed:

1. to input the external clock for Timer/Counter 2, or
2. to output a 50% duty cycle clock ranging from 122 Hz to 8 MHz at a 16 MHz operating frequency (61 Hz to 4 MHz in 12 clock mode).

To configure Timer/Counter 2 as a clock generator, bit
C/#T2 (in T2CON) must be cleared and bit T20E in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

$$\frac{\text{Oscillator Frequency}}{n \times (65536 - \text{RCAP2H, RCAP2L})}$$

n =2 (in 6 clock mode)
4 (in 12 clock mode)

Where (RCAP2H, RCAP2L) = the contents of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode, Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and the Clock-Out frequency will not be the same.

Serial I/O

Full-Duplex, Enhanced UART

The device serial I/O port is a full-duplex port that allows data to be transmitted and received simultaneously in hardware by the transmit and receive registers, respectively, while the software is performing other tasks. The transmit and receive registers are both located in the Serial Data Buffer (SBUF) special function register. Writing to the SBUF register loads the transmit register, and reading from the SBUF register obtains the contents of the receive register.

The UART has four modes of operation which are selected by the Serial Port Mode Specifier (SM0 and SM1) bits of the Serial Port Control (SCON) special function register. In all four modes, transmission is initiated by any instruction that uses the SBUF register as a destination register. Reception is initiated in mode 0 when the Receive Interrupt (RI) flag bit of the Serial Port Control (SCON) SFR is cleared and the Reception Enable/ Disable (REN) bit of the SCON register is set. Reception is initiated in the other modes by the incoming start bit if the REN bit of the SCON register is set.

Framing Error Detection

Framing Error Detection is a feature, which allows the receiving controller to check for valid stop bits in modes 1, 2, or 3. Missing stops bits can be caused by noise in serial lines or from simultaneous transmission by two CPUs.

Framing Error Detection is selected by going to the PCON register and changing SMOD0 = 1 (see Figure 17). If a stop bit is missing, the Framing Error bit (FE) will be set. Software may examine the FE bit after each reception to check for data errors. After the FE bit has been set, it can only be cleared by software. Valid stop bits do not clear FE. When FE is enabled, RI rises on the stop bit, instead of the last data bit (see Figure 18 and Figure 19).

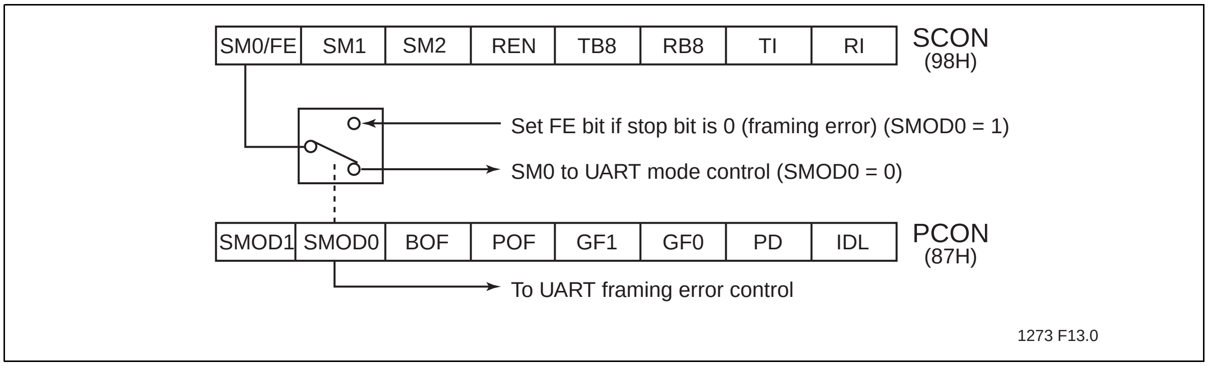

SM0/FE
SM1
SM2
REN
TB8
RB8
TI
RI
SCON
(98H)
Set FE bit if stop bit is 0 (framing error) (SMOD0 = 1)
SM0 to UART mode control (SMOD0 = 0)
SMOD1
SMOD0
BOF
POF
GF1
GF0
PD
IDL
PCON
(87H)
To UART framing error control
1273 F13.0

Figure 17: Framing Error Block Diagram

If the user added a third slave such as the example below:

Slave 3

SADDR	=	1111 1001
SADEN	=	1111 0101
GIVEN	=	1111 X0X1

Select Slave 3 Only		
Slave 2	**Given Address**	**Possible Addresses**
	1111 X0X1	1111 1011 1111 1001

The user could use the possible addresses above to select slave 3 only. Another combination could be to select slave 2 and 3 only as shown below.

Select Slaves 2 & 3 Only	
Slaves 2 & 3	**Possible Addresses**
	1111 0011

More than one slave may have the same SADDR address as well, and a given address could be used to modify the address so that it is unique.

Using the Broadcast Address to Select Slaves

Using the broadcast address, the master can communicate with all the slaves at once. It is formed by performing a logical OR of SADDR and SADEN with ‘0’s in the result treated as “don’t cares”.

Slave 1

1111 0001	=	SADDR
+1111 1010	=	SADEN
1111 1X11	=	Broadcast

“Don’t cares” allow for a wider range in defining the broadcast address, but in most cases, the broadcast address will be FFH.

On reset, SADDR and SADEN are “0”. This produces an given address of all “don’t cares” as well as a broadcast address of all “don’t cares.” This effectively disables Automatic Addressing mode and allows the microcontroller to function as a standard 8051, which does not make use of this feature.

Programmable Counter Array

The Programmable Counter Array (PCA) present on the SST89E/V516RDx is a special 16-bit timer that has five 16-bit capture/compare modules. Each of the modules can be programmed to operate in one of four modes: rising and/or falling edge capture, software timer, high-speed output, or pulse width modulator. The 5th module can be programmed as a Watchdog Timer in addition to the other four modes. Each module has a pin associated with it in port 1. Module 0 is connected to P1.3 (CEX0), module 1 to P1[4] (CEX1), module 2 to P1[5] (CEX2), module 3 to P1[6] (CEX3), and module 4 to P1[7] (CEX4). PCA configuration is shown in Figure 24.

PCA Overview

PCA provides more timing capabilities with less CPU intervention than the standard timer/counter. Its advantages include reduced software overhead and improved accuracy.

The PCA consists of a dedicated timer/counter which serves as the time base for an array of five compare/capture modules. Figure 24 shows a block diagram of the PCA. External events associated with modules are shared with corresponding Port 1 pins. Modules not using the port pins can still be used for standard I/O.

Each of the five modules can be programmed in any of the following modes:

- Rising and/or falling edge capture
- Software timer
- High speed output
- Watchdog Timer (Module 4 only)
- Pulse Width Modulator (PWM)

PCA Timer/Counter

The PCA timer is a free-running 16-bit timer consisting of registers CH and CL (the high and low bytes of the count values). The PCA timer is common time base for all five modules and can be programmed to run at: 1/6 the oscillator frequency, 1/2 the oscillator frequency, Timer 0 overflow, or the input on the ECI pin (P1.2). The timer/counter source is determined from the CPS1 and CPS0 bits in the CMOD SFR as follows (see “PCA Timer/Counter Mode Register (CMOD)” on page 28):

Table 18: PCA Timer/Counter Source

CPS1	CPS0	12 Clock Mode	6 Clock Mode
0	0	f_{OSC} /12	f_{OSC} /6
0	1	f_{OSC} /4	f_{OSC} /2
1	0	Timer 0 overflow	Timer 0 overflow
1	1	External clock at ECI pin (maximum rate = f_{OSC} /8)	External clock at ECI pin (maximum rate = f_{OSC} /4)

T0-0.0 25093

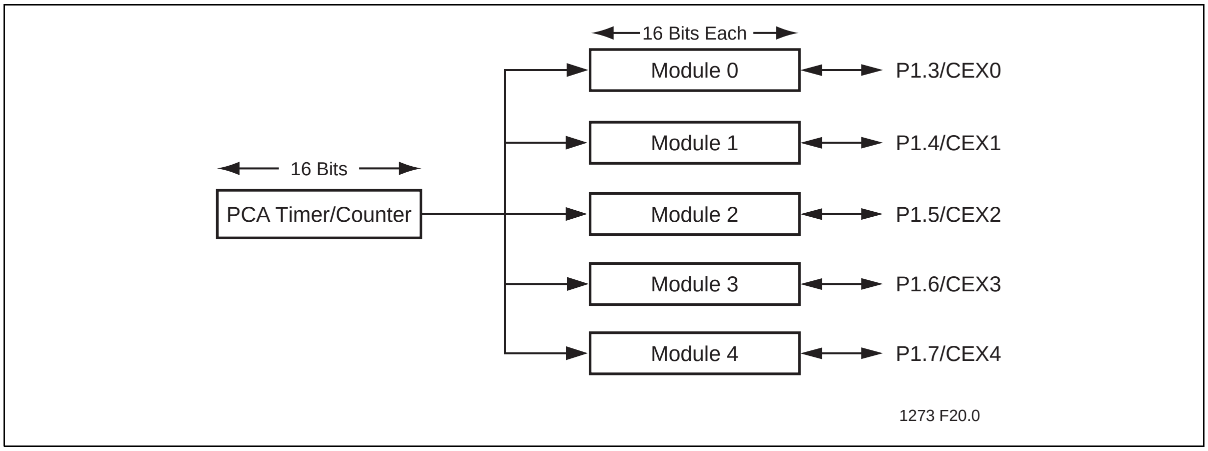


Figure 24: PCA Timer/Counter and Compare/Capture Modules

The table below summarizes various clock inputs at two common frequencies.

Table 19: PCA Timer/Counter Inputs

	Clock Increments	
PCA Timer/Counter Mode	**12 MHz**	**16 MHz**
Mode 0: $f_{OSC}/12$	1 µsec	0.75 µsec
Mode 1:	330 nsec	250 nsec
Mode 2: Timer 0 Overflows[1]		
Timer 0 programmed in:		
8-bit mode	256 µsec	192 µsec
16-bit mode	65 msec	49 µsec
8-bit auto-reload	1 to 255 µsec	0.75 to 191 µsec
Mode 3: External Input MAX	0.66 µsec	0.50 µsec

T0-0.0 25093

[1] In Mode 2, the overflow interrupt for Timer 0 does not need to be enabled.

The four possible CMOD timer modes with and without the overflow interrupt enabled are shown below. This list assumes that PCA will be left running during idle mode.

Table 20: CMOD Values

	CMOD Value	
PCA Count Pulse Selected	**Without Interrupt Enabled**	**With Interrupt Enabled**
Internal clock, $f_{OSC}/12$	00H	01H
Internal clock, $f_{OSC}/4$	02H	03H
Timer 0 overflow	04H	05H
External clock at P1.2	06H	07H

T0-0.0 25093

The CCON register is associated with all PCA timer functions. It contains run control bits and flags for the PCA timer (CF) and all modules. To run the PCA the CR bit (CCON.6) must be set by software. Clearing the bit, will turn off PCA. When the PCA counter overflows, the CF (CCON.7) will be set, and

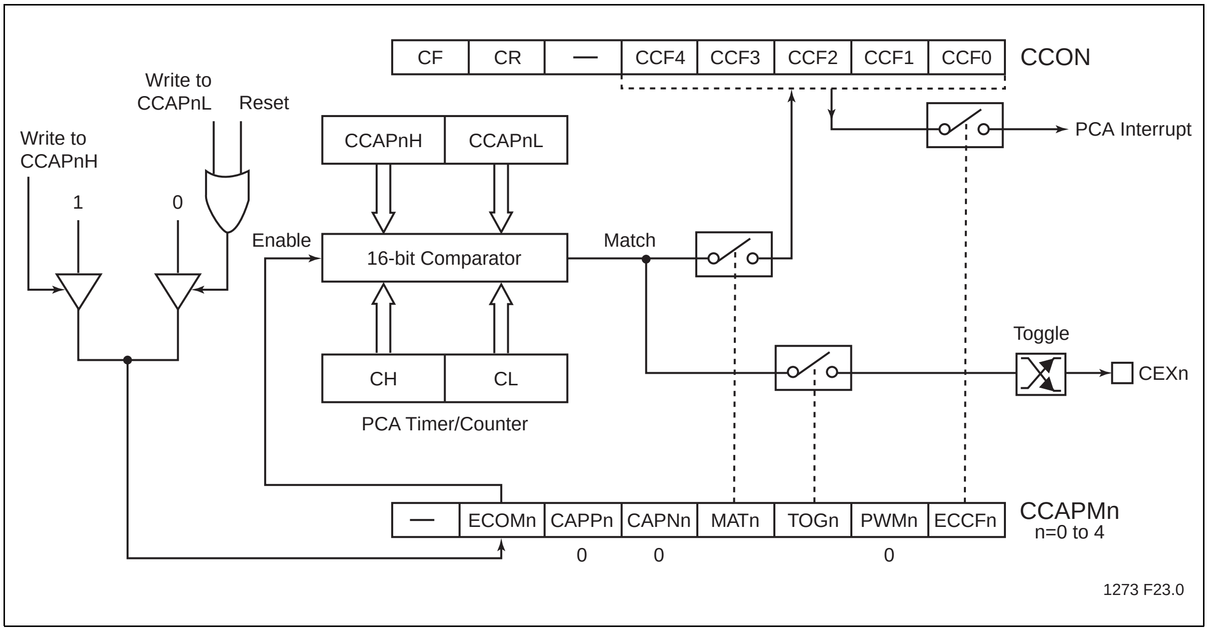


Figure 27:PCA High Speed Output Mode

Pulse Width Modulator

The Pulse Width Modulator (PWM) mode is used to generate 8-bit PWMs by comparing the low byte of the PCA timer (CL) with the low byte of the compare register (CCAPnL). When CL < CCAPnL the output is low. When CL ≥ CCAPnL the output is high. To activate this mode, the user must set the PWM and ECOM bits in the module's CCAPMn SFR. (See Figure 28 and Table 24)

In PWM mode, the frequency of the output depends on the source for the PCA timer. Since there is only one set of CH and CL registers, all modules share the PCA timer and frequency. Duty cycle of the output is controlled by the value loaded into the high byte (CCAPnH). Since writes to the CCAPnH register are asynchronous, a new value written to the high byte will not be shifted into CCAPnL for comparison until the next period of the output (when CL rolls over from 255 to 00).

To calculate values for CCAPnH for any duty cycle, use the following equation:

CCAPnH = 256(1 - Duty Cycle)

where CCAPnH is an 8-bit integer and Duty Cycle is a fraction.

Table 26: Security Lock Access Table

Level	SFST[7:5]	Source Address[1]	Target Address[2]	Byte-Verify Allowed		MOVC Allowed
				External Host[3]	IAP	516RDx
1	000b (unlock)	Block 0	Block 0	Y	N	Y
			Block 1	Y	Y	Y
			External	N/A	N/A	N
		Block 1	Block 0	Y	Y	Y
			Block 1	Y	N	Y
			External	N/A	N/A	N
		External	Block 0/1	Y	Y	N
			External	N/A	N/A	Y

T0-0.0 25093

1. Location of MOVC or IAP instruction
2. Target address is the location of the byte being read
3. External host Byte-Verify access does not depend on a source address.

Interrupts

Interrupt Priority and Polling Sequence

The device supports eight interrupt sources under a four level priority scheme. Table 27 summarizes the polling sequence of the supported interrupts. Note that the SPI serial interface and the UART share the same interrupt vector. (See Figure 32)

Table 27: Interrupt Polling Sequence

Description	Interrupt Flag	Vector Address	Interrupt Enable	Interrupt Priority	Service Priority	Wake-Up Power-down
Ext. Int0	IE0	0003H	EX0	PX0/H	1(highest)	yes
Brown-out	-	004BH	EBO	PBO/H	2	no
T0	TF0	000BH	ET0	PT0/H	3	no
Ext. Int1	IE1	0013H	EX1	PX1/H	4	yes
T1	TF1	001BH	ET1	PT1/H	5	no
PCA	CF/CCFn	0033H	EC	PPCH	6	no
Ext. Int. 2	IE2	003BH	EX2	PX2/H	7	no
Ext. Int. 3	IE3	0043H	EX3	PX3/H	8	no
UART/SPI	TI/RI/SPIF	0023H	ES	PS/H	9	no
T2	TF2, EXF2	002BH	ET2	PT2/H	10	no

T0-0.0 25093

System Clock and Clock Options

Clock Input Options and Recommended Capacitor Values for Oscillator

Shown in Figure 33 are the input and output of an internal inverting amplifier (XTAL1, XTAL2), which can be configured for use as an on-chip oscillator.

When driving the device from an external clock source, XTAL2 should be left disconnected and XTAL1 should be driven.

At start-up, the external oscillator may encounter a higher capacitive load at XTAL1 due to interaction between the amplifier and its feedback capacitance. However, the capacitance will not exceed 15 pF once the external signal meets the V_{IL} and V_{IH} specifications.

Crystal manufacturer, supply voltage, and other factors may cause circuit performance to differ from one application to another. C1 and C2 should be adjusted appropriately for each design. Table 29, shows the typical values for C1 and C2 vs. crystal type for various frequencies

Table 29: Recommended Values for C1 and C2 by Crystal Type

Crystal	C1 = C2
Quartz	20-30pF
Ceramic	40-50pF

T0-0.0 25093

More specific information about on-chip oscillator design can be found in the ***FlashFlex Oscillator Circuit Design Considerations*** application note.

Clock Doubling Option

By default, the device runs at 12 clocks per machine cycle (x1 mode). The device has a clock doubling option to speed up to 6 clocks per machine cycle. Please refer to Table 30 for detail.

Clock double mode can be enabled either via the external host mode or the IAP mode. Please refer to Table 14 for the IAP mode enabling commands (When set, the EDC# bit in SFST register will indicate 6 clock mode.).

The clock double mode is only for doubling the internal system clock and the internal flash memory, i.e. EA#=1. To access the external memory and the peripheral devices, careful consideration must be taken. Also note that the crystal output (XTAL2) will not be doubled.

1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 15mA
   Maximum I_{OL} per 8-bit port: 26mA
   Maximum I_{OL} total for all outputs: 71mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Capacitive loading on Ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and Ports 1 & 3. The noise due to external bus capacitance discharging into the Port 0 & 2 pins when the pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
3. Load capacitance for Port 0, ALE & PSEN#= 100pF, load capacitance for all other outputs = 80pF.
4. Capacitive loading on Ports 0 & 2 may cause the V_{OH} on ALE and PSEN# to momentarily fall below the V_{DD} - 0.7 specification when the address bits are stabilizing.
5. Pins of Ports 1, 2, and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
6. Pin capacitance is characterized but not tested. EA# is 25pF (max).

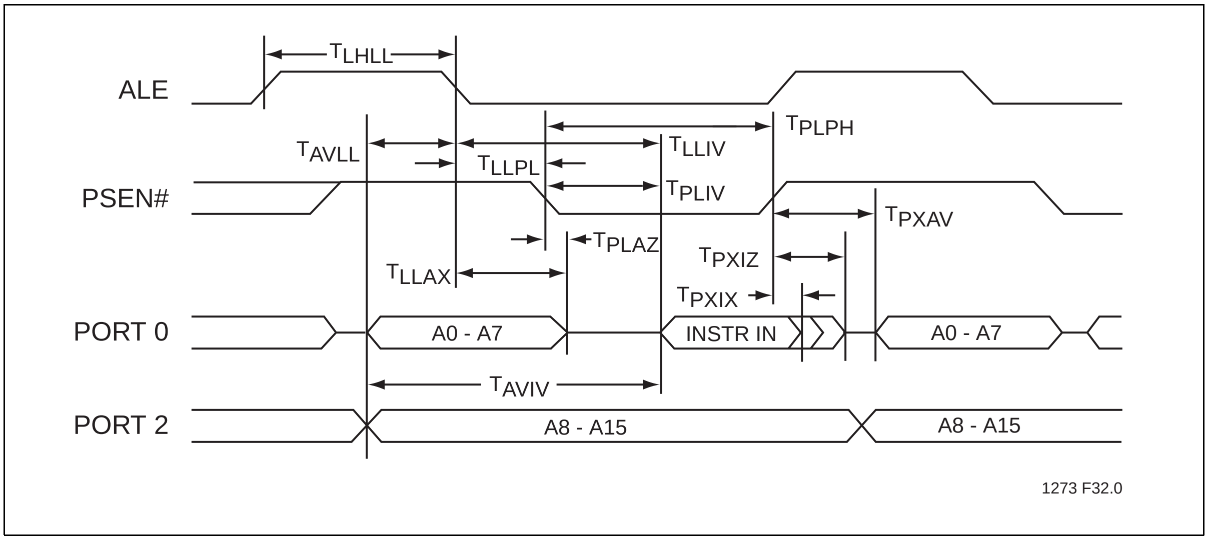


Figure 36: External Program Memory Read Cycle

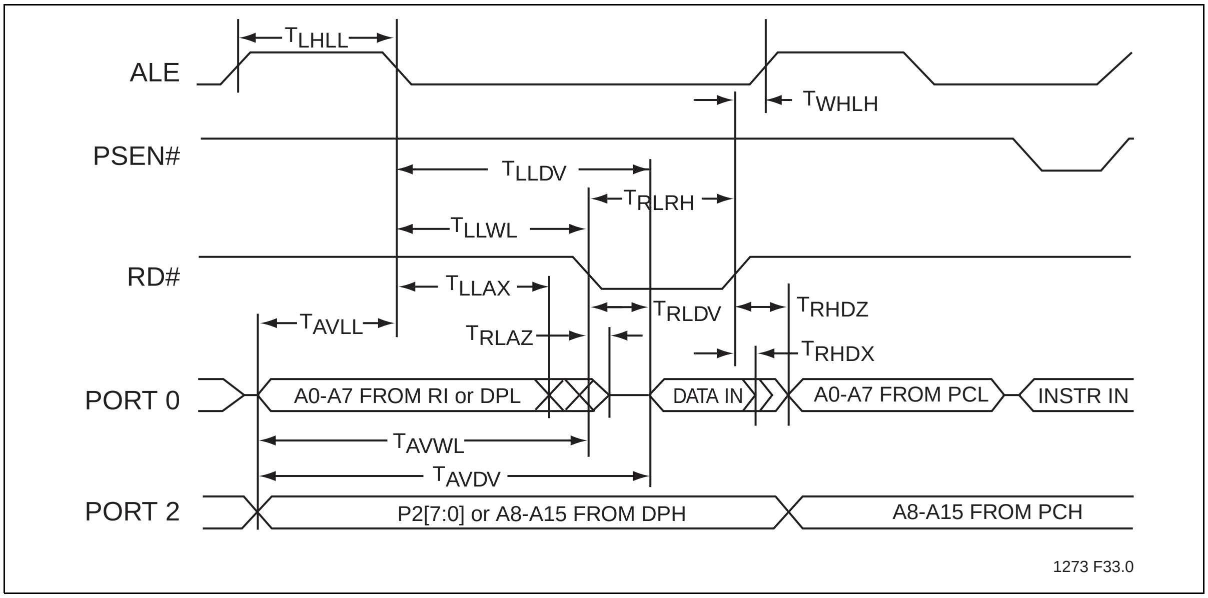


Figure 37: External Data Memory Read Cycle

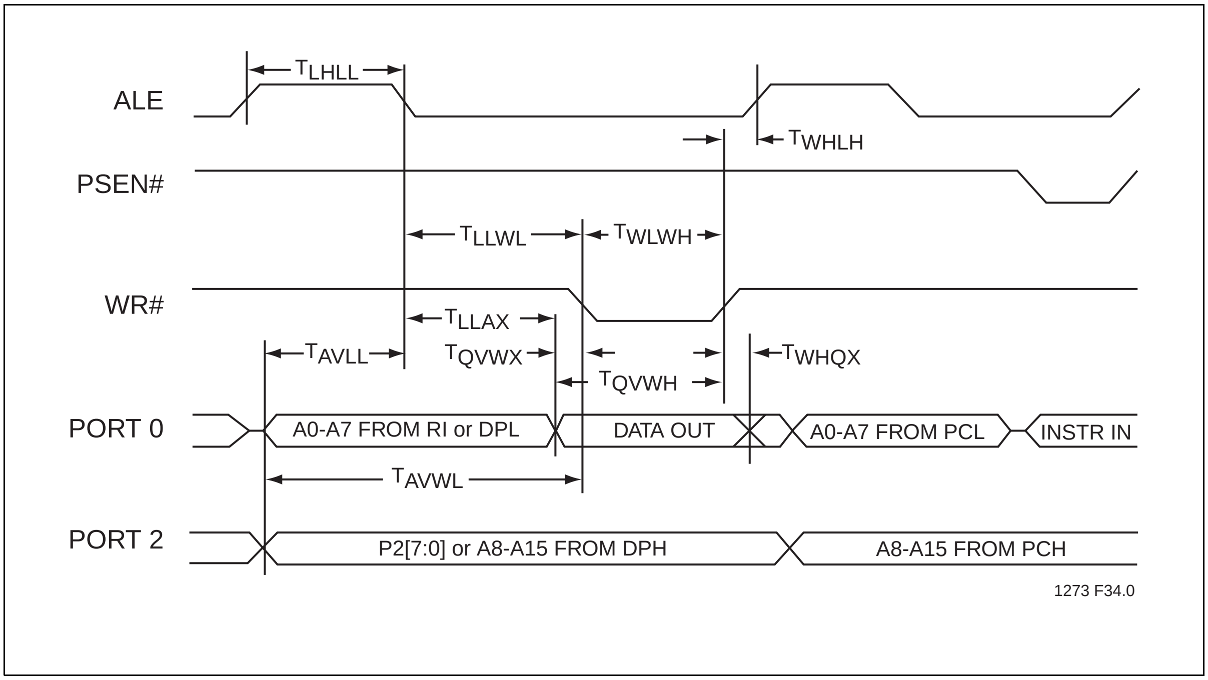


Figure 38: External Data Memory Write Cycle

Table 39: External Clock Drive

		Oscillator						
		12MHz		**40MHz**		**Variable**		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
$1/T_{CLCL}$	Oscillator Frequency					0	40	MHz
T_{CLCL}		83		25				ns
T_{CHCX}	High Time			8.75		$0.35T_{CLCL}$	$0.65T_{CLCL}$	ns
T_{CLCX}	Low Time			8.75		$0.35T_{CLCL}$	$0.65T_{CLCL}$	ns
T_{CLCH}	Rise Time		20		10			ns
T_{CHCL}	Fall Time		20		10			ns

T0-0.0 25093

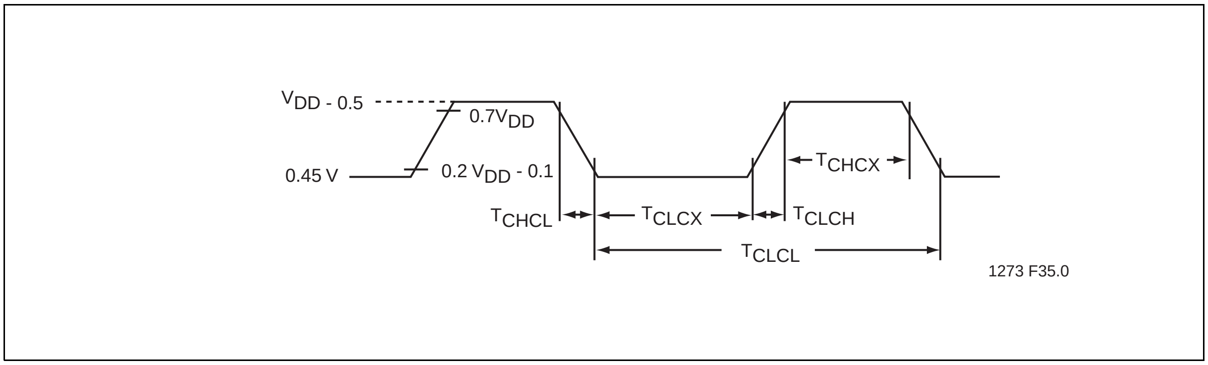


Figure 39: External Clock Drive Waveform