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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | - |
| Core Size | - |
| Speed | - |
| Connectivity | - |
| Peripherals | - |
| Number of I/O | - |
| Program Memory Size | - |
| Program Memory Type | - |
| EEPROM Size | - |
| RAM Size | - |
| Voltage - Supply (Vcc/Vdd) | - |
| Data Converters | - |
| Oscillator Type | - |
| Operating Temperature | - |
| Mounting Type | - |
| Package / Case | - |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/ia186ebplc84ir2 |

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3737 Princeton Drive NE, Suite 130, Albuquerque, NM 87107

# LIST OF FIGURES

# 1. Introduction

The Innovasic Semiconductor IA186EB and IA188EB microcontrollers are form, fit, and function replacements for the original Intel® 80C186EB, 80C188EB, 80L186EB, and 80L188EB 16-bit high-integration embedded processors.

These devices are produced using Innovasic's Managed IC Lifetime Extension System (MILES™). This cloning technology, which produces replacement ICs beyond simple emulations, ensures complete compatibility with the original device, including any "undocumented features." Additionally, the MILES process captures the clone design in such a way that production of the clone can continue even as silicon technology advances.

The IA186EB and IA188EB microcontrollers replace the obsolete Intel 80C186EB and 80C188EB devices, allowing users to retain existing board designs, software compilers/assemblers, and emulation tools, thereby avoiding expensive redesign efforts.

## 1.1 General Description

The Innovasic Semiconductor IA186EB and IA188EB microcontrollers are an upgrade for the 80C186EB/80C188EB microcontroller designs with integrated peripherals to provide increased functionality and reduce system costs. The IA186EB and IA188EB devices are designed to satisfy requirements of embedded products designed for telecommunications, office automation and storage, and industrial controls.

The IA186EB and IA188EB microcontrollers have a set of base peripherals beneficial to many embedded applications and include a standard numeric interface, an interrupt control unit, a chip-select unit, a DRAM refresh control unit, a power management unit, and three 16-bit timer/counters.

The IA186EB and IA188EB microcontrollers are capable of operating at 5.0 or 3.3 volts. This datasheet discusses both modes of operation. Where applicable, characteristics specific to either 3.3 or 5.0 volt operation are identified separately throughout this datasheet.

Additionally, the IA186EB and IA188EB include two integrated serial ports that support both synchronous and asynchronous communications, simplifying inter-processor and display communications. The IA186EB and IA188EB also have an enhanced chip-select unit and two multiplexed I/O ports. The enhanced chip-select unit offers 10 general chip selects, each with the ability to address up to 1 Mbyte. This enhanced unit enables memory-bank switching to expand the IA186EB/IA188EB 1 Mbyte address space. The I/O ports allow for basic functions such as scanning keypads for input. The ports can also be used to control system power consumption, disabling unneeded components.

The serial ports, I/O capabilities, and enhanced chip selects make the IA186EB/IA188EB an excellent processor for portable data acquisition or communication applications.

## 1.2 Features

The primary features of the IA186EB and IA188EB microcontrollers are as follows:

- Low-Power Operating Modes
  - Idle (freezes CPU clocks; peripherals are kept active)
  - Power-Down (freezes all internal clocks)
- Low-Power CPU Core (static)
- Direct Addressing Capability
  - Memory: 1 Mbyte
  - I/O: 64 Kbyte
- I/O Ports
  - 2 each, 8-Bit
  - Multiplexed
- Clock Generator
- Chip Selects
  - 10 each, Programmable
  - Integral Wait-State Generator
- Memory Refresh Control Unit
- Interrupt Controller, Programmable
- Counter/Timers
  - 3 each, 16-Bit
  - Programmable
- Serial Channels
  - 2 each, UARTs
  - Integral Baud Rate Generator
- Operating Frequency (system clock input)
  - 50 MHz @ 5V
  - 32 MHz @ 3.3V

Chapter 4, Functional Description, provides details of the IA186EB and IA188EB microcontrollers, including the features listed above.

# 2. Packaging, Pin Descriptions, and Physical Dimensions

Information on the packages and pin descriptions for the IA186EB and the IA188EB is provided separately. Refer to sections, figures, and tables for information on the device of interest.

## 2.1 Packages and Pinouts

The Innovasic Semiconductor IA186EB and IA188EB microcontroller is available in the following packages:

- 84-Pin Plastic Leaded Chip Carrier (PLCC), equivalent to original PLCC package
- 80-Pin Plastic Quad Flat Pack (PQFP), equivalent to original PQFP package
- 80-Pin Low-Profile Quad Flat Pack (LQFP), equivalent to original SQFP package

### 2.1.5 IA188EB 80 PQFP Package

The pinout for the IA188EB 80 PQFP Package is as shown in Figure 5. The corresponding pinout is provided in Table 4.

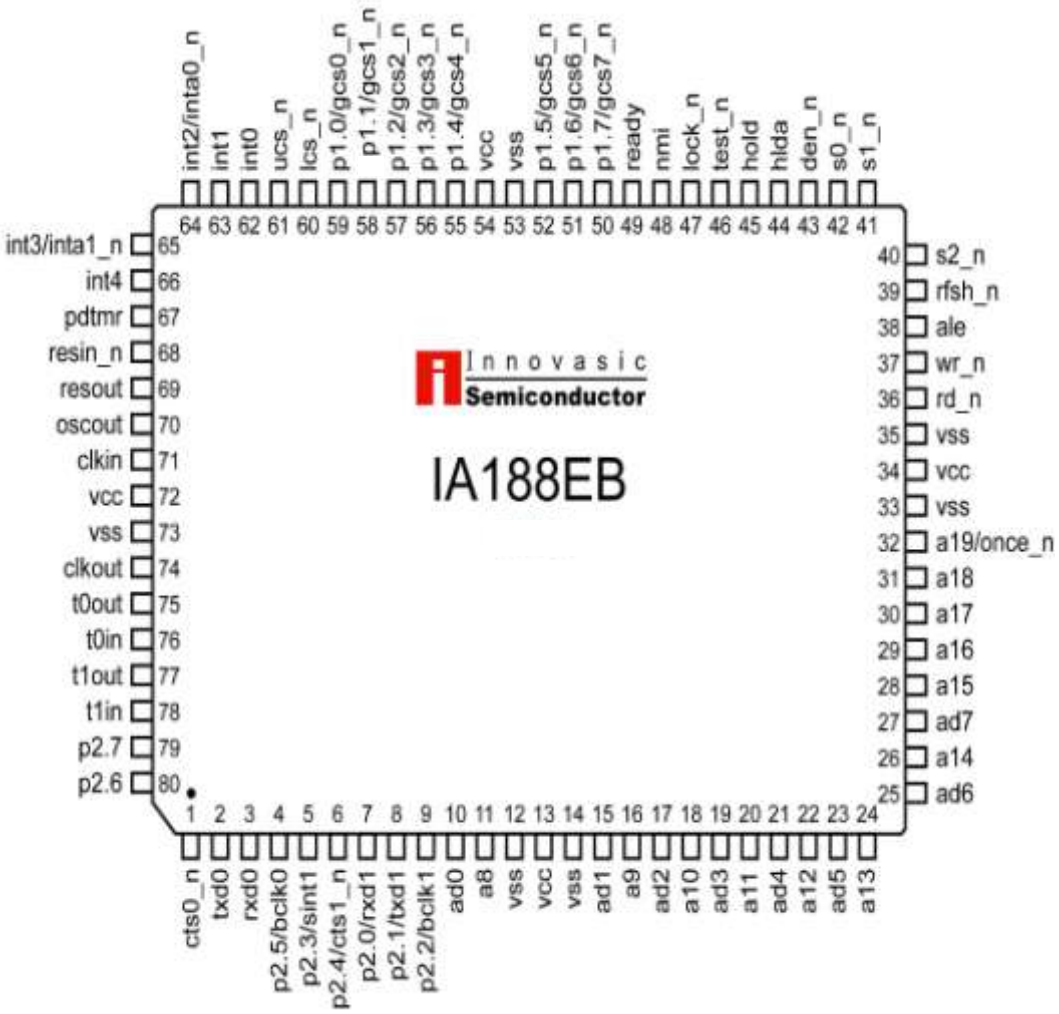


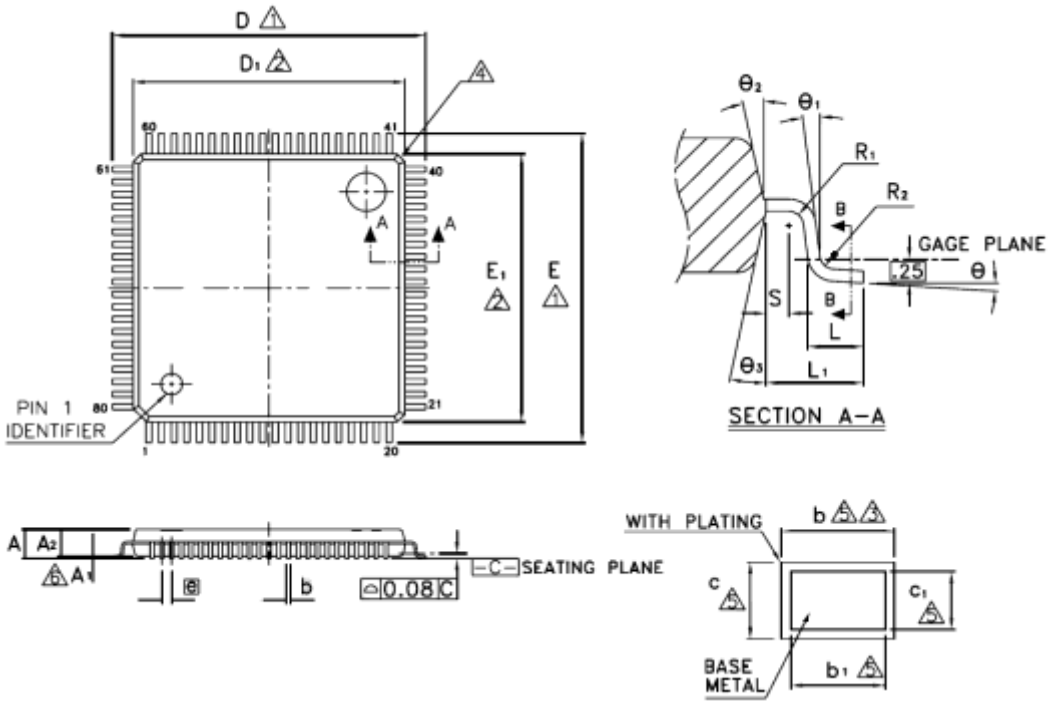

**Figure 5. IA188EB 80-Pin PQFP Package Diagram**

## Table 6. IA188EB 80-Pin LQFP Pin Listing

| Pin | Name | Pin | Name | Pin | Name | Pin | Name |
|---|---|---|---|---|---|---|---|
| 1 | hlda | 21 | int2/inta0_n | 41 | p2.5/bclk0 | 61 | a13 |
| 2 | hold | 22 | int3/inta1_n | 42 | p2.3/sint1 | 62 | ad6 |
| 3 | test_n | 23 | int4 | 43 | p2.4/cts1_n | 63 | a14 |
| 4 | lock_n | 24 | pdtmr | 44 | p2.0/rxd1 | 64 | ad7 |
| 5 | nmi | 25 | resin_n | 45 | p2.1/txd1 | 65 | a15 |
| 6 | ready | 26 | resout | 46 | p2.2/bclk1 | 66 | a16 |
| 7 | p1.7/gcs7_n | 27 | oscout | 47 | ad0 | 67 | a17 |
| 8 | p1.6/gcs6_n | 28 | clkin | 48 | a8 | 68 | a18 |
| 9 | p1.5/gcs5_n | 29 | $V_{cc}$ | 49 | $V_{ss}$ | 69 | a19/once_n |
| 10 | $V_{ss}$ | 30 | $V_{ss}$ | 50 | $V_{cc}$ | 70 | $V_{ss}$ |
| 11 | $V_{cc}$ | 31 | clkout | 51 | $V_{ss}$ | 71 | $V_{cc}$ |
| 12 | p1.4/gcs4_n | 32 | t0out | 52 | ad1 | 72 | $V_{ss}$ |
| 13 | p1.3/gcs3_n | 33 | t0in | 53 | a9 | 73 | rd_n |
| 14 | p1.2/gcs2_n | 34 | t1out | 54 | ad2 | 74 | wr_n |
| 15 | p1.1/gcs1_n | 35 | t1in | 55 | a10 | 75 | ale |
| 16 | p1.0/gcs0_n | 36 | p2.7 | 56 | ad3 | 76 | rfsh_n |
| 17 | lcs_n | 37 | p2.6 | 57 | a11 | 77 | s2_n |
| 18 | ucs_n | 38 | cts0_n | 58 | ad4 | 78 | s1_n |
| 19 | int0 | 39 | txd0 | 59 | a12 | 79 | s0_n |
| 20 | int1 | 40 | rxd0 | 60 | ad5 | 80 | den_n |

### 2.1.9 LQFP Physical Dimensions

The physical dimensions for the 80 LQFP are as shown in Figure 9.




Legend:

| Symbol | Dimension in mm Min | Nom | Max | Dimension in Inch Min | Mom | Max |
|---|---|---|---|---|---|---|
| A | – | – | 1.60 | – | – | 0.063 |
| $A_1$ | 0.05 | – | 0.15 | 0.002 | – | 0.006 |
| $A_2$ | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| b | 0.17 | 0.22 | 0.27 | 0.007 | 0.009 | 0.011 |
| $b_1$ | 0.17 | 0.20 | 0.23 | 0.007 | 0.008 | 0.009 |
| c | 0.09 | – | 0.20 | 0.004 | – | 0.008 |
| $c_1$ | 0.09 | – | 0.16 | 0.004 | – | 0.006 |
| D | 14.00 BSC | | | 0.551 BSC | | |
| $D_1$ | 12.00 BSC | | | 0.472 BSC | | |
| E | 14.00 BSC | | | 0.551 BSC | | |
| $E_1$ | 12.00 BSC | | | 0.472 BSC | | |
| e | 0.50 BSC | | | 0.020 BSC | | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| $L_1$ | 1.00 REF | | | 0.039 REF | | |
| $R_1$ | 0.08 | – | – | 0.003 | – | – |
| $R_2$ | 0.08 | – | 0.20 | 0.003 | – | 0.008 |
| S | 0.20 | – | – | 0.008 | – | – |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| $\theta_1$ | 0° | – | – | 0° | – | – |
| $\theta_2$ | 11° | 12° | 13° | 11° | 12° | 13° |
| $\theta_3$ | 11° | 12° | 13° | 11° | 12° | 13° |

1. To be determined at seating plane C.
2. Dimensions D1 and E1 do not include mold protrusion. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Dimension b does not include dambar protrusion. Dambar cannot be located on the lower radius of the foot.
4. Exact shape of each corner is optional.
5. These dimensions apply to the flat section of the lead between 0.10 and 0.25mm from the lead tip.
6. A1 is defined as the distance from the seating plane to the lowest point of the package body.

Notes:
1. Exact shape of each corner is optional.
2. Controlling dimension: mm.

**Figure 9. 80-Pin LQFP Physical Package Dimensions**

## 2.2 IA186EB Pin/Signal Descriptions

Descriptions of the pin and signal functions for the IA186EB microcontroller are provided in Table 7.

Several of the IA186EB pins have different functions depending on the operating mode of the device. Each of the different signals supported by a pin is listed and defined in Table 7—indexed alphabetically in the first column of the table. Additionally, the name of the pin associated with the signal as well as the pin numbers for the PLCC, LQFP, and PQFP packages are provided in the "Pin" column. Signals not used in a specific package type are designated "NA."

**Table 7. IA186EB Pin/Signal Descriptions**

| Signal | Pin | | | | Description |
|---|---|---|---|---|---|
| | Name | PLCC | LQFP | PQFP | |
| a16 (output only) | a16 | 80 | 66 | 29 | **a**ddress Bits [**16–19**]. Input/Output. These pins provide the four most-significant bits of the Address Bus. During the address portion of the IA186EB bus cycle, Address Bits [16–19] are presented on the bus and can be latched using the ale signal (see table entry). During the data portion of the IA186EB bus cycle, these lines are driven to a logic 0. |
| a17 (output only) | a17 | 81 | 67 | 30 | |
| a18 (output only) | a18 | 82 | 68 | 31 | |
| a19 | **a19**/once_n | 83 | 69 | 32 | |
| ad0 | ad0 | 61 | 47 | 10 | **a**ddress/**d**ata Bits [**0–15**]. Input/Output. These pins provide the multiplexed Address Bus and Data Bus. During the address portion of the IA186EB bus cycle, Address Bits [0–15] are presented on the bus and can be latched using the ale signal (see next table entry). During the data portion of the IA186EB bus cycle, 8- or 16-bit data are present on these lines. |
| ad1 | ad1 | 66 | 52 | 15 | |
| ad2 | ad2 | 68 | 54 | 17 | |
| ad3 | ad3 | 70 | 56 | 19 | |
| ad4 | ad4 | 72 | 58 | 21 | |
| ad5 | ad5 | 74 | 60 | 23 | |
| ad6 | ad6 | 76 | 62 | 25 | |
| ad7 | ad7 | 78 | 64 | 27 | |
| ad8 | ad8 | 62 | 48 | 11 | |
| ad9 | ad9 | 67 | 53 | 16 | |
| ad10 | ad10 | 69 | 55 | 18 | |
| ad11 | ad11 | 71 | 57 | 20 | |
| ad12 | ad12 | 73 | 59 | 22 | |
| ad13 | ad13 | 75 | 61 | 24 | |
| ad14 | ad14 | 77 | 63 | 26 | |
| ad15 | ad15 | 79 | 65 | 28 | |

**Table 7. IA186EB Pin/Signal Descriptions** *(Continued)*

| Signal | Pin | | | | Description |
|---|---|---|---|---|---|
| | Name | PLCC | LQFP | PQFP | |
| clkin | clkin | 41 | 28 | 71 | **cl**oc**k in**put. Input. The **clkin** pin is the input connection for an external clock. An external oscillator operating at two times the required processor operating frequency can be connected to this pin.<br><br>If a crystal is used to supply the clock, it is connected between the **clkin** pin and the **oscout** pin (see oscout table entry). When a crystal is connected, it drives an internal Pierce oscillator to the IA186EB. |
| clkout | clkout | 44 | 31 | 74 | **cl**oc**k out**put. Output. The **clkout** pin provides a timing reference for inputs and outputs of the IA186EB. This clock output is one-half the input clock (**clkin**) frequency. The **clkout** signal has a 50% duty cycle, transitioning every falling edge of **clkin**. |
| cts0_n | cts0_n | 51 | 38 | 1 | **c**lear **t**o **s**end, Serial Port **0**. Input. Active Low. When this input is high (i.e., not asserted), data transmission from Serial Port 0 is inhibited. When the signal is asserted (low), data transmission is permitted. |
| cts1_n | p2.4/**cts1_n** | 56 | 43 | 6 | **c**lear **t**o **s**end, Serial Port **1**. Input. Active Low. When this input is high (i.e., not asserted), data transmission from Serial Port 1 is inhibited. When the signal is asserted (low), data transmission is permitted. |
| den_n | den_n | 11 | 80 | 43 | **d**ata **en**able. Output. Active Low. This signal is used to enable of bidirectional transceivers in a buffered system. The **den_n** signal is asserted (low) only when data is to be transferred on the bus. |
| dt/r_n | dt/r_n | 16 | NA | NA | **d**ata **t**ransmit/**r**eceive. Output. This signal is used to control the direction of data flow for bidirectional buffers in a buffered system. When **dt/r_n** is high, the direction indicated is transmit; when **dt/t_n** is low, the direction indicated is receive. |
| error_n | error_n | 3 | NA | NA | **error**. Input. Active Low. When this signal is asserted (low), it indicates that the last numerics coprocessor operation resulted in an exception condition. |

**Table 8. IA188EB Pin/Signal Descriptions** *(Continued)*

| Signal | Pin | | | | Description |
|---|---|---|---|---|---|
| | Name | PLCC | LQFP | PQFP | |
| test_n | test_n | 14 | 3 | 46 | **test**. Input. Active Low. When the **test_n** input is high (i.e., not asserted), it causes the IA188EB to suspend operation during the execution of the WAIT instruction. Operation resumes when the pin is sampled low (asserted). |
| txd0 | txd0 | 52 | 39 | 2 | Transmit (**tx**) **d**ata, Serial Port **0**. Output. This pin is the serial data output for Serial Port 0. During synchronous serial communications, **txd0** becomes the transmit clock (**rxd0** functions as an output for data transmission). |
| txd1 | p2.1/txd1 | 58 | 45 | 8 | Transmit (**tx**) **d**ata, Serial Port **1**. Output. This pin is the serial data output for Serial Port 1. During synchronous serial communications, **txd1** becomes the transmit clock (**rxd1** functions as an output for data transmission). |
| ucs_n | ucs_n | 30 | 18 | 61 | **u**pper **c**hip **s**elect. Output. Active Low. This pin provides a chip select signal that will be asserted (low) whenever the address of a memory bus cycle is within the address space programmed for that output. |
| $V_{CC}$ | $V_{CC}$ | 1, 23, 42, 64 | 11, 29, 50, 71 | 13, 34, 54, 72 | Power ($\mathbf{V_{CC}}$). This pin provides power for the IA188EB device. It must be connected to a +5V DC power source. |
| $V_{SS}$ | $V_{SS}$ | 2, 22, 43, 63, 65, 84 | 10, 30, 49, 51, 70, 72 | 12, 14, 33, 35, 53, 73 | Ground ($\mathbf{V_{SS}}$). This pin provides the digital ground (0V) for the IA188EB. It must be connected to a $\mathbf{V_{SS}}$ board plane. |
| wr_n | wr_n | 5 | 74 | 37 | **wr**ite. Output. Active Low. When asserted (low), **wr_n** indicates that data available on the data bus are to be latched into the accessed memory or I/O device. |

# 3. Maximum Ratings, Thermal Characteristics, and DC Parameters

For the Innovasic Semiconductor IA186EB and IA188EB microcontrollers, the absolute maximum ratings, thermal characteristics, and DC parameters are provided in Tables 9 through 11, respectively.

### Table 9. IA186EB and IA188EB Absolute Maximum Ratings

| Parameter | Rating |
|---|---|
| Storage Temperature | −40°C to +125°C |
| Supply Voltage with Respect to $v_{ss}$ | −0.3V to +6.0V |
| Voltage on Pins other than Supply with Respect to $v_{ss}$ | −0.3V to +(Vcc + 0.3)V |

### Table 10. IA186EB and IA188EB Thermal Characteristics

| Symbol | Characteristic | Value | Units |
|---|---|---|---|
| $T_A$ | Ambient Temperature | -40°C to 85°C | °C |
| $P_D$ | Power Dissipation | MHz × ICC × V/1000 | W |
| $\Theta_{Ja}$ | 84-Pin PLCC Package | 30.7 | °C/W |
| | 80-Pin PQFP Package | 46 | |
| | 80-Pin LQFP Package | 52 | |
| $T_J$ | Average Junction Temperature | $T_A + (P_D \times \Theta_{Ja})$ | °C |

### 4.1.7 I/O Port Unit

The I/O Port Unit (IPU) on the IA186EB/IA188EB supports two 8-bit channels of input, output, or input/output operation. Port 1 is multiplexed with the chip select pins and is output only. Most of Port 2 is multiplexed with the serial channel pins.

### 4.1.8 Refresh Control Unit

The Refresh Control Unit (RCU) automatically generates a periodic memory read bus cycle to keep dynamic or pseudo-static memory refreshed. A 9-bit counter controls the number of clocks between refresh requests.

A 12-bit address generator is maintained by the RCU and is presented on the a1–a12 address lines during the refresh bus cycle. Address Bits [a13–a19] are programmable to allow the refresh address block to be located on any 8-Kbyte boundary.

### 4.1.9 Power Management Unit

The IA186EB/IA188EB Power Management Unit (PMU) is provided to control the power consumption of the device. The PMU provides three power modes: Active, Idle, and Powerdown.

Active Mode indicates that all units on the IA186EB/IA188EB are functional and the device consumes maximum power (depending on the level of peripheral operation). Idle Mode freezes the clocks of the execution and bus units at a logic zero state (all peripherals continue to operate normally).

The Powerdown mode freezes all internal clocks at a logic zero level and disables the crystal oscillator. All internal registers hold their values provided $V_{CC}$ is maintained. Current consumption is reduced to just transistor junction leakage.

## 4.2 Peripheral Architecture

The IA186EB/IA188EB has integrated several common system peripherals with a CPU core to create a compact, yet powerful system. The integrated peripherals are designed to be flexible and provide logical interconnections between supporting units (e.g., the interrupt control unit supports interrupt requests from the timer/counters or serial channels). The list of integrated peripherals includes:

- 7-Input Interrupt Control Unit
- 3-Channel Timer/Counter Unit
- 2-Channel Serial Communications Unit
- 10-Output Chip-Select Unit
- I/O Port Unit
- Refresh Control Unit

**Table 12. Peripheral Control Block Registers** *(Continued)*

| PCB Offset | Function | PCB Offset | Function | PCB Offset | Function | PCB Offset | Function |
|---|---|---|---|---|---|---|---|
| 20H | Reserved | 60H | Serial0 Baud | A0H | LCS Start | E0H | Reserved |
| 22H | Reserved | 62H | Serial0 Count | A2H | LCS Stop | E2H | Reserved |
| PCB Offset | Offset | PCB Offset | Function | PCB Offset | Function | PCB Offset | Function |
| 24H | Reserved | 64H | Serial0 Control | A4H | UCS Start | E4H | Reserved |
| 26H | Reserved | 66H | Serial0 Status | A6H | UCS Stop | E6H | Reserved |
| 28H | Reserved | 68H | Serial0 RBUF | A8H | Relocation | E8H | Reserved |
| 2AH | Reserved | 6AH | Serial0 TBUF | AAH | Reserved | EAH | Reserved |
| 2CH | Reserved | 6CH | Reserved | ACH | Reserved | ECH | Reserved |
| 2EH | Reserved | 6EH | Reserved | AEH | Reserved | EEH | Reserved |
| 30H | Timer0 Count | 70H | Serial1 Baud | B0H | Refresh Base | F0H | Reserved |
| 32H | Timer0 Compare A | 72H | Serial1 Count | B2H | Refresh Time | F2H | Reserved |
| 34H | Timer0 Compare B | 74H | Serial1 Control | B4H | Refresh Control | F4H | Reserved |
| 36H | Timer0 Control | 76H | Serial1 Status | B6H | Refresh Address | F6H | Reserved |
| 38H | Timer1 Count | 78H | Serial1 RBUF | B8H | Power Control | F8H | Reserved |
| 3AH | Timer1 Compare A | 7AH | Serial1 TBUF | BAH | Reserved | FAH | Reserved |
| 3CH | Timer1 Compare B | 7CH | Reserved | BCH | Step ID[1] | FCH | Reserved |
| 3EH | Timer1 Control | 7EH | Reserved | BEH | Reserved | FEH | Reserved |

**Note:**

[1]The **Step ID** register (offset 0xBC) for Revision 2 of the Innovasic device is read-only, and is uniquely identified in software by having a value of 0x0080. The original Intel device established a value between 0x0000 and 0x0002, depending on the revision of the part.

For specific 5.0- and 3.3-volt characteristics, refer to Tables 13 and 14, respectively.

**Table 13. AC Input Characteristics for 5.0-Volt Operation**

| Symbol | Pins | Min | Max | Units |
|---|---|---|---|---|
| $t_{CHIS}$ | test_n, nmi, int4–int0, bclk1–bclk0, t1in–t0in, ready, cts1_n–cts0_n, p2.6, p2.7 | 10 | – | ns |
| $t_{CHIH}$ | test_n, nmi, int4–int0, bclk1–bclk0, t1in–t0in, ready, cts1_n–cts0_n | 3 | – | ns |
| $t_{CLIS}$ | ad15–ad0, ad7–ad0 (IA188EB), ready | 10 | – | ns |
| $t_{CLIS}$ | hold, pereq, error_n | 10 | – | ns |
| $t_{CLIH}$ | ad15–ad0, ad7–ad0 (IA188EB), ready | 3 | – | ns |
| $t_{CLIH}$ | hold, pereq, error_n | 3 | – | ns |

**Table 14. AC Input Characteristics for 3.3-Volt Operation**

| Symbol | Pins | Min | Max | Units |
|---|---|---|---|---|
| $t_{CHIS}$ | test_n, nmi, int4–int0, bclk1–bclk0, t1in–t0in, ready, cts1_n–cts0_n, p2.6, p2.7 | 10 | – | ns |
| $t_{CHIH}$ | test_n, nmi, int4–int0, bclk1–bclk0, t1in–t0in, ready, cts1_n–cts0_n | 3 | – | ns |
| $t_{CLIS}$ | ad15–ad0, ad7–ad0 (IA188EB), ready | 10 | – | ns |
| $t_{CLIS}$ | hold, pereq, error_n | 10 | – | ns |
| $t_{CLIH}$ | ad15–ad0, ad7–ad0 (IA188EB), ready | 3 | – | ns |
| $t_{CLIH}$ | hold, pereq, error_n | 3 | – | ns |

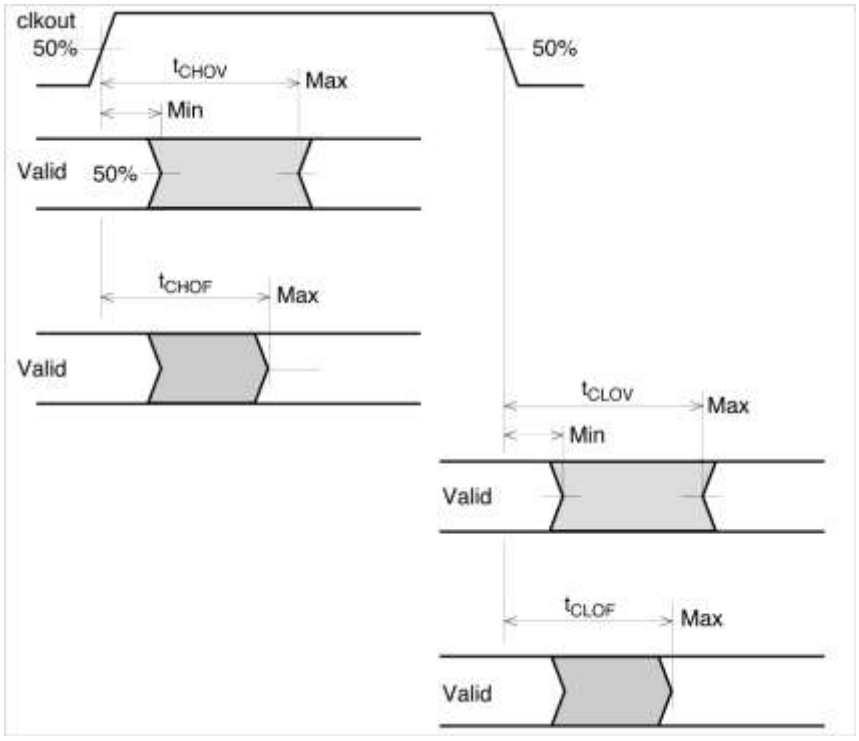



**Figure 13. AC Output Characteristics**

For specific 5.0- and 3.3-volt characteristics, refer to Tables 15 and 16, respectively.

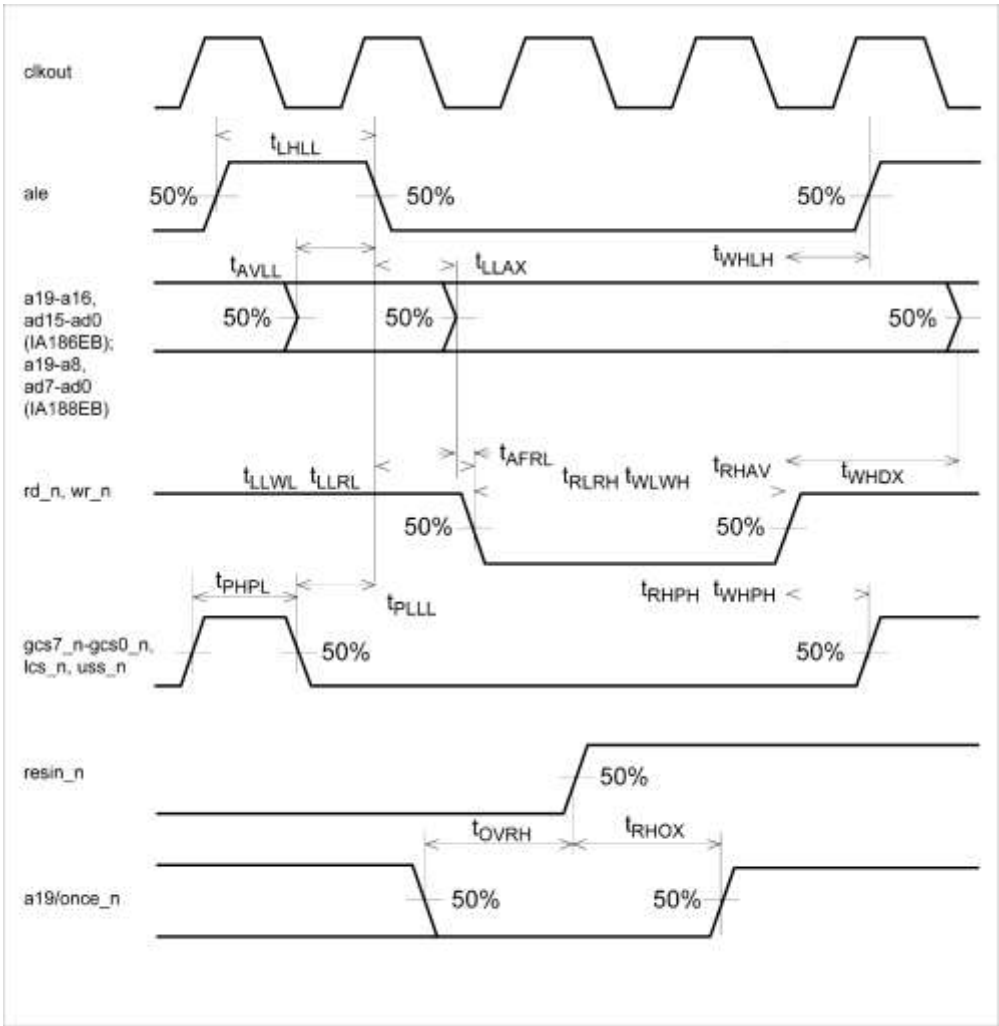



**Figure 14. Relative Timing Characteristics**

For specific relative timing characteristics, refer to Table 17.

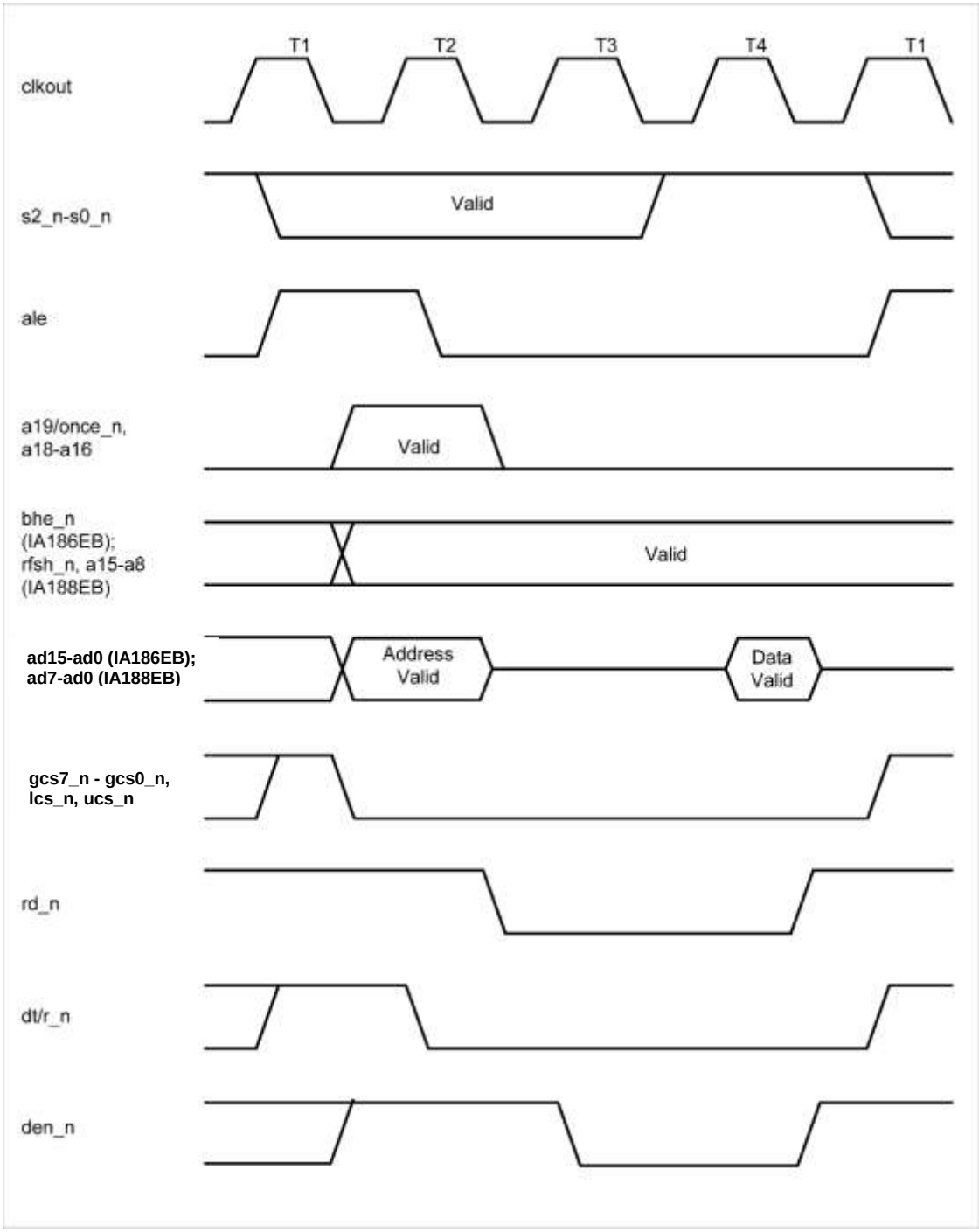



**Figure 20. Read, Fetch, and Refresh Cycle Timing**

**Table 21. Instruction Set Timing** *(Continued)*

| Instruction | Clock Cycles | | Comments |
|---|---|---|---|
| | IA186EB | IA188EB | |
| SHL Register/Memory by CL | 1/20 | 1/24 | register/memory |
| SHL Register/Memory by Count | 1/11 | 1/24 | |
| SHR Register/Memory by 1 | 1/5 | 1/24 | |
| SHR Register/Memory by CL | 1/20 | 1/28 | |
| SHR Register/Memory by Count | 1/11 | 1/24 | |
| SS | 1 | 1 | – |
| STC | 1 | 1 | – |
| SUB Immediate from accumulator | 1 | 1 | - |
| SUB Immediate from register/memory | 1/11 | 1/28 | register/memory |
| SUB Register/memory and register to either | 1/15 | 1/40 | |
| STD | 1 | 1 | – |
| STI | 1 | 1 | – |
| STOS | 6 | 8 | – |
| STOS (repeated n times) | 6+4n | 8+8n | – |
| TEST Immediate data and accumulator | 1 | 1 | – |
| TEST Immediate data and register/memory | 1/16 | 1/16 | register/memory |
| TEST Register/memory and register | 1/12 | 1/20 | register/memory |
| WAIT | 1 | 1 | test_n = 0 |
| XCHG Register with accumulator | 2 | 2 | – |
| XCHG Register/memory with register | 3/16 | 3/20 | register/memory |
| XLAT | 16 | 8 | – |
| XOR Immediate to accumulator | 1 | 1 | – |
| XOR Immediate to register/memory | 1/11 | 1/32 | register/memory |
| XOR Register/memory and register to either | 1/16 | 1/32 | register/memory |

### Errata No. 2

**Problem:** When the extension byte (mod field) is set to "11," some instructions will cause the CPU to hang.

**Description:** Although there are faster versions of each instruction (these are not commonly used by compilers), the following instructions will cause the CPU to hang when the extension byte (mod field) is set to "11":

- 8D (LEA)
- 8F (POP memory)
- C6 (MOV immediate8 to memory/register)
- C7 (MOV immediate16 to memory/register)
- FE (PUSH memory)
- FF (PUSH memory)

**Workaround:** Substitute instructions in the following table.

| Instruction | Workaround |
|---|---|
| 8D (LEA) | Use MOV register (89 or 8B) |
| 8F (POP memory) | Use POP register (0101_0xxx) |
| C6 (MOV immediate8 to memory/register) | Use MOV immediate8 to register (1011_0xxx) |
| C7 (MOV immediate16 to memory/register) | Use MOV immediate16 to register (1011_1xxx) |
| FE (PUSH memory) | Use PUSH register (0101_0xxx) |
| FF (PUSH memory) | Use PUSH register (0101_0xxx) |

### Errata No. 3

**Problem:** When the chip is put in SFNM mode for INT0 or INT1, the LVL bit is automatically set for those interrupts.

**Workaround:** None.

### Errata No. 8

**Problem:** Pin LOCK_n does not have an internal pullup.

**Description:** Because Pin LOCK_n does not have an internal pullup, it will float during reset and bus hold.

**Workaround:** An external pullup may be necessary if there is high external load on the signal.

### Errata No. 9

**Problem:**
The Relocation Register (RELREG, PCB offset 0xA8) can only be modified by an 8-bit write.

**Description:** The Relocation Register (RELREG, PCB offset 0xA8) can only be modified by an 8-bit write. A 16-bit write will have no effect. The 186 EB is unaffected.

**Workaround:** Use an 8-bit access to affect the RELREG register.

### Errata No. 10

**Problem:**
When the timer compare register for any of the timers is set to x0000, the max count is xFFFF instead of x10000 as in the OEM part.

**Description:** The timer output will change one count earlier than it should when the max count is set to x0000.

**Workaround:** The workaround is application dependent. Please contact Innovasic Technical Support if this erratum is an issue.

### Errata No. 11

**Problem:**
NMI cannot bring chip out of powerdown mode.

**Description:** Only a reset brings the part out of powerdown after a HLT instruction is executed with the PWRDN bit set in the PWRCON register.

**Workaround:** Use IDLE instead of PWRDN.