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Data Converters	-
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Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ia186ebplq80ir2

LIST OF TABLES

2. Packaging, Pin Descriptions, and Physical Dimensions

Information on the packages and pin descriptions for the IA186EB and the IA188EB is provided separately. Refer to sections, figures, and tables for information on the device of interest.

2.1 Packages and Pinouts

The Innovasic Semiconductor IA186EB and IA188EB microcontroller is available in the following packages:

- 84-Pin Plastic Leaded Chip Carrier (PLCC), equivalent to original PLCC package
- 80-Pin Plastic Quad Flat Pack (PQFP), equivalent to original PQFP package
- 80-Pin Low-Profile Quad Flat Pack (LQFP), equivalent to original SQFP package

Table 1. IA186EB 84-Pin PLCC Pin Listing

Pin	Name
1	V_{cc}
2	V_{ss}
3	error_n
4	rd_n
5	wr_n
6	ale
7	bhe_n
8	s2_n
9	s1_n
10	s0_n
11	den_n
12	hlda
13	hold
14	test_n/busy
15	lock_n
16	dt/r_n
17	nmi
18	ready
19	p1.7/gcs7_n
20	p1.6/gcs6_n
21	p1.5/gcs5_n

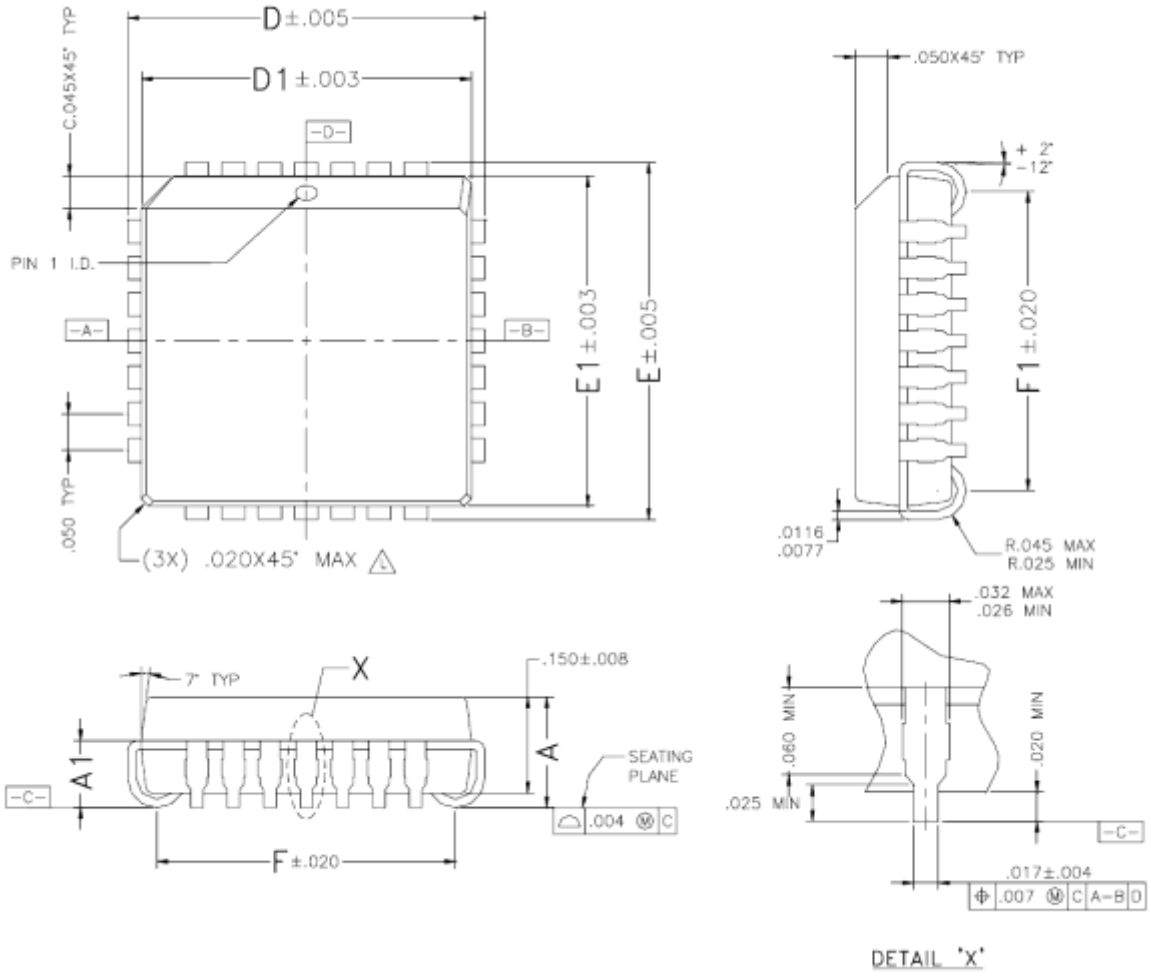
Pin	Name
22	V_{ss}
23	V_{cc}
24	p1.4/gcs4_n
25	p1.3/gcs3_n
26	p1.2/gcs2_n
27	p1.1/gcs1_n
28	p1.0/gcs0_n
29	lcs_n
30	ucs_n
31	int0
32	int1
33	int2/inta0_n
34	int3/inta1_n
35	int4
36	pdtmr
37	resin_n
38	resout
39	pereq
40	oscout
41	clkin
42	V_{cc}

Pin	Name
43	V_{ss}
44	clkout
45	t0out
46	t0in
47	t1out
48	t1in
49	p2.7
50	p2.6
51	cts0_n
52	txd0
53	rxd0
54	p2.5/bclk0
55	p2.3/sint1
56	p2.4/cts1_n
57	p2.0/rxd1
58	p2.1/txd1
59	p2.2/bclk1
60	ncs_n
61	ad0
62	ad8
63	V_{ss}

Pin	Name
64	V_{cc}
65	V_{ss}
66	ad1
67	ad9
68	ad2
69	ad10
70	ad3
71	ad11
72	ad4
73	ad12
74	ad5
75	ad13
76	ad6
77	ad14
78	ad7
79	ad15
80	a16
81	a17
82	a18
83	a19/once_n
84	V_{ss}

2.1.3 PLCC Physical Dimensions

The physical dimensions for the 84 PLCC are as shown in Figure 3.



Legend:

Symbol	Min	Nom	Max
A	0.165″	–	0.180″
A1	0.090″	–	0.120″
D	–	1.190″	–
D1	–	1.154″	–
E	–	1.190″	–
E1	–	1.154″	–
F	–	1.110″	–
F1	–	1.110″	–

Note: The bottom package is bigger than the top package by 0.004 inches (0.002 inches per side). Bottom package dimensions follow those stated in this drawing.

Figure 3. 84-Pin PLCC Physical Package Dimensions

2.1.4 IA186EB 80 PQFP Package

The pinout for the IA186EB 80 PQFP Package is as shown in Figure 4. The corresponding pinout is provided in Table 3.

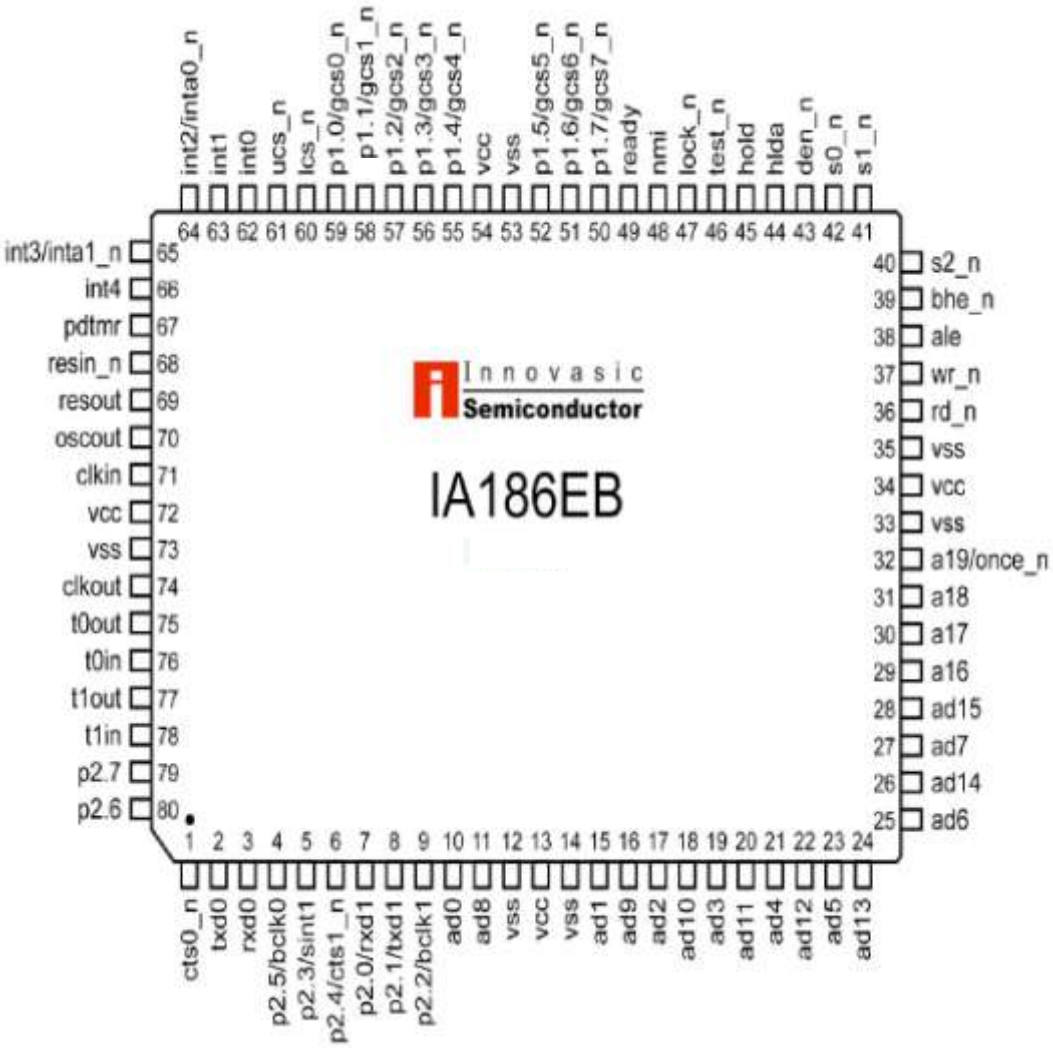


Figure 4. IA186EB 80-Pin PQFP Package Diagram

Table 5. IA186EB 80-Pin LQFP Pin Listing

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	hlda	21	int2/inta0_n	41	p2.5/bclk0	61	ad13
2	hold	22	int3/inta1_n	42	p2.3/sint1	62	ad6
3	test_n	23	int4	43	p2.4/cts1_n	63	ad14
4	lock_n	24	pdtmr	44	p2.0/rxd1	64	ad7
5	nmi	25	resin_n	45	p2.1/txd1	65	ad15
6	ready	26	resout	46	p2.2/bclk1	66	a16
7	p1.7/gcs7_n	27	oscout	47	ad0	67	a17
8	p1.6/gcs6_n	28	clkin	48	ad8	68	a18
9	p1.5/gcs5_n	29	V_{cc}	49	V_{ss}	69	a19/once_n
10	V_{ss}	30	V_{ss}	50	V_{cc}	70	V_{ss}
11	V_{cc}	31	clkout	51	V_{ss}	71	V_{cc}
12	p1.4/gcs4_n	32	t0out	52	ad1	72	V_{ss}
13	p1.3/gcs3_n	33	t0in	53	ad9	73	rd_n
14	p1.2/gcs2_n	34	t1out	54	ad2	74	wr_n
15	p1.1/gcs1_n	35	t1in	55	ad10	75	ale
16	p1.0/gcs0_n	36	p2.7	56	ad3	76	bhe_n
17	lcs_n	37	p2.6	57	ad11	77	s2_n
18	ucs_n	38	cts0_n	58	ad4	78	s1_n
19	int0	39	txd0	59	ad12	79	s0_n
20	int1	40	rxd0	60	ad5	80	den_n

2.1.8 IA188EB 80 LQFP Package

The pinout for the IA188EB 80 LQFP Package is as shown in Figure 8. The corresponding pinout is provided in Table 6.

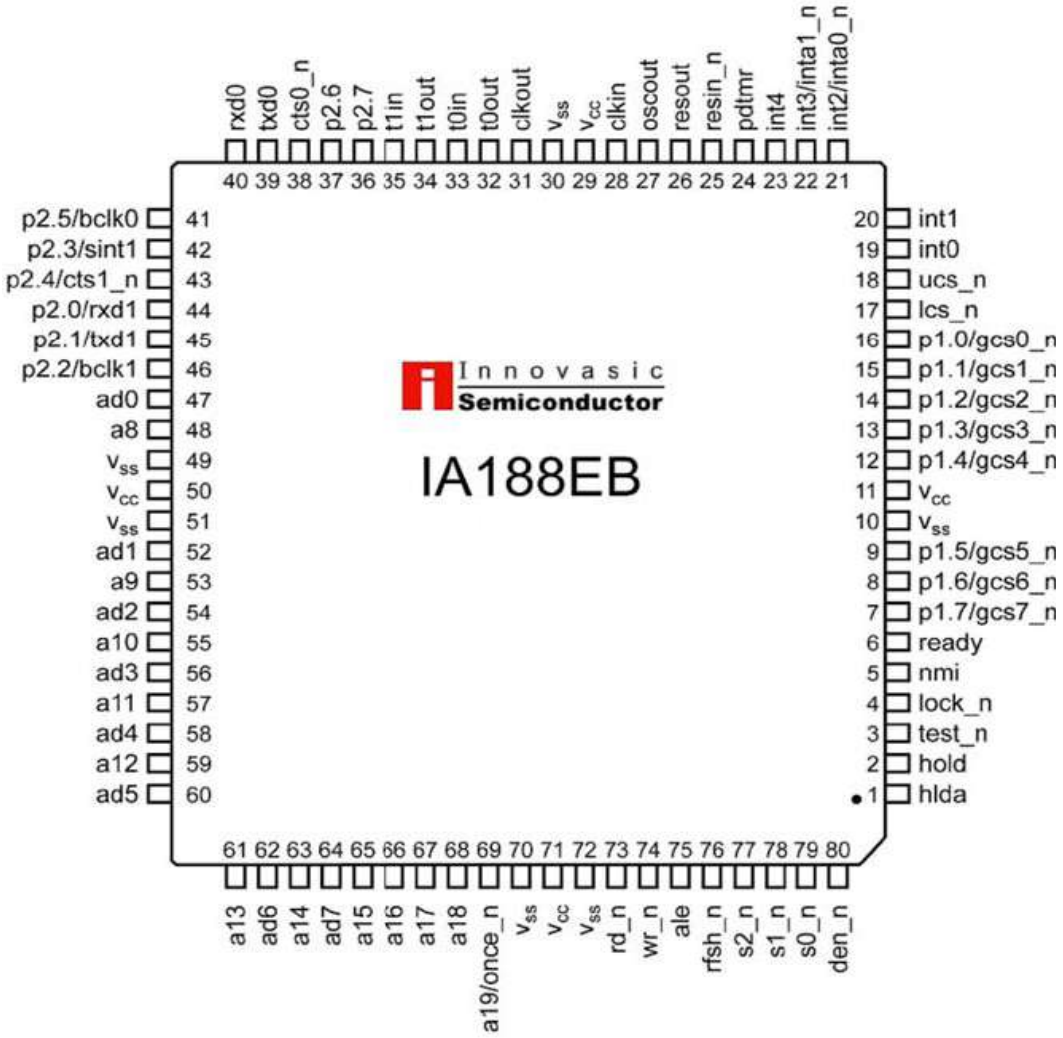


Figure 8. IA188EB 80-Pin LQFP Package Diagram

Table 7. IA186EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	LQFP	PQFP	
clkin	clkin	41	28	71	**cl**oc**k in**put. Input. The **clkin** pin is the input connection for an external clock. An external oscillator operating at two times the required processor operating frequency can be connected to this pin. If a crystal is used to supply the clock, it is connected between the **clkin** pin and the **oscout** pin (see oscout table entry). When a crystal is connected, it drives an internal Pierce oscillator to the IA186EB.
clkout	clkout	44	31	74	**cl**oc**k out**put. Output. The **clkout** pin provides a timing reference for inputs and outputs of the IA186EB. This clock output is one-half the input clock (**clkin**) frequency. The **clkout** signal has a 50% duty cycle, transitioning every falling edge of **clkin**.
cts0_n	cts0_n	51	38	1	**c**lear **t**o **s**end, Serial Port **0**. Input. Active Low. When this input is high (i.e., not asserted), data transmission from Serial Port 0 is inhibited. When the signal is asserted (low), data transmission is permitted.
cts1_n	p2.4/**cts1_n**	56	43	6	**c**lear **t**o **s**end, Serial Port **1**. Input. Active Low. When this input is high (i.e., not asserted), data transmission from Serial Port 1 is inhibited. When the signal is asserted (low), data transmission is permitted.
den_n	den_n	11	80	43	**d**ata **en**able. Output. Active Low. This signal is used to enable of bidirectional transceivers in a buffered system. The **den_n** signal is asserted (low) only when data is to be transferred on the bus.
dt/r_n	dt/r_n	16	NA	NA	**d**ata **t**ransmit/**r**eceive. Output. This signal is used to control the direction of data flow for bidirectional buffers in a buffered system. When **dt/r_n** is high, the direction indicated is transmit; when **dt/t_n** is low, the direction indicated is receive.
error_n	error_n	3	NA	NA	**error**. Input. Active Low. When this signal is asserted (low), it indicates that the last numerics coprocessor operation resulted in an exception condition.

Table 7. IA186EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	LQFP	PQFP	
t1out	t1out	47	34	77	**t**imer **1 out**put. Output. Depending on the Timer Mode programmed for Timer 1, this output can provide a single clock or a continuous waveform.
test_n	**test_n**/busy	14	3	46	**test**. Input. Active Low. When the **test_n** input is high (i.e., not asserted), it causes the IA186EB to suspend operation during the execution of the WAIT instruction. Operation resumes when the pin is sampled low (asserted).
txd0	txd0	52	39	2	Transmit (**tx**) **d**ata, Serial Port **0**. Output. This pin is the serial data output for Serial Port 0. During synchronous serial communications, **txd0** becomes the transmit clock (**rxd0** functions as an output for data transmission).
txd1	p2.1/**txd1**	58	45	8	Transmit (**tx**) **d**ata, Serial Port **1**. Output. This pin is the serial data output for Serial Port 1. During synchronous serial communications, **txd1** becomes the transmit clock (**rxd1** functions as an output for data transmission).
ucs_n	ucs_n	30	18	61	**u**pper **c**hip **s**elect. Output. Active Low. This pin provides a chip select signal that will be asserted (low) whenever the address of a memory bus cycle is within the address space programmed for that output.
v_{cc}	v_{cc}	1, 23, 42, 64	11, 29, 50, 71	13, 34, 54, 72	Power (**v_{cc}**). This pin provides power for the IA186EB device. It must be connected to a +5V DC power source.
v_{ss}	v_{ss}	2, 22, 43, 63, 65, 84	10, 30, 49, 51, 70, 72	12, 14, 33, 35, 53, 73	Ground (**v_{ss}**). This pin provides the digital ground (0V) for the IA186EB. It must be connected to a v_{ss} board plane.
wr_n	wr_n	5	74	37	**wr**ite. Output. Active Low. When asserted (low), **wr_n** indicates that data available on the data bus are to be latched into the accessed memory or I/O device.

Table 8. IA188EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	LQFP	PQFP	
test_n	test_n	14	3	46	**test**. Input. Active Low. When the **test_n** input is high (i.e., not asserted), it causes the IA188EB to suspend operation during the execution of the WAIT instruction. Operation resumes when the pin is sampled low (asserted).
txd0	txd0	52	39	2	Transmit (**tx**) **d**ata, Serial Port **0**. Output. This pin is the serial data output for Serial Port 0. During synchronous serial communications, **txd0** becomes the transmit clock (**rxd0** functions as an output for data transmission).
txd1	p2.1/txd1	58	45	8	Transmit (**tx**) **d**ata, Serial Port **1**. Output. This pin is the serial data output for Serial Port 1. During synchronous serial communications, **txd1** becomes the transmit clock (**rxd1** functions as an output for data transmission).
ucs_n	ucs_n	30	18	61	**u**pper **c**hip **s**elect. Output. Active Low. This pin provides a chip select signal that will be asserted (low) whenever the address of a memory bus cycle is within the address space programmed for that output.
V_{CC}	V_{CC}	1, 23, 42, 64	11, 29, 50, 71	13, 34, 54, 72	Power ($\mathbf{V_{CC}}$). This pin provides power for the IA188EB device. It must be connected to a +5V DC power source.
V_{SS}	V_{SS}	2, 22, 43, 63, 65, 84	10, 30, 49, 51, 70, 72	12, 14, 33, 35, 53, 73	Ground ($\mathbf{V_{SS}}$). This pin provides the digital ground (0V) for the IA188EB. It must be connected to a $\mathbf{V_{SS}}$ board plane.
wr_n	wr_n	5	74	37	**wr**ite. Output. Active Low. When asserted (low), **wr_n** indicates that data available on the data bus are to be latched into the accessed memory or I/O device.

4. Functional Description

4.1 Device Architecture

Architecturally, the IA186EB and IA188EB microcontrollers include the following functional modules:

- Bus Interface Unit
- Clock Generator
- Interrupt Control Unit
- Timer/Counter Unit
- Serial Communications Unit
- Chip-Select Unit
- I/O Port Unit
- Refresh Control Unit
- Power Management Unit

A functional block diagram of the IA186EB/IA188EB is shown in Figure 10. Descriptions of the functional modules are provided in the following subsections.

4.1.1 Bus Interface Unit

The IA186EB/IA188EB bus controller that generates local bus control signals and uses a hold/hlda protocol to share the local bus with other bus masters. The bus controller generates 20 address bits, read and write control signals, and bus-cycle status information. A ready input is used to extend a bus cycle beyond the minimum four clock cycles.

4.1.2 Clock Generator

The IA186EB/IA188EB uses an on-chip clock generator to supply internal and external clocks. The clock generator makes use of a crystal oscillator and includes a divide-by-two counter.

Figure 11 shows the various operating modes of the clock circuit. The clock circuit can use either a parallel resonant fundamental mode crystal network (A) or a third-overtone mode crystal network (B), or it can be driven by an external clock source (C).

The following parameters are recommended when choosing a crystal:

- Temperature Range
  - Application Specific
  - ESR (Equivalent Series Resistance): 40Ω max
  - C0 (Shunt Capacitance of Crystal): 7.0 pF max
  - CL (Load Capacitance): 20 pF ± 2 pF
  - Drive Level: 1 mW max

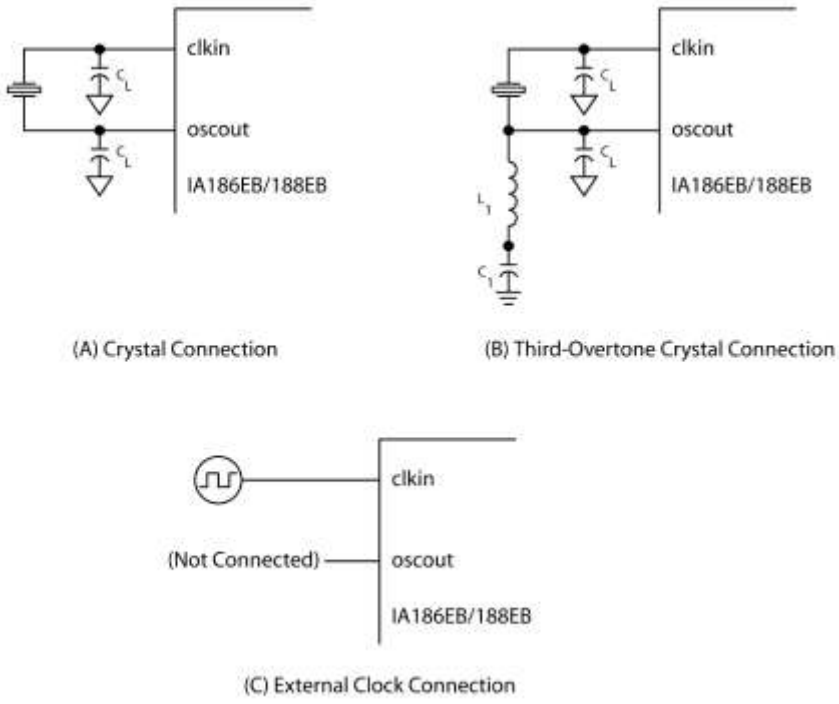


Figure 11. Clock Circuit Connection Options

Table 12. Peripheral Control Block Registers *(Continued)*

PCB Offset	Function	PCB Offset	Function	PCB Offset	Function	PCB Offset	Function
20H	Reserved	60H	Serial0 Baud	A0H	LCS Start	E0H	Reserved
22H	Reserved	62H	Serial0 Count	A2H	LCS Stop	E2H	Reserved
PCB Offset	Offset	PCB Offset	Function	PCB Offset	Function	PCB Offset	Function
24H	Reserved	64H	Serial0 Control	A4H	UCS Start	E4H	Reserved
26H	Reserved	66H	Serial0 Status	A6H	UCS Stop	E6H	Reserved
28H	Reserved	68H	Serial0 RBUF	A8H	Relocation	E8H	Reserved
2AH	Reserved	6AH	Serial0 TBUF	AAH	Reserved	EAH	Reserved
2CH	Reserved	6CH	Reserved	ACH	Reserved	ECH	Reserved
2EH	Reserved	6EH	Reserved	AEH	Reserved	EEH	Reserved
30H	Timer0 Count	70H	Serial1 Baud	B0H	Refresh Base	F0H	Reserved
32H	Timer0 Compare A	72H	Serial1 Count	B2H	Refresh Time	F2H	Reserved
34H	Timer0 Compare B	74H	Serial1 Control	B4H	Refresh Control	F4H	Reserved
36H	Timer0 Control	76H	Serial1 Status	B6H	Refresh Address	F6H	Reserved
38H	Timer1 Count	78H	Serial1 RBUF	B8H	Power Control	F8H	Reserved
3AH	Timer1 Compare A	7AH	Serial1 TBUF	BAH	Reserved	FAH	Reserved
3CH	Timer1 Compare B	7CH	Reserved	BCH	Step ID[1]	FCH	Reserved
3EH	Timer1 Control	7EH	Reserved	BEH	Reserved	FEH	Reserved

Note:

[1]The **Step ID** register (offset 0xBC) for Revision 2 of the Innovasic device is read-only, and is uniquely identified in software by having a value of 0x0080. The original Intel device established a value between 0x0000 and 0x0002, depending on the revision of the part.

For specific 5.0- and 3.3-volt characteristics, refer to Tables 13 and 14, respectively.

Table 13. AC Input Characteristics for 5.0-Volt Operation

Symbol	Pins	Min	Max	Units
t_{CHIS}	test_n, nmi, int4–int0, bclk1–bclk0, t1in–t0in, ready, cts1_n–cts0_n, p2.6, p2.7	10	–	ns
t_{CHIH}	test_n, nmi, int4–int0, bclk1–bclk0, t1in–t0in, ready, cts1_n–cts0_n	3	–	ns
t_{CLIS}	ad15–ad0, ad7–ad0 (IA188EB), ready	10	–	ns
t_{CLIS}	hold, pereq, error_n	10	–	ns
t_{CLIH}	ad15–ad0, ad7–ad0 (IA188EB), ready	3	–	ns
t_{CLIH}	hold, pereq, error_n	3	–	ns

Table 14. AC Input Characteristics for 3.3-Volt Operation

Symbol	Pins	Min	Max	Units
t_{CHIS}	test_n, nmi, int4–int0, bclk1–bclk0, t1in–t0in, ready, cts1_n–cts0_n, p2.6, p2.7	10	–	ns
t_{CHIH}	test_n, nmi, int4–int0, bclk1–bclk0, t1in–t0in, ready, cts1_n–cts0_n	3	–	ns
t_{CLIS}	ad15–ad0, ad7–ad0 (IA188EB), ready	10	–	ns
t_{CLIS}	hold, pereq, error_n	10	–	ns
t_{CLIH}	ad15–ad0, ad7–ad0 (IA188EB), ready	3	–	ns
t_{CLIH}	hold, pereq, error_n	3	–	ns

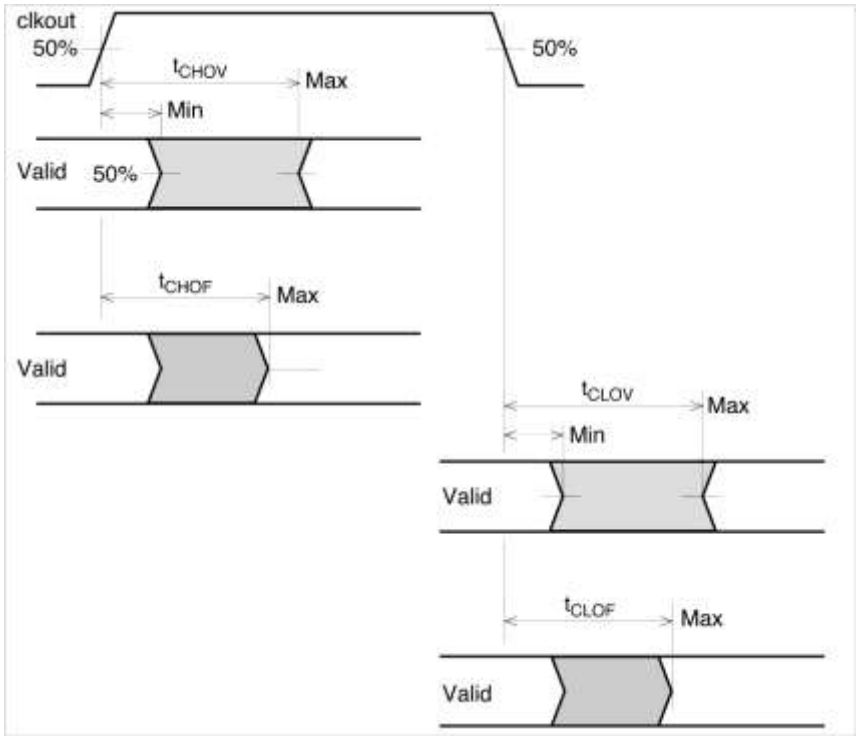


Figure 13. AC Output Characteristics

For specific 5.0- and 3.3-volt characteristics, refer to Tables 15 and 16, respectively.

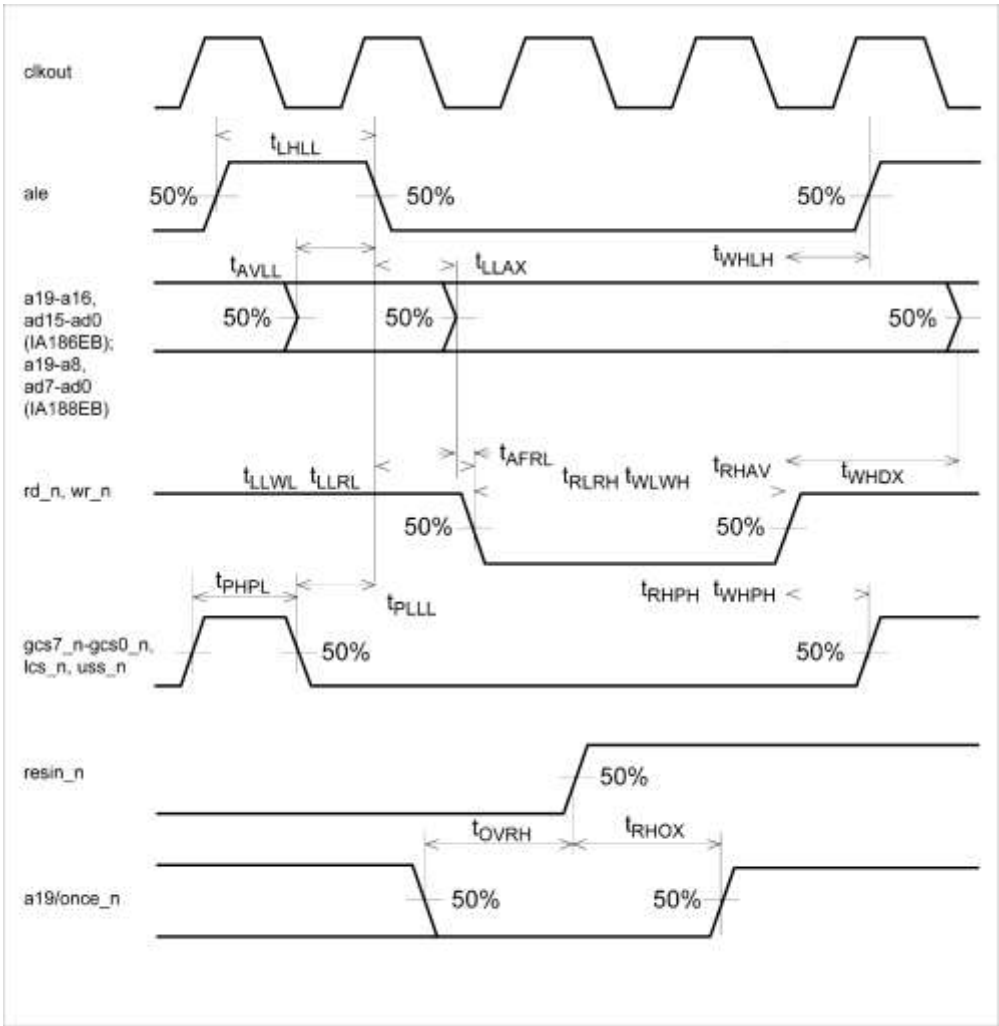


Figure 14. Relative Timing Characteristics

For specific relative timing characteristics, refer to Table 17.

Table 17. Relative Timing Characteristics

Symbol	Parameter	Min	Max	Units
t_{LHLL}	ale Rising to ale Falling	t – 15	–	ns
t_{AVLL}	Address Valid to ale Falling	½t –10	–	ns
t_{PLLL}	Chip Selects Valid to ale Falling	½t –10	–	ns
t_{LLAX}	Address Hold from ale Falling	½t –10	–	ns
t_{LLWL}	ale Falling to wr_n Falling	½t –15	–	ns
t_{LLRL}	ale Falling to rd_n Falling	½t –15	–	ns
t_{WHLH}	wr_n Rising to ale Rising	½t –10	–	ns
t_{AFRL}	Address Float to rd_n Falling	0	–	ns
t_{RLRH}	rd_n Falling to rd_n Rising	(2t) – 5	–	ns
t_{WLWH}	wr_n Falling to wr_n Rising	(2t) – 5	–	ns
t_{RHAV}	rd_n Rising to Address Active	t – 15	–	ns
t_{WHDX}	Output Data Hold after wr_n Rising	t – 15	–	ns
t_{WHPH}	wr_n Rising to Chip Select Rising	½t –10	–	ns
t_{RHPH}	rd_n Rising to Chip Select Rising	½t –10	–	ns
t_{PHPL}	cs_n inactive to cs_n active	½t –10	–	ns
t_{OVRH}	once_n Active to resin_n Rising	t	–	ns
t_{RHOX}	once_n Hold to resin_n Rising	t	–	Ns

5.1 AC Test Conditions

The AC specifications are tested with the 50-pF load shown in Figure 15. Specifications are measured at the $V_{CC}/2$ crossing point unless otherwise specified.

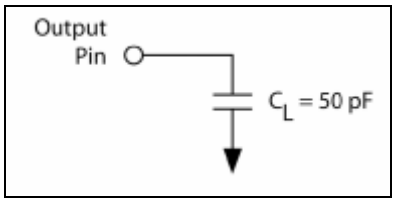


Figure 15. AC Test Load

5.3 Serial Port Mode 0 Timing Characteristics

Serial Port Mode 0 timing characteristics are illustrated in Figure 17 and collected in Table 20.

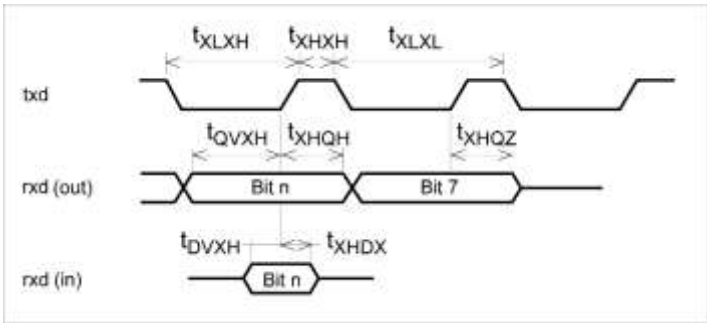


Figure 17. Serial Port Mode 0 Timing Characteristics

Table 20. Serial Port Mode 0 Timing Characteristics

Symbol	Parameter	Minimum	Maximum	Units
t_{XLXL}	txd Clock Period	t (n +1)	–	ns
t_{XLXH}	txd Clock Low to Clock High (n > 1)	2t – 35	2t + 35	ns
t_{XLXH}	txd Clock Low to Clock High (n = 1)	t – 35	t + 35	ns
t_{XHXL}	txd Clock High to Clock Low (n > 1)	(n – 1) t – 35	(n – 1) t + 35	ns
t_{XHXL}	txd Clock High to Clock Low (n = 1)	t – 35	t + 35	ns
t_{QVXH}	rxd Output Data Setup to txd Clock High (n > 1)	(n – 1) t – 35	–	ns
t_{QVXH}	rxd Output Data Setup to txd Clock High (n = 1)	t – 35	–	ns
t_{XHQX}	rxd Output Data Hold after txd Clock High (n > 1)	2t – 35	–	ns
t_{XHQX}	rxd Output Data Hold after txd Clock High (n = 1)	t – 35	–	ns
t_{XHQZ}	rxd Output Data Float after Last txd Clock High	–	t + 20	ns
t_{DVXH}	rxd Input Data Setup to txd Clock High	t + 20	–	ns
t_{XHDX}	rxd Input Data Hold after txd Clock High	0	–	ns

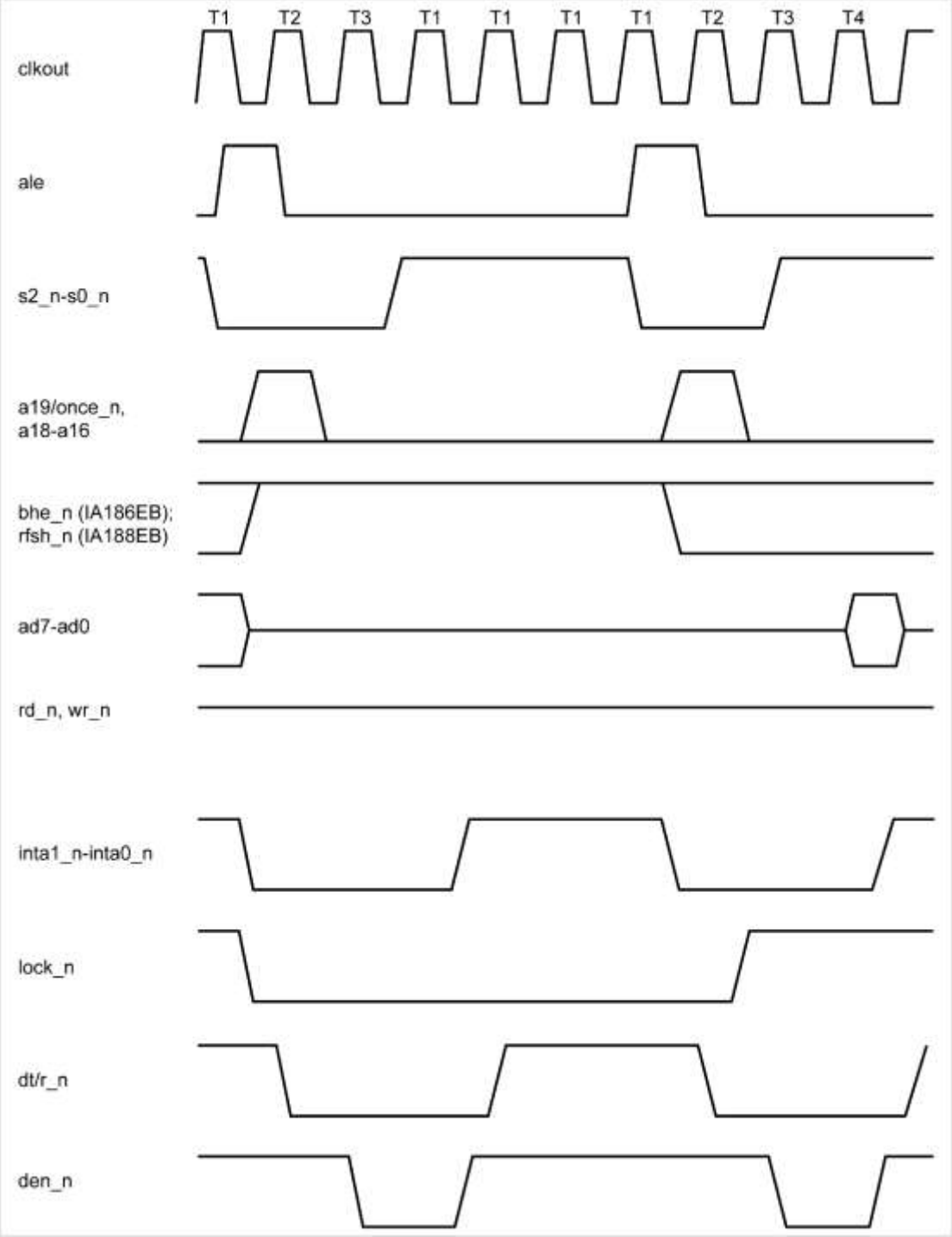


Figure 23. Interrupt Acknowledge (inta1_n, inta0_n) Cycle Timing

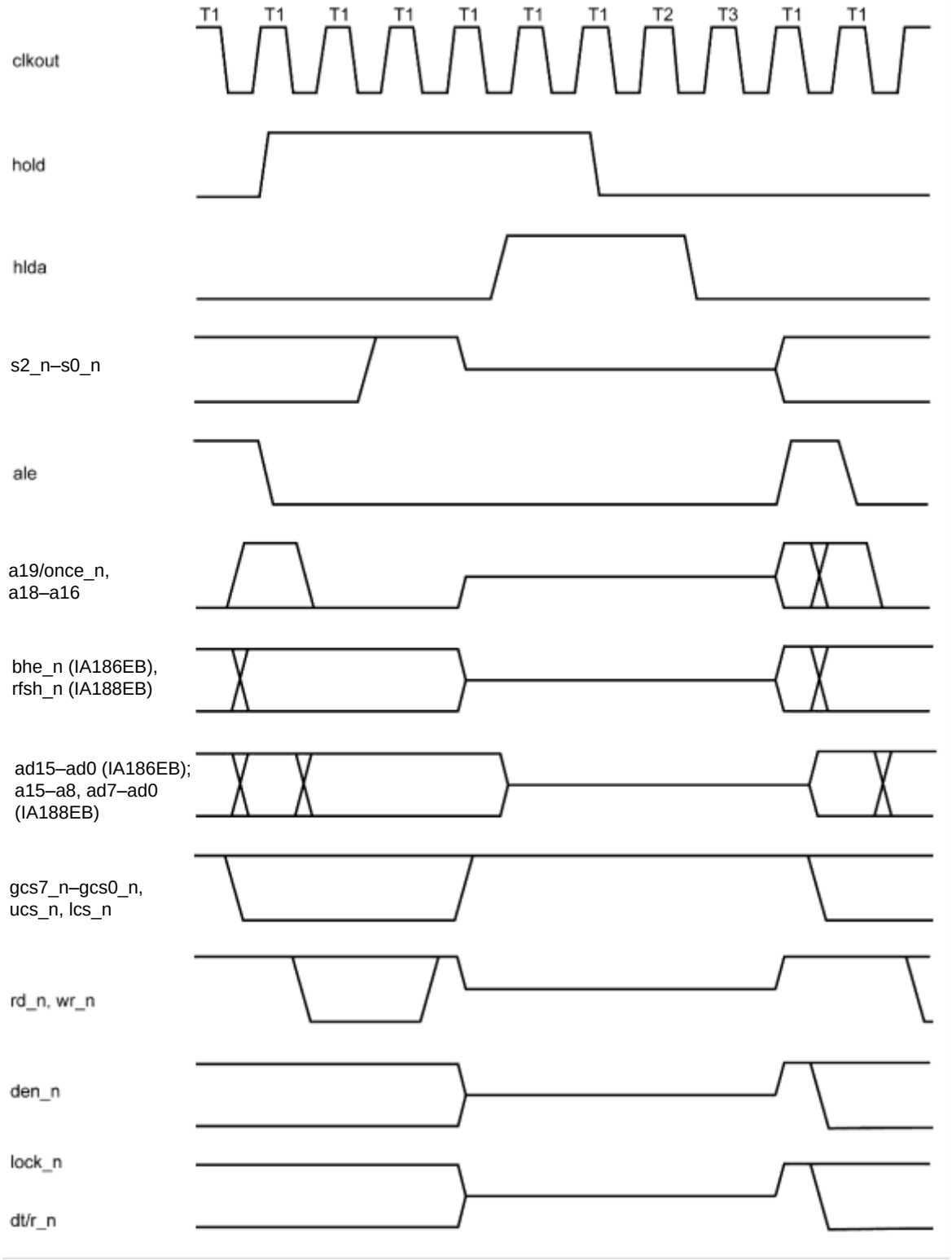


Figure 24. hold/hlda Timing

8. Instruction Execution Times

Table 21 provides IA186EB and IA188EB execution times, mnemonic instruction, and additional information on execution, if required. The execution times apply to all versions of the parts.

Table 21. Instruction Set Timing

Instruction	Clock Cycles		Comments
	IA186EB	IA188EB	
AAA	3	3	–
AAD	6	6	–
AAM	40	40	–
AAS	3	3	–
ADC Immediate to accumulator	1	1	–
ADC Immediate to register/memory	3	13	–
ADC Register/memory with register to either	1/16	1/24	register/memory
ADD Immediate to accumulator	1	1	–
ADD Immediate to register/memory	1/19	1/32	register/memory
ADD Register/memory with register either	1/20	1/28	
AND Immediate to accumulator	1	1	–
AND Immediate to register/memory	1/24	1/33	register/memory
AND Register/memory and register to either	1/12	1/15	
BOUND	20/40	24/64	Interrupt not taken/Interrupt taken
CBW	1	4	–
CLC	1	1	–
CLD	1	1	–
CLI	1	1	–
CMC	2	2	–
CMPS	9	20	–
CS	1	1	–
CWD	1	1	–
DAA	4	4	–
DAS	2	2	–
DEC Register	1	1	–
DEC Register/memory	1/24	1/32	register/memory