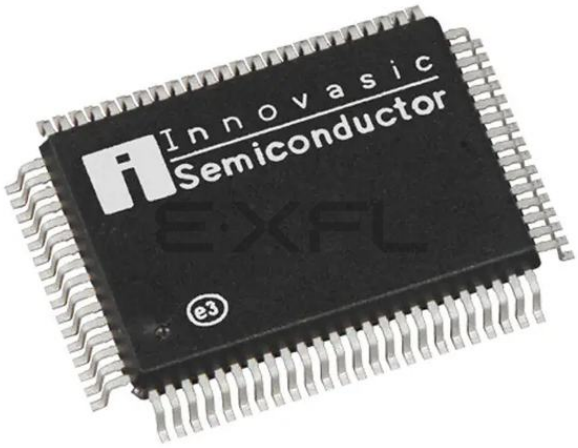

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Program Memory Type	ROMless
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RAM Size	-
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-PQFP (20x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ia186ebpqf80ir2

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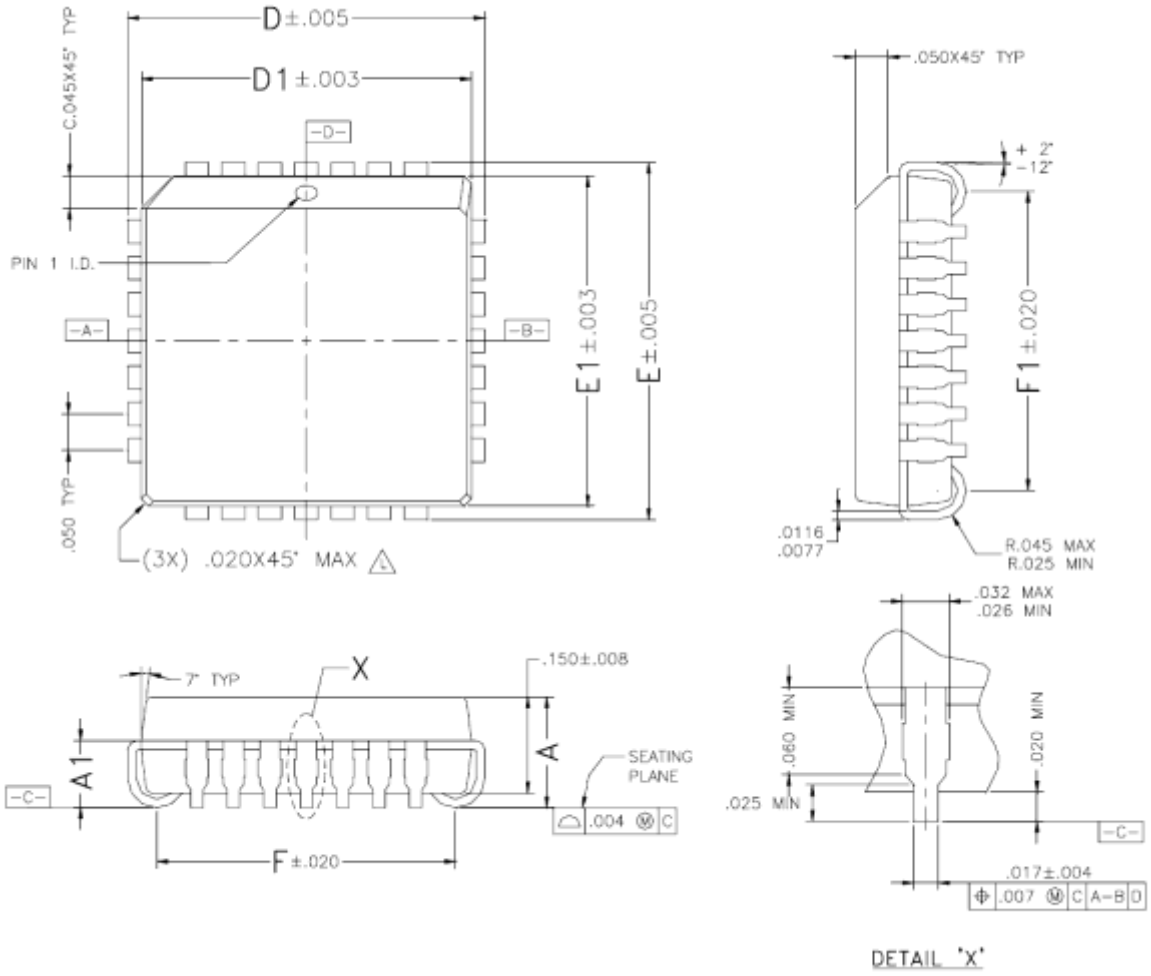
2.1.3 PLCC Physical Dimensions

The physical dimensions for the 84 PLCC are as shown in Figure 3.



Legend:

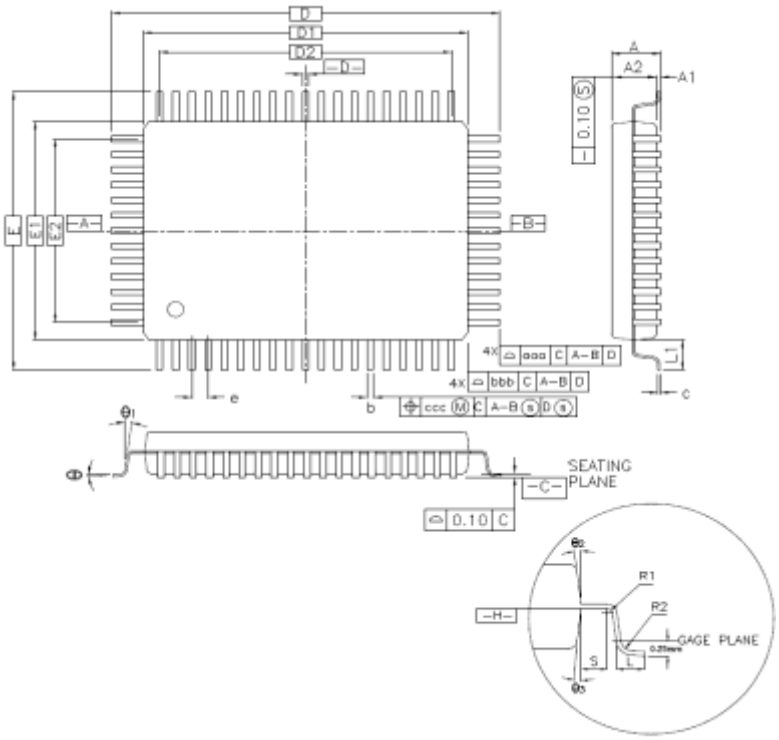
Symbol	Min	Nom	Max
A	0.165″	–	0.180″
A1	0.090″	–	0.120″
D	–	1.190″	–
D1	–	1.154″	–
E	–	1.190″	–
E1	–	1.154″	–
F	–	1.110″	–
F1	–	1.110″	–

Note: The bottom package is bigger than the top package by 0.004 inches (0.002 inches per side). Bottom package dimensions follow those stated in this drawing.

Figure 3. 84-Pin PLCC Physical Package Dimensions

2.1.6 PQFP Physical Dimensions

The physical dimensions for the 80 PQFP are as shown in Figure 6.



Legend:

Symbol	Millimeter Min	Nom	Max	Inch Min	Nom	Max
A	–	–	3.40	–	–	0.134
A1	0.25	–	–	0.010	–	–
A2	2.55	2.72	3.05	0.100	0.107	0.120
D	23.90 Basic			0.941 Basic		
D1	20.00 Basic			0.787 Basic		
E	17.90 Basic			0.705 Basic		
E1	14.00 Basic			0.551 Basic		
R2	0.013	–	0.30	0.005	–	0.012
R1	0.013	–	–	0.005	–	–
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	–	–	0°	–	–
θ2, θ3[a]	7° REF			7° REF		
θ2, θ3[b]	15° REF			15° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.95 REF			0.077 REF		
S	0.40	–	–	0.016	–	–
b	0.30	0.35	0.45	0.012	0.014	0.018
e	0.80 BSC			0.031 BSC		
D2	18.40 REF			0.724		
E2	12.00 REF			0.472		
Tolerances of Form and Position						
aaa	0.25			0.010		
bbb	0.20			0.008		
ccc	0.20			0.008		

[a]Alloy 42 L/F.
[b]Copper L/F.

Notes:
1. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimension D1 and E1 do not include mold mismatch and are determined a datum plane –H–.
2. Dimension b does not include dambar protrusion. Allowable dambar protrusion will not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located on the lower radius of the lead foot.

Figure 6. 80-Pin PQFP Physical Package Dimensions

Table 7. IA186EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	LQFP	PQFP	
ale	ale	6	75	38	**a**ddress **l**atch **e**nable. Output. Active High. This signal is used to latch the address information during the address portion of a bus cycle.
bclk0	p2.5/**bclk0**	54	41	4	**b**aud **cl**oc**k**, Serial Port **0**. Input. The **bclk0** pin can be used to provide an alternate clock source for Serial Port 0. The input clock rate cannot be greater than one-half the operating frequency of the IA186EB.
bclk1	p2.2/**bclk1**	59	46	9	**b**aud **cl**oc**k**, Serial Port **1**. Input. The **bclk1** pin can be used to provide an alternate clock source for Serial Port 1. The input clock rate cannot be greater than one-half the operating frequency of the IA186EB.
bhe_n bhe_n is multi-plexed with refresh_n	bhe_n bhe_n is multi-plexed with refresh_n	7	76	39	**b**yte **h**igh **e**nable. Output. Active Low. When **bhe_n** is asserted (low), it indicates that the bus cycle in progress is transferring data over the upper half of the data bus. Additionally, **bhe_n** and **ad0** encode the following bus information: ad0 bhe_n Bus Status 0 0 Word Transfer 0 1 Even Byte Transfer 1 0 Odd Byte Transfer 1 1 Refresh Operation Note: bhe_n is multiplexed with refresh_n.
busy	test_n/**busy**	14	NA	NA	**busy**. Input. Active High. When the **busy** input is asserted, it causes the IA186EB to suspend operation during the execution of the Intel 80C187 Numerics Coprocessor instructions. Operation resumes when the pin is sampled low. *This applies to the PLCC package only.*

Table 7. IA186EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	LQFP	PQFP	
clkin	clkin	41	28	71	**cl**oc**k in**put. Input. The **clkin** pin is the input connection for an external clock. An external oscillator operating at two times the required processor operating frequency can be connected to this pin. If a crystal is used to supply the clock, it is connected between the **clkin** pin and the **oscout** pin (see oscout table entry). When a crystal is connected, it drives an internal Pierce oscillator to the IA186EB.
clkout	clkout	44	31	74	**cl**oc**k out**put. Output. The **clkout** pin provides a timing reference for inputs and outputs of the IA186EB. This clock output is one-half the input clock (**clkin**) frequency. The **clkout** signal has a 50% duty cycle, transitioning every falling edge of **clkin**.
cts0_n	cts0_n	51	38	1	**c**lear **t**o **s**end, Serial Port **0**. Input. Active Low. When this input is high (i.e., not asserted), data transmission from Serial Port 0 is inhibited. When the signal is asserted (low), data transmission is permitted.
cts1_n	p2.4/**cts1_n**	56	43	6	**c**lear **t**o **s**end, Serial Port **1**. Input. Active Low. When this input is high (i.e., not asserted), data transmission from Serial Port 1 is inhibited. When the signal is asserted (low), data transmission is permitted.
den_n	den_n	11	80	43	**d**ata **en**able. Output. Active Low. This signal is used to enable of bidirectional transceivers in a buffered system. The **den_n** signal is asserted (low) only when data is to be transferred on the bus.
dt/r_n	dt/r_n	16	NA	NA	**d**ata **t**ransmit/**r**eceive. Output. This signal is used to control the direction of data flow for bidirectional buffers in a buffered system. When **dt/r_n** is high, the direction indicated is transmit; when **dt/t_n** is low, the direction indicated is receive.
error_n	error_n	3	NA	NA	**error**. Input. Active Low. When this signal is asserted (low), it indicates that the last numerics coprocessor operation resulted in an exception condition.

Table 7. IA186EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	LQFP	PQFP	
t1out	t1out	47	34	77	**t**imer **1 out**put. Output. Depending on the Timer Mode programmed for Timer 1, this output can provide a single clock or a continuous waveform.
test_n	**test_n**/busy	14	3	46	**test**. Input. Active Low. When the **test_n** input is high (i.e., not asserted), it causes the IA186EB to suspend operation during the execution of the WAIT instruction. Operation resumes when the pin is sampled low (asserted).
txd0	txd0	52	39	2	Transmit (**tx**) **d**ata, Serial Port **0**. Output. This pin is the serial data output for Serial Port 0. During synchronous serial communications, **txd0** becomes the transmit clock (**rxd0** functions as an output for data transmission).
txd1	p2.1/**txd1**	58	45	8	Transmit (**tx**) **d**ata, Serial Port **1**. Output. This pin is the serial data output for Serial Port 1. During synchronous serial communications, **txd1** becomes the transmit clock (**rxd1** functions as an output for data transmission).
ucs_n	ucs_n	30	18	61	**u**pper **c**hip **s**elect. Output. Active Low. This pin provides a chip select signal that will be asserted (low) whenever the address of a memory bus cycle is within the address space programmed for that output.
v_{cc}	v_{cc}	1, 23, 42, 64	11, 29, 50, 71	13, 34, 54, 72	Power (**v_{cc}**). This pin provides power for the IA186EB device. It must be connected to a +5V DC power source.
v_{ss}	v_{ss}	2, 22, 43, 63, 65, 84	10, 30, 49, 51, 70, 72	12, 14, 33, 35, 53, 73	Ground (**v_{ss}**). This pin provides the digital ground (0V) for the IA186EB. It must be connected to a v_{ss} board plane.
wr_n	wr_n	5	74	37	**wr**ite. Output. Active Low. When asserted (low), **wr_n** indicates that data available on the data bus are to be latched into the accessed memory or I/O device.

Table 8. IA188EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	LQFP	PQFP	
bclk1	p2.2/**bclk1**	59	46	9	**b**aud **cl**oc**k**, Serial Port **1**. Input. The **bclk1** pin can be used to provide an alternate clock source for Serial Port 1. The input clock rate cannot be greater than one-half the operating frequency of the IA188EB.
clkin	clkin	41	28	71	**cl**oc**k in**put. Input. The **clkin** pin is the input connection for an external clock. An external oscillator, operating at two times the required processor operating frequency, can be connected to this pin. If a crystal is used to supply the clock, it is connected between the **clkin** pin and the **oscout** pin (see **oscout** table entry). When a crystal is connected, it drives an internal Pierce oscillator to the IA188EB.
clkout	clkout	44	31	74	**cl**oc**k out**put. Output. The **clkout** pin provides a timing reference for inputs and outputs of the IA188EB. This clock output is one-half the input clock (**clkin**) frequency. The **clkout** signal has a 50% duty cycle, transitioning every falling edge of **clkin**.
cts0_n	cts0_n	51	38	1	**c**lear **t**o **s**end, Serial Port **0**. Input. Active Low. When this input is high (i.e., not asserted), data transmission from Serial Port 0 is inhibited. When the signal is asserted (low), data transmission is permitted.
cts1_n	p2.4/**cts1_n**	56	43	6	**c**lear **t**o **s**end, Serial Port **1**. Input. Active Low. When this input is high (i.e., not asserted), data transmission from Serial Port 1 is inhibited. When the signal is asserted (low), data transmission is permitted.
den_n	den_n	11	80	43	**d**ata **en**able. Output. Active Low. This signal is used to enable of bidirectional transceivers in a buffered system. The **den_n** signal is asserted (low) only when data are to be transferred on the bus.
dt/r_n	dt/r_n	16	NA	NA	**d**ata **t**ransmit**/r**eceive. Output. This signal is used to control the direction of data flow for bidirectional buffers in a buffered system. When **dt/r_n** is high, the direction indicated is transmit; when **dt/t_n** is low, the direction indicated is receive.

Table 8. IA188EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	LQFP	PQFP	
p1.0	**p1.0**/gcs0_n	28	16	59	**p**ort **1**, Bit [N] (N = **0**–**7**). Output. Each pin of Port 1, **p1.0**–**p1.7**, can function individually as a general-purpose output line.
p1.1	**p1.1**/gcs1_n	27	15	58	
p1.2	**p1.2**/gcs2_n	26	14	57	
p1.3	**p1.3**/gcs3_n	25	13	56	
p1.4	**p1.4**/gcs4_n	24	12	55	
p1.5	**p1.5**/gcs5_n	21	9	52	
p1.6	**p1.6**/gcs6_n	20	8	51	
p1.7	**p1.7**/gcs7_n	19	7	50	
p2.0	**p2.0**/rxd1	57	44	7	**p**ort **2**, Bit [**0**]. Input/Output. This pin functions as a general-purpose I/O line.
p2.1	**p2.1**/txd1	58	45	8	**p**ort **2**, Bit [**1**]. Output. This pin functions as a general-purpose output line.
p2.2	**p2.2**/bclk1	59	46	9	**p**ort **2**, Bit [**2**]. Input. This pin functions as a general-purpose input line.
p2.3	**p2.3**/sint1	55	42	5	**p**ort **2**, Bit [**3**]. Output. This pin functions as a general-purpose output line.
p2.4	**p2.4**/cts1_n	56	43	6	**p**ort **2**, Bit [**4**]. Input. This pin functions as a general-purpose input line.
p2.5	**p2.5**/bclk0	54	41	4	**p**ort **2**, Bit [**5**]. Input. This pin functions as a general-purpose input line.
p2.6	p2.6	50	37	80	**p**ort **2**, Bit [**6**]. Input/Output (open drain). This pin functions as a general-purpose bidirectional input/output line.
p2.7	p2.7	49	36	79	**p**ort **2**, Bit [**7**]. Input/Output (open drain). This pin functions as a general-purpose bidirectional input/output line.

Table 8. IA188EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	LQFP	PQFP	
test_n	test_n	14	3	46	**test**. Input. Active Low. When the **test_n** input is high (i.e., not asserted), it causes the IA188EB to suspend operation during the execution of the WAIT instruction. Operation resumes when the pin is sampled low (asserted).
txd0	txd0	52	39	2	Transmit (**tx**) **d**ata, Serial Port **0**. Output. This pin is the serial data output for Serial Port 0. During synchronous serial communications, **txd0** becomes the transmit clock (**rxd0** functions as an output for data transmission).
txd1	p2.1/txd1	58	45	8	Transmit (**tx**) **d**ata, Serial Port **1**. Output. This pin is the serial data output for Serial Port 1. During synchronous serial communications, **txd1** becomes the transmit clock (**rxd1** functions as an output for data transmission).
ucs_n	ucs_n	30	18	61	**u**pper **c**hip **s**elect. Output. Active Low. This pin provides a chip select signal that will be asserted (low) whenever the address of a memory bus cycle is within the address space programmed for that output.
V_{CC}	V_{CC}	1, 23, 42, 64	11, 29, 50, 71	13, 34, 54, 72	Power ($\mathbf{V_{CC}}$). This pin provides power for the IA188EB device. It must be connected to a +5V DC power source.
V_{SS}	V_{SS}	2, 22, 43, 63, 65, 84	10, 30, 49, 51, 70, 72	12, 14, 33, 35, 53, 73	Ground ($\mathbf{V_{SS}}$). This pin provides the digital ground (0V) for the IA188EB. It must be connected to a $\mathbf{V_{SS}}$ board plane.
wr_n	wr_n	5	74	37	**wr**ite. Output. Active Low. When asserted (low), **wr_n** indicates that data available on the data bus are to be latched into the accessed memory or I/O device.

Table 11. IA186EB and IA188EB DC Parameters

Symbol	Parameter	Min	Max	Units	Notes
5.0V Operation V_{CC}	Supply Voltage	4.5	5.5	V	–
3.3V Operation V_{CC}	Supply Voltage	3.0	3.6	V	–
V_{IL}	Input Low Voltage	−0.3	0.3 V_{CC}	V	input hysteresis on resin_n = 0.50V
V_{IH}	Input High Voltage	0.7 V_{CC}	V_{CC} + 0.3	V	–
V_{OL}	Output Low Voltage Vcc = 5.5V or 3.6V	–	0.4	V	I_{OL} = 12mA
V_{OH}	Output High Voltage Vcc = 4.5V/3.0V	3.5/2.4	–	V	I_{OH} = −12 mA
I_{LEAK}	Input Leakage Current for Pins: ad15–ad0, ad7–ad0 (IA188EB), ready, hold, resin_n; clkin, test_n, nmi, int4–int0, t0in, t1in, rdx0, bclk0_n, cts0_n, rxd1, bclk1_n, cts1_n, p2.6, p2.7	–	± 1	µA	0V ≤ V_{IN} ≤ V_{CC}
	Input Leakage Current for Pins (@3.3V): pereq	+ .147	+.625	mA	V_{IN} = V_{CC}
	Input Leakage Current for Pins (@3.3V): a19/once_n, a18–a16, lock_n, error_n	− .147	−.625	mA	V_{IN} =0V
	Input Leakage Current for Pins (@5V): pereq	+ .227	+.833	mA	V_{IN} = V_{CC}
	Input Leakage Current for Pins (@5V): a19/once_n, a18–a16, lock_n, error_n	− .227	−.833	mA	V_{IN} =0V
I_{LO}	Output Leakage Current	–	± 10	µA	0.45 ≤ V_{OUT} ≤ V_{CC}
I_{ID}	Supply Current (IDLE) - @ 50 MHz	–	90	mA	–
C_{IN}	Input Pin Capacitance	0	5	pF	T_F = 1 MHz
C_{OUT}	Output Pin Capacitance	0	5	pF	T_F = 1 MHz
Operating temperature is -40°C to +85°C.					

For specific 5.0- and 3.3-volt characteristics, refer to Tables 13 and 14, respectively.

Table 13. AC Input Characteristics for 5.0-Volt Operation

Symbol	Pins	Min	Max	Units
t_{CHIS}	test_n, nmi, int4–int0, bclk1–bclk0, t1in–t0in, ready, cts1_n–cts0_n, p2.6, p2.7	10	–	ns
t_{CHIH}	test_n, nmi, int4–int0, bclk1–bclk0, t1in–t0in, ready, cts1_n–cts0_n	3	–	ns
t_{CLIS}	ad15–ad0, ad7–ad0 (IA188EB), ready	10	–	ns
t_{CLIS}	hold, pereq, error_n	10	–	ns
t_{CLIH}	ad15–ad0, ad7–ad0 (IA188EB), ready	3	–	ns
t_{CLIH}	hold, pereq, error_n	3	–	ns

Table 14. AC Input Characteristics for 3.3-Volt Operation

Symbol	Pins	Min	Max	Units
t_{CHIS}	test_n, nmi, int4–int0, bclk1–bclk0, t1in–t0in, ready, cts1_n–cts0_n, p2.6, p2.7	10	–	ns
t_{CHIH}	test_n, nmi, int4–int0, bclk1–bclk0, t1in–t0in, ready, cts1_n–cts0_n	3	–	ns
t_{CLIS}	ad15–ad0, ad7–ad0 (IA188EB), ready	10	–	ns
t_{CLIS}	hold, pereq, error_n	10	–	ns
t_{CLIH}	ad15–ad0, ad7–ad0 (IA188EB), ready	3	–	ns
t_{CLIH}	hold, pereq, error_n	3	–	ns

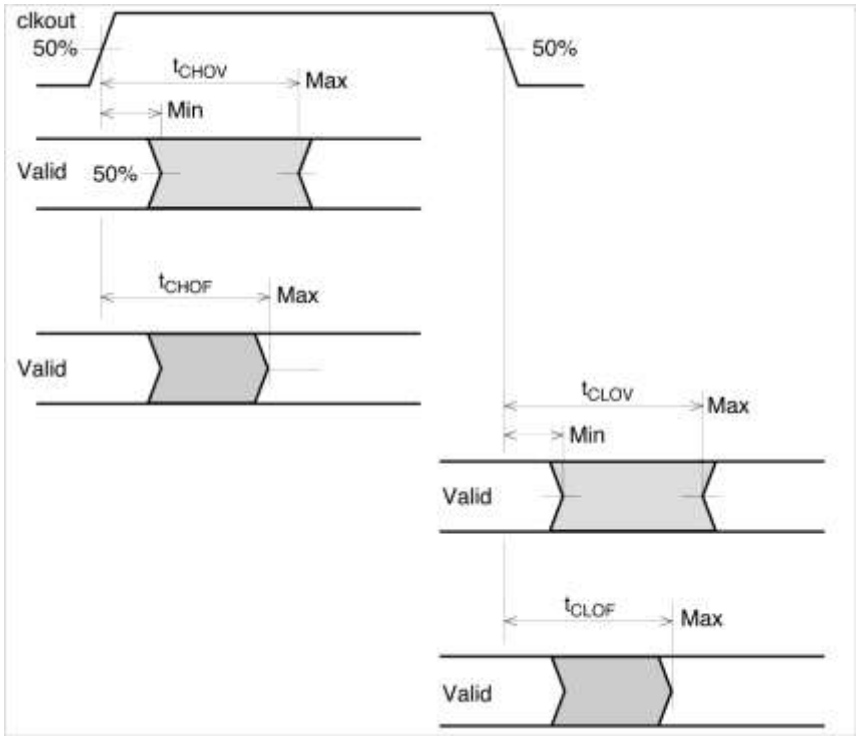


Figure 13. AC Output Characteristics

For specific 5.0- and 3.3-volt characteristics, refer to Tables 15 and 16, respectively.

Table 15. AC Output Characteristics for 5.0-Volt Operation

Symbol	Parameter	Min	Max	Units
t_{CHOV}	ale, s2–s0_n, den_n, dt/r_n, bhe_n, rfsh_n (IA188EB), lock_n, a19–a16	3	17	ns
	gcs0–gcs7_n, lcs_n, ucs_n, ncs_n, rd_n, wr_n	3	20	ns
t_{CLOV}	bhe_n, rfsh_n (IA188EB), den_n, lock_n, resout, hlda, t0out, t1out, a19–a16	3	17	ns
	rd_n , wr_n, gcs7–gcs0_n, lcs_n, ucs_n, ad15–ad0, ad7–ad0 (IA188EB), a15–a8 (IA188EB), ncs_n, inta1_n–inta0_n, s2_n–s0_n	3	20	ns
t_{CHOF}	re_n, wr_n, bhe_n, rfsh_n (IA188EB), dt/r_n, lock_n, s2_n–s0_n, a19–a16	0	20	ns
t_{CLOF}	den_n, ad15–ad0, ad7–ad0 (IA188EB), a15–a8 (IA188EB)	0	20	ns

Table 16. AC Output Characteristics for 3.3-Volt Operation

Symbol	Parameter	Min	Max	Units
t_{CHOV}	ale, s2–s0_n, den_n, dt/r_n, bhe_n, rfsh_n (IA188EB), lock_n, a19–a16	3	25	ns
	gcs0–gcs7_n, lcs_n, ucs_n, ncs_n, rd_n, wr_n	3	30	ns
t_{CLOV}	bhe_n, rfsh_n (IA188EB), den_n, lock_n, resout, hlda, t0out, t1out, a19–a16	3	25	ns
	rd_n , wr_n, gcs7–gcs0_n, lcs_n, ucs_n, ad15–ad0, ad7–ad0 (IA188EB), a15–a8 (IA188EB), ncs_n, inta1_n–inta0_n, s2_n–s0_n	3	30	ns
t_{CHOF}	re_n, wr_n, bhe_n, rfsh_n (IA188EB), dt/r_n, lock_n, s2_n–s0_n, a19–a16	0	30	ns
t_{CLOF}	den_n, ad15–ad0, ad7–ad0 (IA188EB), a15–a8 (IA188EB)	0	30	ns

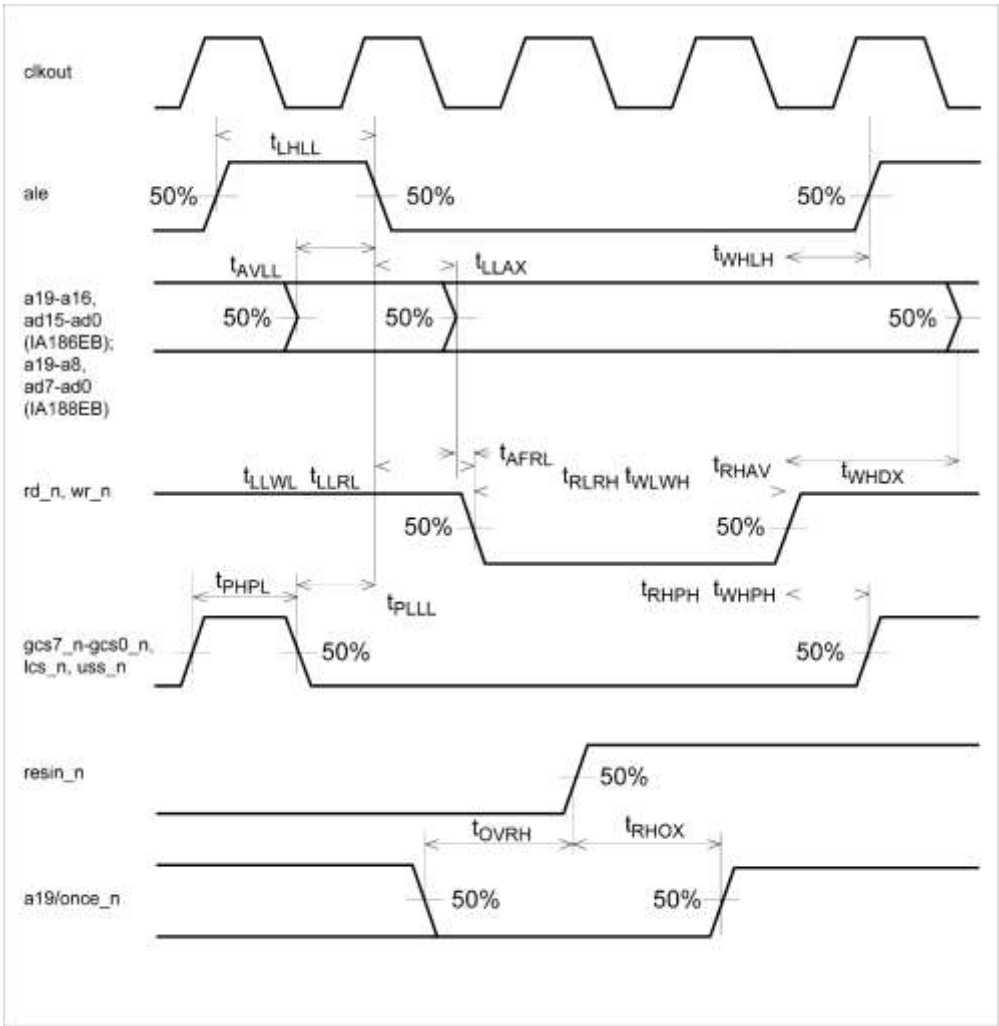


Figure 14. Relative Timing Characteristics

For specific relative timing characteristics, refer to Table 17.

Table 17. Relative Timing Characteristics

Symbol	Parameter	Min	Max	Units
t_{LHLL}	ale Rising to ale Falling	t – 15	–	ns
t_{AVLL}	Address Valid to ale Falling	½t –10	–	ns
t_{PLLL}	Chip Selects Valid to ale Falling	½t –10	–	ns
t_{LLAX}	Address Hold from ale Falling	½t –10	–	ns
t_{LLWL}	ale Falling to wr_n Falling	½t –15	–	ns
t_{LLRL}	ale Falling to rd_n Falling	½t –15	–	ns
t_{WHLH}	wr_n Rising to ale Rising	½t –10	–	ns
t_{AFRL}	Address Float to rd_n Falling	0	–	ns
t_{RLRH}	rd_n Falling to rd_n Rising	(2t) – 5	–	ns
t_{WLWH}	wr_n Falling to wr_n Rising	(2t) – 5	–	ns
t_{RHAV}	rd_n Rising to Address Active	t – 15	–	ns
t_{WHDX}	Output Data Hold after wr_n Rising	t – 15	–	ns
t_{WHPH}	wr_n Rising to Chip Select Rising	½t –10	–	ns
t_{RHPH}	rd_n Rising to Chip Select Rising	½t –10	–	ns
t_{PHPL}	cs_n inactive to cs_n active	½t –10	–	ns
t_{OVRH}	once_n Active to resin_n Rising	t	–	ns
t_{RHOX}	once_n Hold to resin_n Rising	t	–	Ns

5.1 AC Test Conditions

The AC specifications are tested with the 50-pF load shown in Figure 15. Specifications are measured at the $V_{CC}/2$ crossing point unless otherwise specified.

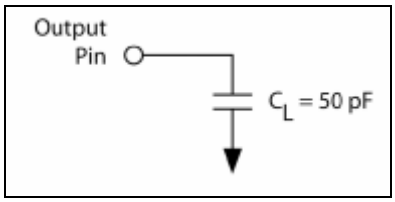


Figure 15. AC Test Load

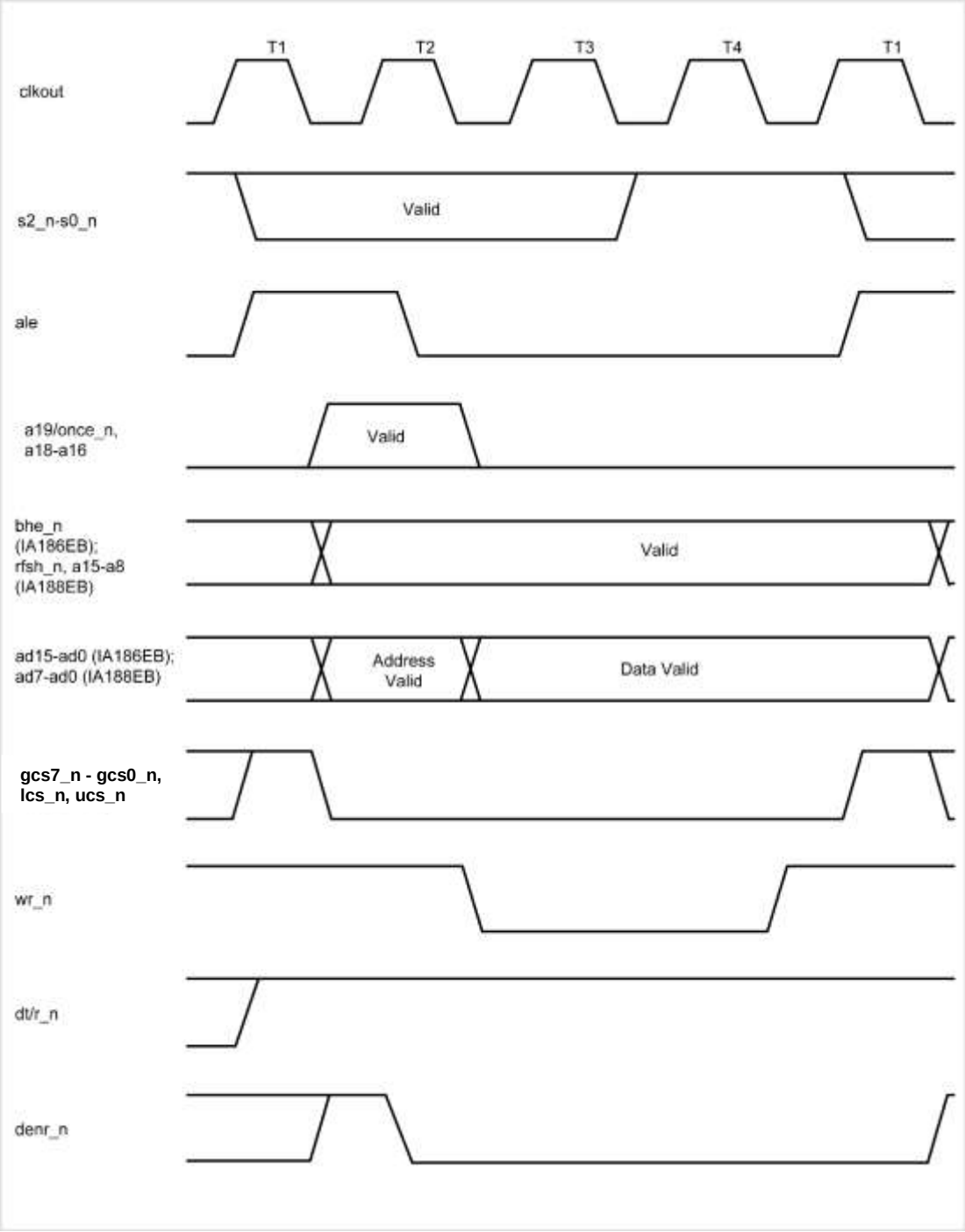


Figure 21. Write Cycle Timing

Table 21. Instruction Set Timing *(Continued)*

Instruction	Clock Cycles		Comments
	IA186EB	IA188EB	
SHL Register/Memory by CL	1/20	1/24	register/memory
SHL Register/Memory by Count	1/11	1/24	
SHR Register/Memory by 1	1/5	1/24	
SHR Register/Memory by CL	1/20	1/28	
SHR Register/Memory by Count	1/11	1/24	
SS	1	1	–
STC	1	1	–
SUB Immediate from accumulator	1	1	-
SUB Immediate from register/memory	1/11	1/28	register/memory
SUB Register/memory and register to either	1/15	1/40	
STD	1	1	–
STI	1	1	–
STOS	6	8	–
STOS (repeated n times)	6+4n	8+8n	–
TEST Immediate data and accumulator	1	1	–
TEST Immediate data and register/memory	1/16	1/16	register/memory
TEST Register/memory and register	1/12	1/20	register/memory
WAIT	1	1	test_n = 0
XCHG Register with accumulator	2	2	–
XCHG Register/memory with register	3/16	3/20	register/memory
XLAT	16	8	–
XOR Immediate to accumulator	1	1	–
XOR Immediate to register/memory	1/11	1/32	register/memory
XOR Register/memory and register to either	1/16	1/32	register/memory

Innovasic Part Number Cross-Reference

Tables 22 through 24 cross-reference the Innovasic part number with the corresponding Intel part number.

Table 22. Innovasic Part Number Cross-Reference for the PLCC

Innovasic Part Number	Intel Part Number	Package Type	Temperature Grades
IA186EBPLC84IR2 lead free (RoHS-compliant)	EE80C186EB25 EE80C186EB20 EN80C186EB25 EN80C186EB20 EN80C186EB13 N80C186EB25 N80C186EB20 N80C186EB13 TN80C186EB25 TN80C186EB20 TN80C186EB13 N80L186EB16 N80L186EB13 TN80L186EB16 TN80L186EB13 EN80L186EB13	84-Pin PLCC	Commercial and industrial
IA188EBPLC84IR2 lead free (RoHS-compliant)	EE80C188EB25 EE80C188EB20 EE80C188EB13 EN80C188EB25 EN80C188EB20 EN80C188EB13 N80C188EB25 N80C188EB20 N80C188EB13 TN80C188EB25 TN80C188EB20 TN80C188EB13 EE80L188EB16 EN80L188EB13 N80L188EB16 N80L188EB13 TN80L188EB16 TN80L188EB13	84-Pin PLCC	Commercial and industrial

Errata No. 2

Problem: When the extension byte (mod field) is set to "11," some instructions will cause the CPU to hang.

Description: Although there are faster versions of each instruction (these are not commonly used by compilers), the following instructions will cause the CPU to hang when the extension byte (mod field) is set to "11":

- 8D (LEA)
- 8F (POP memory)
- C6 (MOV immediate8 to memory/register)
- C7 (MOV immediate16 to memory/register)
- FE (PUSH memory)
- FF (PUSH memory)

Workaround: Substitute instructions in the following table.

Instruction	Workaround
8D (LEA)	Use MOV register (89 or 8B)
8F (POP memory)	Use POP register (0101_0xxx)
C6 (MOV immediate8 to memory/register)	Use MOV immediate8 to register (1011_0xxx)
C7 (MOV immediate16 to memory/register)	Use MOV immediate16 to register (1011_1xxx)
FE (PUSH memory)	Use PUSH register (0101_0xxx)
FF (PUSH memory)	Use PUSH register (0101_0xxx)

Errata No. 3

Problem: When the chip is put in SFNM mode for INT0 or INT1, the LVL bit is automatically set for those interrupts.

Workaround: None.

Date	Revision	Description	Page(s)
September 4, 2009	08	Added a note to Table 12 regarding the Step ID register.	50
February 25, 2011	09	Elimination of pages with SnPb lead plating options	74-76
March 23, 2011	10	Updated Instruction Set Timing Table to incorporate DIV and IDIV values.	70
June 12, 2011	11	Added Errata 11 and 12.	77, 78, 81
July 5, 2011	12	Added Errata 13.	78, 82
July 10, 2011	13	Added Errata 14.	78, 82

10. For Additional Information

The Innovasic Semiconductor IA186EB and IA188EB microcontrollers are form, fit, and function replacements for the original Intel® 80C186EB, 80C188EB, 80L186EB, and 80L188EB 16-bit high-integration embedded processors.

The Innovasic Support Team wants our information to be complete, accurate, useful, and easy to understand. Please feel free to contact our experts at Innovasic at any time with suggestions, comments, or questions.

Innovasic Support Team
3737 Princeton NE
Suite 130
Albuquerque, NM 87107

(505) 883-5263
Fax: (505) 883-5477
Toll Free: (888) 824-4184
E-mail: support@innovasic.com
Website: http://www.Innovasic.com