Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	-
Core Size	8/16-Bit
Speed	50MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	16
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ia188ebplq80ir2

2.1.4 IA186EB 80 PQFP Package

The pinout for the IA186EB 80 PQFP Package is as shown in Figure 4. The corresponding pinout is provided in Table 3.

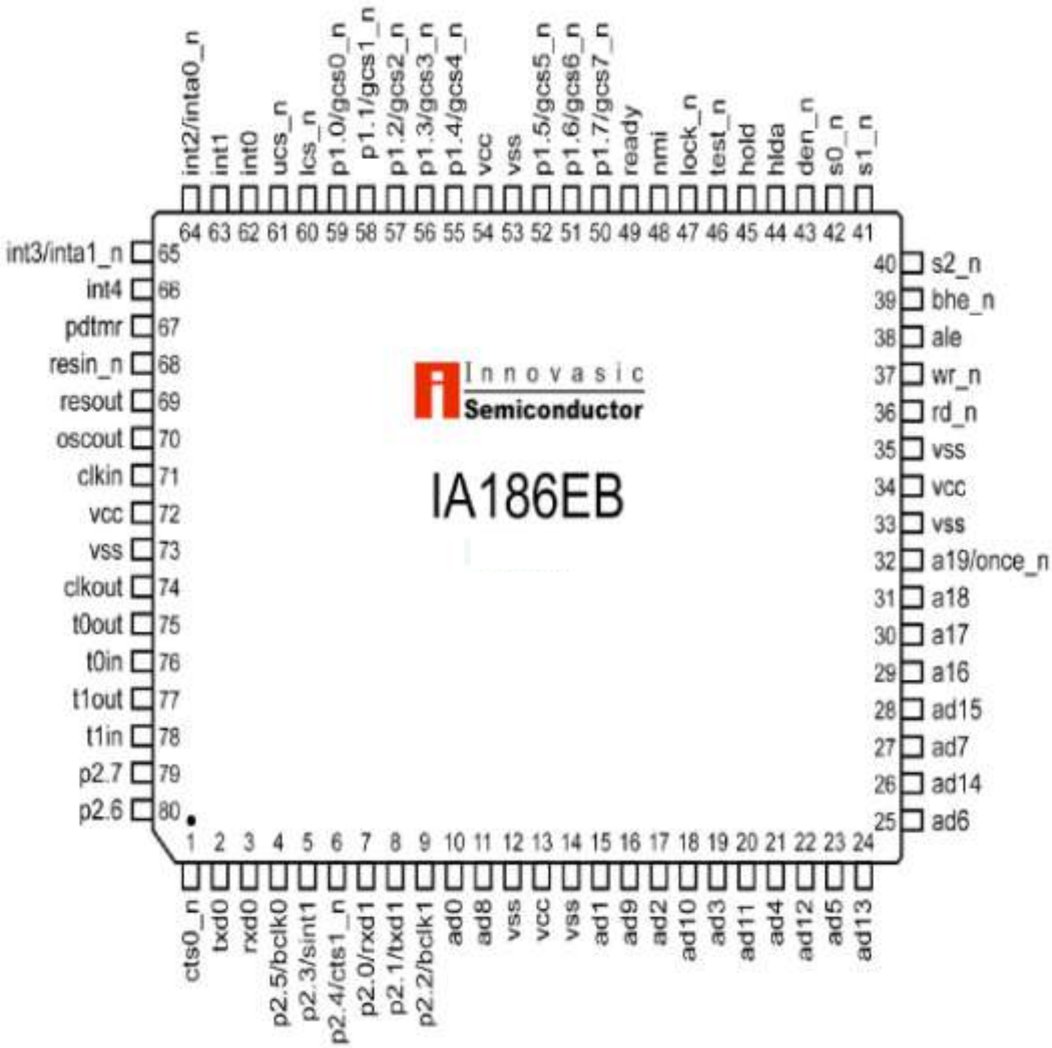

Figure 4. IA186EB 80-Pin PQFP Package Diagram

Table 3. IA186EB 80-Pin PQFP Pin Listing

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	cts0_n	21	ad4	41	s1_n	61	ucs_n
2	txd0	22	ad12	42	s0_n	62	int0
3	rxd0	23	ad5	43	den_n	63	int1
4	p2.5/bclk0	24	ad13	44	hlda	64	int2/inta0_n
5	p2.3/sint1	25	ad6	45	hold	65	int3/inta1_n
6	p2.4/cts1_n	26	ad14	46	test_n	66	int4
7	p2.0/rxd1	27	ad7	47	lock_n	67	pdtmr
8	p2.1/txd1	28	ad15	48	nmi	68	resin_n
9	p2.2/bclk1	29	a16	49	ready	69	resout
10	ad0	30	a17	50	p1.7/gcs7_n	70	oscout
11	ad8	31	a18	51	p1.6/gcs6_n	71	clkin
12	Vss	32	a19/once_n	52	p1.5/gcs5_n	72	Vcc
13	Vcc	33	Vss	53	Vss	73	Vss
14	Vss	34	Vcc	54	Vcc	74	clkout
15	ad1	35	Vss	55	p1.4/gcs4_n	75	t0out
16	ad9	36	rd_n	56	p1.3/gcs3_n	76	t0in
17	ad2	37	wr_n	57	p1.2/gcs2_n	77	t1out
18	ad10	38	ale	58	p1.1/gcs1_n	78	t1in
19	ad3	39	bhe_n	59	p1.0/gcs0_n	79	p2.7
20	ad11	40	s2_n	60	lcs_n	80	p2.6

Table 4. IA188EB 80-Pin PQFP Pin Listing

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	cts0_n	21	ad4	41	s1_n	61	ucs_n
2	txd0	22	a12	42	s0_n	62	int0
3	rxd0	23	ad5	43	den_n	63	int1
4	p2.5/bclk0	24	a13	44	hlda	64	int2/inta0_n
5	p2.3/sint1	25	ad6	45	hold	65	int3/inta1_n
6	p2.4/cts1_n	26	a14	46	test_n	66	int4
7	p2.0/rxd1	27	ad7	47	lock_n	67	pdtmr
8	p2.1/txd1	28	a15	48	nmi	68	resin_n
9	p2.2/bclk1	29	a16	49	ready	69	resout
10	ad0	30	a17	50	p1.7/gcs7_n	70	oscout
11	a8	31	a18	51	p1.6/gcs6_n	71	clkin
12	Vss	32	a19/once_n	52	p1.5/gcs5_n	72	Vcc
13	Vcc	33	Vss	53	Vss	73	Vss
14	Vss	34	Vcc	54	Vcc	74	clkout
15	ad1	35	Vss	55	p1.4/gcs4_n	75	t0out
16	a9	36	rd_n	56	p1.3/gcs3_n	76	t0in
17	ad2	37	wr_n	57	p1.2/gcs2_n	77	t1out
18	a10	38	ale	58	p1.1/gcs1_n	78	t1in
19	ad3	39	rfsh_n	59	p1.0/gcs0_n	79	p2.7
20	a11	40	s2_n	60	lcs_n	80	p2.6

2.2 IA186EB Pin/Signal Descriptions

Descriptions of the pin and signal functions for the IA186EB microcontroller are provided in Table 7.

Several of the IA186EB pins have different functions depending on the operating mode of the device. Each of the different signals supported by a pin is listed and defined in Table 7—indexed alphabetically in the first column of the table. Additionally, the name of the pin associated with the signal as well as the pin numbers for the PLCC, LQFP, and PQFP packages are provided in the "Pin" column. Signals not used in a specific package type are designated "NA."

Table 7. IA186EB Pin/Signal Descriptions

<table>
<tr><th rowspan="2">Signal</th><th colspan="4">Pin</th><th rowspan="2">Description</th></tr>
<tr><th>Name</th><th>PLCC</th><th>LQFP</th><th>PQFP</th></tr>
<tr><td>a16 (output only)</td><td>a16</td><td>80</td><td>66</td><td>29</td><td rowspan="4">address Bits [16–19]. Input/Output. These pins provide the four most-significant bits of the Address Bus. During the address portion of the IA186EB bus cycle, Address Bits [16–19] are presented on the bus and can be latched using the ale signal (see table entry). During the data portion of the IA186EB bus cycle, these lines are driven to a logic 0.</td></tr>
<tr><td>a17 (output only)</td><td>a17</td><td>81</td><td>67</td><td>30</td></tr>
<tr><td>a18 (output only)</td><td>a18</td><td>82</td><td>68</td><td>31</td></tr>
<tr><td>a19</td><td>a19/once_n</td><td>83</td><td>69</td><td>32</td></tr>
<tr><td>ad0</td><td>ad0</td><td>61</td><td>47</td><td>10</td><td rowspan="16">address/data Bits [0–15]. Input/Output. These pins provide the multiplexed Address Bus and Data Bus. During the address portion of the IA186EB bus cycle, Address Bits [0–15] are presented on the bus and can be latched using the ale signal (see next table entry). During the data portion of the IA186EB bus cycle, 8- or 16-bit data are present on these lines.</td></tr>
<tr><td>ad1</td><td>ad1</td><td>66</td><td>52</td><td>15</td></tr>
<tr><td>ad2</td><td>ad2</td><td>68</td><td>54</td><td>17</td></tr>
<tr><td>ad3</td><td>ad3</td><td>70</td><td>56</td><td>19</td></tr>
<tr><td>ad4</td><td>ad4</td><td>72</td><td>58</td><td>21</td></tr>
<tr><td>ad5</td><td>ad5</td><td>74</td><td>60</td><td>23</td></tr>
<tr><td>ad6</td><td>ad6</td><td>76</td><td>62</td><td>25</td></tr>
<tr><td>ad7</td><td>ad7</td><td>78</td><td>64</td><td>27</td></tr>
<tr><td>ad8</td><td>ad8</td><td>62</td><td>48</td><td>11</td></tr>
<tr><td>ad9</td><td>ad9</td><td>67</td><td>53</td><td>16</td></tr>
<tr><td>ad10</td><td>ad10</td><td>69</td><td>55</td><td>18</td></tr>
<tr><td>ad11</td><td>ad11</td><td>71</td><td>57</td><td>20</td></tr>
<tr><td>ad12</td><td>ad12</td><td>73</td><td>59</td><td>22</td></tr>
<tr><td>ad13</td><td>ad13</td><td>75</td><td>61</td><td>24</td></tr>
<tr><td>ad14</td><td>ad14</td><td>77</td><td>63</td><td>26</td></tr>
<tr><td>ad15</td><td>ad15</td><td>79</td><td>65</td><td>28</td></tr>
</table>

Table 7. IA186EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	LQFP	PQFP	
clkin	clkin	41	28	71	**cl**ock **in**put. Input. The **clkin** pin is the input connection for an external clock. An external oscillator operating at two times the required processor operating frequency can be connected to this pin. If a crystal is used to supply the clock, it is connected between the **clkin** pin and the **oscout** pin (see oscout table entry). When a crystal is connected, it drives an internal Pierce oscillator to the IA186EB.
clkout	clkout	44	31	74	**cl**ock **out**put. Output. The **clkout** pin provides a timing reference for inputs and outputs of the IA186EB. This clock output is one-half the input clock (**clkin**) frequency. The **clkout** signal has a 50% duty cycle, transitioning every falling edge of **clkin**.
cts0_n	cts0_n	51	38	1	**c**lear **t**o **s**end, Serial Port **0**. Input. Active Low. When this input is high (i.e., not asserted), data transmission from Serial Port 0 is inhibited. When the signal is asserted (low), data transmission is permitted.
cts1_n	p2.4/**cts1_n**	56	43	6	**c**lear **t**o **s**end, Serial Port **1**. Input. Active Low. When this input is high (i.e., not asserted), data transmission from Serial Port 1 is inhibited. When the signal is asserted (low), data transmission is permitted.
den_n	den_n	11	80	43	**d**ata **en**able. Output. Active Low. This signal is used to enable of bidirectional transceivers in a buffered system. The **den_n** signal is asserted (low) only when data is to be transferred on the bus.
dt/r_n	dt/r_n	16	NA	NA	**d**ata **t**ransmit/**r**eceive. Output. This signal is used to control the direction of data flow for bidirectional buffers in a buffered system. When **dt/r_n** is high, the direction indicated is transmit; when **dt/t_n** is low, the direction indicated is receive.
error_n	error_n	3	NA	NA	**error**. Input. Active Low. When this signal is asserted (low), it indicates that the last numerics coprocessor operation resulted in an exception condition.

Table 7. IA186EB Pin/Signal Descriptions *(Continued)*

Signal	Pin Name	PLCC	LQFP	PQFP	Description
gcs0_n	p1.0/**gcs0_n**	28	16	59	**g**eneric **c**hip **s**elect **n** (n = 0–7). Output. Active Low. When programmed and enabled, each of these pins provide a chip select signal that will be asserted (low) whenever the address of a memory or I/O bus cycle is within the address space programmed for that output.
gcs1_n	p1.1/**gcs1_n**	27	15	58	
gcs2_n	p1.2/**gcs2_n**	26	14	57	
gcs3_n	p1.3/**gcs3_n**	25	13	56	
gcs4_n	p1.4/**gcs4_n**	24	12	55	
gcs5_n	p1.5/**gcs5_n**	21	9	52	
gcs6_n	p1.6/**gcs6_n**	20	8	51	
gcs7_n	p1.7/**gcs7_n**	19	7	50	
hlda	hlda	12	1	44	**h**o**l**d **a**cknowledge. Output. Active High. When **hlda** is asserted (high), it indicates that the IA186EB has relinquished control of the local bus to another bus master in response to a HOLD request (see next table entry). When **hlda** is asserted, the IA186EB data bus and control signals float, allowing another bus master to drive the signals directly.
hold	hold	13	2	45	**hold**. Input. Active High. This signal is a request indicating that an external bus master wishes to gain control of the local bus. The IA186EB will relinquish control of the local bus between instruction boundaries not conditioned by a LOCK prefix.
int0 (input)	int0 (input only)	31	19	62	**interrupt n** (n = 0-4). Input/Output. Active High. These maskable inputs interrupt program flow and cause execution to continue at an interrupt vector of a specific interrupt type as follows: **int0**: Type 12 **int1**: Type 13 **int2**: Type 14 **int3**: Type 15 **int4**: Type 17 To allow interrupt expansion, **int0** and **int1** can be used with the interrupt acknowledge signals **inta0_n** and **inta1_n** (see next table entries) to serve as external interrupt inputs or interrupt acknowledge outputs.
int1 (input)	int1 (input only)	32	20	63	
int2	**int2**/inta0_n	33	21	64	
int3	**int3**/inta1_n	34	22	65	
int4 (input)	int4 (input only)	35	23	66	
inta0_n	int2/**inta0_n**	33	21	64	**int**errupt **a**cknowledge **0**. Input/Output. Active Low. This pin provides an interrupt acknowledge handshake in response to an interrupt request on the **int0** pin (see previous table entry).

Table 7. IA186EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	LQFP	PQFP	
pdtmr	pdtmr	36	24	67	**p**ower-**d**own **t**i**m**e**r**. Input/Output (push-pull). Note: The IA186EB enters Powerdown Mode when the PWRDN bit in the Power Control Register is set to 1 and a HALT instruction is executed. Exit from the Powerdown Mode occurs upon receipt of a non-maskable interrupt (i.e., assertion of the **nmi** input) or a reset (i.e., assertion of the **resin_n** input). The **pdtmr** pin, which is normally connected to an external capacitor, determines the amount of time that the IA186EB waits before resuming normal operation after an exit from the Powerdown when a non-maskable interrupt is received—essentially a delay between the assertion of the **nmi** input and the enabling of the IA186EB internal clocks. The delay required depends on the start-up characteristics of the crystal oscillator. The **pdtmr** pin does not apply when the Powerdown Mode is exited by the receipt of a reset (i.e., the assertion **resin_n**).
pereq	pereq	39	NA	NA	numerics co**p**rocessor **e**xternal **req**uest. Input. Active High. When asserted (high), this signal indicates that a data transfer between an Intel 80C187 Numerics Coprocessor.and memory is pending. *This applies to the PLCC only.*
rd_n	rd_n	4	73	36	**r**ea**d**. Output. Active Low. When asserted (low), **rd_n** indicates that the accessed memory or I/O device must drive data from the location being accessed onto the data bus.
ready	ready	18	6	49	**ready**. Input. Active High. When asserted (high) the **ready** line indicates a bus-cycle completion. This signal must be active to terminate any bus cycle unless the IA186EB Chip-Select Unit is configured to ignore ready.
resin_n	resin_n	37	25	68	**res**et **in**put. Input. Active Low. When **resin_n** is asserted (low), the IA186EB immediately terminates any bus cycle in progress and assumes an initialized state. All pins are driven to a known state, and **resout** (see next table entry) is asserted.

2.3 IA188EB Pin/Signal Descriptions

Descriptions of the pin and signal functions for the IA188EB microcontroller are provided in Table 8.

Several of the IA188EB pins have different functions depending on the operating mode of the device. Each of the different signals supported by a pin is listed and defined in Table 8—indexed alphabetically in the first column of the table. Additionally, the name of the pin associated with the signal as well as the pin numbers for the PLCC, LQFP, and LQFP packages are provided in the "Pin" column.

Table 8. IA188EB Pin/Signal Descriptions

Signal	Pin				Description
	Name	PLCC	LQFP	PQFP	
a8	a8	62	48	11	**a**ddress Bits [**8-19**]. Output. These pins provide the 12 most-significant bits of the Address Bus. During the entire IA188EB bus cycle, Address Bits [8–19] are presented on the bus and can be latched using the **ale** signal (see table entry).
a9	a9	67	53	16	
a10	a10	69	55	18	
a11	a11	71	57	20	
a12	a12	73	59	22	
a13	a13	75	61	24	
a14	a14	77	63	26	
a15	a15	79	65	28	
a16	a16	80	66	29	
a17	a17	81	67	30	
a18	a18	82	68	31	
a19	**a19**/once_n	83	69	32	
ad0	ad0	61	47	10	**a**ddress/**d**ata Bits [**0**–**7**]. Input/Output. These pins provide a multiplexed Address Bus and Data Bus. During the address portion of the IA188EB bus cycle, Address Bits [0–7] are presented on the bus and can be latched using the **ale** signal (see next table entry). During the data portion of the IA188EB bus cycle, 8-bit data are present on these lines.
ad1	ad1	66	52	15	
ad2	ad2	68	54	17	
ad3	ad3	70	56	19	
ad4	ad4	72	58	21	
ad5	ad5	74	60	23	
ad6	ad6	76	62	25	
ad7	ad7	78	64	27	
ale	ale	6	75	38	**a**ddress **l**atch **e**nable. Output. Active High. This signal is used to latch the address information during the address portion of a bus cycle.
bclk0	p2.5/**bclk0**	54	41	4	**b**aud **cl**oc**k**, Serial Port **0**. Input. The **bclk0** pin can be used to provide an alternate clock source for Serial Port 0. The input clock rate cannot be greater than one-half the operating frequency of the IA188EB.

Table 8. IA188EB Pin/Signal Descriptions *(Continued)*

<table>
<tr><th rowspan="2">Signal</th><th colspan="4">Pin</th><th rowspan="2">Description</th></tr>
<tr><th>Name</th><th>PLCC</th><th>LQFP</th><th>PQFP</th></tr>
<tr><td>rxd0</td><td>rxd0</td><td>53</td><td>40</td><td>3</td><td>Receive (rx) data, Serial Port 0. Input/Output. This pin is the serial data input for Serial Port 0. During synchronous serial communications, rxd0 is bidirectional and functions an output for data transmission (txd0 becomes the clock).</td></tr>
<tr><td>rxd1</td><td>p2.0/rxd1</td><td>57</td><td>44</td><td>7</td><td>Receive (rx) data, Serial Port 1. Input/Output. This pin is the serial data input for Serial Port 1. During synchronous serial communications, rxd1 is bidirectional and functions an output for data transmission (txd1 becomes the clock).</td></tr>
<tr><td>s0_n</td><td>s0_n</td><td>10</td><td>79</td><td>42</td><td rowspan="3">statusN (N = 0–2). Output. During a bus cycle the status (i.e., type) of cycle is encoded on these lines as follows:

s2_n s1_n s0_n Bus Cycle Status

0 0 0 Interrupt Acknowledge
0 0 1 Read I/O
0 1 0 Write I/O
0 1 1 Processor HALT
1 0 0 Queue Instruction Fetch
1 0 1 Read Memory
1 1 0 Write Memory
1 1 1 No Bus Activity</td></tr>
<tr><td>s1_n</td><td>s1_n</td><td>9</td><td>78</td><td>41</td></tr>
<tr><td>s2_n</td><td>s2_n</td><td>8</td><td>77</td><td>40</td></tr>
<tr><td>sint1</td><td>p2.3/sint1</td><td>55</td><td>42</td><td>5</td><td>serial interrupt, Serial Port 1. Output. Active High. When sint1 is asserted (high), it indicates that Serial Port 1 requires service.</td></tr>
<tr><td>t0in</td><td>t0in</td><td>46</td><td>33</td><td>76</td><td>timer 0 input. Input. Depending on the Timer Mode programmed for Timer 0, this input is used either as clock input or a control signal.</td></tr>
<tr><td>t0out</td><td>t0out</td><td>45</td><td>32</td><td>75</td><td>timer 0 output. Output. Depending on the Timer Mode programmed for Timer 0, this output can provide a single clock or a continuous waveform.</td></tr>
<tr><td>t1in</td><td>t1in</td><td>48</td><td>35</td><td>78</td><td>timer 1 input. Input. Depending on the Timer Mode programmed for Timer 1, this input is used either as clock input or a control signal.</td></tr>
<tr><td>t1out</td><td>t1out</td><td>47</td><td>34</td><td>77</td><td>timer 1 output. Output. Depending on the Timer Mode programmed for Timer 1, this output can provide a single clock or a continuous waveform.</td></tr>
</table>

3. Maximum Ratings, Thermal Characteristics, and DC Parameters

For the Innovasic Semiconductor IA186EB and IA188EB microcontrollers, the absolute maximum ratings, thermal characteristics, and DC parameters are provided in Tables 9 through 11, respectively.

Table 9. IA186EB and IA188EB Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−40°C to +125°C
Supply Voltage with Respect to v_{ss}	−0.3V to +6.0V
Voltage on Pins other than Supply with Respect to v_{ss}	−0.3V to +(Vcc + 0.3)V

Table 10. IA186EB and IA188EB Thermal Characteristics

Symbol	Characteristic	Value	Units
T_A	Ambient Temperature	-40°C to 85°C	°C
P_D	Power Dissipation	MHz × ICC × V/1000	W
Θ_{Ja}	84-Pin PLCC Package	30.7	°C/W
	80-Pin PQFP Package	46	
	80-Pin LQFP Package	52	
T_J	Average Junction Temperature	$T_A + (P_D \times \Theta_{Ja})$	°C

4. Functional Description

4.1 Device Architecture

Architecturally, the IA186EB and IA188EB microcontrollers include the following functional modules:

- Bus Interface Unit
- Clock Generator
- Interrupt Control Unit
- Timer/Counter Unit
- Serial Communications Unit
- Chip-Select Unit
- I/O Port Unit
- Refresh Control Unit
- Power Management Unit

A functional block diagram of the IA186EB/IA188EB is shown in Figure 10. Descriptions of the functional modules are provided in the following subsections.

4.1.1 Bus Interface Unit

The IA186EB/IA188EB bus controller that generates local bus control signals and uses a hold/hlda protocol to share the local bus with other bus masters. The bus controller generates 20 address bits, read and write control signals, and bus-cycle status information. A ready input is used to extend a bus cycle beyond the minimum four clock cycles.

4.1.2 Clock Generator

The IA186EB/IA188EB uses an on-chip clock generator to supply internal and external clocks. The clock generator makes use of a crystal oscillator and includes a divide-by-two counter.

Figure 11 shows the various operating modes of the clock circuit. The clock circuit can use either a parallel resonant fundamental mode crystal network (A) or a third-overtone mode crystal network (B), or it can be driven by an external clock source (C).

The following parameters are recommended when choosing a crystal:

- Temperature Range
  - Application Specific
  - ESR (Equivalent Series Resistance): 40Ω max
  - C0 (Shunt Capacitance of Crystal): 7.0 pF max
  - CL (Load Capacitance): 20 pF ± 2 pF
  - Drive Level: 1 mW max

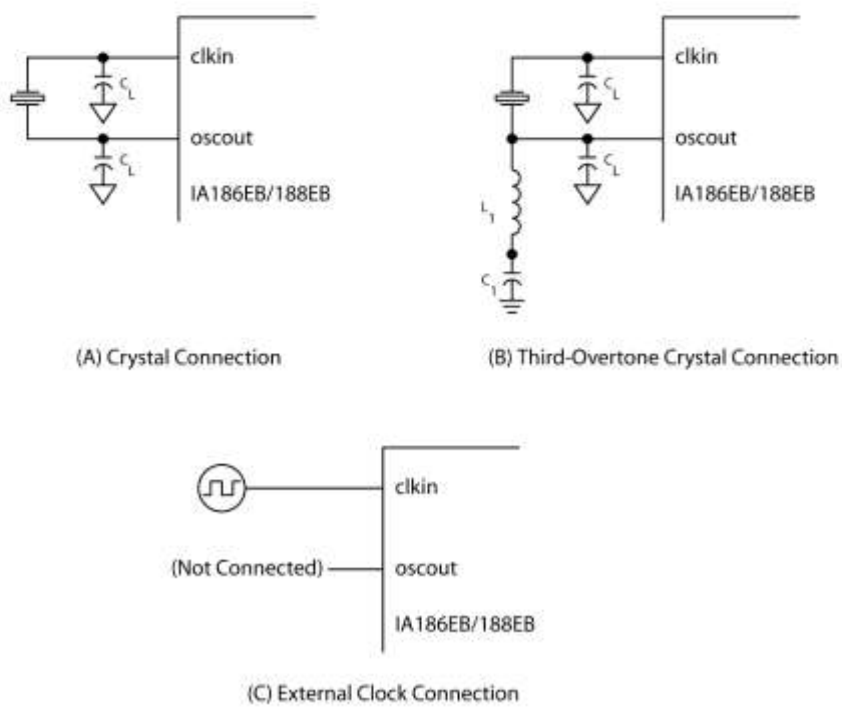

Figure 11. Clock Circuit Connection Options

- Power Management Unit

The registers associated with each integrated peripheral are contained within a 128 × 16 register file called the Peripheral Control Block (PCB). The PCB can be located in either memory or I/O space on any 256-byte address boundary.

Table 12 provides a list of the registers associated with the PCB.

Table 12. Peripheral Control Block Registers

PCB Offset	Function	PCB Offset	Function	PCB Offset	Function	PCB Offset	Function
00H	Reserved	40H	Timer2 Count	80H	GCS0 Start	C0H	Reserved
02H	End Of Interrupt	42H	Timer2 Compare	82H	GCS0 Stop	C2H	Reserved
04H	Poll	44H	Reserved	84H	GCS1 Start	C4H	Reserved
06H	Poll Status	46H	Timer2 Control	86H	GCS1 Stop	C6H	Reserved
08H	Interrupt Mask	48H	Reserved	88H	GCS2 Start	C8H	Reserved
0AH	Priority Mask	4AH	Reserved	8AH	GCS2 Stop	CAH	Reserved
0CH	In-Service	4CH	Reserved	8CH	GCS3 Start	CCH	Reserved
0EH	Interrupt Request	4EH	Reserved	8EH	GCS3 Stop	CEH	Reserved
10H	Interrupt Status	50H	Port 1 Direction	90H	GCS4 Start	D0H	Reserved
12H	Timer Control	52H	Port 1 Pin	92H	GCS4 Stop	D2H	Reserved
14H	Serial Control	54H	Port 1 Control	94H	GCS5 Start	D4H	Reserved
16H	INT4 Control	56H	Port 1 Latch	96H	GCS5 Stop	D6H	Reserved
18H	INT0 Control	58H	Port 2 Direction	98H	GCS6 Start	D8H	Reserved
1AH	INT1 Control	5AH	Port 2 Pin	9AH	GCS6 Stop	DAH	Reserved
1CH	INT2 Control	5CH	Port 2 Control	9CH	GCS7 Start	DCH	Reserved
1EH	INT3 Control	5EH	Port 2 Latch	9EH	GCS7 Stop	DEH	Reserved

Table 12. Peripheral Control Block Registers *(Continued)*

PCB Offset	Function	PCB Offset	Function	PCB Offset	Function	PCB Offset	Function
20H	Reserved	60H	Serial0 Baud	A0H	LCS Start	E0H	Reserved
22H	Reserved	62H	Serial0 Count	A2H	LCS Stop	E2H	Reserved
PCB Offset	Offset	PCB Offset	Function	PCB Offset	Function	PCB Offset	Function
24H	Reserved	64H	Serial0 Control	A4H	UCS Start	E4H	Reserved
26H	Reserved	66H	Serial0 Status	A6H	UCS Stop	E6H	Reserved
28H	Reserved	68H	Serial0 RBUF	A8H	Relocation	E8H	Reserved
2AH	Reserved	6AH	Serial0 TBUF	AAH	Reserved	EAH	Reserved
2CH	Reserved	6CH	Reserved	ACH	Reserved	ECH	Reserved
2EH	Reserved	6EH	Reserved	AEH	Reserved	EEH	Reserved
30H	Timer0 Count	70H	Serial1 Baud	B0H	Refresh Base	F0H	Reserved
32H	Timer0 Compare A	72H	Serial1 Count	B2H	Refresh Time	F2H	Reserved
34H	Timer0 Compare B	74H	Serial1 Control	B4H	Refresh Control	F4H	Reserved
36H	Timer0 Control	76H	Serial1 Status	B6H	Refresh Address	F6H	Reserved
38H	Timer1 Count	78H	Serial1 RBUF	B8H	Power Control	F8H	Reserved
3AH	Timer1 Compare A	7AH	Serial1 TBUF	BAH	Reserved	FAH	Reserved
3CH	Timer1 Compare B	7CH	Reserved	BCH	Step ID[1]	FCH	Reserved
3EH	Timer1 Control	7EH	Reserved	BEH	Reserved	FEH	Reserved

Note:

[1]The **Step ID** register (offset 0xBC) for Revision 2 of the Innovasic device is read-only, and is uniquely identified in software by having a value of 0x0080. The original Intel device established a value between 0x0000 and 0x0002, depending on the revision of the part.

6. Reset Operation

The IA186EB/IA188EB will perform a reset operation any time the resin_n pin is active. Figure 18 shows the reset sequence when power is applied to the IA186EB/IA188EB. An external clock connected to clkin must not exceed the V_{CC} threshold being applied to the processor. This is normally not a problem if the clock driver is supplied with the same V_{CC} that supplies the processor. When attaching a crystal to the device, resin_n must remain active until both V_{CC} and clkout are stable (the length of time is application-specific and depends on the startup characteristics of the crystal circuit). The resin_n pin is designed to operate correctly using an RC reset circuit, but the designer must ensure that the ramp time for V_{CC} is not so long that resin_n is never really sampled at a logic low level when V_{CC} reaches minimum operating conditions.

Note: Failure to assert resin_n while the device is powering up will result in unpredictable operation.

Figure 19, Warm Reset Timing, shows the timing sequence when resin_n is applied after V_{cc} is stable and the device has been operating. Any bus operation that is in progress at the time resin_n is asserted will terminate immediately.

While resin_n is active, bus signals lock_n, a19/once_n, and a18–a16 are configured as inputs and weakly held high by internal pull-up transistors. Only a19/ once_n can be overdriven to a low-to-enable ONCE Mode.

7. Bus Timing

Figures 18 through 26 on the following pages present the various bus cycles that are generated by the processor. The figures show the relationship of the various bus signals to clkout. Together with the information present in AC Characteristics, the figures allow the user to determine all the critical timing analysis needed for a given application.

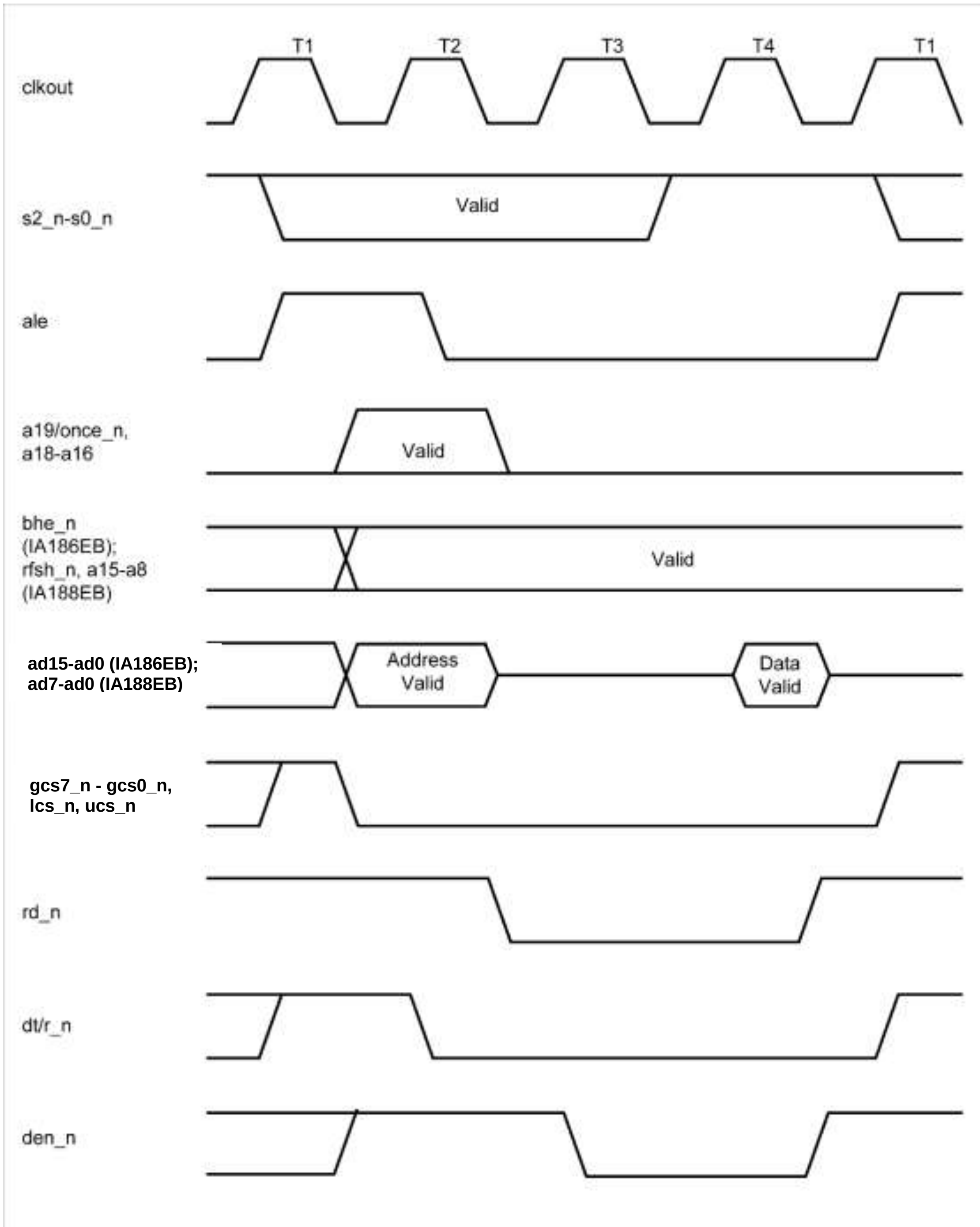

Figure 20. Read, Fetch, and Refresh Cycle Timing

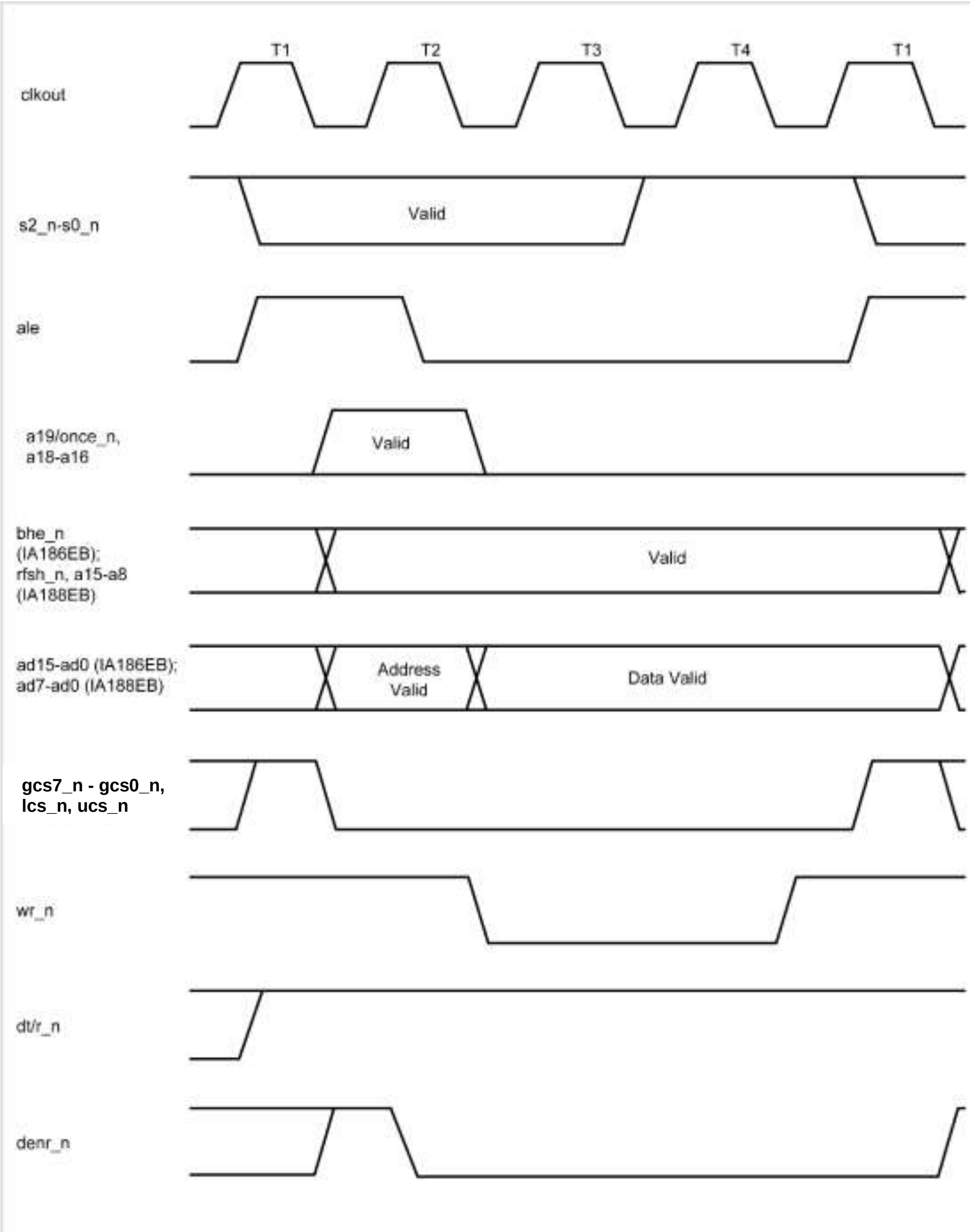

Figure 21. Write Cycle Timing

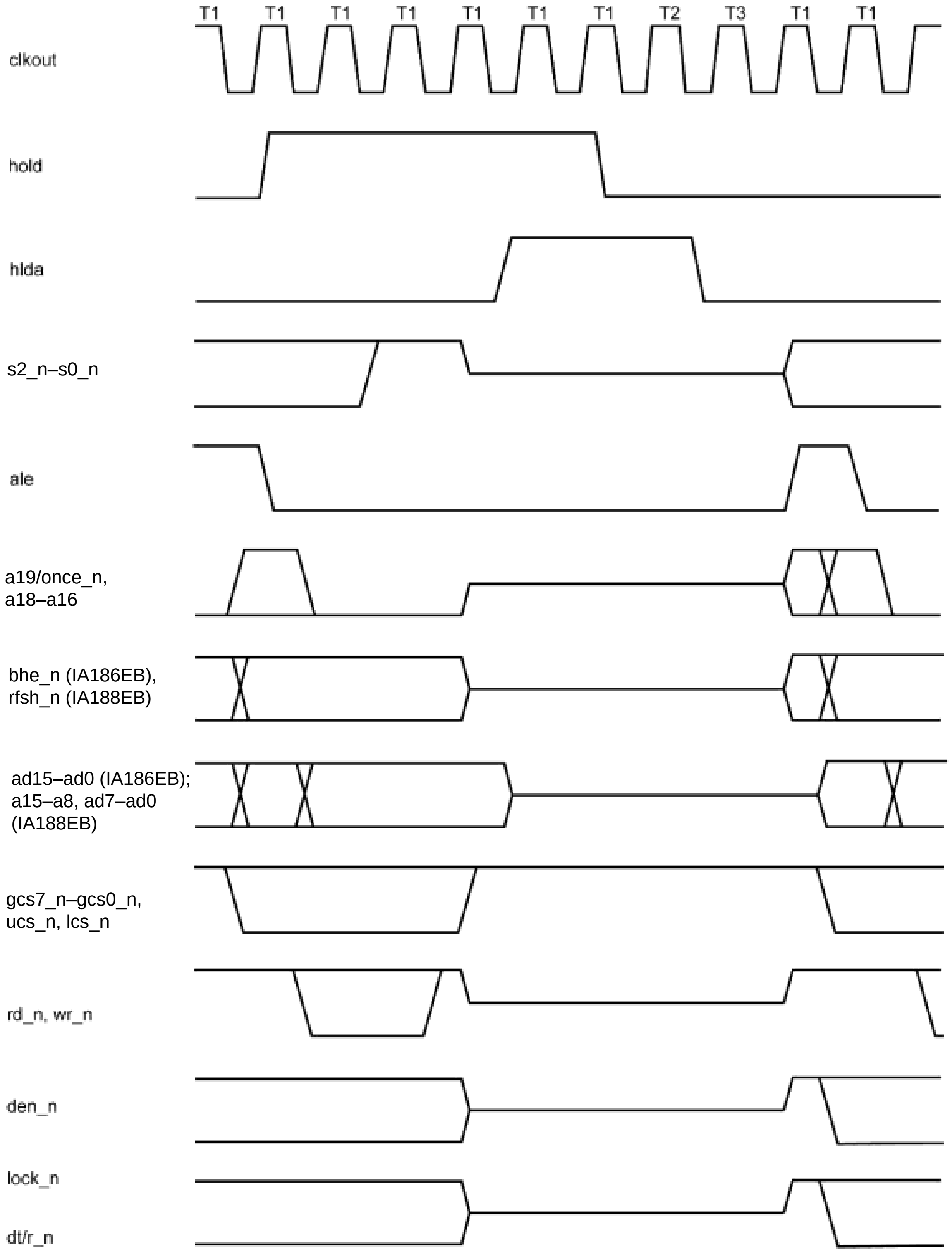

Figure 24. hold/hlda Timing

Table 21. Instruction Set Timing *(Continued)*

Instruction	Clock Cycles IA186EB	IA188EB	Comments
DIV Memory-Byte	46	46	–
DIV Memory-Word	49	51	–
DIV Register-Byte	39	39	–
DIV Register-Word	39	39	–
IDIV Memory-Byte	46	46	–
IDIV Memory-Word	49	51	–
IDIV Register-Byte	39	39	–
IDIV Register-Word	39	39	–
IMUL Immediate (signed)	5/24	5/33	register/memory
IMUL Memory-Byte	4	20	–
IMUL Memory-Word	13	28	–
IMUL Register-Byte	5	5	–
IMUL Register-Word	5	5	–
INC Register	1	1	–
INS	8	16	–
INS (repeated *n* times)	8+8*n*	16+16*n*	–
INT Type specified	33	41	–
INT Type 3	33	41	–
INTO	33	48	–
IRET	30	30	–
JA	3/5	3/5	Jump not taken/Jump taken
JAE	3/5	3/5	
JB	3/5	3/5	
JBE	3/5	3/5	
JCXZ	3/4	3/4	Jump not taken/Jump taken
JE	3/5	3/5	Jump not taken/Jump taken
JG	3/5	3/5	
JGE	3/5	3/5	
JL	3/5	3/5	
JLE	3/5	3/5	
JMP Direct intersegment	3	3	–
JMP Direct within segment	3	3	–
JMP Short/long	4	4	–
JNA	3/5	3/5	Jump not taken/Jump taken
JNAE	3/5	3/5	
JNB	3/5	3/5	
JNBE	3/5	3/5	
JNE	3/5	3/5	
JNG	3/5	3/5	
JNGE	3/5	3/5	
JNL	3/5	3/5	
JNLE	3/5	3/5	
JNO	3/5	3/5	
JNP	3/5	3/5	

Errata No. 12

Problem:
Illegal serial port modes do not match OEM part.

Description: If the mode bits of the serial control register (S1CON, S0CON) are set to an illegal encoding (0x5, 0x6, or 0x7), the Innovasic part acts as though it were in mode 4. The OEM part acts as if it were in mode 1.

Workaround: Use a valid encoding for serial mode.

Errata No. 13

Problem:

Non-maskable interrupt (NMI) can be pre-empted by maskable interrupt.

Description: When instruction execution unit is in Decode state for 2 or more consecutive cycles and an NMI is recognized, it could be pre-empted by a maskable interrupt.

Workaround: None.

Errata No. 14

Problem:

Ready signal may not be recognized in bus cycles with zero wait states.

Description: When a chip select is set to use the ready signal to extend a bus cycle that normally has no wait states (Start register bits 3-0 == 0000), the ready signal may not be recognized in time to extend the bus cycle.

Workaround: Set wait states to 1 or more if using ready to extend bus cycles.