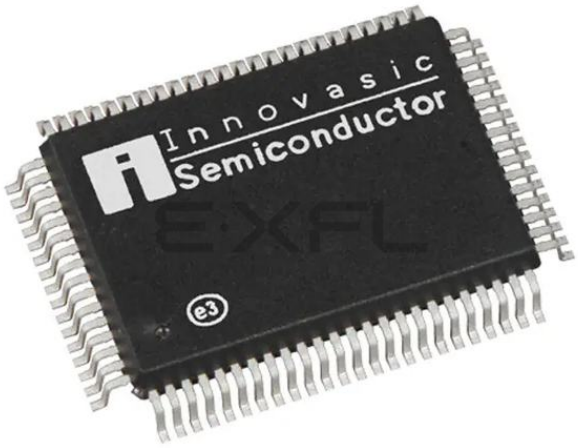

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	-
Core Size	8/16-Bit
Speed	50MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	16
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-PQFP (20x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ia188ebpqf80ir2

LIST OF TABLES

1. Introduction

The Innovasic Semiconductor IA186EB and IA188EB microcontrollers are form, fit, and function replacements for the original Intel® 80C186EB, 80C188EB, 80L186EB, and 80L188EB 16-bit high-integration embedded processors.

These devices are produced using Innovasic's Managed IC Lifetime Extension System (MILES™). This cloning technology, which produces replacement ICs beyond simple emulations, ensures complete compatibility with the original device, including any "undocumented features." Additionally, the MILES process captures the clone design in such a way that production of the clone can continue even as silicon technology advances.

The IA186EB and IA188EB microcontrollers replace the obsolete Intel 80C186EB and 80C188EB devices, allowing users to retain existing board designs, software compilers/assemblers, and emulation tools, thereby avoiding expensive redesign efforts.

1.1 General Description

The Innovasic Semiconductor IA186EB and IA188EB microcontrollers are an upgrade for the 80C186EB/80C188EB microcontroller designs with integrated peripherals to provide increased functionality and reduce system costs. The IA186EB and IA188EB devices are designed to satisfy requirements of embedded products designed for telecommunications, office automation and storage, and industrial controls.

The IA186EB and IA188EB microcontrollers have a set of base peripherals beneficial to many embedded applications and include a standard numeric interface, an interrupt control unit, a chip-select unit, a DRAM refresh control unit, a power management unit, and three 16-bit timer/counters.

The IA186EB and IA188EB microcontrollers are capable of operating at 5.0 or 3.3 volts. This datasheet discusses both modes of operation. Where applicable, characteristics specific to either 3.3 or 5.0 volt operation are identified separately throughout this datasheet.

Additionally, the IA186EB and IA188EB include two integrated serial ports that support both synchronous and asynchronous communications, simplifying inter-processor and display communications. The IA186EB and IA188EB also have an enhanced chip-select unit and two multiplexed I/O ports. The enhanced chip-select unit offers 10 general chip selects, each with the ability to address up to 1 Mbyte. This enhanced unit enables memory-bank switching to expand the IA186EB/IA188EB 1 Mbyte address space. The I/O ports allow for basic functions such as scanning keypads for input. The ports can also be used to control system power consumption, disabling unneeded components.

The serial ports, I/O capabilities, and enhanced chip selects make the IA186EB/IA188EB an excellent processor for portable data acquisition or communication applications.

2. Packaging, Pin Descriptions, and Physical Dimensions

Information on the packages and pin descriptions for the IA186EB and the IA188EB is provided separately. Refer to sections, figures, and tables for information on the device of interest.

2.1 Packages and Pinouts

The Innovasic Semiconductor IA186EB and IA188EB microcontroller is available in the following packages:

- 84-Pin Plastic Leaded Chip Carrier (PLCC), equivalent to original PLCC package
- 80-Pin Plastic Quad Flat Pack (PQFP), equivalent to original PQFP package
- 80-Pin Low-Profile Quad Flat Pack (LQFP), equivalent to original SQFP package

Table 1. IA186EB 84-Pin PLCC Pin Listing

Pin	Name
1	V_{cc}
2	V_{ss}
3	error_n
4	rd_n
5	wr_n
6	ale
7	bhe_n
8	s2_n
9	s1_n
10	s0_n
11	den_n
12	hlda
13	hold
14	test_n/busy
15	lock_n
16	dt/r_n
17	nmi
18	ready
19	p1.7/gcs7_n
20	p1.6/gcs6_n
21	p1.5/gcs5_n

Pin	Name
22	V_{ss}
23	V_{cc}
24	p1.4/gcs4_n
25	p1.3/gcs3_n
26	p1.2/gcs2_n
27	p1.1/gcs1_n
28	p1.0/gcs0_n
29	lcs_n
30	ucs_n
31	int0
32	int1
33	int2/inta0_n
34	int3/inta1_n
35	int4
36	pdtmr
37	resin_n
38	resout
39	pereq
40	oscout
41	clkin
42	V_{cc}

Pin	Name
43	V_{ss}
44	clkout
45	t0out
46	t0in
47	t1out
48	t1in
49	p2.7
50	p2.6
51	cts0_n
52	txd0
53	rxd0
54	p2.5/bclk0
55	p2.3/sint1
56	p2.4/cts1_n
57	p2.0/rxd1
58	p2.1/txd1
59	p2.2/bclk1
60	ncs_n
61	ad0
62	ad8
63	V_{ss}

Pin	Name
64	V_{cc}
65	V_{ss}
66	ad1
67	ad9
68	ad2
69	ad10
70	ad3
71	ad11
72	ad4
73	ad12
74	ad5
75	ad13
76	ad6
77	ad14
78	ad7
79	ad15
80	a16
81	a17
82	a18
83	a19/once_n
84	V_{ss}

2.1.2 IA188EB 84 PLCC Package

The pinout for the IA188EB 84 PLCC Package is as shown in Figure 2. The corresponding pinout is provided in Table 2.

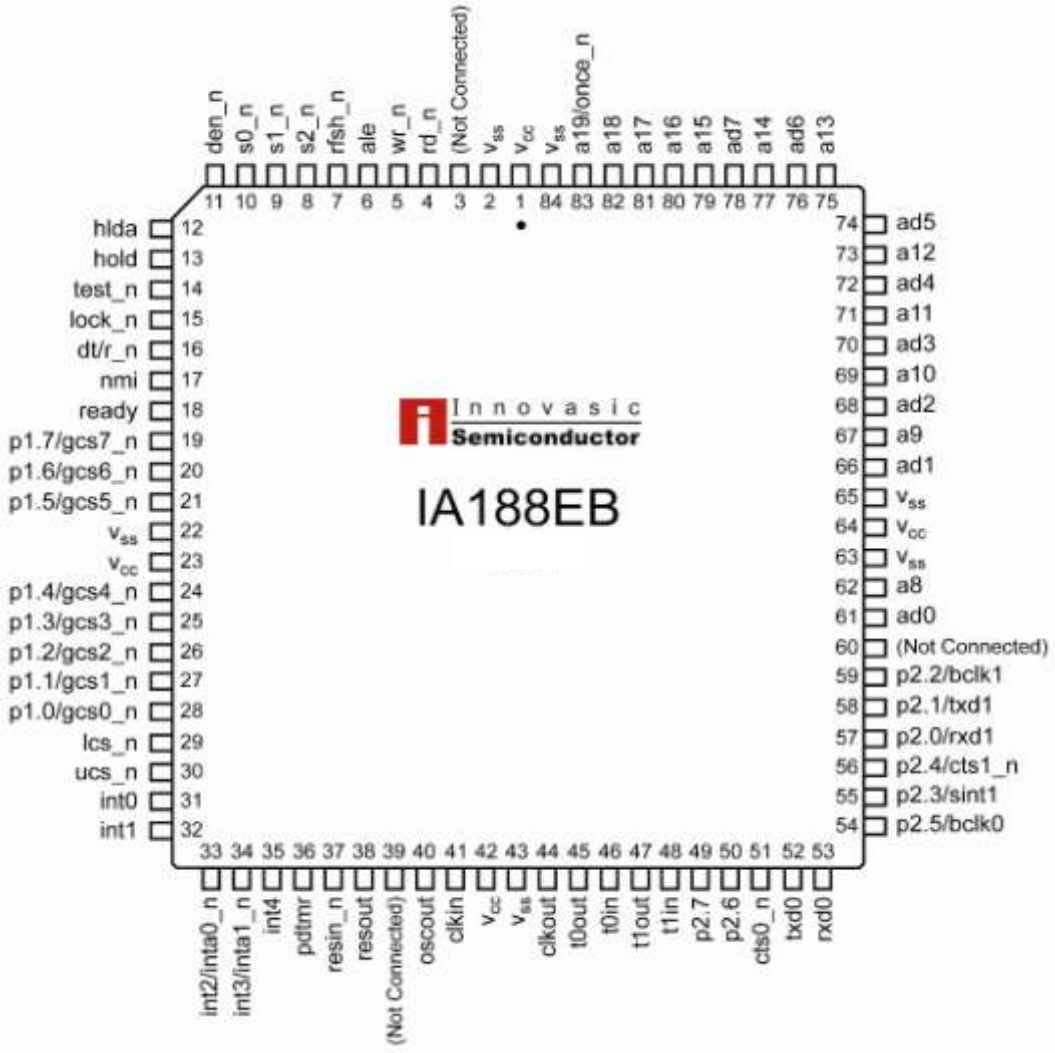

Figure 2. IA188EB 84-Pin PLCC Package Diagram

Table 5. IA186EB 80-Pin LQFP Pin Listing

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	hlda	21	int2/inta0_n	41	p2.5/bclk0	61	ad13
2	hold	22	int3/inta1_n	42	p2.3/sint1	62	ad6
3	test_n	23	int4	43	p2.4/cts1_n	63	ad14
4	lock_n	24	pdtmr	44	p2.0/rxd1	64	ad7
5	nmi	25	resin_n	45	p2.1/txd1	65	ad15
6	ready	26	resout	46	p2.2/bclk1	66	a16
7	p1.7/gcs7_n	27	oscout	47	ad0	67	a17
8	p1.6/gcs6_n	28	clkin	48	ad8	68	a18
9	p1.5/gcs5_n	29	V_{cc}	49	V_{ss}	69	a19/once_n
10	V_{ss}	30	V_{ss}	50	V_{cc}	70	V_{ss}
11	V_{cc}	31	clkout	51	V_{ss}	71	V_{cc}
12	p1.4/gcs4_n	32	t0out	52	ad1	72	V_{ss}
13	p1.3/gcs3_n	33	t0in	53	ad9	73	rd_n
14	p1.2/gcs2_n	34	t1out	54	ad2	74	wr_n
15	p1.1/gcs1_n	35	t1in	55	ad10	75	ale
16	p1.0/gcs0_n	36	p2.7	56	ad3	76	bhe_n
17	lcs_n	37	p2.6	57	ad11	77	s2_n
18	ucs_n	38	cts0_n	58	ad4	78	s1_n
19	int0	39	txd0	59	ad12	79	s0_n
20	int1	40	rxd0	60	ad5	80	den_n

2.1.8 IA188EB 80 LQFP Package

The pinout for the IA188EB 80 LQFP Package is as shown in Figure 8. The corresponding pinout is provided in Table 6.

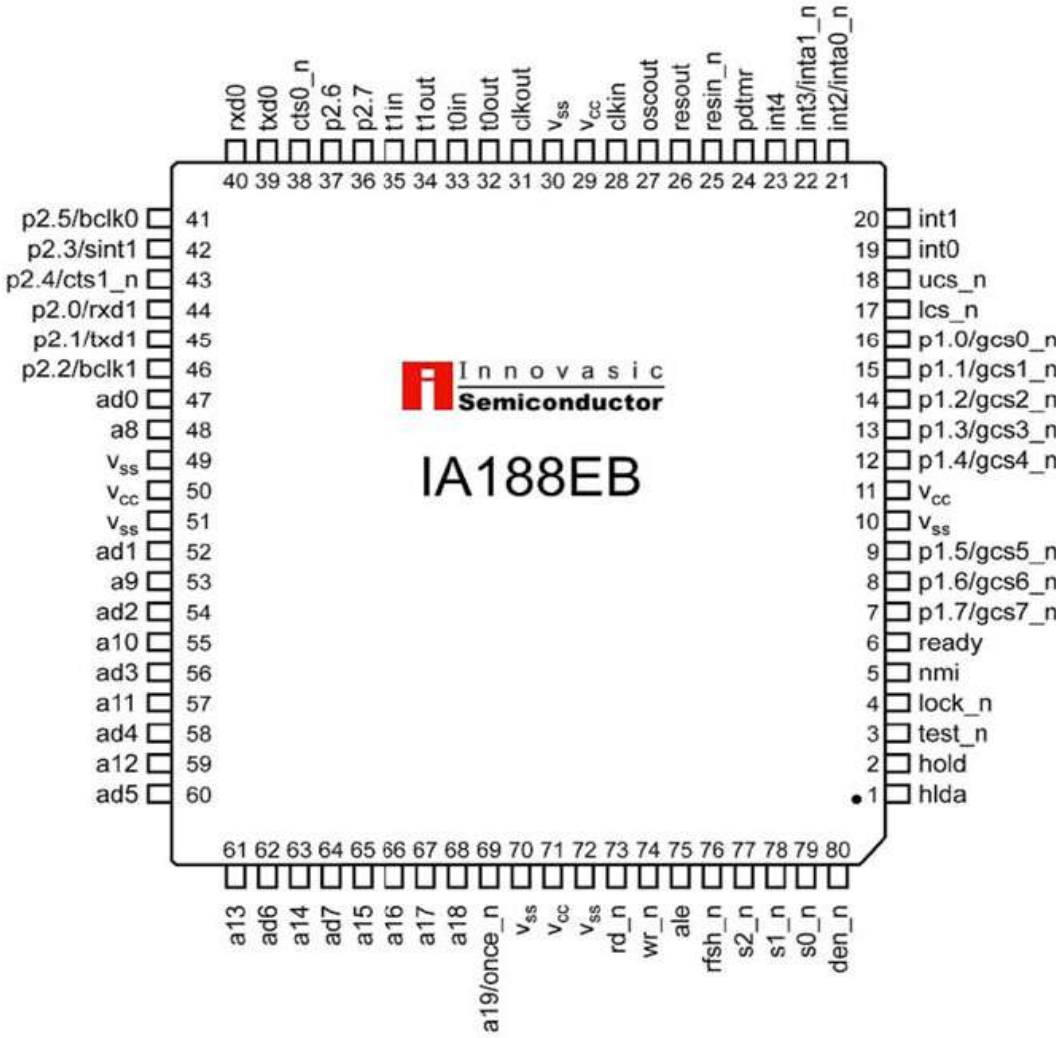

Figure 8. IA188EB 80-Pin LQFP Package Diagram

Table 6. IA188EB 80-Pin LQFP Pin Listing

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	hlda	21	int2/inta0_n	41	p2.5/bclk0	61	a13
2	hold	22	int3/inta1_n	42	p2.3/sint1	62	ad6
3	test_n	23	int4	43	p2.4/cts1_n	63	a14
4	lock_n	24	pdtmr	44	p2.0/rxd1	64	ad7
5	nmi	25	resin_n	45	p2.1/txd1	65	a15
6	ready	26	resout	46	p2.2/bclk1	66	a16
7	p1.7/gcs7_n	27	oscout	47	ad0	67	a17
8	p1.6/gcs6_n	28	clkin	48	a8	68	a18
9	p1.5/gcs5_n	29	V_{cc}	49	V_{ss}	69	a19/once_n
10	V_{ss}	30	V_{ss}	50	V_{cc}	70	V_{ss}
11	V_{cc}	31	clkout	51	V_{ss}	71	V_{cc}
12	p1.4/gcs4_n	32	t0out	52	ad1	72	V_{ss}
13	p1.3/gcs3_n	33	t0in	53	a9	73	rd_n
14	p1.2/gcs2_n	34	t1out	54	ad2	74	wr_n
15	p1.1/gcs1_n	35	t1in	55	a10	75	ale
16	p1.0/gcs0_n	36	p2.7	56	ad3	76	rfsh_n
17	lcs_n	37	p2.6	57	a11	77	s2_n
18	ucs_n	38	cts0_n	58	ad4	78	s1_n
19	int0	39	txd0	59	a12	79	s0_n
20	int1	40	rxd0	60	ad5	80	den_n

Table 7. IA186EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	LQFP	PQFP	
ale	ale	6	75	38	**a**ddress **l**atch **e**nable. Output. Active High. This signal is used to latch the address information during the address portion of a bus cycle.
bclk0	p2.5/**bclk0**	54	41	4	**b**aud **cl**oc**k**, Serial Port **0**. Input. The **bclk0** pin can be used to provide an alternate clock source for Serial Port 0. The input clock rate cannot be greater than one-half the operating frequency of the IA186EB.
bclk1	p2.2/**bclk1**	59	46	9	**b**aud **cl**oc**k**, Serial Port **1**. Input. The **bclk1** pin can be used to provide an alternate clock source for Serial Port 1. The input clock rate cannot be greater than one-half the operating frequency of the IA186EB.
bhe_n bhe_n is multi-plexed with refresh_n	bhe_n bhe_n is multi-plexed with refresh_n	7	76	39	**b**yte **h**igh **e**nable. Output. Active Low. When **bhe_n** is asserted (low), it indicates that the bus cycle in progress is transferring data over the upper half of the data bus. Additionally, **bhe_n** and **ad0** encode the following bus information: ad0 bhe_n Bus Status 0 0 Word Transfer 0 1 Even Byte Transfer 1 0 Odd Byte Transfer 1 1 Refresh Operation Note: bhe_n is multiplexed with refresh_n.
busy	test_n/**busy**	14	NA	NA	**busy**. Input. Active High. When the **busy** input is asserted, it causes the IA186EB to suspend operation during the execution of the Intel 80C187 Numerics Coprocessor instructions. Operation resumes when the pin is sampled low. *This applies to the PLCC package only.*

Table 8. IA188EB Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	LQFP	PQFP	
p1.0	**p1.0**/gcs0_n	28	16	59	**p**ort **1**, Bit [N] (N = **0**–**7**). Output. Each pin of Port 1, **p1.0**–**p1.7**, can function individually as a general-purpose output line.
p1.1	**p1.1**/gcs1_n	27	15	58	
p1.2	**p1.2**/gcs2_n	26	14	57	
p1.3	**p1.3**/gcs3_n	25	13	56	
p1.4	**p1.4**/gcs4_n	24	12	55	
p1.5	**p1.5**/gcs5_n	21	9	52	
p1.6	**p1.6**/gcs6_n	20	8	51	
p1.7	**p1.7**/gcs7_n	19	7	50	
p2.0	**p2.0**/rxd1	57	44	7	**p**ort **2**, Bit [**0**]. Input/Output. This pin functions as a general-purpose I/O line.
p2.1	**p2.1**/txd1	58	45	8	**p**ort **2**, Bit [**1**]. Output. This pin functions as a general-purpose output line.
p2.2	**p2.2**/bclk1	59	46	9	**p**ort **2**, Bit [**2**]. Input. This pin functions as a general-purpose input line.
p2.3	**p2.3**/sint1	55	42	5	**p**ort **2**, Bit [**3**]. Output. This pin functions as a general-purpose output line.
p2.4	**p2.4**/cts1_n	56	43	6	**p**ort **2**, Bit [**4**]. Input. This pin functions as a general-purpose input line.
p2.5	**p2.5**/bclk0	54	41	4	**p**ort **2**, Bit [**5**]. Input. This pin functions as a general-purpose input line.
p2.6	p2.6	50	37	80	**p**ort **2**, Bit [**6**]. Input/Output (open drain). This pin functions as a general-purpose bidirectional input/output line.
p2.7	p2.7	49	36	79	**p**ort **2**, Bit [**7**]. Input/Output (open drain). This pin functions as a general-purpose bidirectional input/output line.

- Power Management Unit

The registers associated with each integrated peripheral are contained within a 128 × 16 register file called the Peripheral Control Block (PCB). The PCB can be located in either memory or I/O space on any 256-byte address boundary.

Table 12 provides a list of the registers associated with the PCB.

Table 12. Peripheral Control Block Registers

PCB Offset	Function	PCB Offset	Function	PCB Offset	Function	PCB Offset	Function
00H	Reserved	40H	Timer2 Count	80H	GCS0 Start	C0H	Reserved
02H	End Of Interrupt	42H	Timer2 Compare	82H	GCS0 Stop	C2H	Reserved
04H	Poll	44H	Reserved	84H	GCS1 Start	C4H	Reserved
06H	Poll Status	46H	Timer2 Control	86H	GCS1 Stop	C6H	Reserved
08H	Interrupt Mask	48H	Reserved	88H	GCS2 Start	C8H	Reserved
0AH	Priority Mask	4AH	Reserved	8AH	GCS2 Stop	CAH	Reserved
0CH	In-Service	4CH	Reserved	8CH	GCS3 Start	CCH	Reserved
0EH	Interrupt Request	4EH	Reserved	8EH	GCS3 Stop	CEH	Reserved
10H	Interrupt Status	50H	Port 1 Direction	90H	GCS4 Start	D0H	Reserved
12H	Timer Control	52H	Port 1 Pin	92H	GCS4 Stop	D2H	Reserved
14H	Serial Control	54H	Port 1 Control	94H	GCS5 Start	D4H	Reserved
16H	INT4 Control	56H	Port 1 Latch	96H	GCS5 Stop	D6H	Reserved
18H	INT0 Control	58H	Port 2 Direction	98H	GCS6 Start	D8H	Reserved
1AH	INT1 Control	5AH	Port 2 Pin	9AH	GCS6 Stop	DAH	Reserved
1CH	INT2 Control	5CH	Port 2 Control	9CH	GCS7 Start	DCH	Reserved
1EH	INT3 Control	5EH	Port 2 Latch	9EH	GCS7 Stop	DEH	Reserved

4.3 Reference Documents

Additional information on the operation and programming of the 80C186EB/80C188EB can be found in the following Intel publications:

- 80C186EB/80C188EB and 80L186EB/80L188EB 16-Bit High-Integration Embedded Processors (272433-006)
- 80C186EB/80C188EB Microprocessor User's Manual (270830-00n)

5. AC Specifications

This chapter defines the AC specifications of the IA186EB/IA188EB. Input characteristics are provided in Figure 12 and Tables 13 and 14. Output characteristics are provided in Figure 13 and Tables 15 and 16. Relative timing characteristics are provided in Figure 14 and Table 17. Clock input and clock output timing characteristics are provided in Figure 18 and Tables 18 and 19. Additional timing information is provided in Chapter 7, Bus Timing, and Chapter 8, Instruction Execution Times.

The following test conditions were used to derive the values in Tables 13 – 16: Rev. 0 was tested at 100C and 4.75V; Rev. 2 was tested at 100C and 4.5V.

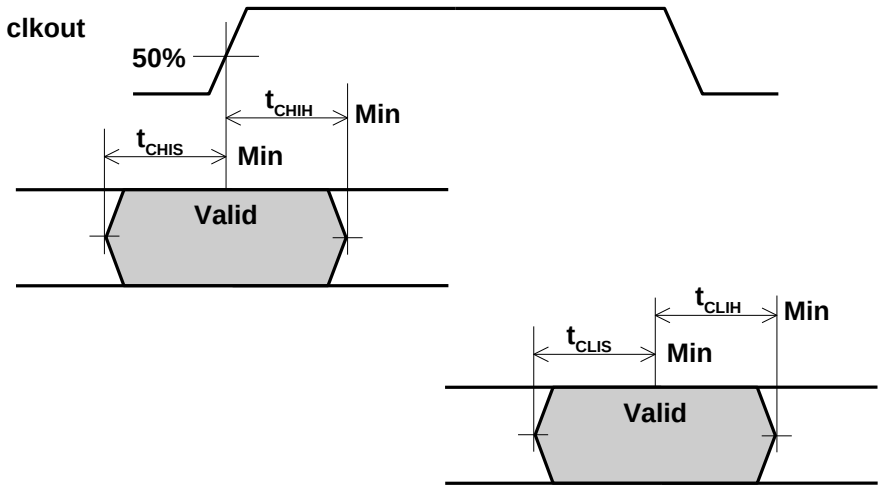

Figure 12. AC Input Characteristics

Table 17. Relative Timing Characteristics

Symbol	Parameter	Min	Max	Units
t_{LHLL}	ale Rising to ale Falling	t – 15	–	ns
t_{AVLL}	Address Valid to ale Falling	½t –10	–	ns
t_{PLLL}	Chip Selects Valid to ale Falling	½t –10	–	ns
t_{LLAX}	Address Hold from ale Falling	½t –10	–	ns
t_{LLWL}	ale Falling to wr_n Falling	½t –15	–	ns
t_{LLRL}	ale Falling to rd_n Falling	½t –15	–	ns
t_{WHLH}	wr_n Rising to ale Rising	½t –10	–	ns
t_{AFRL}	Address Float to rd_n Falling	0	–	ns
t_{RLRH}	rd_n Falling to rd_n Rising	(2t) – 5	–	ns
t_{WLWH}	wr_n Falling to wr_n Rising	(2t) – 5	–	ns
t_{RHAV}	rd_n Rising to Address Active	t – 15	–	ns
t_{WHDX}	Output Data Hold after wr_n Rising	t – 15	–	ns
t_{WHPH}	wr_n Rising to Chip Select Rising	½t –10	–	ns
t_{RHPH}	rd_n Rising to Chip Select Rising	½t –10	–	ns
t_{PHPL}	cs_n inactive to cs_n active	½t –10	–	ns
t_{OVRH}	once_n Active to resin_n Rising	t	–	ns
t_{RHOX}	once_n Hold to resin_n Rising	t	–	Ns

5.1 AC Test Conditions

The AC specifications are tested with the 50-pF load shown in Figure 15. Specifications are measured at the $V_{CC}/2$ crossing point unless otherwise specified.

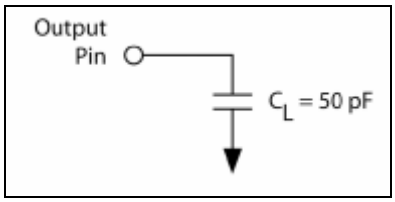

Figure 15. AC Test Load

6. Reset Operation

The IA186EB/IA188EB will perform a reset operation any time the resin_n pin is active. Figure 18 shows the reset sequence when power is applied to the IA186EB/IA188EB. An external clock connected to clkin must not exceed the V_{CC} threshold being applied to the processor. This is normally not a problem if the clock driver is supplied with the same V_{CC} that supplies the processor. When attaching a crystal to the device, resin_n must remain active until both V_{CC} and clkout are stable (the length of time is application-specific and depends on the startup characteristics of the crystal circuit). The resin_n pin is designed to operate correctly using an RC reset circuit, but the designer must ensure that the ramp time for V_{CC} is not so long that resin_n is never really sampled at a logic low level when V_{CC} reaches minimum operating conditions.

Note: Failure to assert resin_n while the device is powering up will result in unpredictable operation.

Figure 19, Warm Reset Timing, shows the timing sequence when resin_n is applied after V_{cc} is stable and the device has been operating. Any bus operation that is in progress at the time resin_n is asserted will terminate immediately.

While resin_n is active, bus signals lock_n, a19/once_n, and a18–a16 are configured as inputs and weakly held high by internal pull-up transistors. Only a19/ once_n can be overdriven to a low-to-enable ONCE Mode.

7. Bus Timing

Figures 18 through 26 on the following pages present the various bus cycles that are generated by the processor. The figures show the relationship of the various bus signals to clkout. Together with the information present in AC Characteristics, the figures allow the user to determine all the critical timing analysis needed for a given application.

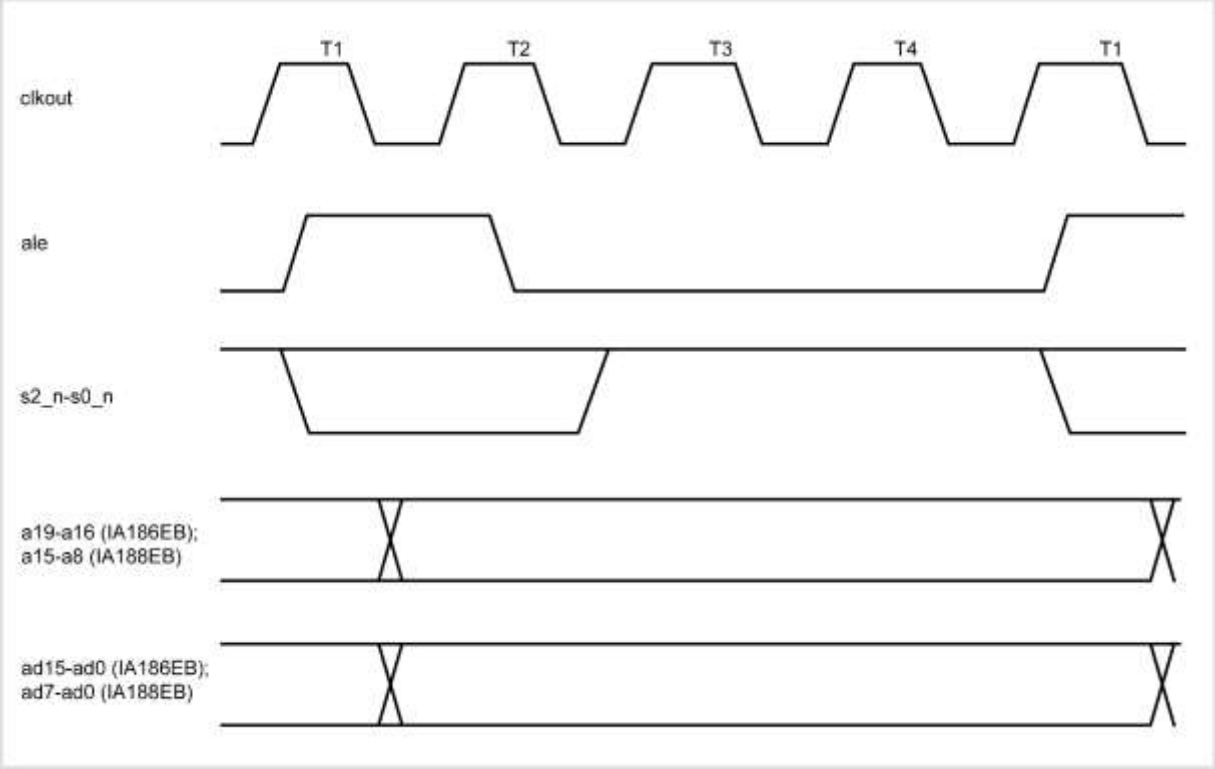

Figure 22. Halt Cycle Timing

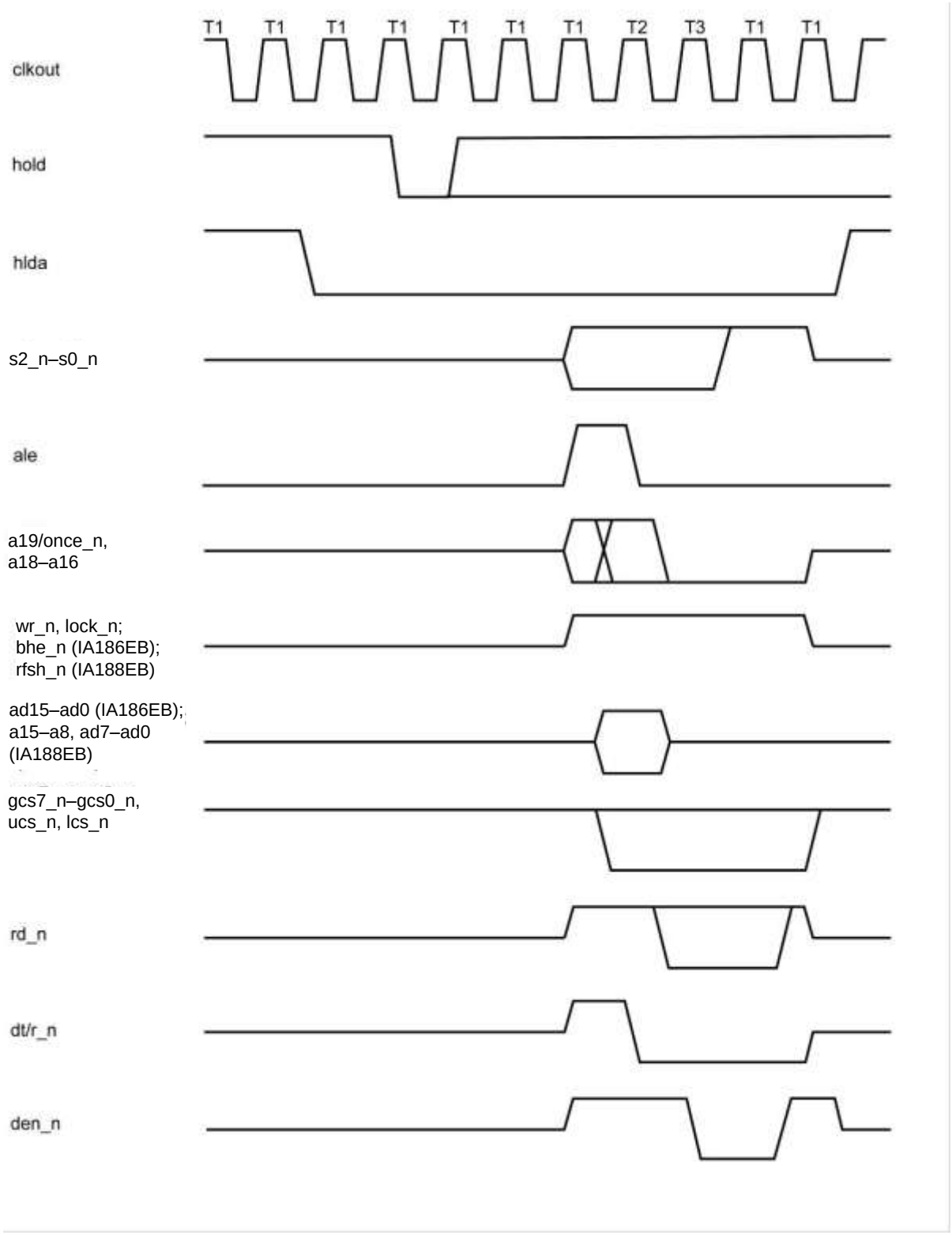

Figure 25. Refresh During Hold Acknowledge Timing

Table 21. Instruction Set Timing *(Continued)*

Instruction	Clock Cycles		Comments
	IA186EB	IA188EB	
JNS	3/5	3/5	Jump not taken/Jump taken
JNZ	3/5	3/5	
JO	3/5	3/5	
JP	3/5	3/5	
JPE	3/5	3/5	
JPO	3/5	3/5	
JS	3/5	3/5	
JZ	3/5	3/5	
LAHF	2	2	–
LDS	1/24	1/33	register/memory
LEA	3	3	–
LEAVE	12	12	–
LES	12	32	–
LOCK	1	1	–
LODS	8	12	–
LODS (repeated *n* times)	8+8*n*	12+12*n*	–
LOOP	3/4	3/4	Loop not taken/Loop taken
LOOPE	3/4	3/4	Loop not taken/Loop taken
LOOPNE	3/4	3/4	
LOOPNZ	3/4	3/4	
LOOPZ	3/4	3/4	
MOV Accumulator to memory	5	8/12	8-bit/16-bit
MOV Immediate to register	1	1	-
MOV Immediate to register/memory	1/5	1/12	register/memory
MOV Memory to accumulator	5	8/12	8-bit/16-bit
MOV Register to Register/Memory	2/5	2/20	register/memory
MOV Register/memory to register	2/5	2/20	
MOV Register/memory to segment register	2/5	2/20	
MOV Segment register to register/memory	2/5	2/20	
MOVS	24	32	–
MOVS (repeated *n* times)	24+24*n*	32+32*n*	–
MUL Memory-Byte	16	20	–
MUL Memory-Word	15	25	–
MUL Register-Byte	5	5	–
MUL Register-Word	5	5	–
NEG	1/32	1/15	register/memory
NOP	1	1	–
NOT	1/24	1/24	register/memory
OR Immediate to accumulator	1	1	–

Table 21. Instruction Set Timing *(Continued)*

Instruction	Clock Cycles		Comments
	IA186EB	IA188EB	
OR Immediate to register/memory	1/32	1/32	register/memory
OR Register/memory and register to either	1/32	1/24	
OUT Fixed port	5	8/12	8-bit/16-bit
OUT Variable port	5	12	–
OUTS	8	12/20	8-bit/16-bit
OUTS (repeated *n* times)	8+8*n*	12/20+12/20*n*	8-bit/16-bit
POP Memory	10	20	–
POP Register	10	12	–
POP Segment register	16	12	–
POPA	80	93	–
POPF	13	13	–
PUSH Immediate	8	12	–
PUSH Memory	15	28	–
PUSH Register	4	12	–
PUSH Segment register	4	12	–
PUSHA	64	72	–
PUSHF	4	16	–
RET Inter-segment	14	21	–
RET Inter-segment adding immediate to SP	25	21	–
RET Within segment	14	13	–
RET Within segment adding immediate to SP	16	13	–
ROL Register/Memory by 1	1/8	1/16	register/memory
ROL Register/Memory by CL	1/8	1/16	
ROL Register/Memory by Count	1/8	1/24	
ROR Register/Memory by 1	1/8	1/16	
ROR Register/Memory by CL	1/8	1/16	
ROR Register/Memory by Count	1/8	1/24	
SAHF	2	2	–
SBB Immediate from accumulator	1	1	–
SBB Immediate from register/memory	1/15	1/28	register/memory
SBB Register/memory and register to either	1/11	1/40	register/memory
SCAS	11	8/12	8-bit/16-bit
SCAS (repeated *n* times)	11+8*n*	8/12+8/12*n*	8-bit/16-bit
SHL Register/Memory by 1	5	1/32	register/memory

Innovasic Part Number Cross-Reference

Tables 22 through 24 cross-reference the Innovasic part number with the corresponding Intel part number.

Table 22. Innovasic Part Number Cross-Reference for the PLCC

Innovasic Part Number	Intel Part Number	Package Type	Temperature Grades
IA186EBPLC84IR2 lead free (RoHS-compliant)	EE80C186EB25 EE80C186EB20 EN80C186EB25 EN80C186EB20 EN80C186EB13 N80C186EB25 N80C186EB20 N80C186EB13 TN80C186EB25 TN80C186EB20 TN80C186EB13 N80L186EB16 N80L186EB13 TN80L186EB16 TN80L186EB13 EN80L186EB13	84-Pin PLCC	Commercial and industrial
IA188EBPLC84IR2 lead free (RoHS-compliant)	EE80C188EB25 EE80C188EB20 EE80C188EB13 EN80C188EB25 EN80C188EB20 EN80C188EB13 N80C188EB25 N80C188EB20 N80C188EB13 TN80C188EB25 TN80C188EB20 TN80C188EB13 EE80L188EB16 EN80L188EB13 N80L188EB16 N80L188EB13 TN80L188EB16 TN80L188EB13	84-Pin PLCC	Commercial and industrial

Date	Revision	Description	Page(s)
September 4, 2009	08	Added a note to Table 12 regarding the Step ID register.	50
February 25, 2011	09	Elimination of pages with SnPb lead plating options	74-76
March 23, 2011	10	Updated Instruction Set Timing Table to incorporate DIV and IDIV values.	70
June 12, 2011	11	Added Errata 11 and 12.	77, 78, 81
July 5, 2011	12	Added Errata 13.	78, 82
July 10, 2011	13	Added Errata 14.	78, 82