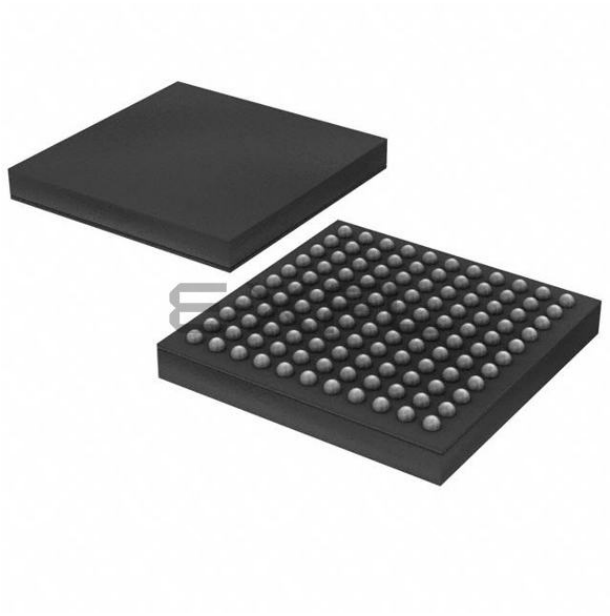

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	93
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-VFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32wg395f64-bga120

Table 2.1. Configuration Summary

Module	Configuration	Pin Connections
Cortex-M4	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
USB	Full configuration	USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID
EBI	Full configuration	EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NANDWEn, EBI_REn, EBI_VSNC, EBI_WEn
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
I2C1	Full configuration	I2C1_SDA, I2C1_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration with I2S	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
UART1	Full configuration	U1_TX, U1_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
TIMER3	Full configuration	TIM3_CC[2:0]
RTC	Full configuration	NA
BURTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O

Module	Configuration	Pin Connections
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	93 pins	Available pins are shown in Table 4.3 (p. 68)

2.3 Memory Map

The *EFM32WG395* memory map is shown in Figure 2.2 (p. 9), with RAM and Flash sizes for the largest memory configuration.

Figure 2.2. EFM32WG395 Memory Map with largest RAM and Flash sizes

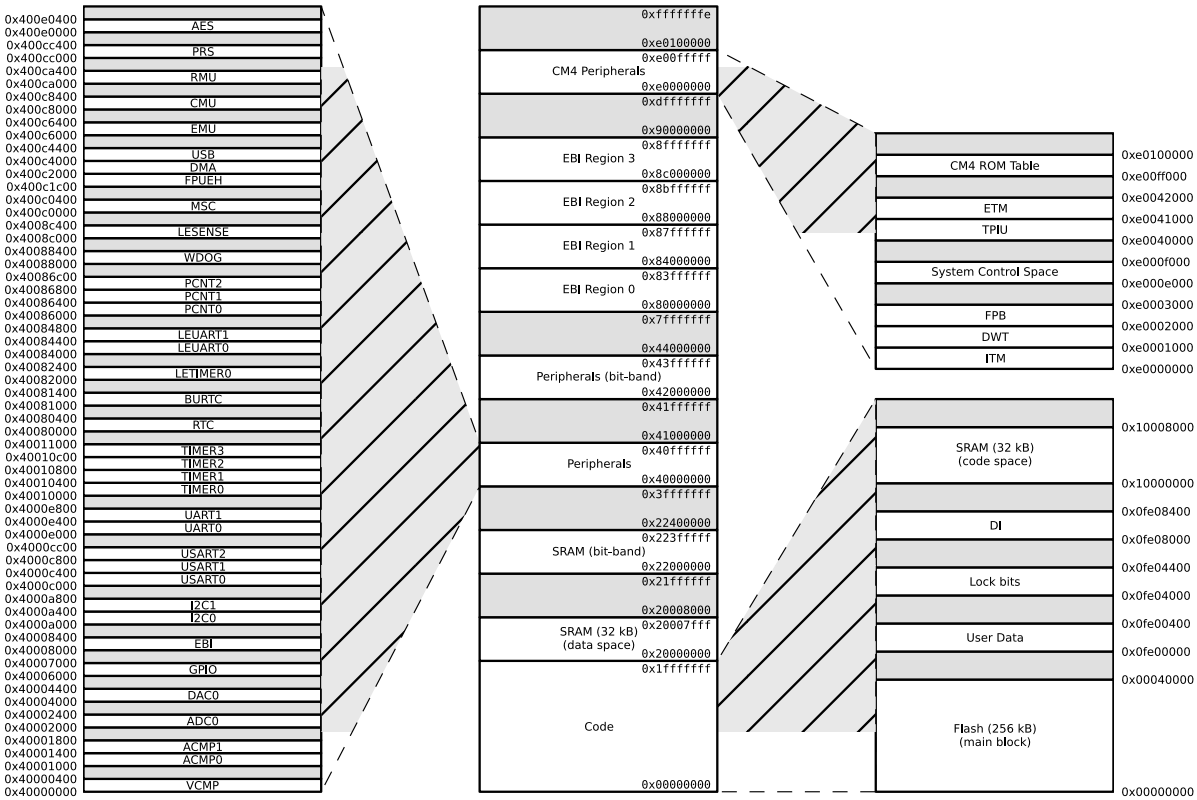


Figure 3.5. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11MHz

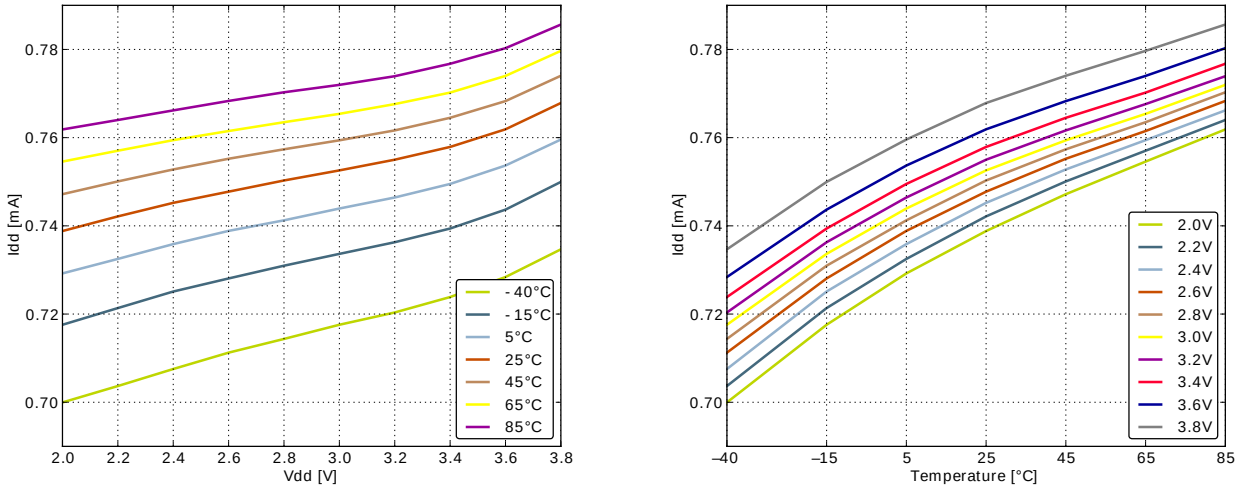


Figure 3.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 6.6MHz

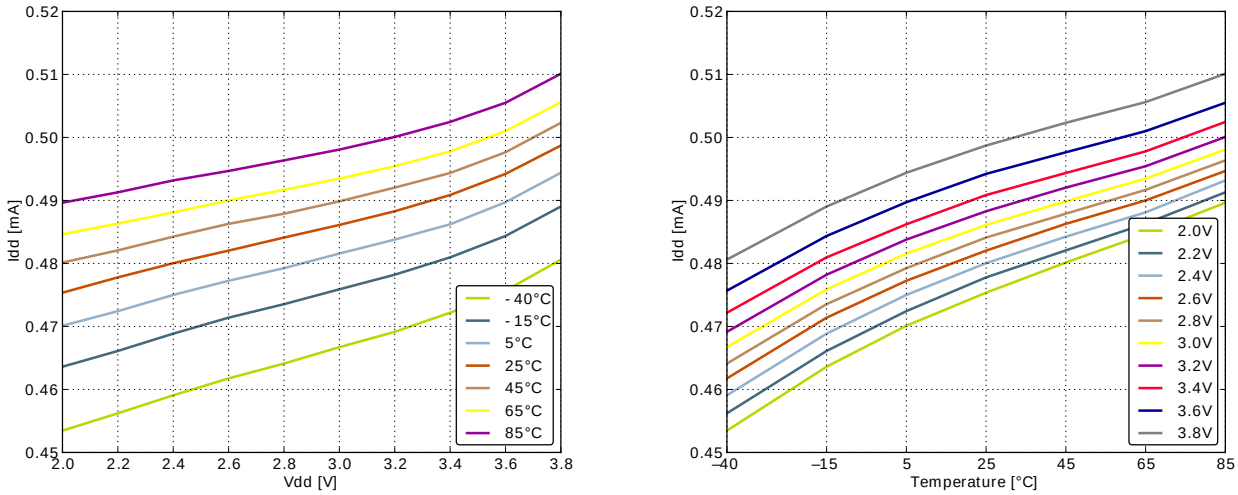
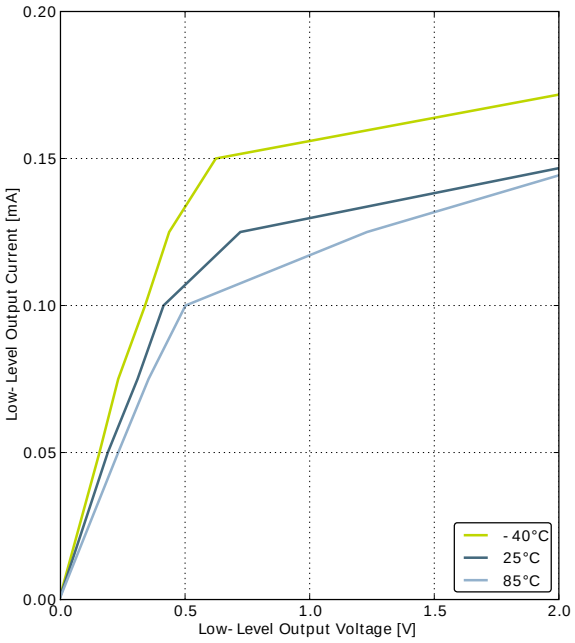
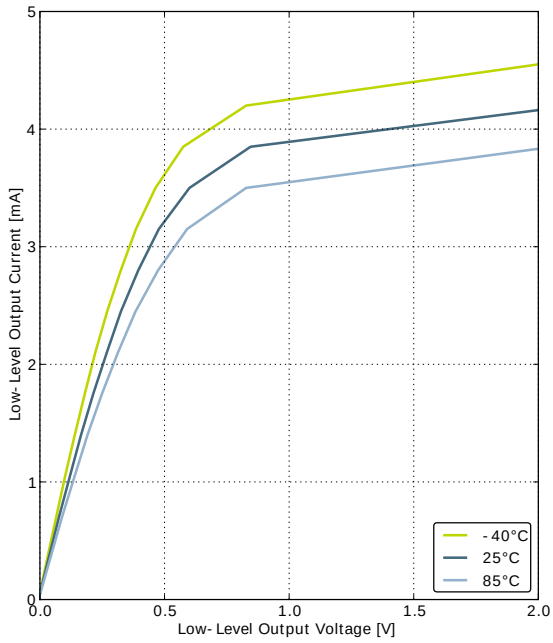


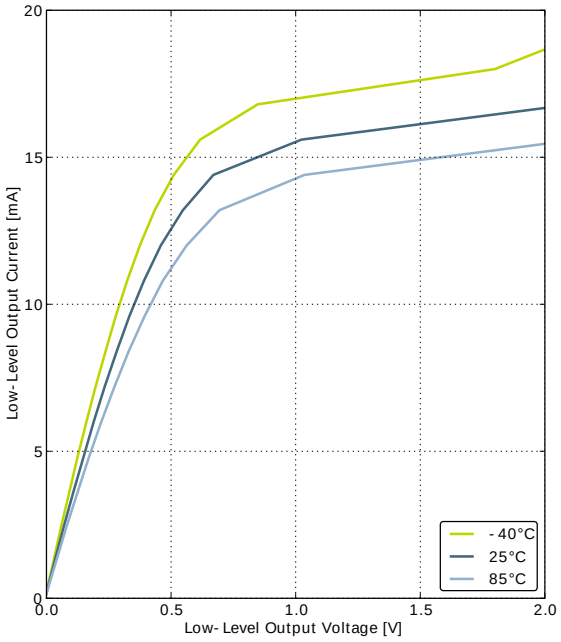
Figure 3.11. Typical Low-Level Output Current, 2V Supply Voltage



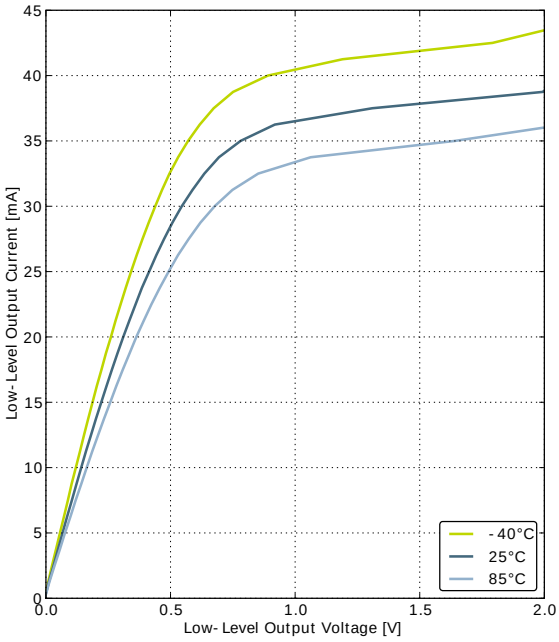
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

3.9 Oscillators

3.9.1 LFXO

Table 3.9. LFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFXO}	Supported nominal crystal frequency			32.768		kHz
ESR_{LFXO}	Supported crystal equivalent series resistance (ESR)			30	120	kOhm
C_{LFXOL}	Supported crystal external load range		X[1]		25	pF
I_{LFXO}	Current consumption for core and buffer after startup.	ESR=30 kOhm, C_L=10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t_{LFXO}	Start- up time.	ESR=30 kOhm, C_L=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		400		ms

[1]See Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup in energyAware Designer in Simplicity Studio

For safe startup of a given crystal, the energyAware Designer in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

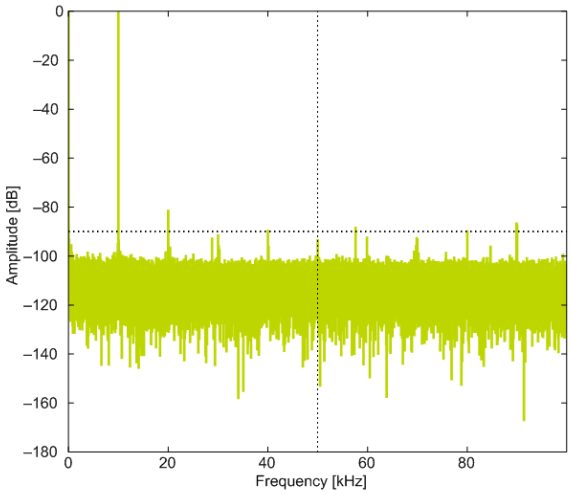
3.9.2 HFXO

Table 3.10. HFXO

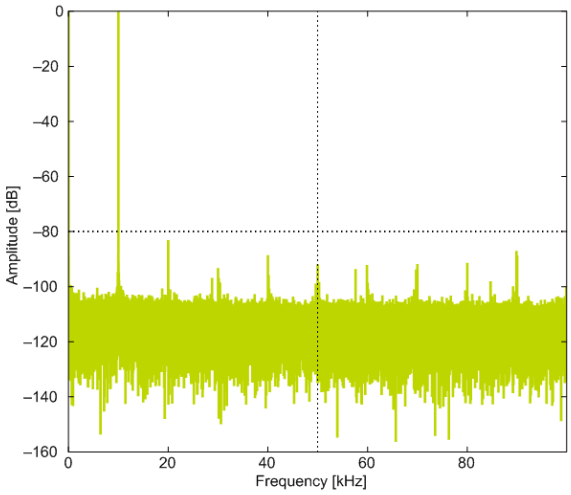
Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFXO}	Supported nominal crystal Frequency		4		48	MHz
ESR_{HFXO}	Supported crystal equivalent series resistance (ESR)	Crystal frequency 48 MHz			50	Ohm
		Crystal frequency 32 MHz		30	60	Ohm
		Crystal frequency 4 MHz		400	1500	Ohm
g_{mHFXO}	The transconductance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C_{HFXOL}	Supported crystal external load range		5		25	pF
I_{HFXO}	Current consumption for HFXO after startup	4 MHz: ESR=400 Ohm, C_L=20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		µA
		32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		µA
t_{HFXO}	Startup time	32 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11		400		µs

3.10.1 Typical performance

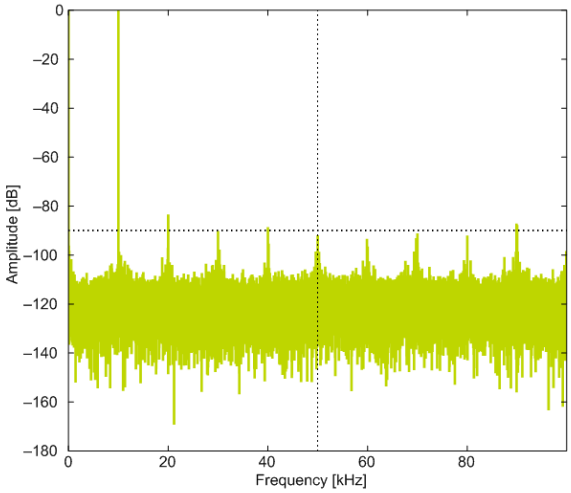
Figure 3.26. ADC Frequency Spectrum, Vdd = 3V, Temp = 25°C



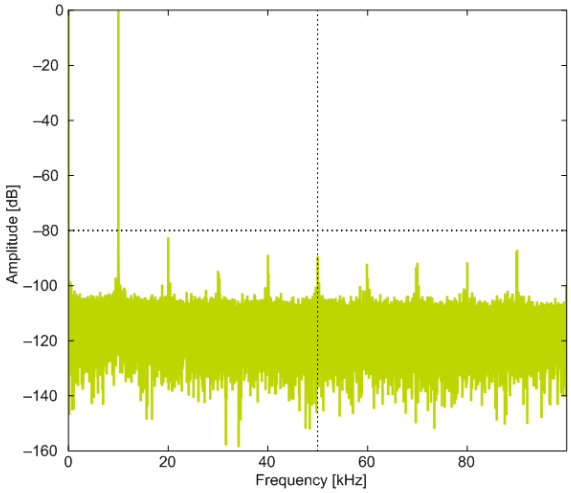
1.25V Reference



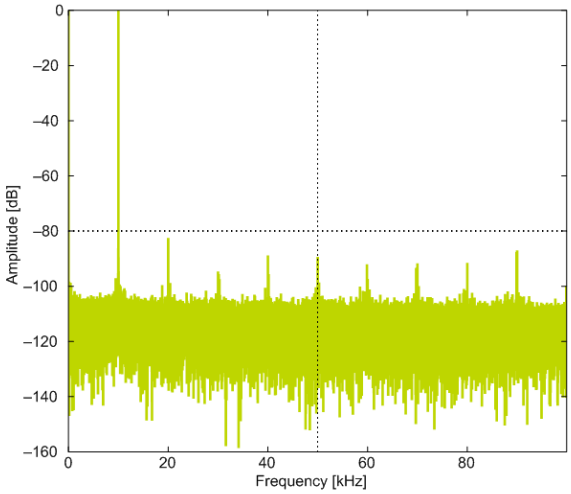
2.5V Reference



2XVDDVSS Reference

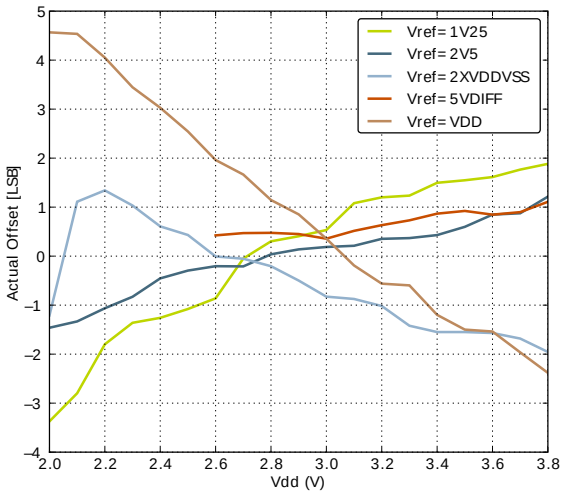


5VDIFF Reference

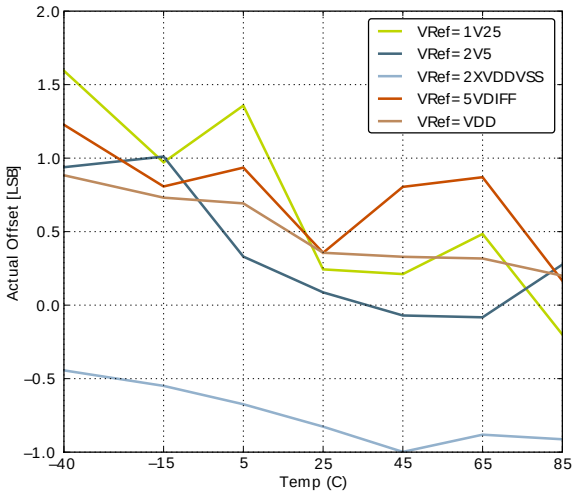


VDD Reference

Figure 3.29. ADC Absolute Offset, Common Mode = Vdd /2

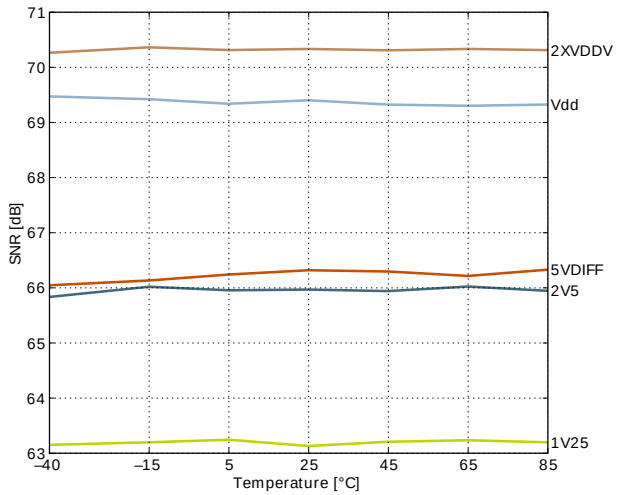


Offset vs Supply Voltage, Temp = 25°C

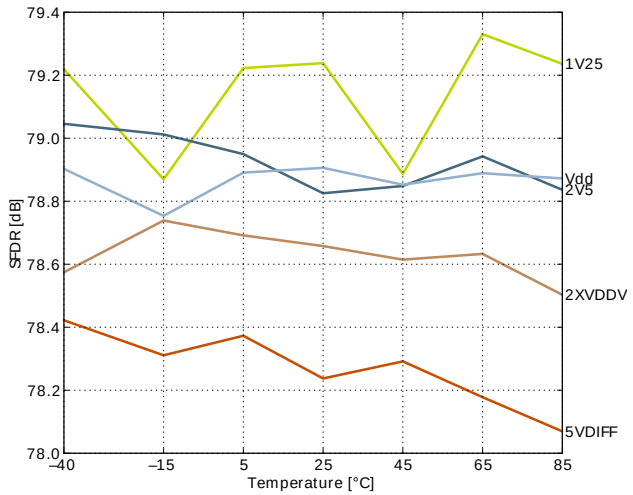


Offset vs Temperature, Vdd = 3V

Figure 3.30. ADC Dynamic Performance vs Temperature for all ADC References, Vdd = 3V



Signal to Noise Ratio (SNR)



Spurious-Free Dynamic Range (SFDR)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		58		dB
		500 kSamples/s, 12 bit, differential, V_{DD} reference		59		dB
$SNDR_{DAC}$	Signal to Noise-pulse Distortion Ratio (SNDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		57		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		54		dB
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		56		dB
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		53		dB
		500 kSamples/s, 12 bit, differential, V_{DD} reference		55		dB
$SFDR_{DAC}$	Spurious-Free Dynamic Range(SFDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		62		dBc
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		56		dBc
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		61		dBc
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		55		dBc
		500 kSamples/s, 12 bit, differential, V_{DD} reference		60		dBc
$V_{DACOFFSET}$	Offset voltage	After calibration, single ended		2	9	mV
		After calibration, differential		2		mV
DNL_{DAC}	Differential non-linearity			±1		LSB
INL_{DAC}	Integral non-linearity			±5		LSB
MC_{DAC}	No missing codes			12		bits

[1]Measured with a static input code and no loading on the output.

3.12 Operational Amplifier (OPAMP)

The electrical characteristics for the Operational Amplifiers are based on simulations.

Table 3.17. OPAMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{OPAMP}	Active Current	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, Unity Gain		370	460	µA
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, Unity Gain		95	135	µA

Table 3.27. I2C Fast-mode Plus (Fm+)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		1000[1]	kHz
t_{LOW}	SCL clock low time	0.5			µs
t_{HIGH}	SCL clock high time	0.26			µs
$t_{SU,DAT}$	SDA set-up time	50			ns
$t_{HD,DAT}$	SDA hold time	8			ns
$t_{SU,STA}$	Repeated START condition set-up time	0.26			µs
$t_{HD,STA}$	(Repeated) START condition hold time	0.26			µs
$t_{SU,STO}$	STOP condition set-up time	0.26			µs
t_{BUF}	Bus free time between a STOP and a START condition	0.5			µs

[1]For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32WG Reference Manual.

3.17 USART SPI

Figure 3.43. SPI Master Timing

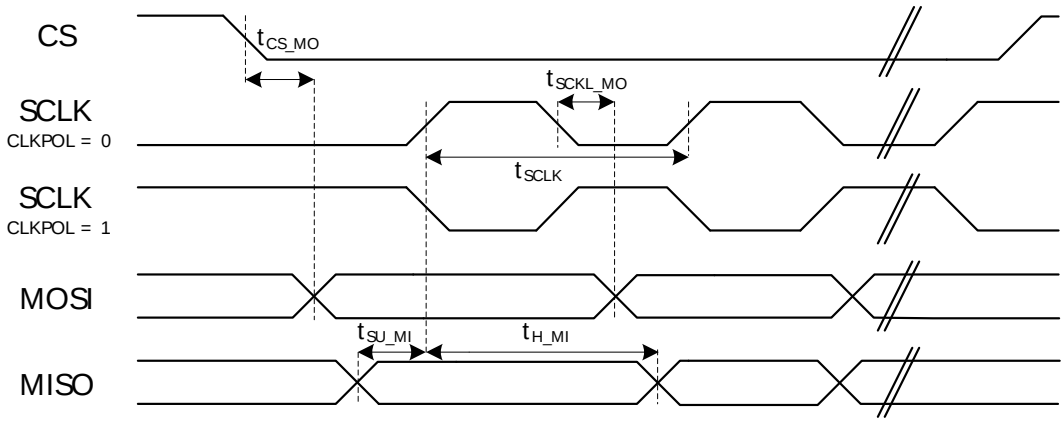


Table 3.28. SPI Master Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{SCLK} [1] [2]	SCLK period		2 * $t_{HFPERCLK}$			ns
t_{CS_MO} [1] [2]	CS to MOSI		-2.00		2.00	ns
t_{SCLK_MO} [1] [2]	SCLK to MOSI		-1.00		3.00	ns
t_{SU_MI} [1] [2]	MISO setup time	IOVDD = 3.0 V	36.00			ns
t_{H_MI} [1] [2]	MISO hold time		-6.00			ns

[1]Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
[2]Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

Table 3.29. SPI Master Timing with SSSEARLY and SMSDELAY

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{SCLK} [1] [2]	SCLK period		2 * $t_{HFPER-CLK}$			ns
t_{CS_MO} [1] [2]	CS to MOSI		-2.00		2.00	ns
t_{SCLK_MO} [1] [2]	SCLK to MOSI		-1.00		3.00	ns
t_{SU_MI} [1] [2]	MISO setup time	IOVDD = 3.0 V	-32.00			ns
t_{H_MI} [1] [2]	MISO hold time		63.00			ns

[1]Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
[2]Measurement done at 10% and 90% of V_{DD} (figure shows 50% of $_{VDD}$)

Figure 3.44. SPI Slave Timing

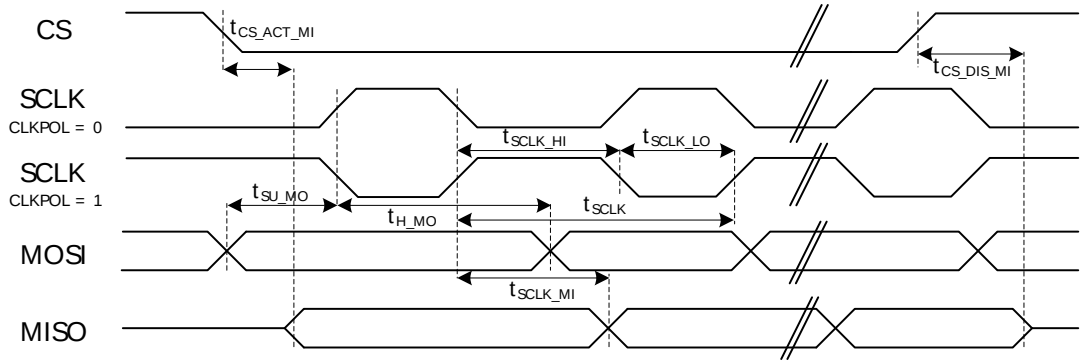


Table 3.30. SPI Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{SCLK_sl} [1] [2]	SCKL period	6 * $t_{HFPER-CLK}$			ns
t_{SCLK_hi} [1] [2]	SCLK high period	3 * $t_{HFPER-CLK}$			ns
t_{SCLK_lo} [1] [2]	SCLK low period	3 * $t_{HFPER-CLK}$			ns
$t_{CS\_ACT\_MI}$ [1] [2]	CS active to MISO	5.00		35.00	ns
$t_{CS\_DIS\_MI}$ [1] [2]	CS disable to MISO	5.00		35.00	ns
t_{SU_MO} [1] [2]	MOSI setup time	5.00			ns
t_{H_MO} [1] [2]	MOSI hold time	2 + 2 * $t_{HF-PERCLK}$			ns
t_{SCLK_MI} [1] [2]	SCLK to MISO	7 + $t_{HFPER-CLK}$		42 + 2 * $t_{HFPERCLK}$	ns

[1]Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
[2]Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

Table 3.31. SPI Slave Timing with SSSEARLY and SMSDELAY

Symbol	Parameter	Min	Typ	Max	Unit
t_{SCLK_sl} [1] [2]	SCKL period	6 * $t_{HFPER-CLK}$			ns

BGA120 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
M2	PC4	ACMP0_CH4 DAC0_P0 / OPAMP_P0	EBI_A26 #0/1/2	TIM0_CDTI2 #4 LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0 I2C1_SDA #0	LES_CH4 #0
M3	PA8		EBI_DCLK #0/1/2	TIM2_CC0 #0		
M4	PA10		EBI_VSNC #0/1/2	TIM2_CC2 #0		
M5	PA13		EBI_A01 #0/1/2	TIM2_CC1 #1		
M6	PA14		EBI_A02 #0/1/2	TIM2_CC2 #1		
M7	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
M8	AVSS_1	Analog ground 1.				
M9	AVDD_2	Analog power supply 2.				
M10	AVDD_1	Analog power supply 1.				
M11	AVSS_0	Analog ground 0.				
M12	PD3	ADC0_CH3 OPAMP_N2		TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2
M13	PD6	ADC0_CH6 DAC0_P1 / OPAMP_P1		TIM1_CC0 #4 LETIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
N1	PB8	LFXTAL_N		TIM1_CC1 #3	US0_RX #4 US1_CS #0	
N2	PC5	ACMP0_CH5 DAC0_N0 / OPAMP_N0	EBI_NANDWEn #0/1/2	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
N3	PA9		EBI_DTEN #0/1/2	TIM2_CC1 #0		
N4	PA11		EBI_HSNC #0/1/2			
N5	PA12		EBI_A00 #0/1/2	TIM2_CC0 #1		
N6	PB11	DAC0_OUT0 / OPAMP_OUT0		TIM1_CC2 #3 LETIM0_OUT0 #1	I2C1_SDA #1	
N7	PB12	DAC0_OUT1 / OPAMP_OUT1		LETIM0_OUT1 #1	I2C1_SCL #1	
N8	AVSS_2	Analog ground 2.				
N9	PB13	HFXTAL_P			US0_CLK #4/5 LEU0_TX #1	
N10	PB14	HFXTAL_N			US0_CS #4/5 LEU0_RX #1	
N11	AVDD_0	Analog power supply 0.				
N12	PD2	ADC0_CH2	EBI_A27 #0/1/2	TIM0_CC1 #3	USB_DMPU #0 US1_CLK #1	DBG_SWO #3
N13	PD5	ADC0_CH5 OPAMP_OUT2 #0			LEU0_RX #0	ETM_TD3 #0/2

4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 62). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 4.2. Alternate functionality overview

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2							Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3							Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4							Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5							Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6							Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7							Analog comparator ACMP0, channel 7.
ACMP0_O	PE13	PE2	PD6					Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8							Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9							Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10							Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11							Analog comparator ACMP1, channel 3.
ACMP1_CH4	PC12							Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13							Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14							Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15							Analog comparator ACMP1, channel 7.
ACMP1_O	PF2	PE3	PD7					Analog comparator ACMP1, digital output.
ADC0_CH0	PD0							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1							Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2							Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3							Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11							Bootloader RX
BOOT_TX	PE10							Bootloader TX
BU_STAT	PE3							Backup Power Domain status, whether or not the system is in backup mode
BU_VIN	PD8							Battery input for Backup Power Domain
BU_VOUT	PE2							Power output for Backup Power Domain
CMU_CLK0	PA2	PC12	PD7					Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8	PE12					Clock Management Unit, clock output number 1.
DAC0_N0 / OPAMP_N0	PC5							Operational Amplifier 0 external negative input.
DAC0_N1 / OPAMP_N1	PD7							Operational Amplifier 1 external negative input.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
OPAMP_N2	PD3							Operational Amplifier 2 external negative input.
DAC0_OUT0 / OPAMP_OUT0	PB11							Digital to Analog Converter DAC0_OUT0 / OPAMP output channel number 0.
DAC0_OUT0ALT / OPAMP_OUT0ALT	PC0	PC1	PC2	PC3	PD0			Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0.
DAC0_OUT1 / OPAMP_OUT1	PB12							Digital to Analog Converter DAC0_OUT1 / OPAMP output channel number 1.
DAC0_OUT1ALT / OPAMP_OUT1ALT	PC12	PC13	PC14	PC15	PD1			Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1.
OPAMP_OUT2	PD5	PD0						Operational Amplifier 2 output.
DAC0_P0 / OPAMP_P0	PC4							Operational Amplifier 0 external positive input.
DAC0_P1 / OPAMP_P1	PD6							Operational Amplifier 1 external positive input.
OPAMP_P2	PD4							Operational Amplifier 2 external positive input.
DBG_SWCLK	PF0	PF0	PF0	PF0				Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1	PF1	PF1				Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15	PD1	PD2				Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_A00	PA12	PA12	PA12					External Bus Interface (EBI) address output pin 00.
EBI_A01	PA13	PA13	PA13					External Bus Interface (EBI) address output pin 01.
EBI_A02	PA14	PA14	PA14					External Bus Interface (EBI) address output pin 02.
EBI_A03	PB9	PB9	PB9					External Bus Interface (EBI) address output pin 03.
EBI_A04	PB10	PB10	PB10					External Bus Interface (EBI) address output pin 04.
EBI_A05	PC6	PC6	PC6					External Bus Interface (EBI) address output pin 05.
EBI_A06	PC7	PC7	PC7					External Bus Interface (EBI) address output pin 06.
EBI_A07	PE0	PE0	PE0					External Bus Interface (EBI) address output pin 07.
EBI_A08	PE1	PE1	PE1					External Bus Interface (EBI) address output pin 08.
EBI_A09	PE2	PC9	PC9					External Bus Interface (EBI) address output pin 09.
EBI_A10	PE3	PC10	PC10					External Bus Interface (EBI) address output pin 10.
EBI_A11	PE4	PE4	PE4					External Bus Interface (EBI) address output pin 11.
EBI_A12	PE5	PE5	PE5					External Bus Interface (EBI) address output pin 12.
EBI_A13	PE6	PE6	PE6					External Bus Interface (EBI) address output pin 13.
EBI_A14	PE7	PE7	PE7					External Bus Interface (EBI) address output pin 14.
EBI_A15	PC8	PC8	PC8					External Bus Interface (EBI) address output pin 15.
EBI_A16	PB0	PB0	PB0					External Bus Interface (EBI) address output pin 16.
EBI_A17	PB1	PB1	PB1					External Bus Interface (EBI) address output pin 17.
EBI_A18	PB2	PB2	PB2					External Bus Interface (EBI) address output pin 18.
EBI_A19	PB3	PB3	PB3					External Bus Interface (EBI) address output pin 19.
EBI_A20	PB4	PB4	PB4					External Bus Interface (EBI) address output pin 20.
EBI_A21	PB5	PB5	PB5					External Bus Interface (EBI) address output pin 21.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
EBI_A22	PB6	PB6	PB6					External Bus Interface (EBI) address output pin 22.
EBI_A23	PC0	PC0	PC0					External Bus Interface (EBI) address output pin 23.
EBI_A24	PC1	PC1	PC1					External Bus Interface (EBI) address output pin 24.
EBI_A25	PC2	PC2	PC2					External Bus Interface (EBI) address output pin 25.
EBI_A26	PC4	PC4	PC4					External Bus Interface (EBI) address output pin 26.
EBI_A27	PD2	PD2	PD2					External Bus Interface (EBI) address output pin 27.
EBI_AD00	PE8	PE8	PE8					External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9	PE9	PE9					External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10	PE10	PE10					External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11	PE11	PE11					External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12	PE12	PE12					External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13	PE13	PE13					External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14	PE14	PE14					External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	PE15	PE15	PE15					External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15	PA15	PA15					External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	PA0	PA0	PA0					External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	PA1	PA1	PA1					External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2	PA2	PA2					External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3	PA3	PA3					External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4	PA4	PA4					External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5	PA5	PA5					External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6	PA6	PA6					External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	PF3	PC11	PC11					External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	PF2	PF2	PF2					External Bus Interface (EBI) Hardware Ready Control input.
EBI_BL0	PF6	PF6	PF6					External Bus Interface (EBI) Byte Lane/Enable pin 0.
EBI_BL1	PF7	PF7	PF7					External Bus Interface (EBI) Byte Lane/Enable pin 1.
EBI_CS0	PD9	PD9	PD9					External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10	PD10	PD10					External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11	PD11	PD11					External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12	PD12	PD12					External Bus Interface (EBI) Chip Select output 3.
EBI_CSTFT	PA7	PA7	PA7					External Bus Interface (EBI) Chip Select output TFT.
EBI_DCLK	PA8	PA8	PA8					External Bus Interface (EBI) TFT Dot Clock pin.
EBI_DTEN	PA9	PA9	PA9					External Bus Interface (EBI) TFT Data Enable pin.

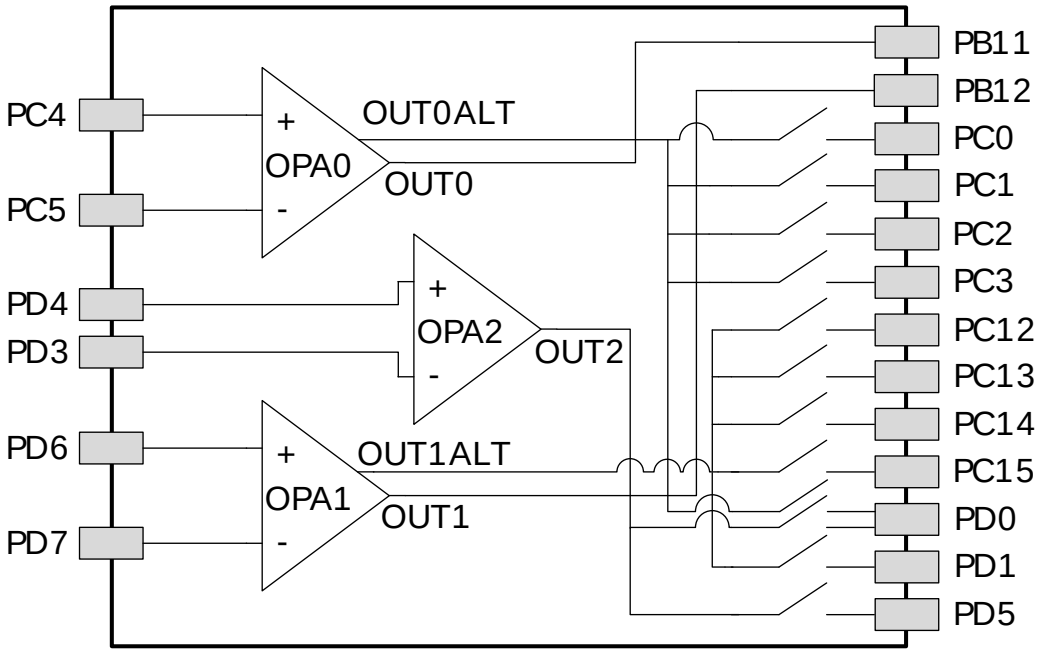
Table 4.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	-	-	-	PF12	PF11	PF10	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

4.4 Opamp Pinout Overview

The specific opamp terminals available in *EFM32WG395* is shown in Figure 4.2 (p. 68) .

Figure 4.2. Opamp Pinout



5 PCB Layout and Soldering

5.1 Recommended PCB Layout

Figure 5.1. BGA120 PCB Land Pattern

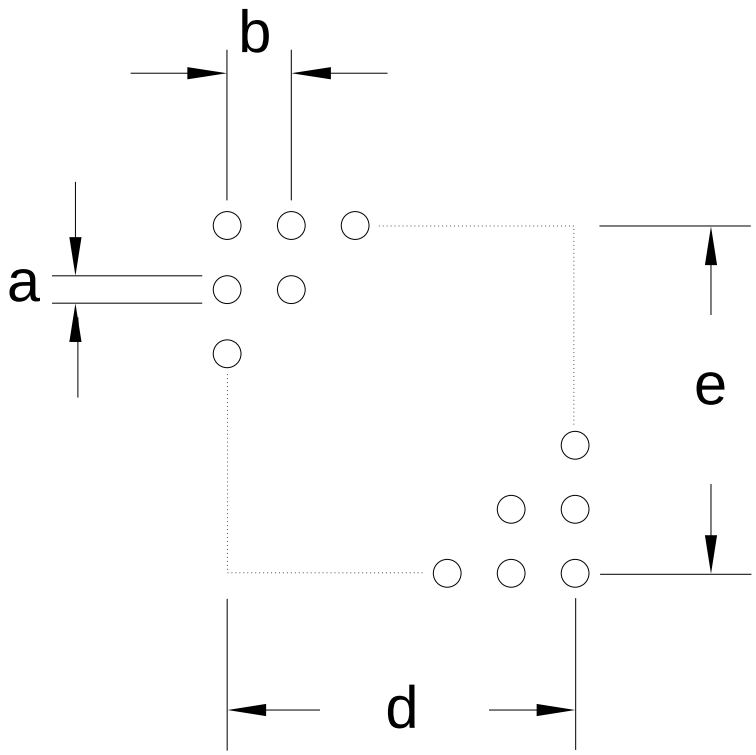


Table 5.1. BGA120 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.25
b	0.50
d	6.00
e	6.00

Figure 5.2. BGA120 PCB Solder Mask

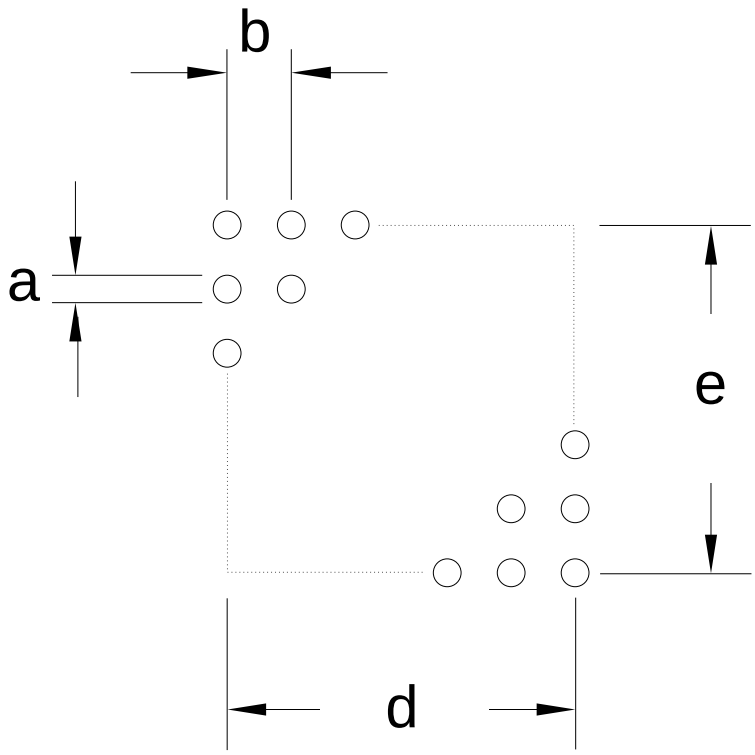


Table 5.2. BGA120 PCB Solder Mask Dimensions (Dimensions in mm)

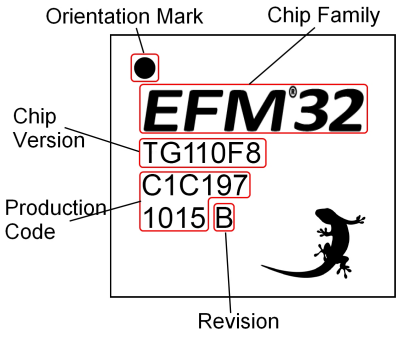
Symbol	Dim. (mm)
a	0.35
b	0.50
d	6.00
e	6.00

6 Chip Marking, Revision and Errata

6.1 Chip Marking

In the illustration below package fields and position are shown.

Figure 6.1. Example Chip Marking (top view)



6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 73) .

6.3 Errata

Please see the errata document for EFM32WG395 for description and resolution of device erratas. This document is available in Simplicity Studio and online at: http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit

Corrected the ADC resolution from 12, 10 and 6 bit to 12, 8 and 6 bit.

Updated the EM0 and EM1 current consumption numbers. Updated the the EM1 plots and removed the EM0 plots.

Updated Environmental information.

Updated trademark, disclaimer and contact information.

Other minor corrections.

7.4 Revision 1.20

June 28th, 2013

Corrected pinout top view figure.

Updated PCB Land Pattern, PCB Solder Mask and PCB Stencil Design figures.

Updated power requirements in the Power Management section.

Removed minimum load capacitance figure and table. Added reference to application note.

Other minor corrections.

7.5 Revision 1.10

May 6th, 2013

Updated current consumption table and figures in Electrical characteristics section.

Other minor corrections.

7.6 Revision 1.00

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

Corrected BGA solder balls material from Sn96.5/Ag3/Cu0.5 to SAC105.

Other minor corrections.

7.7 Revision 0.95

May 3rd, 2012

Updated EM2/EM3 current consumption at 85°C.

7.8 Revision 0.90

February 27th, 2012

Initial preliminary release.

List of Tables