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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 6x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c773-i-sp

FIGURE 1-2: PIC16C774 BLOCK DIAGRAM

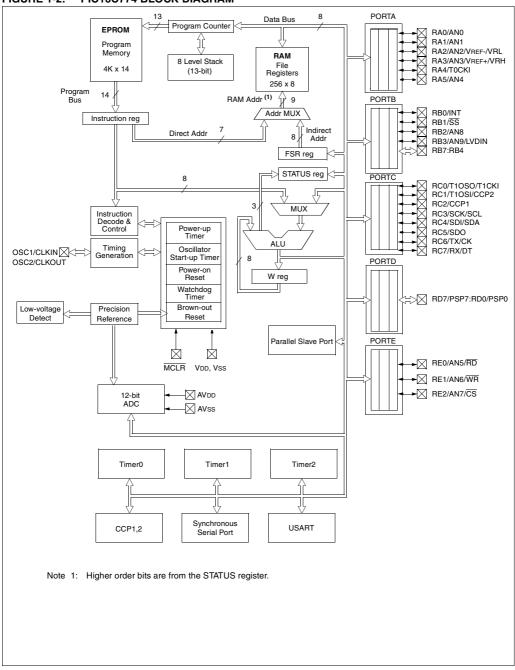


TABLE 1-1 **PIC16C773 PINOUT DESCRIPTION**

Pin Name	DIP, SSOP, SOIC Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	9	I	ST/CMOS ⁽³⁾	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	10	0	_	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR/VPP	1	I/P	ST	Master clear (reset) input or programming voltage input. This pin is an active low reset to the device.
				PORTA is a bi-directional I/O port.
RA0/AN0	2	I/O	TTL	RA0 can also be analog input0
RA1/AN1	3	I/O	TTL	RA1 can also be analog input1
RA2/AN2/VREF-/VRL	4	I/O	TTL	RA2 can also be analog input2 or negative analog reference voltage input or internal voltage reference low
RA3/AN3/VREF+/VRH	5	I/O	TTL	RA3 can also be analog input3 or positive analog reference voltage input or internal voltage reference high
RA4/T0CKI	6	I/O	ST	RA4 can also be the clock input to the Timer0 module. Output is open drain type.
				PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	21	I/O	TTL/ST ⁽¹⁾	RB0 can also be the external interrupt pin.
RB1/SS	22	I/O	TTL/ST ⁽¹⁾	RB1 can also be the SSP slave select
RB2/AN8	23	I/O	TTL	RB2 can also be analog input8
RB3/AN9/LVDIN	24	I/O	TTL	RB3 can also be analog input9 or the low voltage detect input reference
RB4	25	I/O	TTL	Interrupt on change pin.
RB5	26	I/O	TTL	Interrupt on change pin.
RB6	27	I/O	TTL/ST ⁽²⁾	Interrupt on change pin. Serial programming clock.
RB7	28	I/O	TTL/ST ⁽²⁾	Interrupt on change pin. Serial programming data.
				PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	11	I/O	ST	RC0 can also be the Timer1 oscillator output or Timer1 clock input.
RC1/T1OSI/CCP2	12	I/O	ST	RC1 can also be the Timer1 oscillator input or Capture2 input/ Compare2 output/PWM2 output.
RC2/CCP1	13	I/O	ST	RC2 can also be the Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	14	I/O	ST	RC3 can also be the synchronous serial clock input/output for both SPI and I ² C modes.
RC4/SDI/SDA	15	I/O	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I ² C mode).
RC5/SDO	16	I/O	ST	RC5 can also be the SPI Data Out (SPI mode).
RC6/TX/CK	17	I/O	ST	RC6 can also be the USART Asynchronous Transmit or Synchronous Clock.
RC7/RX/DT	18	I/O	ST	RC7 can also be the USART Asynchronous Receive or Synchronous Data.
AVss	8	Р		Ground reference for A/D converter
AVDD	7	P		Positive supply for A/D converter
Vss	19	Р	_	Ground reference for logic and I/O pins.
VDD	20	Р	_	Positive supply for logic and I/O pins.
Legend: I = input (D = output		I/O = input	/output P = power

— = Not used

TTL = TTL input

ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured for the multiplexed function.
2: This buffer is a Schmitt Trigger input when used in serial programming mode.

3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

2.2.2.5 PIR1 REGISTER

This register contains the individual flag bits for the peripheral interrupts.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

FIGURE 2-7: PIR1 REGISTER (ADDRESS 0Ch)

R/W-0 PSPIF ⁽¹⁾	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	Б	Deedeble hit		
bit7	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF bit0	W U	= Readable bit = Writable bit = Unimplemented bit, read as '0' = Value at POR reset		
bit 7:	PSPIF ⁽¹⁾ : Parallel Slave Port Read/Write Interrupt Flag bit 1 = A read or a write operation has taken place (must be cleared in software) 0 = No read or write has occurred										
bit 6:	ADIF: A/D Converter Interrupt Flag bit 1 = An A/D conversion completed (must be cleared in software) 0 = The A/D conversion is not complete										
bit 5:	1 = The L	ART Rece JSART rec JSART rec	eive buffe	r is full (cle	eared by re	ading RCF	REG)				
bit 4:	1 = The L	ART Trans JSART trai JSART trai	nsmit buff	er is empty		by writing	to TXREG)				
bit 3:	1 = The tr	ansmissio	n/reception	n is comp	pt Flag bit lete (must	be cleared	in software	e)			
bit 2:	0 = Waiting to transmit/receive CCP1IF: CCP1 Interrupt Flag bit Capture Mode 1 = A TMR1 register capture occurred (must be cleared in software) 0 = No TMR1 register capture occurred Compare Mode 1 = A TMR1 register compare match occurred (must be cleared in software) 0 = No TMR1 register compare match occurred PWM Mode										
bit 1:	Unused in this mode TMR2IF: TMR2 to PR2 Match Interrupt Flag bit 1 = TMR2 to PR2 match occurred (must be cleared in software) 0 = No TMR2 to PR2 match occurred										
bit 0:	1 = TMR1	TMR1 Over register of register o	verflowed	I (must be	bit cleared in	software)					
Note 1:	PSPIF is	reserved o	on the 28-	pin device	s, always n	naintain thi	s bit clear.				

FIGURE 3-2: BLOCK DIAGRAM OF RA1:RA0 AND RA5 PINS

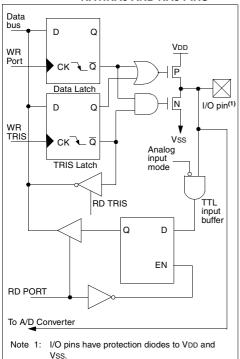


FIGURE 3-3: BLOCK DIAGRAM OF RA4/T0CKI PIN

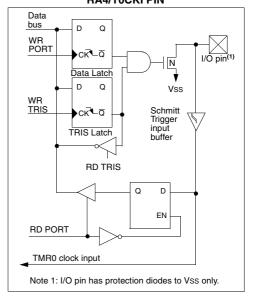


TABLE 3-1 PORTA FUNCTIONS

Name	Bit#	Buffer	Function
RA0/AN0	bit0	TTL	Input/output or analog input0
RA1/AN1	bit1	TTL	Input/output or analog input1
RA2/AN2/VREF-/VRL	bit2	TTL	Input/output or analog input2 or VREF- input or internal reference voltage low
RA3/AN3/VREF+/VRH	bit3	TTL	Input/output or analog input or VREF+ input or output of internal reference voltage high
RA4/T0CKI	bit4	ST	Input/output or external clock input for Timer0 Output is open drain type
RA5/AN4 ⁽¹⁾	bit5	TTL	Input/output or analog input

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: RA5 is reserved on the 28-pin devices, maintain this bit clear.

TABLE 3-2 SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
05h	PORTA ⁽¹⁾	_	_	RA5	RA4	RA3	RA2	RA1	RA0	0x 0000	0u 0000
85h	TRISA ⁽¹⁾	_	_	PORTA [PORTA Data Direction Register						11 1111
9Fh	ADCON1	ADFM	VCFG2	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

Note 1: PORTA<5>, TRISA<5> are reserved on the 28-pin devices, maintain these bits clear.

TABLE 3-9 PORTE FUNCTIONS

Name	Bit#	Buffer Type	Function
RE0/RD/AN5	bit0	ST/TTL ⁽¹⁾	Input/output port pin or read control input in parallel slave port mode or analog input: RD
			1 = Not a read operation 0 = Read operation. Reads PORTD register (if chip selected)
RE1/WR/AN6	bit1	ST/TTL ⁽¹⁾	Input/output port pin or write control input in parallel slave port mode or analog input: WR 1 = Not a write operation 0 = Write operation. Writes PORTD register (if chip selected)
RE2/CS/AN7	bit2	ST/TTL ⁽¹⁾	Input/output port pin or chip select control input in parallel slave port mode or analog input: CS 1 = Device is not selected 0 = Device is selected

Legend: ST = Schmitt Trigger input TTL = TTL input

Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in Parallel Slave Port Mode.

TABLE 3-10 SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
09h	PORTE	_	_	_	_	_	RE2	RE1	RE0	xxx	uuu
89h	TRISE	IBF	OBF	IBOV	PSPMODE	_	PORTE Data Direction Bits		0000 -111	0000 -111	
9Fh	ADCON1	ADFM	VCFG2	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	0000 0000	0000 0000

 $\label{eq:local_local_local_local_local_local} \textbf{Legend:} \quad \textbf{x} = \textbf{unknown}, \textbf{u} = \textbf{unchanged}, \textbf{-} = \textbf{unimplemented read as '0'}. \textbf{Shaded cells are not used by PORTE}.$

5.1.1 TIMER1 COUNTER OPERATION

In this mode, Timer1 is being incremented via an external source. Increments occur on a rising edge. After Timer1 is enabled in counter mode, the module must first have a falling edge before the counter begins to increment.

FIGURE 5-2: **TIMER1 INCREMENTING EDGE**

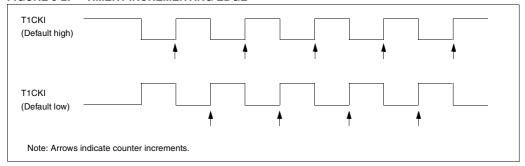
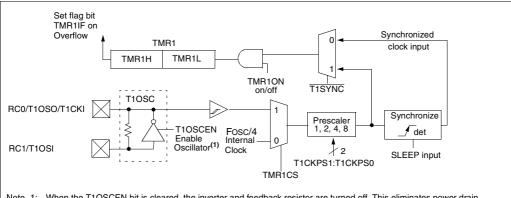


FIGURE 5-3: **TIMER1 BLOCK DIAGRAM**



Note 1: When the T1OSCEN bit is cleared, the inverter and feedback resistor are turned off. This eliminates power drain.

NOTES:

determine when the transmission/reception has completed. The SSPBUF must be read and/or written. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur. Example 8-1 shows the loading of the SSPBUF (SSPSR) for data transmission.

EXAMPLE 8-1: LOADING THE SSPBUF (SSPSR) REGISTER

		٠,	o. o,	
	BSF	STATUS,	RP0	;Specify Bank 1
LOOP	BTFSS	SSPSTAT,	BF	;Has data been
				;received
				;(transmit
				;complete)?
	GOTO	LOOP		;No
	BCF	STATUS,	RP0	;Specify Bank 0
	MOVF	SSPBUF,	W	;W reg = contents
				;of SSPBUF
	MOVWF	RXDATA		;Save in user RAM
	MOVF	TXDATA,	W	;W reg = contents
				; of TXDATA
	MOVWF	SSPBUF		;New data to xmit

The SSPSR is not directly readable or writable, and can only be accessed by addressing the SSPBUF register. Additionally, the MSSP status register (SSPSTAT) indicates the various status conditions.

8.1.2 ENABLING SPI I/O

To enable the serial port, MSSP Enable bit, SSPEN (SSPCON<5>) must be set. To reset or reconfigure SPI mode, clear bit SSPEN, re-initialize the SSPCON registers, and then set bit SSPEN. This configures the

SDI, SDO, SCK, and \overline{SS} pins as serial port pins. For the pins to behave as the serial port function, some must have their data direction bits (in the TRIS register) appropriately programmed. That is:

- · SDI is automatically controlled by the SPI module
- SDO must have TRISC<5> cleared
- SCK (Master mode) must have TRISC<3> cleared
- · SCK (Slave mode) must have TRISC<3> set
- SS must have TRISA<5> set

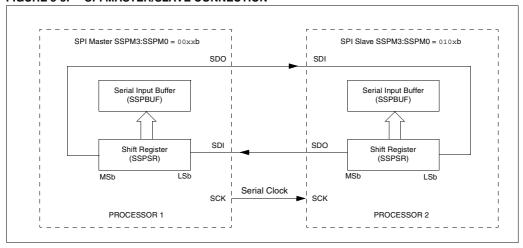
Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value.

8.1.3 TYPICAL CONNECTION

Figure 8-5 shows a typical connection between two microcontrollers. The master controller (Processor 1) initiates the data transfer by sending the SCK signal. Data is shifted out of both shift registers on their programmed clock edge, and latched on the opposite edge of the clock. Both processors should be programmed to same Clock Polarity (CKP), then both controllers would send and receive data at the same time. Whether the data is meaningful (or dummy data) depends on the application software. This leads to three scenarios for data transmission:

- Master sends data Slave sends dummy data
- · Master sends data Slave sends data
- Master sends dummy data Slave sends data

FIGURE 8-5: SPI MASTER/SLAVE CONNECTION



- The MSSP Module shifts in the ACK bit from the slave device, and writes its value into the SSPCON2 register (SSPCON2<6>).
- The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSPIF bit.
- k) The user generates a STOP condition by setting the STOP enable bit PEN in SSPCON2.
- Interrupt is generated once the STOP condition is complete.

8.2.8 BAUD RATE GENERATOR

In I²C master mode, the reload value for the BRG is located in the lower 7 bits of the SSPADD register (Figure 8-18). When the BRG is loaded with this value, the BRG counts down to 0 and stops until another reload has taken place. The BRG count is decremented twice per instruction cycle (TCY) on the Q2 and Q4 clock.

In I²C master mode, the BRG is reloaded automatically. If Clock Arbitration is taking place for instance, the BRG will be reloaded when the SCL pin is sampled high (Figure 8-19).

FIGURE 8-18: BAUD RATE GENERATOR BLOCK DIAGRAM

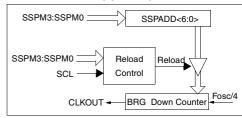
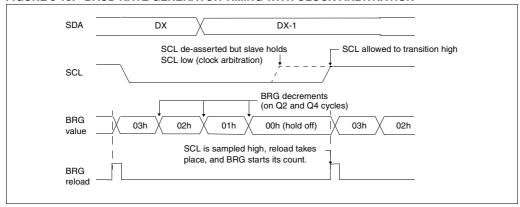
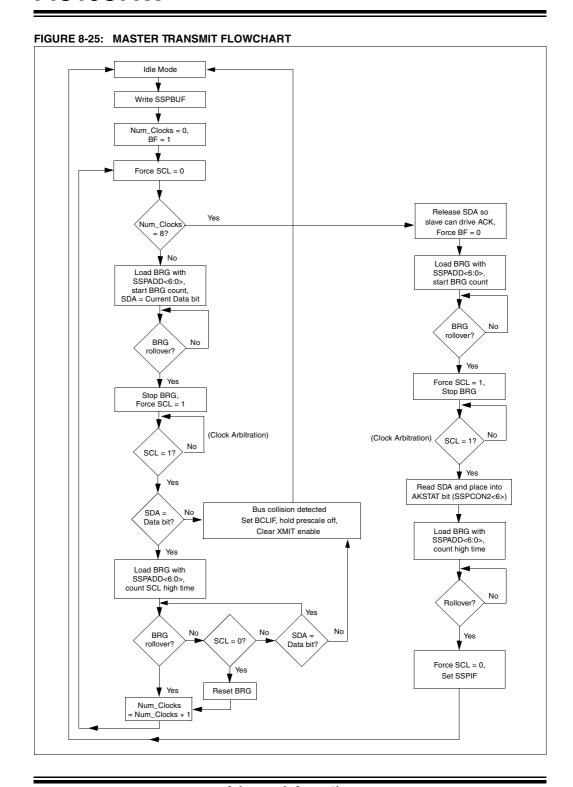


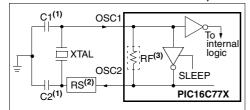
FIGURE 8-19: BAUD RATE GENERATOR TIMING WITH CLOCK ARBITRATION





NOTES:

FIGURE 12-2: CRYSTAL/CERAMIC
RESONATOR OPERATION
(HS, XT OR LP
OSC CONFIGURATION)



Note1: See Table 12-1 and Table 12-2 for recommended values of C1 and C2.

- A series resistor (RS) may be required for AT strip cut crystals.
- 3: RF varies with the crystal chosen.

FIGURE 12-3: EXTERNAL CLOCK INPUT OPERATION (HS OSC CONFIGURATION)

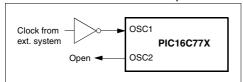


TABLE 12-1 CERAMIC RESONATORS

Ranges Te	Ranges Tested:							
Mode	Freq	Freq OSC1 OSC						
XT	455 kHz 2.0 MHz 4.0 MHz	68 - 100 pF 15 - 68 pF 15 - 68 pF	68 - 100 pF 15 - 68 pF 15 - 68 pF					
HS	8.0 MHz 16.0 MHz	10 - 68 pF 10 - 22 pF	10 - 68 pF 10 - 22 pF					
note	These values are for design guidance only. See notes at bottom of page. Resonators Used:							
455 kHz	Panasonic E	FO-A455K04B	± 0.3%					
2.0 MHz	Murata Erie	CSA2.00MG	± 0.5%					
4.0 MHz	Murata Erie	Murata Erie CSA4.00MG ± 0.5%						
8.0 MHz	Murata Erie CSA8.00MT ± 0.5%							
16.0 MHz Murata Erie CSA16.00MX ± 0.5%								
All resonators used did not have built-in capacitors.								

TABLE 12-2 CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

		•					
Osc Type	Crystal Freq	Cap. Range C1	Cap. Range C2				
LP	32 kHz	33 pF	33 pF				
	200 kHz	15 pF	15 pF				
XT	200 kHz	47-68 pF	47-68 pF				
	1 MHz	15 pF	15 pF				
	4 MHz	15 pF	15 pF				
HS	4 MHz	15 pF	15 pF				
	8 MHz	15-33 pF	15-33 pF				
	20 MHz	15-33 pF	15-33 pF				
These	values are	for design guidar	nce only. See				
notes a	at bottom of	page.					
	Crys	tals Used					
32 kHz	Epson C-00	01R32.768K-A	± 20 PPM				
200 kHz	STD XTL 2	00.000KHz	± 20 PPM				
1 MHz	ECS ECS-	± 50 PPM					
4 MHz	ECS ECS-40-20-1 ± 50 PPM						
8 MHz	EPSON CA	EPSON CA-301 8.000M-C ± 30 PPM					
20 MHz	EPSON CA	A-301 20.000M-C	± 30 PPM				

- Note 1: Recommended values of C1 and C2 are identical to the ranges tested (Table 12-1).
 - Higher capacitance increases the stability of oscillator but also increases the start-up time.
 - Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
 - 4: Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification.

12.8 Time-out Sequence

On power-up the time-out sequence is as follows: First PWRT time-out is invoked by the POR pulse. When the PWRT delay expires the Oscillator Start-up Timer is activated. The total time-out will vary based on oscillator configuration and the status of the PWRT. For example, in RC mode with the PWRT disabled, there will be no time-out at all. Figure 12-7, Figure 12-8, Figure 12-9 and Figure 12-10 depict time-out sequences on power-up.

Since the time-outs occur from the POR pulse, if MCLR is kept low long enough, the time-outs will expire. Then bringing MCLR high will begin execution immediately (Figure 12-9). This is useful for testing purposes or to synchronize more than one PICmicro microcontroller operating in parallel.

Table 12-5 shows the reset conditions for some special function registers, while Table 12-6 shows the reset conditions for all the registers.

12.9 <u>Power Control/Status Register</u> (PCON)

The Power Control/Status Register, PCON has two status bits that provide indication of which power-up type reset occurred

Bit0 is Brown-out Reset Status bit, $\overline{\text{BOR}}$. Bit $\overline{\text{BOR}}$ is set on a Power-on Reset. It must then be set by the user and checked on subsequent resets to see if bit $\overline{\text{BOR}}$ cleared, indicating a BOR occurred. However, if the brown-out circuitry is disabled, the $\overline{\text{BOR}}$ bit is a "Don't Care" bit and is considered unknown upon a POR.

Bit1 is POR (Power-on Reset Status bit). It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

TABLE 12-3 TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-	·up	Brown-out	Wake-up from	
Oscillator Configuration	PWRTE = 0	PWRTE = 1	Brown-out	SLEEP	
XT, HS, LP	72 ms + 1024Tosc	1024Tosc	72 ms + 1024Tosc	1024Tosc	
RC	72 ms	_	72 ms	_	

TABLE 12-4 STATUS BITS AND THEIR SIGNIFICANCE

POR	BOR	ТО	PD	
0	1	1	1	Power-on Reset
0	х	0	х	Illegal, TO is set on POR
0	x	x	0	Illegal, PD is set on POR
1	0	1	1	Brown-out Reset
1	1	0	1	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	MCLR Reset during normal operation
1	1	1	0	MCLR Reset during SLEEP or interrupt wake-up from SLEEP

TABLE 12-5 RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	01
MCLR Reset during normal operation	000h	000u uuuu	uu
MCLR Reset during SLEEP	000h	0001 0uuu	uu
WDT Reset	000h	0000 luuu	uu
WDT Wake-up	PC + 1	uuu0 0uuu	uu
Brown-out Reset	000h	0001 1uuu	u0
Interrupt wake-up from SLEEP	PC + 1 ⁽¹⁾	uuu1 0uuu	uu

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.

Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

FIGURE 15-14: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

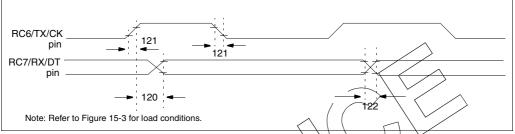


TABLE 15-15 USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typt	Max	Units	Conditions
120*	TckH2dtV	SYNC XMIT (MASTER & SLAVE)	PIC16 C 7774/773	_	_	80	ns	
		Clock high to data out valid	PIC16LC774/773	_	_	100	ns	
121*	Tckrf	Clock out rise time and fall time	PIC16 C 774/773	_	_	45	ns	
		(Master Mode)	PIC16 LC 774/773	_	_	50	ns	
122*	Tdtrf	Data out rise time and fall time	PIC16 C 774/773	_	_	45	ns	
			PIC16 LC 774/773	_	_	50	ns	

^{*} These parameters are characterized but not tested.

FIGURE 15-15: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING

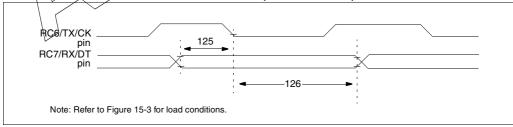


TABLE 15-16 USART SYNCHRONOUS RECEIVE REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
125*	TdtV2ckL	SYNC RCV (MASTER & SLAVE) Data setup before CK ↓ (DT setup time)	15	1	-	ns	
126*	TckL2dtl	Data hold after CK ↓ (DT hold time)	15		_	ns	

These parameters are characterized but not tested.

^{†:} Data in "Typ" column is at \$V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

^{†:} Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

16.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

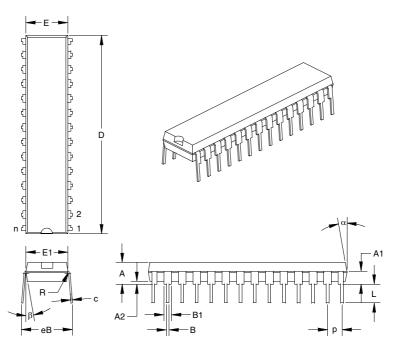
In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified VDD range). This is for **information only** and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a **statistical summary** of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution at 25° C. 'Max' or 'min' represents (mean + 3σ) or (mean - 3σ) respectively, where σ is standard deviation, over the whole temperature range.

Graphs and Tables not available at this time.

17.2 K04-070 28-Lead Skinny Plastic Dual In-line (SP) – 300 mil

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units			INCHES*		М	ILLIMETER	S
Dimension Limits		MIN	MON	MAX	MIN	MOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		28			28	
Pitch	р		0.100			2.54	
Lower Lead Width	В	0.016	0.019	0.022	0.41	0.48	0.56
Upper Lead Width	B1 [†]	0.040	0.053	0.065	1.02	1.33	1.65
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	С	0.008	0.010	0.012	0.20	0.25	0.30
Top to Seating Plane	Α	0.140	0.150	0.160	3.56	3.81	4.06
Top of Lead to Seating Plane	A1	0.070	0.090	0.110	1.78	2.29	2.79
Base to Seating Plane	A2	0.015	0.020	0.025	0.38	0.51	0.64
Tip to Seating Plane	L	0.125	0.130	0.135	3.18	3.30	3.43
Package Length	D [‡]	1.345	1.365	1.385	34.16	34.67	35.18
Molded Package Width	E‡	0.280	0.288	0.295	7.11	7.30	7.49
Radius to Radius Width	E1	0.270	0.283	0.295	6.86	7.18	7.49
Overall Row Spacing	eB	0.320	0.350	0.380	8.13	8.89	9.65
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

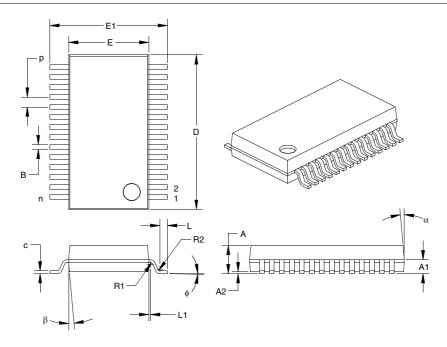
^{*} Controlling Parameter.

[†] Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

[‡] Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

17.5 K04-073 28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units			INCHES		М	ILLIMETER	S*
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	р		0.026			0.65	
Number of Pins	n		28			28	
Overall Pack. Height	Α	0.068	0.073	0.078	1.73	1.86	1.99
Shoulder Height	A1	0.026	0.036	0.046	0.66	0.91	1.17
Standoff	A2	0.002	0.005	0.008	0.05	0.13	0.21
Molded Package Length	D [‡]	0.396	0.402	0.407	10.07	10.20	10.33
Molded Package Width	E [‡]	0.205	0.208	0.212	5.20	5.29	5.38
Outside Dimension	E1	0.301	0.306	0.311	7.65	7.78	7.90
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.015	0.020	0.025	0.38	0.51	0.64
Foot Angle	ф	0	4	8	0	4	8
Radius Centerline	L1	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	С	0.005	0.007	0.009	0.13	0.18	0.22
Lower Lead Width	B [†]	0.010	0.012	0.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

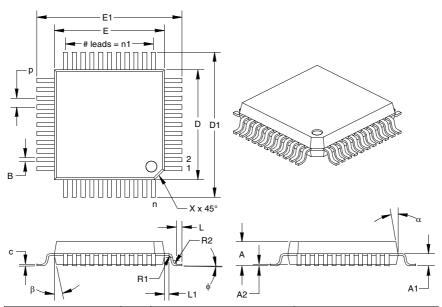
^{*} Controlling Parameter.

[†] Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

[‡] Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

17.9 K04-071 44-Lead Plastic Quad Flatpack (PQ) 10x10x2 mm Body, 1.6/0.15 mm Lead Form

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units			INCHES		MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	р		0.031			0.80	
Number of Pins	n		44			44	
Pins along Width	n1		11			11	
Overall Pack. Height	Α	0.079	0.086	0.093	2.00	2.18	2.35
Shoulder Height	A1	0.032	0.044	0.056	0.81	1.11	1.41
Standoff	A2	0.002	0.006	0.010	0.05	0.15	0.25
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.012	0.015	0.13	0.30	0.38
Foot Length	L	0.015	0.020	0.025	0.38	0.51	0.64
Foot Angle	ф	0	3.5	7	0	3.5	7
Radius Centerline	L1	0.011	0.016	0.021	0.28	0.41	0.53
Lead Thickness	С	0.005	0.007	0.009	0.13	0.18	0.23
Lower Lead Width	В [†]	0.012	0.015	0.018	0.30	0.37	0.45
Outside Tip Length	D1	0.510	0.520	0.530	12.95	13.20	13.45
Outside Tip Width	E1	0.510	0.520	0.530	12.95	13.20	13.45
Molded Pack. Length	D [‡]	0.390	0.394	0.398	9.90	10.00	10.10
Molded Pack. Width	E [‡]	0.390	0.394	0.398	9.90	10.00	10.10
Pin 1 Corner Chamfer	Χ	0.025	0.035	0.045	0.635	0.89	1.143
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	12	15	5	12	15

Controlling Parameter.

[†] Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

[‡] Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E." JEDEC equivalent:MS-022 AB

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