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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c774-e-p

4.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- Internal or external clock select
- Edge select for external clock
- 8-bit software programmable prescaler
- Interrupt on overflow from FFh to 00h

Figure 4-1 is a simplified block diagram of the Timer0 module.

Additional information on timer modules is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

4.1 Timer0 Operation

Timer0 can operate as a timer or as a counter.

Timer mode is selected by clearing bit T0CS (OPTION_REG<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting bit T0CS (OPTION_REG<5>). In counter mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit T0SE (OPTION_REG<4>). Clearing bit T0SE selects the rising edge. Restrictions on the external clock input are discussed in below.

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (TOSC). Also, there is a delay in the actual incrementing of Timer0 after synchronization.

Additional information on external clock requirements is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

4.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 4-2). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The prescaler is not readable or writable.

The PSA and PS2:PS0 bits (OPTION_REG<3:0>) determine the prescaler assignment and prescale ratio.

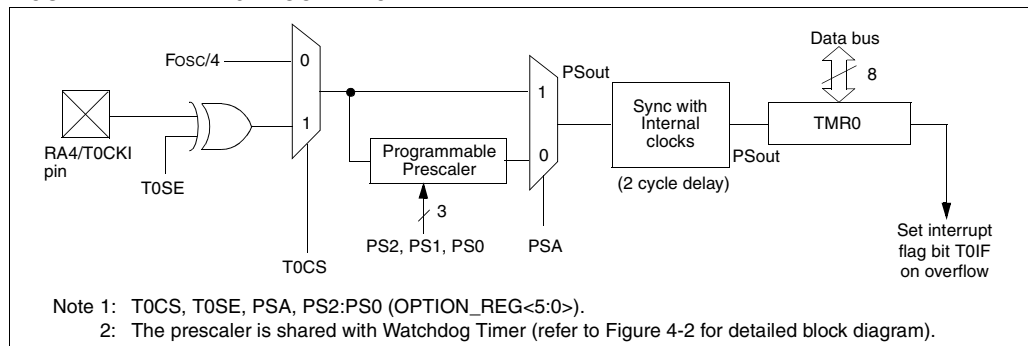
Clearing bit PSA will assign the prescaler to the Timer0 module. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable.

Setting bit PSA will assign the prescaler to the Watchdog Timer (WDT). When the prescaler is assigned to the WDT, prescale values of 1:1, 1:2, ..., 1:128 are selectable.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g. CLRF 1, MOVWF 1, BSF 1,x,...etc.) will clear the prescaler. When assigned to WDT, a CLRWD instruction will clear the prescaler along with the WDT.

Note: Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count, but will not change the prescaler assignment.

FIGURE 4-1: TIMER0 BLOCK DIAGRAM



7.1 Capture Mode

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin RC2/CCP1. An event is defined as:

- every falling edge
- every rising edge
- every 4th rising edge
- every 16th rising edge

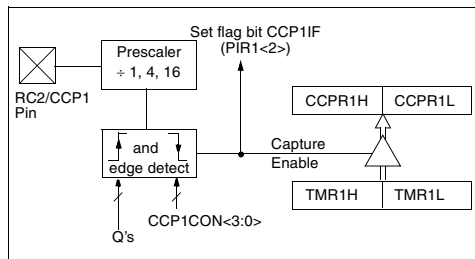
An event is selected by control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). When a capture is made, the interrupt request flag bit CCP1IF (PIR1<2>) is set. It must be cleared in software. If another capture occurs before the value in register CCPR1 is read, the old captured value will be lost.

7.1.1 CCP PIN CONFIGURATION

In Capture mode, the RC2/CCP1 pin should be configured as an input by setting the TRISC<2> bit.

Note: If the RC2/CCP1 is configured as an output, a write to the port can cause a capture condition.

FIGURE 7-2: CAPTURE MODE OPERATION BLOCK DIAGRAM



7.1.2 TIMER1 MODE SELECTION

Timer1 must be running in timer mode or synchronized counter mode for the CCP module to use the capture feature. In asynchronous counter mode, the capture operation may not work.

7.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep bit CCP1IE (PIE1<2>) clear to avoid false interrupts and should clear the flag bit CCP1IF following any such change in operating mode.

7.1.4 CCP PRESCALER

There are four prescaler settings, specified by bits CCP1M3:CCP1M0. Whenever the CCP module is turned off, or the CCP module is not in capture mode, the prescaler counter is cleared. This means that any reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore the first capture may be from a non-zero prescaler. Example 7-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the "false" interrupt.

EXAMPLE 7-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
CLRF    CCP1CON    ;Turn CCP module off
MOVLW  NEW_CAPT_PS ;Load the W reg with
                        ; the new prescaler
MOVWF  CCP1CON     ; mode value and CCP ON

MOVWF  CCP1CON     ;Load CCP1CON with this
                        ; value
```

FIGURE 8-3: SSPCON2: SYNC SERIAL PORT CONTROL REGISTER2 (ADDRESS 91h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GCEN	AKSTAT	AKDT	AKEN	RCEN	PEN	RSEN	SEN
bit7				bit0			

R =Readable bit
W =Writable bit
U =Unimplemented bit,
Read as '0'
- n =Value at POR reset

bit 7: **GCEN:** General Call Enable bit (In I²C slave mode only)
1 = Enable interrupt when a general call address (0000h) is received in the SSPSR.
0 = General call address disabled.

bit 6: **AKSTAT:** Acknowledge Status bit (In I²C master mode only)
In master transmit mode:
1 = Acknowledge was not received from slave
0 = Acknowledge was received from slave

bit 5: **AKDT:** Acknowledge Data bit (In I²C master mode only)
In master receive mode:
Value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive.
1 = Not Acknowledge
0 = Acknowledge

bit 4: **AKEN:** Acknowledge Sequence Enable bit (In I²C master mode only).
In master receive mode:
1 = Initiate Acknowledge sequence on SDA and SCL pins, and transmit AKDT data bit. Automatically cleared by hardware.
0 = Acknowledge sequence idle

bit 3: **RCEN:** Receive Enable bit (In I²C master mode only).
1 = Enables Receive mode for I²C
0 = Receive idle

bit 2: **PEN:** Stop Condition Enable bit (In I²C master mode only).
SCK release control
1 = Initiate Stop condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Stop condition idle

bit 1: **RSEN:** Repeated Start Condition Enabled bit (In I²C master mode only)
1 = Initiate Repeated Start condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Repeated Start condition idle.

bit 0: **SEN:** Start Condition Enabled bit (In I²C master mode only)
1 = Initiate Start condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Start condition idle.

Note: For bits AKEN, RCEN, PEN, RSEN, SEN: If the I²C module is not in the idle mode, this bit may not be set (no spooling), and the SSPBUF may not be written (or writes to the SSPBUF are disabled).

The SSPSTAT register gives the status of the data transfer. This information includes detection of a START (S) or STOP (P) bit, specifies if the received byte was data or address if the next byte is the completion of 10-bit address, and if this will be a read or write data transfer.

SSPBUF is the register to which the transfer data is written to or read from. The SSPSR register shifts the data in or out of the device. In receive operations, the SSPBUF and SSPSR create a doubled buffered receiver. This allows reception of the next byte to begin before reading the last byte of received data. When the complete byte is received, it is transferred to the SSPBUF register and flag bit SSPIF is set. If another complete byte is received before the SSPBUF register is read, a receiver overflow has occurred and bit SSPOV (SSPCON<6>) is set and the byte in the SSPSR is lost.

The SSPADD register holds the slave address. In 10-bit mode, the user needs to write the high byte of the address (1111 0 A9 A8 0). Following the high byte address match, the low byte of the address needs to be loaded (A7:A0).

8.2.1 SLAVE MODE

In slave mode, the SCL and SDA pins must be configured as inputs. The MSSP module will override the input state with the output data when required (slave-transmitter).

When an address is matched or the data transfer after an address match is received, the hardware automatically will generate the acknowledge (ACK) pulse, and then load the SSPBUF register with the received value currently in the SSPSR register.

There are certain conditions that will cause the MSSP module not to give this ACK pulse. These are if either (or both):

- a) The buffer full bit BF (SSPSTAT<0>) was set before the transfer was received.
- b) The overflow bit SSPOV (SSPCON<6>) was set before the transfer was received.

If the BF bit is set, the SSPSR register value is not loaded into the SSPBUF, but bit SSPIF and SSPOV are set. Table 8-2 shows what happens when a data transfer byte is received, given the status of bits BF and SSPOV. The shaded cells show the condition where user software did not properly clear the overflow condition. Flag bit BF is cleared by reading the SSPBUF register while bit SSPOV is cleared through software.

The SCL clock input must have a minimum high and low time for proper operation. The high and low times of the I^2C specification as well as the requirement of the MSSP module is shown in timing parameter #100 and parameter #101 of the Electrical Specifications.

8.2.1.1 ADDRESSING

Once the MSSP module has been enabled, it waits for a START condition to occur. Following the START condition, the 8-bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock (SCL) line. The value of register SSPSR<7:1> is compared to the value of the SSPADD register. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match, and the BF and SSPOV bits are clear, the following events occur:

- a) The SSPSR register value is loaded into the SSPBUF register on the falling edge of the 8th SCL pulse.
- b) The buffer full bit, BF is set on the falling edge of the 8th SCL pulse.
- c) An ACK pulse is generated.
- d) SSP interrupt flag bit, SSPIF (PIR1<3>) is set (interrupt is generated if enabled) - on the falling edge of the 9th SCL pulse.

In 10-bit address mode, two address bytes need to be received by the slave. The five Most Significant bits (MSBs) of the first address byte specify if this is a 10-bit address. Bit $\overline{R}/\overline{W}$ (SSPSTAT<2>) must specify a write so the slave device will receive the second address byte. For a 10-bit address the first byte would equal '1111 0 A9 A8 0', where A9 and A8 are the two MSBs of the address. The sequence of events for a 10-bit address is as follows, with steps 7- 9 for slave-transmitter:

1. Receive first (high) byte of Address (bits SSPIF, BF, and bit UA (SSPSTAT<1>) are set).
2. Update the SSPADD register with second (low) byte of Address (clears bit UA and releases the SCL line).
3. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
4. Receive second (low) byte of Address (bits SSPIF, BF, and UA are set).
5. Update the SSPADD register with the first (high) byte of Address. This will clear bit UA and release the SCL line.
6. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
7. Receive Repeated Start condition.
8. Receive first (high) byte of Address (bits SSPIF and BF are set).
9. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.

Note: Following the Repeated Start condition (step 7) in 10-bit mode, the user only needs to match the first 7-bit address. The user does not update the SSPADD for the second half of the address.

- i) The MSSP Module shifts in the ACK bit from the slave device, and writes its value into the SSPCON2 register (SSPCON2<6>).
- j) The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSPIF bit.
- k) The user generates a STOP condition by setting the STOP enable bit PEN in SSPCON2.
- l) Interrupt is generated once the STOP condition is complete.

8.2.8 BAUD RATE GENERATOR

In I²C master mode, the reload value for the BRG is located in the lower 7 bits of the SSPADD register (Figure 8-18). When the BRG is loaded with this value, the BRG counts down to 0 and stops until another reload has taken place. The BRG count is decremented twice per instruction cycle (T_{cy}) on the Q2 and Q4 clock.

In I²C master mode, the BRG is reloaded automatically. If Clock Arbitration is taking place for instance, the BRG will be reloaded when the SCL pin is sampled high (Figure 8-19).

FIGURE 8-18: BAUD RATE GENERATOR BLOCK DIAGRAM

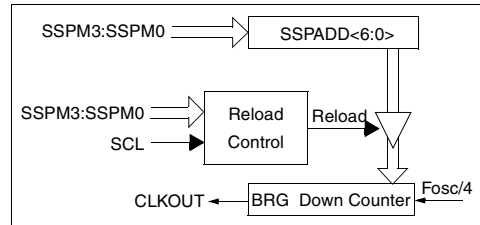


FIGURE 8-19: BAUD RATE GENERATOR TIMING WITH CLOCK ARBITRATION

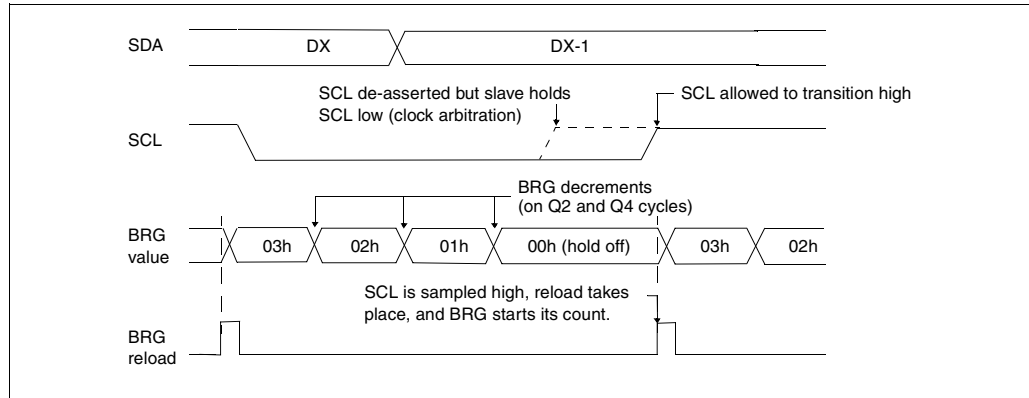
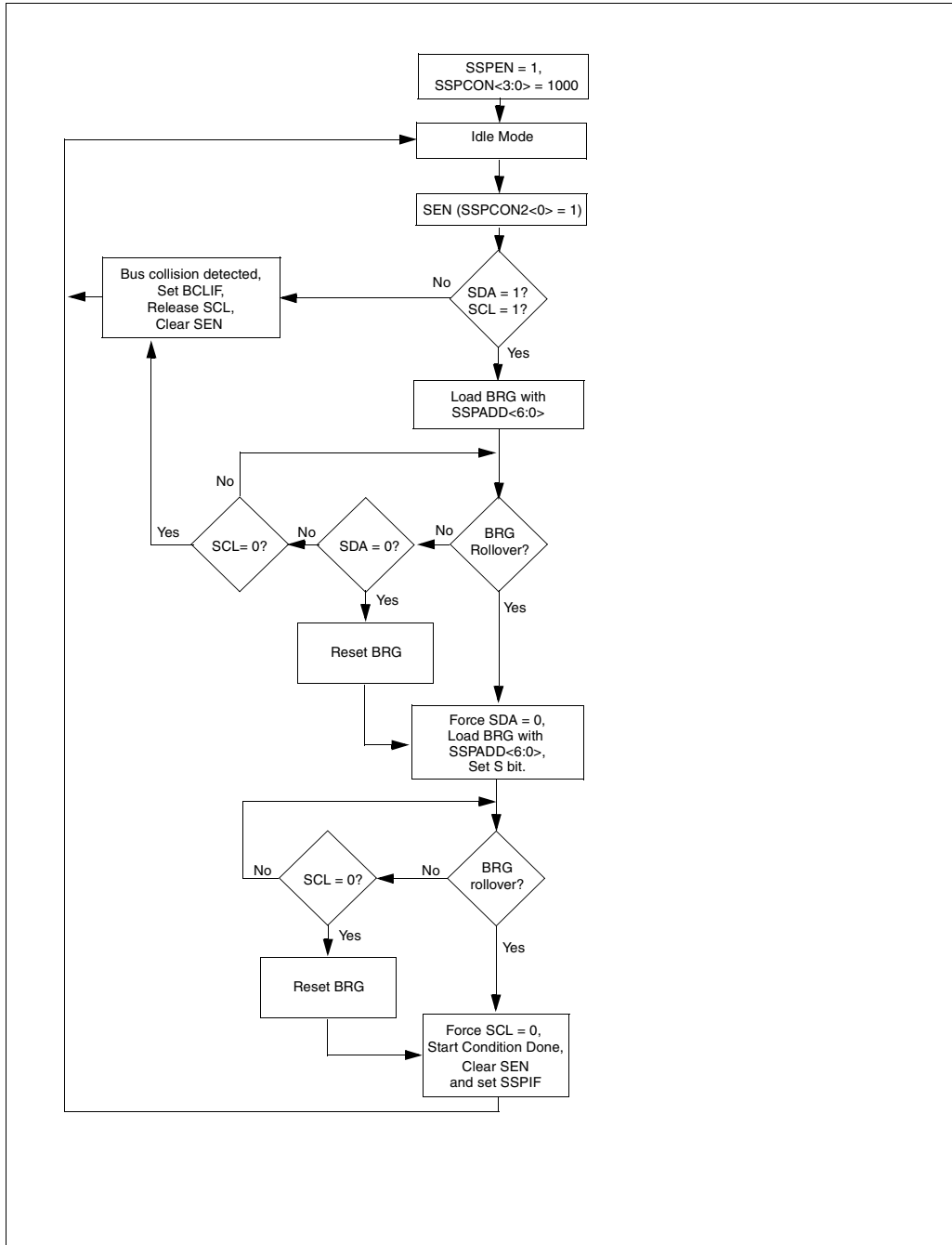


FIGURE 8-21: START CONDITION FLOWCHART



8.2.13 ACKNOWLEDGE SEQUENCE TIMING

An acknowledge sequence is enabled by setting the acknowledge sequence enable bit, **AKEN** (**SSPCON2<4>**). When this bit is set, the **SCL** pin is pulled low and the contents of the acknowledge data bit is presented on the **SDA** pin. If the user wishes to generate an acknowledge, then the **AKDT** bit should be cleared. If not, the user should set the **AKDT** bit before starting an acknowledge sequence. The baud rate generator then counts for one rollover period (T_{BRG}), and the **SCL** pin is de-asserted (pulled high). When the **SCL** pin is sampled high (clock arbitration), the baud

rate generator counts for T_{BRG} . The **SCL** pin is then pulled low. Following this, the **AKEN** bit is automatically cleared, the baud rate generator is turned off, and the **SSP** module then goes into **IDLE** mode. (Figure 8-29)

8.2.13.13 WCOL STATUS FLAG

If the user writes the **SSPBUF** when an acknowledge sequence is in progress, then **WCOL** is set and the contents of the buffer are unchanged (the write doesn't occur).

FIGURE 8-29: ACKNOWLEDGE SEQUENCE WAVEFORM

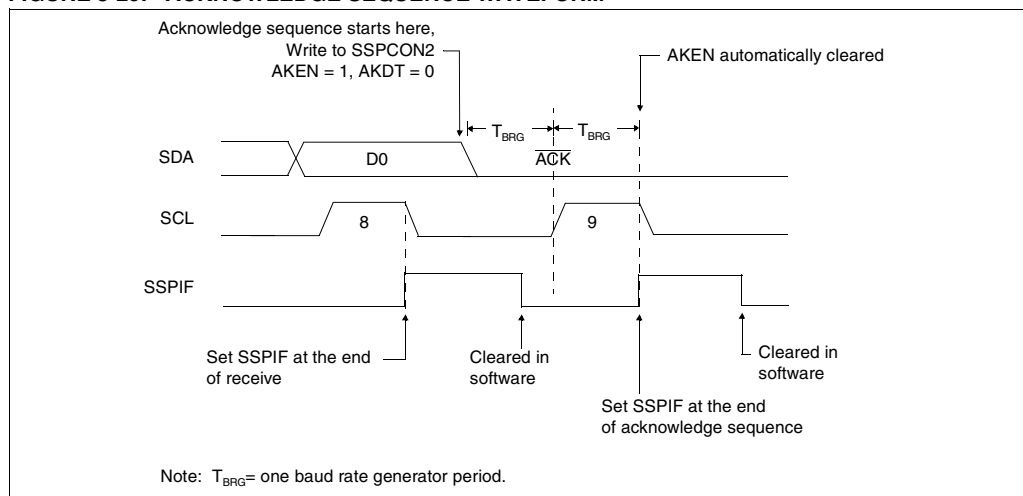
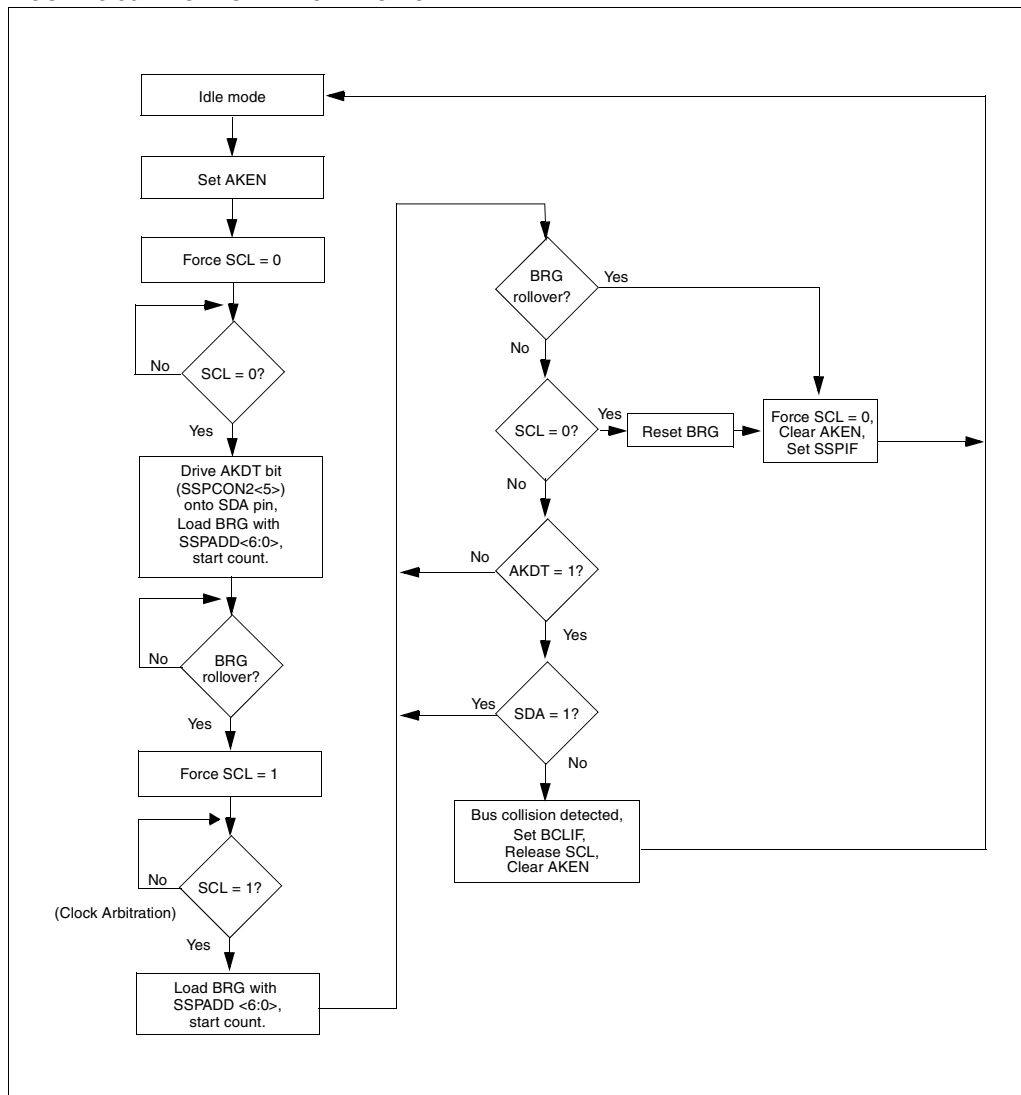


FIGURE 8-30: ACKNOWLEDGE FLOWCHART



8.2.15 CLOCK ARBITRATION

Clock arbitration occurs when the master, during any receive, transmit, or repeated start/stop condition, deasserts the SCL pin (SCL allowed to float high). When the SCL pin is allowed to float high, the baud rate generator (BRG) is suspended from counting until the SCL pin is actually sampled high. When the SCL pin is sampled high, the baud rate generator is reloaded with the contents of SSPADD<6:0> and begins counting. This ensures that the SCL high time will always be at least one BRG rollover count in the event that the clock is held low by an external device (Figure 8-33).

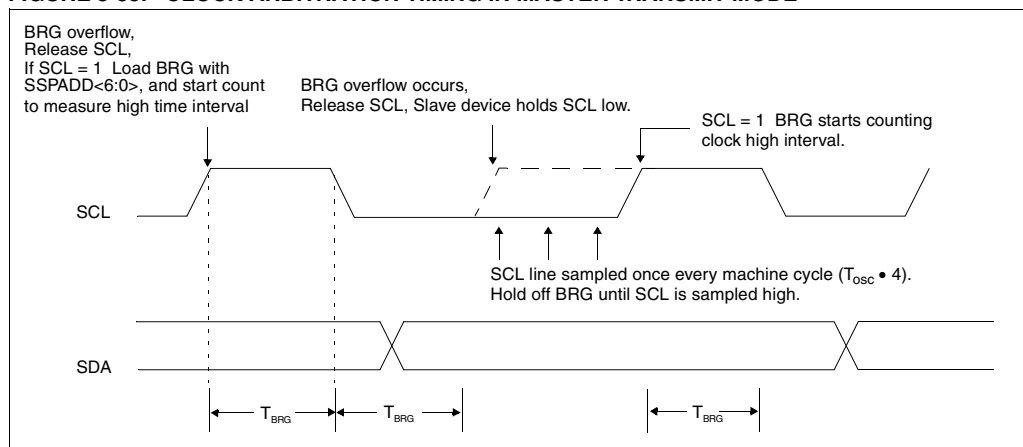
8.2.16 SLEEP OPERATION

While in sleep mode, the I²C module can receive addresses or data, and when an address match or complete byte transfer occurs wake the processor from sleep (if the SSP interrupt is enabled).

8.2.17 EFFECTS OF A RESET

A reset disables the SSP module and terminates the current transfer.

FIGURE 8-33: CLOCK ARBITRATION TIMING IN MASTER TRANSMIT MODE



8.2.18 MULTI-MASTER COMMUNICATION, BUS COLLISION, AND BUS ARBITRATION

Multi-Master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDA pin, arbitration takes place when the master outputs a '1' on SDA by letting SDA float high and another master asserts a '0'. When the SCL pin floats high, data should be stable. If the expected data on SDA is a '1' and the data sampled on the SDA pin = '0', then a bus collision has taken place. The master will set the Bus Collision Interrupt Flag, BCLIF and reset the I²C port to its IDLE state. (Figure 8-34).

If a transmit was in progress when the bus collision occurred, the transmission is halted, the BF flag is cleared, the SDA and SCL lines are de-asserted, and the SSPBUF can be written to. When the user services the bus collision interrupt service routine, and if the I²C bus is free, the user can resume communication by asserting a START condition.

If a START, Repeated Start, STOP, or Acknowledge condition was in progress when the bus collision occurred, the condition is aborted, the SDA and SCL lines are de-asserted, and the respective control bits in the SSPCON2 register are cleared. When the user services the bus collision interrupt service routine, and if the I²C bus is free, the user can resume communication by asserting a START condition.

The Master will continue to monitor the SDA and SCL pins, and if a STOP condition occurs, the SSPIF bit will be set.

A write to the SSPBUF will start the transmission of data at the first data bit, regardless of where the transmitter left off when bus collision occurred.

In multi-master mode, the interrupt generation on the detection of start and stop conditions allows the determination of when the bus is free. Control of the I²C bus can be taken when the P bit is set in the SSPSTAT register, or the bus is idle and the S and P bits are cleared.

FIGURE 8-34: BUS COLLISION TIMING FOR TRANSMIT AND ACKNOWLEDGE

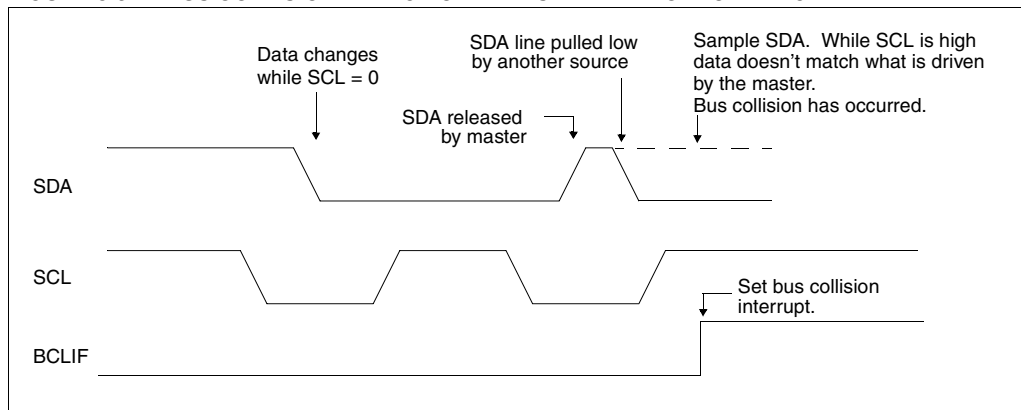


FIGURE 9-4: ASYNCHRONOUS TRANSMISSION

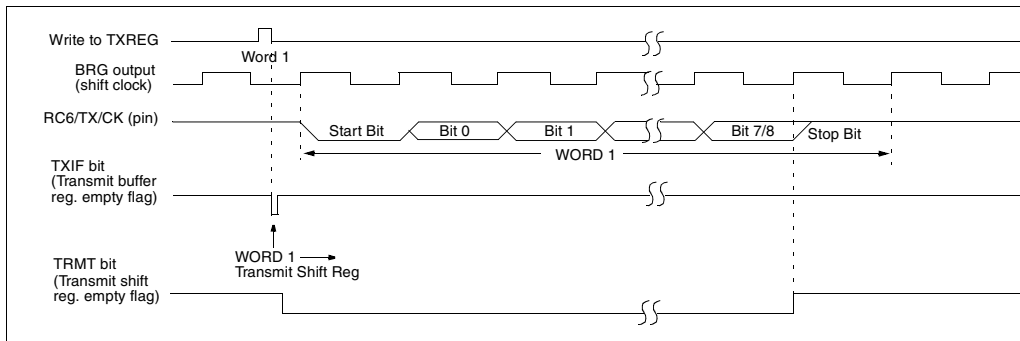


FIGURE 9-5: ASYNCHRONOUS TRANSMISSION (BACK TO BACK)

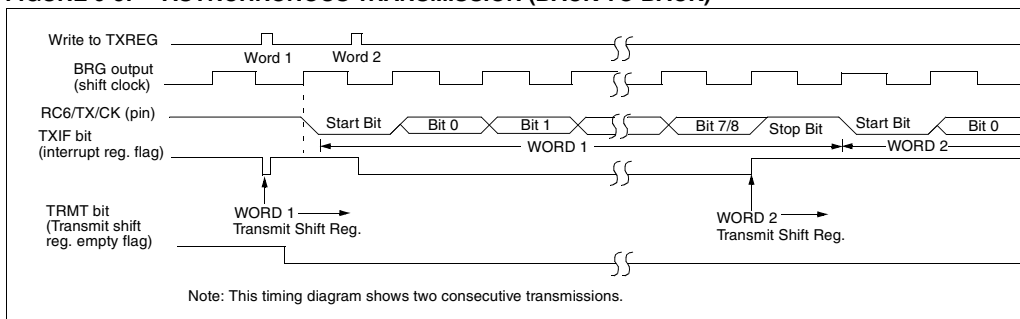


TABLE 9-6 REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
19h	TXREG	USART Transmit Register								0000 0000	0000 0000
8Ch	PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Asynchronous Transmission.

Note 1: Bits PSPIE and PSPIF are reserved on the 28-pin devices, always maintain these bits clear.

FIGURE 9-6: USART RECEIVE BLOCK DIAGRAM

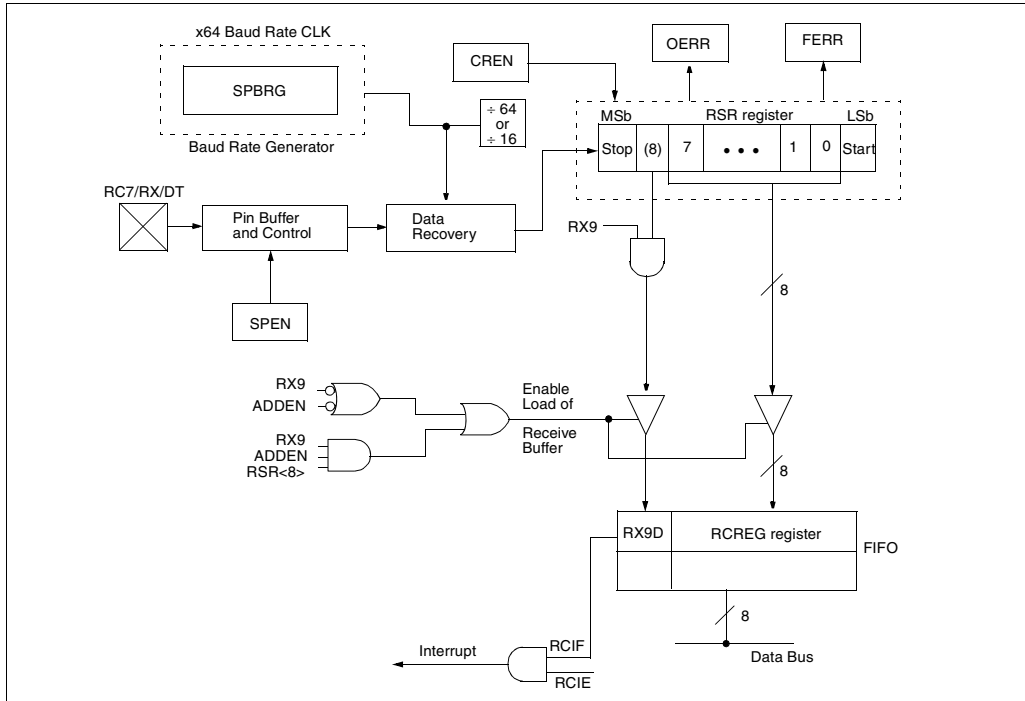


FIGURE 9-7: ASYNCHRONOUS RECEPTION WITH ADDRESS DETECT

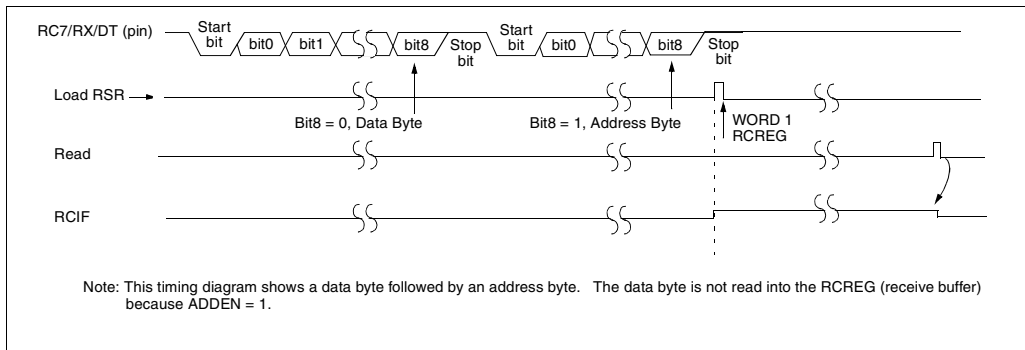


FIGURE 10-2: REFCON: VOLTAGE REFERENCE CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
VRHEN	VRLEN	VRHOEN	VRLOEN	—	—	—	—
bit7				bit0			

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n =Value at POR reset

bit 7: **VRHEN:** Voltage Reference High Enable bit (VRH = 4.096V)
1 = Enabled, powers up reference generator
0 = Disabled, powers down reference generator if unused by LVD, BOR, or VRL

bit 6: **VRLEN:** Voltage Reference Low Enable bit (VRL = 2.048V)
1 = Enabled, powers up reference generator
0 = Disabled, powers down reference generator if unused by LVD, BOR, or VRH

bit 5: **VRHOEN:** High Voltage Reference Output Enable bit
1 = Enabled, VRH analog reference is presented on RA3 if enabled (VRHEN = 1)
0 = Disabled, analog reference is used internally only

bit 4: **VRLOEN:** Low Voltage Reference Output Enable bit
1 = Enabled, VRL analog reference is presented on RA2 if enabled (VRLEN = 1)
0 = Disabled, analog reference is used internally only

bit 3-0: **Unimplemented:** Read as '0'

10.1 Bandgap Voltage Reference

The bandgap module generates a stable voltage reference of 1.22V over a range of temperatures and device supply voltages. This module is enabled anytime any of the following are enabled:

- Brown-out Reset
- Low-voltage Detect
- Either of the internal analog references (VRH, VRL)

Whenever the above are all disabled, the bandgap module is disabled and draws no current.

10.2 Internal VREF for A/D Converter

The bandgap output voltage is used to generate two stable references for the A/D converter module. These references are enabled in software to provide the user with the means to turn them on and off in order to minimize current consumption. Each reference can be individually enabled.

The 4.096V reference (VRH) is enabled with control bit VRHEN (REFCON<7>). When this bit is set, the gain amplifier is enabled. After a specified start-up time a stable reference of 4.096V is generated and can be used by the A/D converter as the VRH input.

The 2.048V reference (VRL) is enabled by setting control bit VRLEN (REFCON<6>). When this bit is set, the gain amplifier is enabled. After a specified start up time a stable reference of 2.048V is generated and can be used by the A/D converter as the VRL input.

Each voltage reference can source/sink up to 5 mA of current.

Each reference, if enabled, can be presented on an external pin by setting the VRHOEN (high reference output enable) or VRLOEN (low reference output enable) control bit. If the reference is not enabled, the VRHOEN and VRLOEN bits will have no effect on the corresponding pin. The device specific pin can then be used as general purpose I/O.

Note: If VRH or VRL is enabled and the other reference (VRL or VRH), the BOR, and the LVD modules are not enabled, the bandgap will require a start-up time of no more than 50 μ s before the bandgap reference is stable. Before using the internal VRH or VRL reference, ensure that the bandgap reference voltage is stable by monitoring the BGST bit in the LVDCON register. The voltage references will not be reliable until the bandgap is stable as shown by BGST being set.

The value that is in the ADRESH and ADRESL registers are not modified for a Power-on Reset. The ADRESH and ADRESL registers will contain unknown data after a Power-on Reset.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine acquisition time, see Section 11.6. After this acquisition time has elapsed the A/D conversion can be started. The following steps should be followed for doing an A/D conversion:

11.2 Configuring the A/D Module

11.3 Configuring Analog Port Pins

The ADCON1 and TRIS registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bit set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS3:CHS0 bits and the TRIS bits.

Note 1: When reading the PORTA or PORTE register, all pins configured as analog input channels will read as cleared (a low level). When reading the PORTB register, all pins configured as analog input channels will read as set (a high level). Pins configured as digital inputs, will convert an analog input. Analog levels on a digitally configured input will not affect the conversion accuracy.

Note 2: Analog levels on any pin that is defined as a digital input (including the ANx pins), may cause the input buffer to consume current that is out of the devices specification.

11.3.1 CONFIGURING THE REFERENCE VOLTAGES

The VCFG bits in the ADCON1 register configure the A/D module reference inputs. The reference high input can come from an internal reference (VRH) or (VRL), an external reference (VREF+), or AVDD. The low reference input can come from an internal reference (VRL), an external reference (VREF-), or AVSS. If an external reference is chosen for the reference high or reference low inputs, the port pin that multiplexes the incoming external references is configured as an analog input, regardless of the values contained in the A/D port configuration bits (PCFG3:PCFG0).

After the A/D module has been configured as desired, and the analog input channels have their corresponding TRIS bits selected for port inputs, the selected channel must be acquired before conversion is started. The A/D conversion cycle can be initiated by setting the GO/DONE bit. The A/D conversion begins, and lasts for 13TAD. The following steps should be followed for performing an A/D conversion:

1. Configure the A/D module
 - Configure analog pins / voltage reference / and digital I/O (ADCON1)
 - Select A/D input channel (ADCON0)
 - Select A/D conversion clock (ADCON0)
 - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if required)
 - Clear ADIF bit
 - Set ADIE bit
 - Set PEIE bit
 - Set GIE bit
3. Wait the required acquisition time (3TAD)
4. Start conversion
 - Set GO/DONE bit (ADCON0)
5. Wait 13TAD until A/D conversion is complete, by either:
 - Polling for the GO/DONE bit to be cleared
 OR
 - Waiting for the A/D interrupt
6. Read A/D Result registers (ADRESH and ADRESL), clear ADIF if required.
7. For next conversion, go to step 1, step 2 or step 3 as required.

Clearing the GO/DONE bit during a conversion will abort the current conversion. The ADRESH and ADRESL registers **WILL** be updated with the partially completed A/D conversion value. That is, the ADRESH and ADRESL registers **WILL** contain the value of the current incomplete conversion.

Note: Do not set the ADON bit and the GO/DONE bit in the same instruction. Doing so will cause the GO/DONE bit to be automatically cleared.

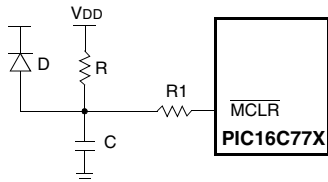
12.4 Power-On Reset (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.5V - 2.1V). To take advantage of the POR, just tie the MCLR pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is specified. See Electrical Specifications for details. For a slow rise time, see Figure 12-6.

Two delay timers have been provided which hold the device in reset after a POR (dependant upon device configuration) so that all operational parameters have been met prior to releasing to device to resume/begin normal operation.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met. Brown-out Reset may be used to meet the startup conditions, or if necessary an external POR circuit may be implemented to delay end of reset for as long as needed.

FIGURE 12-6: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



- Note 1: External Power-on Reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
- 2: $R < 40 \text{ k}\Omega$ is recommended to make sure that voltage drop across R does not violate the device's electrical specification.
- 3: $R1 = 100\Omega$ to $1 \text{ k}\Omega$ will limit any current flowing into MCLR from external capacitor C in the event of MCLR/VPP pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

12.5 Power-up Timer (PWRT)

The Power-up Timer provides a fixed 72 ms nominal time-out on power-up type resets only. For a POR, the PWRT is invoked when the POR pulse is generated. For a BOR, the PWRT is invoked when the device exits the reset condition (VDD rises above BOR trippoint). The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as the PWRT is active. The PWRT's time delay is designed to allow VDD to rise to an acceptable level. A configuration bit is provided to enable/disable the PWRT for the POR only. For a BOR the PWRT is always available regardless of the configuration bit setting.

The power-up time delay will vary from chip to chip due to VDD, temperature, and process variation. See DC parameters for details.

12.6 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on a power-up type reset or a wake-up from SLEEP.

12.7 Brown-Out Reset (BOR)

The Brown-out Reset module is used to generate a reset when the supply voltage falls below a specified trip voltage. The trip voltage is configurable to any one of four voltages provided by the BORV1:BORV0 configuration word bits.

Configuration bit, BODEN, can disable (if clear/programmed) or enable (if set) the Brown-out Reset circuitry. If VDD falls below the specified trippoint for greater than parameter #35 in the electrical specifications section, the brown-out situation will reset the chip. A reset may not occur if VDD falls below the trippoint for less than parameter #35. The chip will remain in Brown-out Reset until VDD rises above BVDD. The Power-up Timer will be invoked at that point and will keep the chip in RESET an additional 72 ms. If VDD drops below BVDD while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above BVDD, the Power-up Timer will again begin a 72 ms time delay. Even though the PWRT is always enabled when brown-out is enabled, the PWRT configuration word bit should be cleared (enabled) when brown-out is enabled.

FIGURE 12-8: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD}): CASE 1

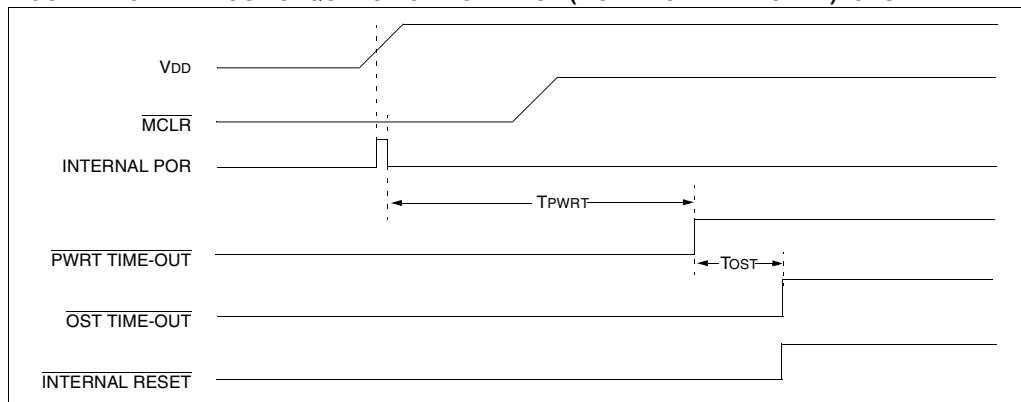


FIGURE 12-9: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD}): CASE 2

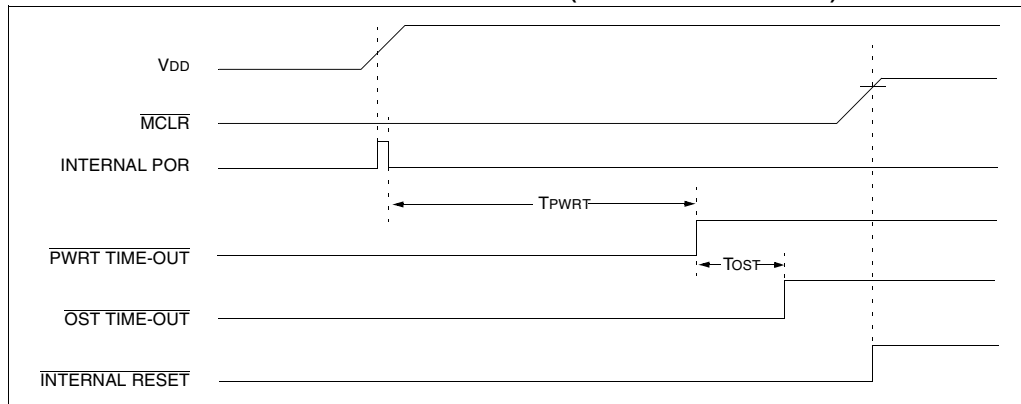
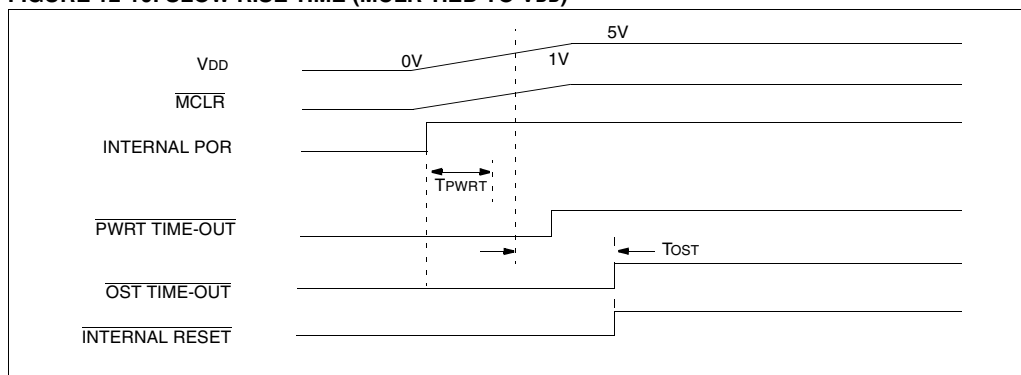


FIGURE 12-10: SLOW RISE TIME ($\overline{\text{MCLR}}$ TIED TO V_{DD})



14.6 SIMICE Entry-Level Hardware Simulator

SIMICE is an entry-level hardware development system designed to operate in a PC-based environment with Microchip's simulator MPLAB™-SIM. Both SIMICE and MPLAB-SIM run under Microchip Technology's MPLAB Integrated Development Environment (IDE) software. Specifically, SIMICE provides hardware simulation for Microchip's PIC12C5XX, PIC12CE5XX, and PIC16C5X families of PICmicro 8-bit microcontrollers. SIMICE works in conjunction with MPLAB-SIM to provide non-real-time I/O port emulation. SIMICE enables a developer to run simulator code for driving the target system. In addition, the target system can provide input to the simulator code. This capability allows for simple and interactive debugging without having to manually generate MPLAB-SIM stimulus files. SIMICE is a valuable debugging tool for entry-level system development.

14.7 PICDEM-1 Low-Cost PICmicro Demonstration Board

The PICDEM-1 is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The users can program the sample microcontrollers provided with the PICDEM-1 board, on a PRO MATE II or PICSTART-Plus programmer, and easily test firmware. The user can also connect the PICDEM-1 board to the MPLAB-ICE emulator and download the firmware to the emulator for testing. Additional prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push-button switches and eight LEDs connected to PORTB.

14.8 PICDEM-2 Low-Cost PIC16CXX Demonstration Board

The PICDEM-2 is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-2 board, on a PRO MATE II programmer or PICSTART-Plus, and easily test firmware. The MPLAB-ICE emulator may also be used with the PICDEM-2 board to test firmware. Additional prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push-button switches, a potentiometer for simulated analog input, a Serial EEPROM to demonstrate usage of the I²C bus and separate headers for connection to an LCD module and a keypad.

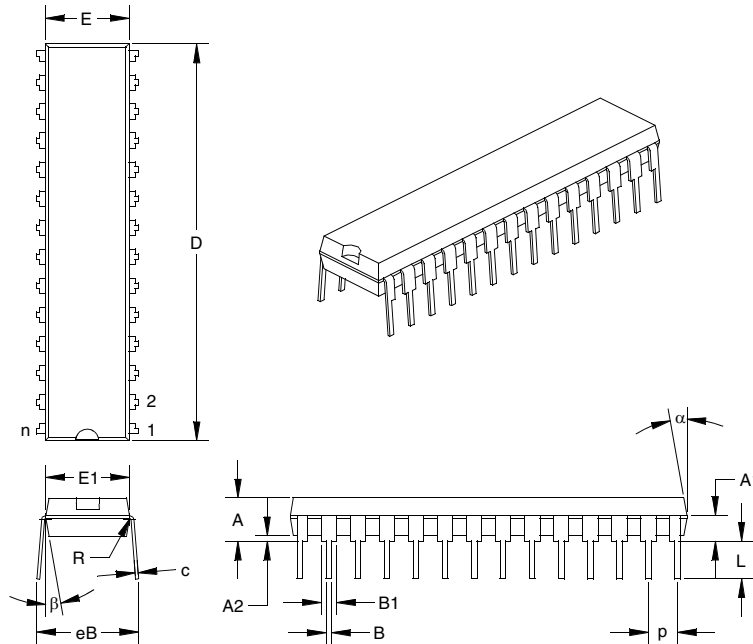
14.9 PICDEM-3 Low-Cost PIC16CXXX Demonstration Board

The PICDEM-3 is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with a LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-3 board, on a PRO MATE II programmer or PICSTART Plus with an adapter socket, and easily test firmware. The MPLAB-ICE emulator may also be used with the PICDEM-3 board to test firmware. Additional prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include an RS-232 interface, push-button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM-3 board is an LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM-3 provides an additional RS-232 interface and Windows 3.1 software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

NOTES:

17.2 K04-070 28-Lead Skinny Plastic Dual In-line (SP) – 300 mil

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		28			28	
Pitch	p		0.100			2.54	
Lower Lead Width	B	0.016	0.019	0.022	0.41	0.48	0.56
Upper Lead Width	B1†	0.040	0.053	0.065	1.02	1.33	1.65
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Top to Seating Plane	A	0.140	0.150	0.160	3.56	3.81	4.06
Top of Lead to Seating Plane	A1	0.070	0.090	0.110	1.78	2.29	2.79
Base to Seating Plane	A2	0.015	0.020	0.025	0.38	0.51	0.64
Tip to Seating Plane	L	0.125	0.130	0.135	3.18	3.30	3.43
Package Length	D‡	1.345	1.365	1.385	34.16	34.67	35.18
Molded Package Width	E‡	0.280	0.288	0.295	7.11	7.30	7.49
Radius to Radius Width	E1	0.270	0.283	0.295	6.86	7.18	7.49
Overall Row Spacing	eB	0.320	0.350	0.380	8.13	8.89	9.65
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter.

† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

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