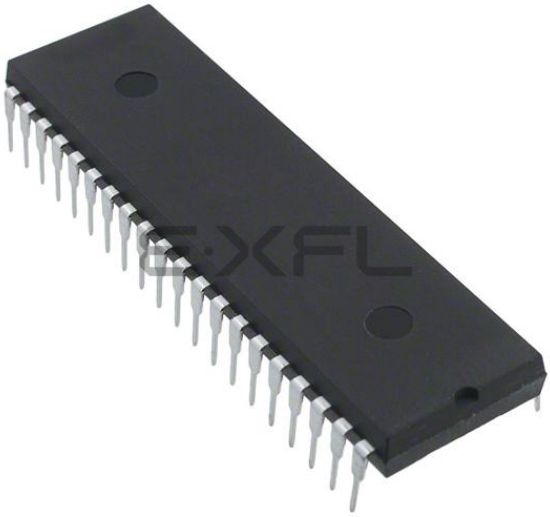


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 33 |
| Program Memory Size | 7KB (4K x 14) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4V ~ 5.5V |
| Data Converters | A/D 10x12b |
| Oscillator Type | External |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 40-DIP (0.600", 15.24mm) |
| Supplier Device Package | 40-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16c774-p |

**NOTES:**

**FIGURE 8-1: SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS: 94h)**

| R/W-0 | R/W-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| SMP | CKE | D/$\overline{A}$ | P | S | R/$\overline{W}$ | UA | BF |
| bit7 | | | | | | | bit0 |

R =Readable bit
W =Writable bit
U =Unimplemented bit, read as '0'
- n =Value at POR reset

bit 7: **SMP:** Sample bit
SPI Master Mode
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time
SPI Slave Mode
SMP must be cleared when SPI is used in slave mode
In $I^2C$ master or slave mode:
1= Slew rate control disabled for standard speed mode (100 kHz and 1 MHz)
0= Slew rate control enabled for high speed mode (400 kHz)

bit 6: **CKE**: SPI Clock Edge Select (Figure 8-6, Figure 8-8, and Figure 8-9)
CKP = 0
1 = Data transmitted on rising edge of SCK
0 = Data transmitted on falling edge of SCK
CKP = 1
1 = Data transmitted on falling edge of SCK
0 = Data transmitted on rising edge of SCK

bit 5: **D/A**: Data/$\overline{\text{Address}}$ bit ($I^2C$ mode only)
1 = Indicates that the last byte received or transmitted was data
0 = Indicates that the last byte received or transmitted was address

bit 4: **P**: Stop bit
($I^2C$ mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared)
1 = Indicates that a stop bit has been detected last (this bit is '0' on RESET)
0 = Stop bit was not detected last

bit 3: **S**: Start bit
($I^2C$ mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared)
1 = Indicates that a start bit has been detected last (this bit is '0' on RESET)
0 = Start bit was not detected last

bit 2: **R/W**: Read/Write bit information ($I^2C$ mode only)
This bit holds the R/W bit information following the last address match. This bit is only valid from the address match to the next start bit, stop bit, or not $\overline{\text{ACK}}$ bit.
In $I^2C$ slave mode:
1 = Read
0 = Write
In $I^2C$ master mode:
1 = Transmit is in progress
0 = Transmit is not in progress.
Or'ing this bit with SEN, RSEN, PEN, RCEN, or AKEN will indicate if the MSSP is in IDLE mode

bit 1: **UA**: Update Address (10-bit $I^2C$ mode only)
1 = Indicates that the user needs to update the address in the SSPADD register
0 = Address does not need to be updated

bit 0: **BF**: Buffer Full Status bit
Receive (SPI and $I^2C$ modes)
1 = Receive complete, SSPBUF is full
0 = Receive not complete, SSPBUF is empty
Transmit ($I^2C$ mode only)
1 = Data Transmit in progress (does not include the $\overline{\text{ACK}}$ and stop bits), SSPBUF is full
0 = Data Transmit complete (does not include the $\overline{\text{ACK}}$ and stop bits), SSPBUF is empty

### 8.1.5 SLAVE MODE

In slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched the interrupt flag bit SSPIF (PIR1<3>) is set.

While in slave mode the external clock is supplied by the external clock source on the SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in sleep mode, the slave can transmit/receive data. When a byte is received the device will wake-up from sleep.

### 8.1.6 SLAVE SELECT SYNCHRONIZATION

The $\overline{SS}$ pin allows a synchronous slave mode. The SPI must be in slave mode with $\overline{SS}$ pin control enabled (SSPCON<3:0> = 0100). The pin must not be driven low for the $\overline{SS}$ pin to function as an input. TRISA<5> must be set. When the $\overline{SS}$ pin is low, transmission and reception are enabled and the SDO pin is driven. When the $\overline{SS}$ pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte, and becomes a floating output. External pull-up/ pull-down resistors may be desirable, depending on the application.

| | |
|---|---|
| **Note:** | When the SPI module is in Slave Mode with $\overline{SS}$ pin control enabled, (SSPCON<3:0> = 0100) the SPI module will reset if the $\overline{SS}$ pin is set to VDD. |
| **Note:** | If the SPI is used in Slave Mode with CKE = '1', then $\overline{SS}$ pin control must be enabled. |

When the SPI module resets, the bit counter is forced to 0. This can be done by either forcing the $\overline{SS}$ pin to a high level or clearing the SSPEN bit.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function) since it cannot create a bus conflict.

**FIGURE 8-7: SLAVE SYNCHRONIZATION WAVEFORM**

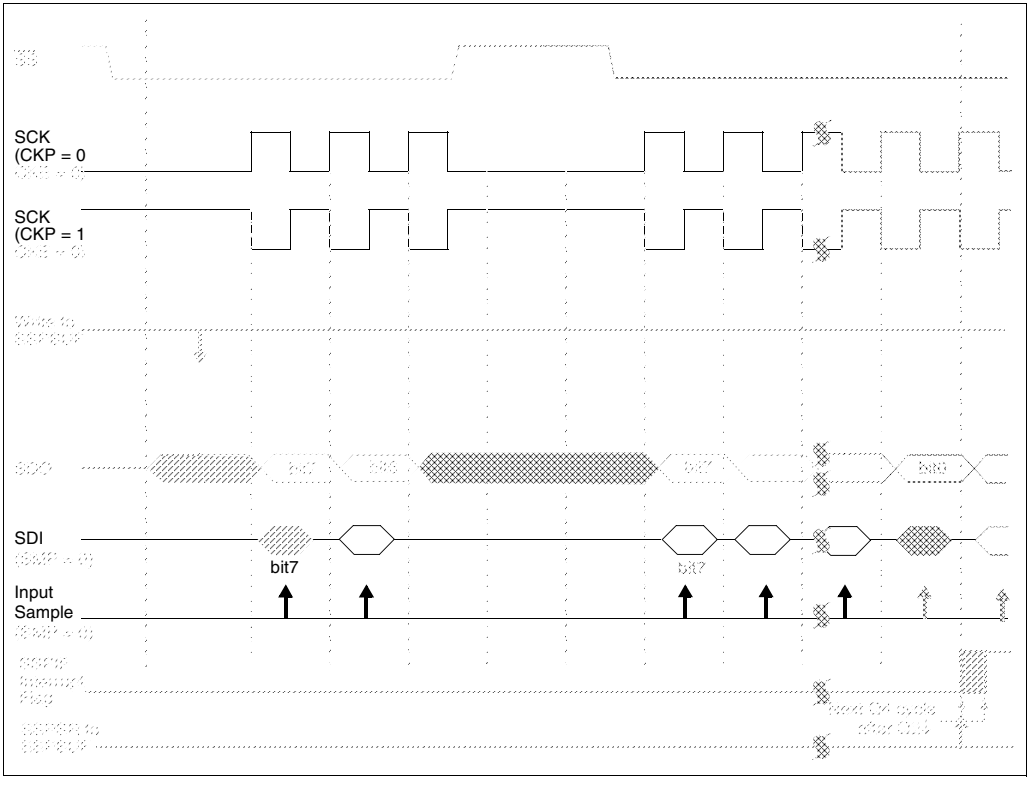
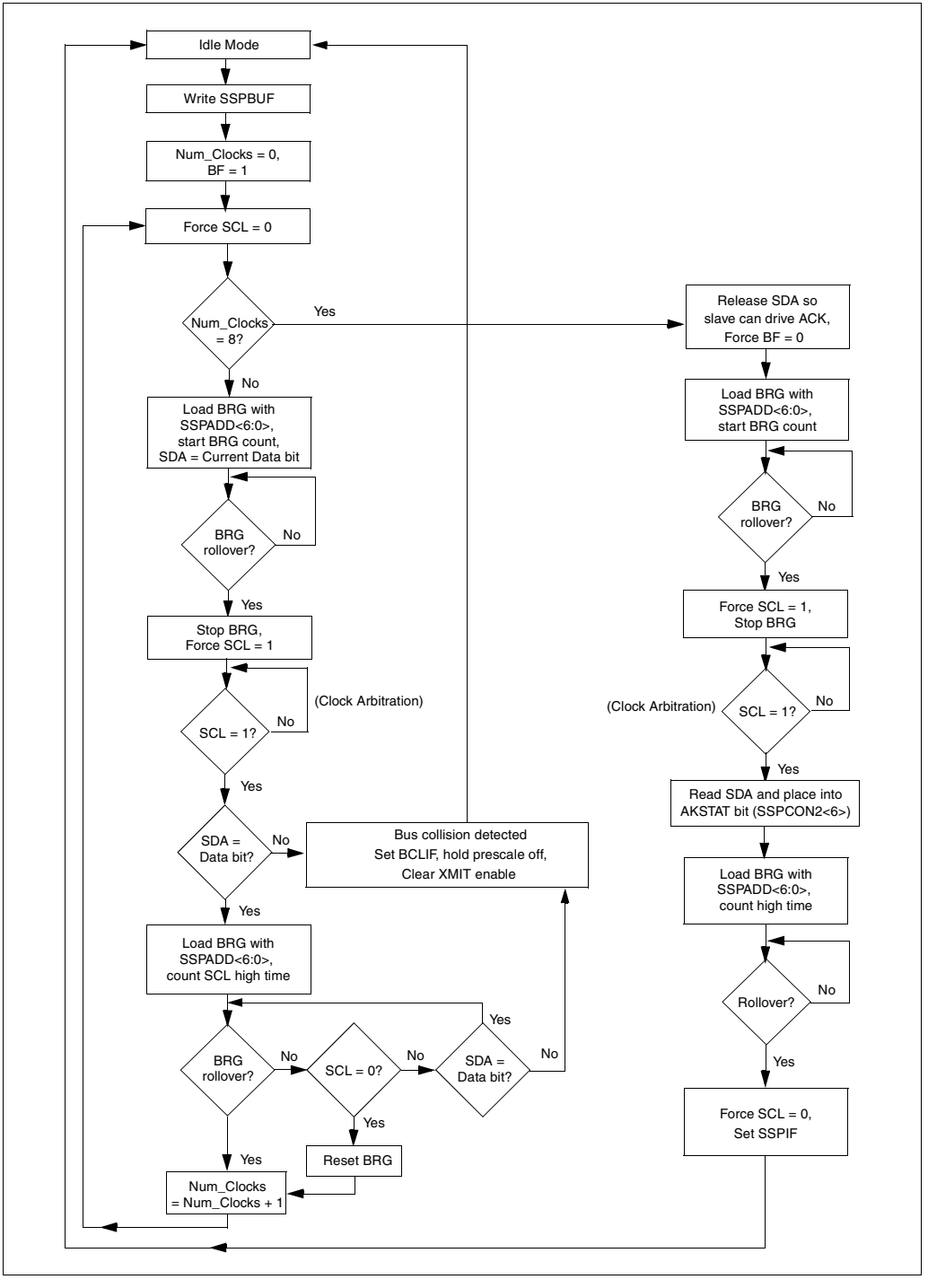


**FIGURE 8-25: MASTER TRANSMIT FLOWCHART**



### 8.2.12 I²C MASTER MODE RECEPTION

Master mode reception is enabled by programming the receive enable bit, RCEN (SSPCON2<3>).

| | |
|---|---|
| **Note:** | The SSP Module must be in an IDLE STATE before the RCEN bit is set, or the RCEN bit will be disregarded. |

The baud rate generator begins counting, and on each rollover, the state of the SCL pin changes (high to low/ low to high) and data is shifted into the SSPSR. After the falling edge of the eighth clock, the receive enable flag is automatically cleared, the contents of the SSPSR are loaded into the SSPBUF, the BF flag is set, the SSPIF is set, and the baud rate generator is suspended from counting, holding SCL low. The SSP is now in IDLE state, awaiting the next command. When the buffer is read by the CPU, the BF flag is automatically cleared. The user can then send an acknowledge bit at the end of reception, by setting the acknowledge sequence enable bit, AKEN (SSPCON2<4>).

#### 8.2.12.10 BF STATUS FLAG

In receive operation, BF is set when an address or data byte is loaded into SSPBUF from SSPSR. It is cleared when SSPBUF is read.

#### 8.2.12.11 SSPOV STATUS FLAG

In receive operation, SSPOV is set when 8 bits are received into the SSPSR, and the BF flag is already set from a previous reception.

#### 8.2.12.12 WCOL STATUS FLAG

If the user writes the SSPBUF when a receive is already in progress (i.e. SSPSR is still shifting in a data byte), then WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

## 9.0 ADDRESSABLE UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (USART)

The Universal Synchronous Asynchronous Receiver Transmitter (USART) module is one of the two serial I/O modules. (USART is also known as a Serial Communications Interface or SCI). The USART can be configured as a full duplex asynchronous system that can communicate with peripheral devices such as CRT terminals and personal computers, or it can be configured as a half duplex synchronous system that can communicate with peripheral devices such as A/D or D/A integrated circuits, Serial EEPROMs etc.

The USART can be configured in the following modes:

- Asynchronous (full duplex)
- Synchronous - Master (half duplex)
- Synchronous - Slave (half duplex)

Bit SPEN (RCSTA<7>), and bits TRISC<7:6>, have to be set in order to configure pins RC6/TX/CK and RC7/RX/DT as the Universal Synchronous Asynchronous Receiver Transmitter.

The USART module also has a multi-processor communication capability using 9-bit address detection.

**FIGURE 9-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER (ADDRESS 98h)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R-1 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CSRC | TX9 | TXEN | SYNC | — | BRGH | TRMT | TX9D |
| bit7 | | | | | | | bit0 |

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n =Value at POR reset

bit 7: **CSRC**: Clock Source Select bit

Asynchronous mode
Don't care

Synchronous mode
1 = Master mode (Clock generated internally from BRG)
0 = Slave mode (Clock from external source)

bit 6: **TX9**: 9-bit Transmit Enable bit
1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

bit 5: **TXEN**: Transmit Enable bit
1 = Transmit enabled
0 = Transmit disabled
Note: SREN/CREN overrides TXEN in SYNC mode.

bit 4: **SYNC**: USART Mode Select bit
1 = Synchronous mode
0 = Asynchronous mode

bit 3: **Unimplemented:** Read as '0'

bit 2: **BRGH**: High Baud Rate Select bit

Asynchronous mode
1 = High speed
0 = Low speed

Synchronous mode
Unused in this mode

bit 1: **TRMT**: Transmit Shift Register Status bit
1 = TSR empty
0 = TSR full

bit 0: **TX9D**: 9th bit of transmit data. Can be parity bit.

**TABLE 9-5 BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 1)**

| BAUD RATE (K) | FOSC = 20 MHz | | | 16 MHz | | | 10 MHz | | | 7.16 MHz | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | KBAUD | % ERROR | SPBRG value (decimal) | KBAUD | % ERROR | SPBRG value (decimal) | KBAUD | % ERROR | SPBRG value (decimal) | KBAUD | % ERROR | SPBRG value (decimal) |
| 9.6 | 9.615 | +0.16 | 129 | 9.615 | +0.16 | 103 | 9.615 | +0.16 | 64 | 9.520 | -0.83 | 46 |
| 19.2 | 19.230 | +0.16 | 64 | 19.230 | +0.16 | 51 | 18.939 | -1.36 | 32 | 19.454 | +1.32 | 22 |
| 38.4 | 37.878 | -1.36 | 32 | 38.461 | +0.16 | 25 | 39.062 | +1.7 | 15 | 37.286 | -2.90 | 11 |
| 57.6 | 56.818 | -1.36 | 21 | 58.823 | +2.12 | 16 | 56.818 | -1.36 | 10 | 55.930 | -2.90 | 7 |
| 115.2 | 113.636 | -1.36 | 10 | 111.111 | -3.55 | 8 | 125 | +8.51 | 4 | 111.860 | -2.90 | 3 |
| 250 | 250 | 0 | 4 | 250 | 0 | 3 | NA | - | - | NA | - | - |
| 625 | 625 | 0 | 1 | NA | - | - | 625 | 0 | 0 | NA | - | - |
| 1250 | 1250 | 0 | 0 | NA | - | - | NA | - | - | NA | - | - |

| BAUD RATE (K) | FOSC = 5.068 MHz | | | 4 MHz | | | 3.579 MHz | | | 1 MHz | | | 32.768 kHz | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | KBAUD | % ERROR | SPBRG value (decimal) | KBAUD | % ERROR | SPBRG value (decimal) | KBAUD | % ERROR | SPBRG value (decimal) | KBAUD | % ERROR | SPBRG value (decimal) | KBAUD | % ERROR | SPBRG value (decimal) |
| 9.6 | 9.6 | 0 | 32 | NA | - | - | 9.727 | +1.32 | 22 | 8.928 | -6.99 | 6 | NA | - | - |
| 19.2 | 18.645 | -2.94 | 16 | 1.202 | +0.17 | 207 | 18.643 | -2.90 | 11 | 20.833 | +8.51 | 2 | NA | - | - |
| 38.4 | 39.6 | +3.12 | 7 | 2.403 | +0.13 | 103 | 37.286 | -2.90 | 5 | 31.25 | -18.61 | 1 | NA | - | - |
| 57.6 | 52.8 | -8.33 | 5 | 9.615 | +0.16 | 25 | 55.930 | -2.90 | 3 | 62.5 | +8.51 | 0 | NA | - | - |
| 115.2 | 105.6 | -8.33 | 2 | 19.231 | +0.16 | 12 | 111.860 | -2.90 | 1 | NA | - | - | NA | - | - |
| 250 | NA | - | - | NA | - | - | 223.721 | -10.51 | 0 | NA | - | - | NA | - | - |
| 625 | NA | - | - | NA | - | - | NA | - | - | NA | - | - | NA | - | - |
| 1250 | NA | - | - | NA | - | - | NA | - | - | NA | - | - | NA | - | - |

## 9.2 USART Asynchronous Mode

In this mode, the USART uses standard nonreturn-to-zero (NRZ) format (one start bit, eight or nine data bits and one stop bit). The most common data format is 8-bits. An on-chip dedicated 8-bit baud rate generator can be used to derive standard baud rate frequencies from the oscillator. The USART transmits and receives the LSb first. The USART's transmitter and receiver are functionally independent but use the same data format and baud rate. The baud rate generator produces a clock either x16 or x64 of the bit shift rate, depending on bit BRGH (TXSTA<2>). Parity is not supported by the hardware, but can be implemented in software (and stored as the ninth data bit). Asynchronous mode is stopped during SLEEP.

Asynchronous mode is selected by clearing bit SYNC (TXSTA<4>).

The USART Asynchronous module consists of the following important elements:

- Baud Rate Generator
- Sampling Circuit
- Asynchronous Transmitter
- Asynchronous Receiver

### 9.2.1 USART ASYNCHRONOUS TRANSMITTER

The USART transmitter block diagram is shown in Figure 9-3. The heart of the transmitter is the transmit (serial) shift register (TSR). The shift register obtains its data from the read/write transmit buffer, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the STOP bit has been transmitted from the previous load. As soon as the STOP bit is transmitted, the TSR is loaded with new data from the TXREG register (if available). Once the TXREG register transfers the data to the TSR register (occurs in one TCY), the TXREG register is empty and flag bit TXIF (PIR1<4>) is set. This interrupt can be enabled/disabled by setting/clearing enable bit TXIE ( PIE1<4>). Flag bit TXIF will be set regardless of the state of enable bit TXIE and cannot be cleared in software. It will reset only when new data is loaded into the TXREG register. While flag bit TXIF indicated the status of the TXREG register, another bit TRMT (TXSTA<1>) shows the status of the TSR register. Status bit TRMT is a read only bit which is set when the TSR register is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty.

| | |
|---|---|
| **Note 1:** | The TSR register is not mapped in data memory so it is not available to the user. |
| **Note 2:** | Flag bit TXIF is set when enable bit TXEN is set. |

Steps to follow when setting up an Asynchronous Transmission:

1. Initialize the SPBRG register for the appropriate baud rate. If a high speed baud rate is desired, set bit BRGH. (Section 9.1)
2. Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
3. If interrupts are desired, then set enable bit TXIE.
4. If 9-bit transmission is desired, then set transmit bit TX9.
5. Enable the transmission by setting bit TXEN, which will also set bit TXIF.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
7. Load data to the TXREG register (starts transmission).

**FIGURE 9-3: USART TRANSMIT BLOCK DIAGRAM**

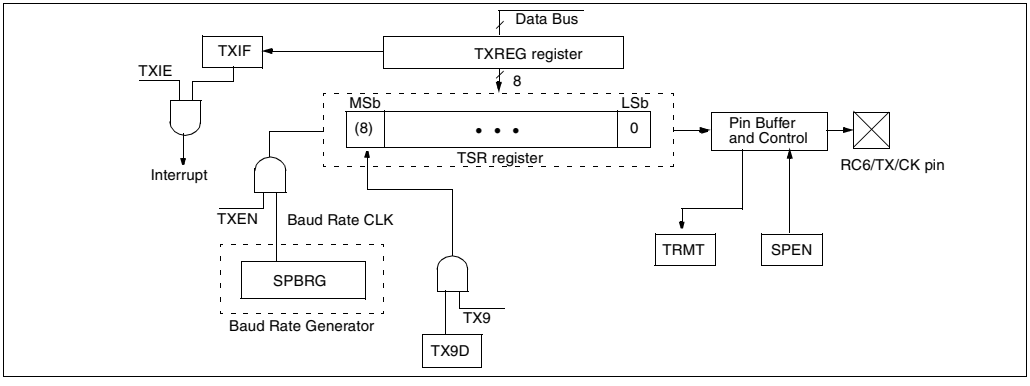


**FIGURE 9-4: ASYNCHRONOUS TRANSMISSION**

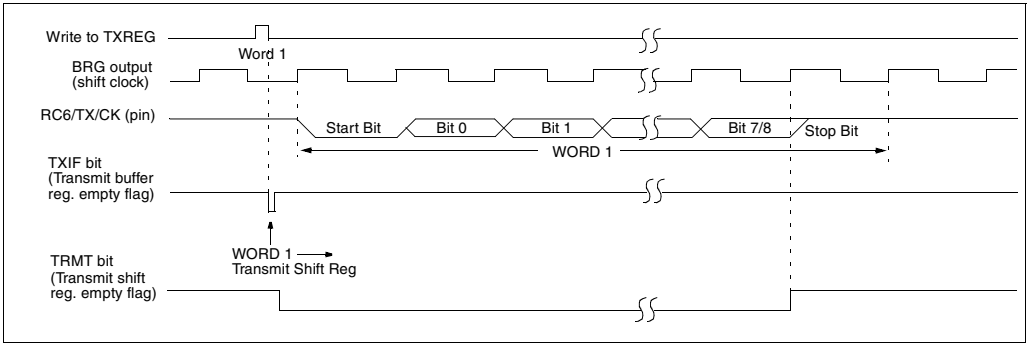
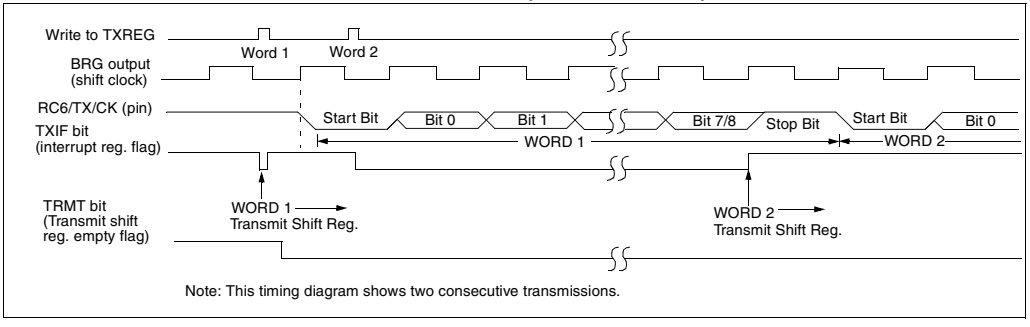



**FIGURE 9-5: ASYNCHRONOUS TRANSMISSION (BACK TO BACK)**




Note: This timing diagram shows two consecutive transmissions.

**TABLE 9-6 REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0Ch | PIR1 | PSPIF(1) | ADIF | RCIF | TXIF | SSPIF | CCP1IF | TMR2IF | TMR1IF | 0000 0000 | 0000 0000 |
| 18h | RCSTA | SPEN | RX9 | SREN | CREN | ADDEN | FERR | OERR | RX9D | 0000 000x | 0000 000x |
| 19h | TXREG | USART Transmit Register | | | | | | | | 0000 0000 | 0000 0000 |
| 8Ch | PIE1 | PSPIE(1) | ADIE | RCIE | TXIE | SSPIE | CCP1IE | TMR2IE | TMR1IE | 0000 0000 | 0000 0000 |
| 98h | TXSTA | CSRC | TX9 | TXEN | SYNC | — | BRGH | TRMT | TX9D | 0000 -010 | 0000 -010 |
| 99h | SPBRG | Baud Rate Generator Register | | | | | | | | 0000 0000 | 0000 0000 |

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Asynchronous Transmission.
Note 1: Bits PSPIE and PSPIF are reserved on the 28-pin devices, always maintain these bits clear.

## 9.3 USART Synchronous Master Mode

In Synchronous Master mode, the data is transmitted in a half-duplex manner i.e. transmission and reception do not occur at the same time. When transmitting data, the reception is inhibited and vice versa. Synchronous mode is entered by setting bit SYNC (TXSTA<4>). In addition enable bit SPEN (RCSTA<7>) is set in order to configure the RC6/TX/CK and RC7/RX/DT I/O pins to CK (clock) and DT (data) lines respectively. The Master mode indicates that the processor transmits the master clock on the CK line. The Master mode is entered by setting bit CSRC (TXSTA<7>).

### 9.3.1 USART SYNCHRONOUS MASTER TRANSMISSION

The USART transmitter block diagram is shown in Figure 9-3. The heart of the transmitter is the transmit (serial) shift register (TSR). The shift register obtains its data from the read/write transmit buffer register TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR is loaded with new data from the TXREG (if available). Once the TXREG register transfers the data to the TSR register (occurs in one Tcycle), the TXREG is empty and interrupt bit, TXIF (PIR1<4>) is set. The interrupt can be enabled/disabled by setting/clearing enable bit TXIE (PIE1<4>). Flag bit TXIF will be set regardless of the state of enable bit TXIE and cannot be cleared in software. It will reset only when new data is loaded into the TXREG register. While flag bit TXIF indicates the status of the TXREG register, another bit TRMT (TXSTA<1>) shows the status of the TSR register. TRMT is a read only bit which is set when the TSR is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty. The TSR is not mapped in data memory so it is not available to the user.

Steps to follow when setting up a Synchronous Master Transmission:

1. Initialize the SPBRG register for the appropriate baud rate (Section 9.1).
2. Enable the synchronous master serial port by setting bits SYNC, SPEN, and CSRC.
3. If interrupts are desired, then set enable bit TXIE.
4. If 9-bit transmission is desired, then set bit TX9.
5. Enable the transmission by setting bit TXEN.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
7. Start transmission by loading data to the TXREG register.

**TABLE 9-8 REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0Ch | PIR1 | PSPIF(1) | ADIF | RCIF | TXIF | SSPIF | CCP1IF | TMR2IF | TMR1IF | 0000 0000 | 0000 0000 |
| 18h | RCSTA | SPEN | RX9 | SREN | CREN | ADDEN | FERR | OERR | RX9D | 0000 000x | 0000 000x |
| 19h | TXREG | USART Transmit Register | | | | | | | | 0000 0000 | 0000 0000 |
| 8Ch | PIE1 | PSPIE(1) | ADIE | RCIE | TXIE | SSPIE | CCP1IE | TMR2IE | TMR1IE | 0000 0000 | 0000 0000 |
| 98h | TXSTA | CSRC | TX9 | TXEN | SYNC | — | BRGH | TRMT | TX9D | 0000 -010 | 0000 -010 |
| 99h | SPBRG | Baud Rate Generator Register | | | | | | | | 0000 0000 | 0000 0000 |

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used for Synchronous Master Transmission.
Note 1: Bits PSPIE and PSPIF are reserved on the 28-pin devices, always maintain these bits clear.

**TABLE 9-10 REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0Ch | PIR1 | PSPIF(1) | ADIF | RCIF | TXIF | SSPIF | CCP1IF | TMR2IF | TMR1IF | 0000 0000 | 0000 0000 |
| 18h | RCSTA | SPEN | RX9 | SREN | CREN | ADDEN | FERR | OERR | RX9D | 0000 000x | 0000 000x |
| 19h | TXREG | USART Transmit Register | | | | | | | | 0000 0000 | 0000 0000 |
| 8Ch | PIE1 | PSPIE(1) | ADIE | RCIE | TXIE | SSPIE | CCP1IE | TMR2IE | TMR1IE | 0000 0000 | 0000 0000 |
| 98h | TXSTA | CSRC | TX9 | TXEN | SYNC | — | BRGH | TRMT | TX9D | 0000 -010 | 0000 -010 |
| 99h | SPBRG | Baud Rate Generator Register | | | | | | | | 0000 0000 | 0000 0000 |

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for Synchronous Slave Transmission.
Note 1: Bits PSPIE and PSPIF are reserved on the 28-pin devices, always maintain these bits clear.

**TABLE 9-11 REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0Ch | PIR1 | PSPIF(1) | ADIF | RCIF | TXIF | SSPIF | CCP1IF | TMR2IF | TMR1IF | 0000 0000 | 0000 0000 |
| 18h | RCSTA | SPEN | RX9 | SREN | CREN | ADDEN | FERR | OERR | RX9D | 0000 000x | 0000 000x |
| 1Ah | RCREG | USART Receive Register | | | | | | | | 0000 0000 | 0000 0000 |
| 8Ch | PIE1 | PSPIE(1) | ADIE | RCIE | TXIE | SSPIE | CCP1IE | TMR2IE | TMR1IE | 0000 0000 | 0000 0000 |
| 98h | TXSTA | CSRC | TX9 | TXEN | SYNC | — | BRGH | TRMT | TX9D | 0000 -010 | 0000 -010 |
| 99h | SPBRG | Baud Rate Generator Register | | | | | | | | 0000 0000 | 0000 0000 |

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for Synchronous Slave Reception.
Note 1: Bits PSPIE and PSPIF are reserved on the 28-pin devices, always maintain these bits clear.

**TABLE 12-6 INITIALIZATION CONDITIONS FOR ALL REGISTERS (Cont.'d)**

| Register | Devices | | Power-on Reset, Brown-out Reset | MCLR Resets WDT Reset | Wake-up via WDT or Interrupt |
|---|---|---|---|---|---|
| TRISA | 773 | 774 | ---1 1111 | ---1 1111 | ---u uuuu |
| | 773 | 774 | --11 1111 | --11 1111 | --uu uuuu |
| TRISB | 773 | 774 | 1111 1111 | 1111 1111 | uuuu uuuu |
| TRISC | 773 | 774 | 1111 1111 | 1111 1111 | uuuu uuuu |
| TRISD | 773 | 774 | 1111 1111 | 1111 1111 | uuuu uuuu |
| TRISE | 773 | 774 | 0000 -111 | 0000 -111 | uuuu -uuu |
| PIE1 | 773 | 774 | r000 0000 | r000 0000 | ruuu uuuu |
| | 773 | 774 | 0000 0000 | 0000 0000 | uuuu uuuu |
| PIE2 | 773 | 774 | 0--- 0--0 | 0--- 0--0 | u--- u--u |
| PCON | 773 | 774 | ---- --qq | ---- --uu | ---- --uu |
| PR2 | 773 | 774 | 1111 1111 | 1111 1111 | 1111 1111 |
| SSPADD | 773 | 774 | 0000 0000 | 0000 0000 | uuuu uuuu |
| SSPSTAT | 773 | 774 | 0000 0000 | 0000 0000 | uuuu uuuu |
| TXSTA | 773 | 774 | 0000 -010 | 0000 -010 | uuuu -uuu |
| SPBRG | 773 | 774 | 0000 0000 | 0000 0000 | uuuu uuuu |
| REFCON | 773 | 774 | 0000 ---- | 0000 ---- | uuuu ---- |
| LVDCON | 773 | 774 | --00 0101 | --00 0101 | --uu uuuu |
| ADRESL | 773 | 774 | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| ADCON1 | 773 | 774 | 0000 000 | 0000 0000 | uuuu uuuu |

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

Note 1: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 12-5 for reset value for specific condition.

**FIGURE 12-7: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD)**

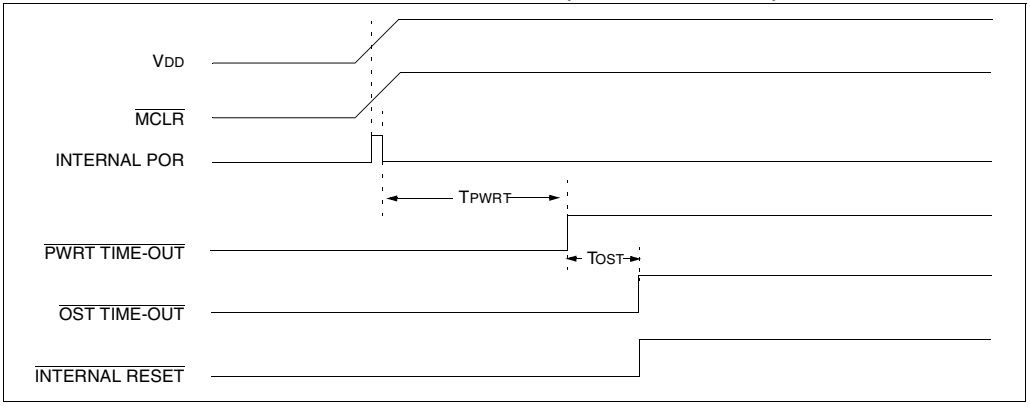
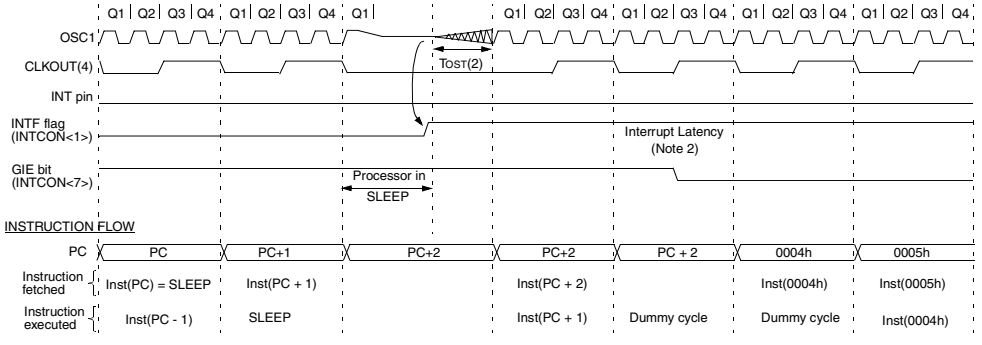


**FIGURE 12-14: WAKE-UP FROM SLEEP THROUGH INTERRUPT**




Note 1: XT, HS or LP oscillator mode assumed.
2: TOST = 1024TOSC (drawing not to scale) This delay will not be there for RC osc mode.
3: GIE = '1' assumed. In this case after wake- up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.
4: CLKOUT is not available in these osc modes, but shown here for timing reference.

## 12.14 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

| **Note:** | Microchip does not recommend code protecting windowed devices. |
|---|---|

## 12.15 ID Locations

Four memory locations (2000h - 2003h) are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify. It is recommended that only the 4 least significant bits of the ID location are used.

For ROM devices, these values are submitted along with the ROM code.

## 12.16 In-Circuit Serial Programming

PIC16CXXX microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

For complete details of serial programming, please refer to the In-Circuit Serial Programming (ICSP™) Guide, (DS30277).

## 13.0 INSTRUCTION SET SUMMARY

Each PIC16CXXX instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16CXX instruction set summary in Table 13-2 lists **byte-oriented**, **bit-oriented**, and **literal and control** operations. Table 13-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an eight or eleven bit constant or literal value.

**TABLE 13-1 OPCODE FIELD DESCRIPTIONS**

| Field | Description |
|---|---|
| f | Register file address (0x00 to 0x7F) |
| W | Working register (accumulator) |
| b | Bit address within an 8-bit file register |
| k | Literal field, constant data or label |
| x | Don't care location (= 0 or 1)<br>The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools. |
| d | Destination select; d = 0: store result in W,<br>d = 1: store result in file register f.<br>Default is d = 1 |
| PC | Program Counter |
| $\overline{TO}$ | Time-out bit |
| $\overline{PD}$ | Power-down bit |

The instruction set is highly orthogonal and is grouped into three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs.

Table 13-2 lists the instructions recognized by the MPASM assembler.

Figure 13-1 shows the general formats that the instructions can have.

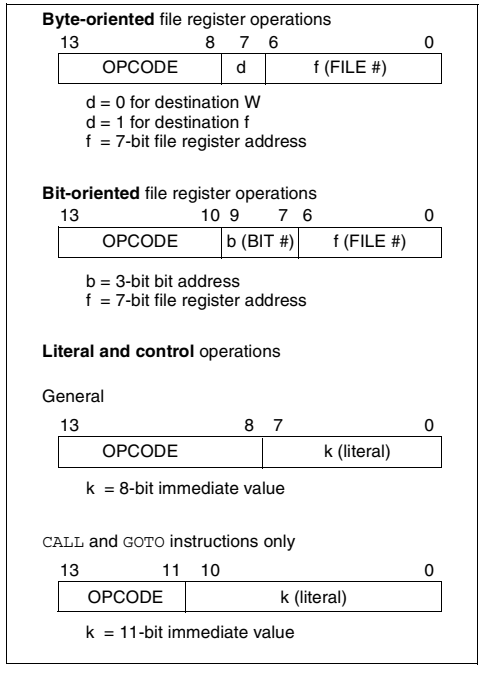
**Note:** To maintain upward compatibility with future PIC16CXXX products, do not use the OPTION and TRIS instructions.

All examples use the following format to represent a hexadecimal number:

0xhh

where h signifies a hexadecimal digit.

**FIGURE 13-1: GENERAL FORMAT FOR INSTRUCTIONS**




A description of each instruction is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

**FIGURE 15-1: LOW-VOLTAGE DETECT CHARACTERISTICS**

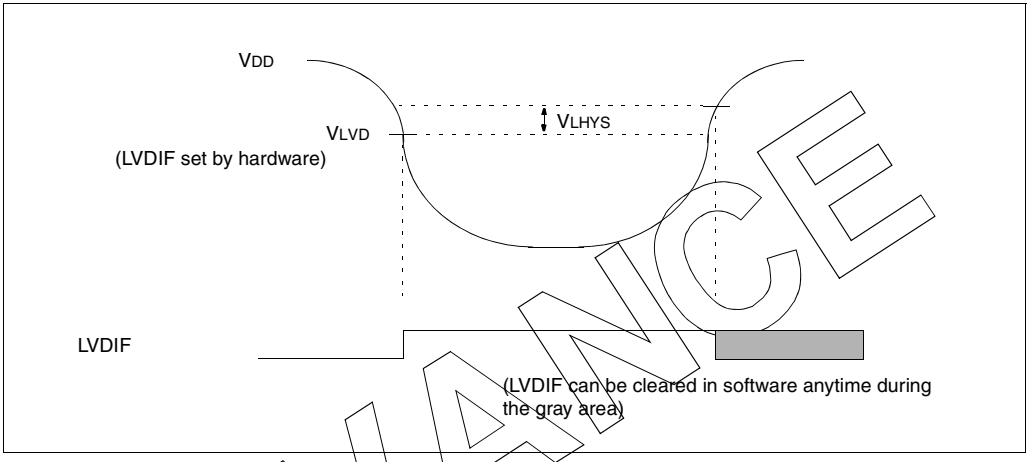




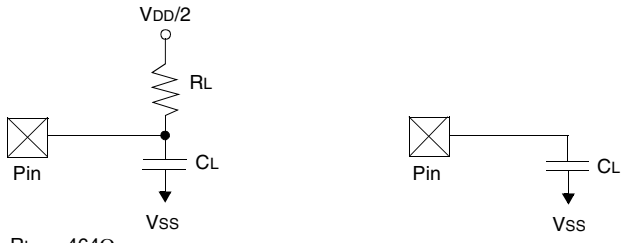

**TABLE 15-3 ELECTRICAL CHARACTERISTICS: LVD**

| DC CHARACTERISTICS | | | | **Standard Operating Conditions (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for industrial and<br>0°C ≤ TA ≤ +70°C for commercial<br>Operating voltage VDD range as described in DC spec Section 15.1 and Section 15.2. | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | | **Symbol** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D420 | LVD Voltage | LVV = 0100 | | 2.5 | 2.58 | 2.66 | V | |
| | | LVV = 0101 | | 2.7 | 2.78 | 2.86 | V | |
| | | LVV = 0110 | | 2.8 | 2.89 | 2.98 | V | |
| | | LVV = 0111 | | 3.0 | 3.1 | 3.2 | V | |
| | | LVV = 1000 | | 3.3 | 3.41 | 3.52 | V | |
| | | LVV = 1001 | | 3.5 | 3.61 | 3.72 | V | |
| | | LVV = 1010 | | 3.6 | 3.72 | 3.84 | V | |
| | | LVV = 1011 | | 3.8 | 3.92 | 4.04 | V | |
| | | LVV = 1100 | | 4.0 | 4.13 | 4.26 | V | |
| | | LVV = 1101 | | 4.2 | 4.33 | 4.46 | V | |
| | | LVV = 1110 | | 4.5 | 4.64 | 4.78 | V | |
| D421 | Supply Current | | ΔILVD | — | 10 | 20 | μA | |
| D422* | LVD Voltage Drift Temperature coefficient | | TCVOUT | — | 15 | 50 | ppm/°C | |
| D423* | LVD Voltage Drift with respect to VDD Regulation | | ΔVLVD/ ΔVDD | — | — | 50 | μV/V | |
| D424* | Low-voltage Detect Hysteresis | | VLHYS | TBD | — | 100 | mV | |

* These parameters are characterized but not tested.

**Note 1:** Production tested at Tamb = 25°C. Specifications over temp limits ensured by characterization.

**FIGURE 15-3: LOAD CONDITIONS**




$R_L$ = 464Ω

$C_L$ = 50 pF for all pins except OSC2, but including PORTD and PORTE outputs as ports

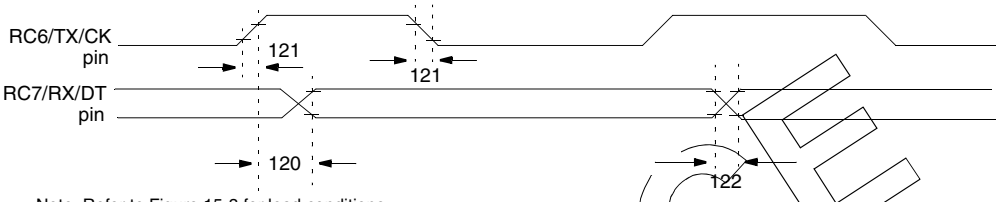
15 pF for OSC2 output

Note: PORTD and PORTE are not implemented on the PIC16C773.



**FIGURE 15-14: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING**




Note: Refer to Figure 15-3 for load conditions.

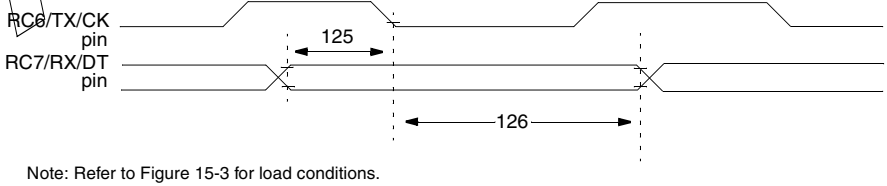
**TABLE 15-15 USART SYNCHRONOUS TRANSMISSION REQUIREMENTS**

| Param No. | Sym | Characteristic | | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| 120* | TckH2dtV | SYNC XMIT (MASTER & SLAVE) Clock high to data out valid | PIC16**C**774/773 | — | — | 80 | ns | |
| | | | PIC16**LC**774/773 | — | — | 100 | ns | |
| 121* | Tckrf | Clock out rise time and fall time (Master Mode) | PIC16**C**774/773 | — | — | 45 | ns | |
| | | | PIC16**LC**774/773 | — | — | 50 | ns | |
| 122* | Tdtrf | Data out rise time and fall time | PIC16**C**774/773 | — | — | 45 | ns | |
| | | | PIC16**LC**774/773 | — | — | 50 | ns | |

* These parameters are characterized but not tested.

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 15-15: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING**




Note: Refer to Figure 15-3 for load conditions.

**TABLE 15-16 USART SYNCHRONOUS RECEIVE REQUIREMENTS**

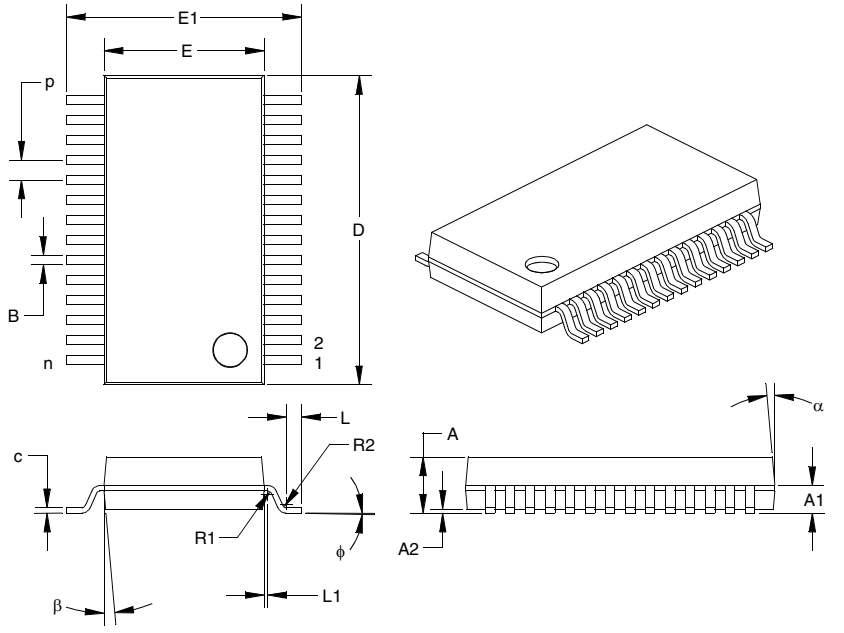
| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 125* | TdtV2ckL | SYNC RCV (MASTER & SLAVE) Data setup before CK ↓ (DT setup time) | 15 | — | — | ns | |
| 126* | TckL2dtl | Data hold after CK ↓ (DT hold time) | 15 | — | — | ns | |

* These parameters are characterized but not tested.

†: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

### 17.5 K04-073 28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | | MILLIMETERS* | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Pitch | p | | 0.026 | | | 0.65 | |
| Number of Pins | n | | 28 | | | 28 | |
| Overall Pack. Height | A | 0.068 | 0.073 | 0.078 | 1.73 | 1.86 | 1.99 |
| Shoulder Height | A1 | 0.026 | 0.036 | 0.046 | 0.66 | 0.91 | 1.17 |
| Standoff | A2 | 0.002 | 0.005 | 0.008 | 0.05 | 0.13 | 0.21 |
| Molded Package Length | D‡ | 0.396 | 0.402 | 0.407 | 10.07 | 10.20 | 10.33 |
| Molded Package Width | E‡ | 0.205 | 0.208 | 0.212 | 5.20 | 5.29 | 5.38 |
| Outside Dimension | E1 | 0.301 | 0.306 | 0.311 | 7.65 | 7.78 | 7.90 |
| Shoulder Radius | R1 | 0.005 | 0.005 | 0.010 | 0.13 | 0.13 | 0.25 |
| Gull Wing Radius | R2 | 0.005 | 0.005 | 0.010 | 0.13 | 0.13 | 0.25 |
| Foot Length | L | 0.015 | 0.020 | 0.025 | 0.38 | 0.51 | 0.64 |
| Foot Angle | ϕ | 0 | 4 | 8 | 0 | 4 | 8 |
| Radius Centerline | L1 | 0.000 | 0.005 | 0.010 | 0.00 | 0.13 | 0.25 |
| Lead Thickness | c | 0.005 | 0.007 | 0.009 | 0.13 | 0.18 | 0.22 |
| Lower Lead Width | B† | 0.010 | 0.012 | 0.015 | 0.25 | 0.32 | 0.38 |
| Mold Draft Angle Top | α | 0 | 5 | 10 | 0 | 5 | 10 |
| Mold Draft Angle Bottom | β | 0 | 5 | 10 | 0 | 5 | 10 |

* Controlling Parameter.

† Dimension “B” does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003” (0.076 mm) per side or 0.006” (0.152 mm) more than dimension “B.”

‡ Dimensions “D” and “E” do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010” (0.254 mm) per side or 0.020” (0.508 mm) more than dimensions “D” or “E.”

**NOTES:**

**E**

Errata ..... 4
External Power-on Reset Circuit ..... 132

**F**

Firmware Instructions ..... 143
Flowcharts
- Acknowledge ..... 86
- Master Receiver ..... 83
- Master Transmit ..... 80
- Restart Condition ..... 77
- Start Condition ..... 75
- Stop Condition ..... 88

FSR Register ..... 13, 14, 15
Fuzzy Logic Dev. System (*fuzzy*TECH®-MP) ..... 147

**G**

GCE ..... 56
General Call Address Sequence ..... 69
General Call Address Support ..... 69
General Call Enable bit, GCE ..... 56

**I**

I/O Ports ..... 27
$I^2C$ ..... 63
$I^2C$ Master Mode Receiver Flowchart ..... 83
$I^2C$ Master Mode Reception ..... 82
$I^2C$ Master Mode Restart Condition ..... 76
$I^2C$ Mode Selection ..... 63
$I^2C$ Module
- Acknowledge Flowchart ..... 86
- Acknowledge Sequence timing ..... 85
- Addressing ..... 64
- Baud Rate Generator ..... 73
- Block Diagram ..... 71
- BRG Block Diagram ..... 73
- BRG Reset due to SDA Collision ..... 92
- BRG Timing ..... 73
- Bus Arbitration ..... 90
- Bus Collision ..... 90
  - Acknowledge ..... 90
  - Restart Condition ..... 93
  - Restart Condition Timing (Case1) ..... 93
  - Restart Condition Timing (Case2) ..... 93
  - Start Condition ..... 91
  - Start Condition Timing ..... 91, 92
  - Stop Condition ..... 94
  - Stop Condition Timing (Case1) ..... 94
  - Stop Condition Timing (Case2) ..... 94
  - Transmit Timing ..... 90
- Bus Collision timing ..... 90
- Clock Arbitration ..... 89
- Clock Arbitration Timing (Master Transmit) ..... 89
- Conditions to not give $\overline{ACK}$ Pulse ..... 64
- General Call Address Support ..... 69
- Master Mode ..... 71
- Master Mode 7-bit Reception timing ..... 84
- Master Mode Operation ..... 72
- Master Mode Start Condition ..... 74
- Master Mode Transmission ..... 79
- Master Mode Transmit Sequence ..... 72
- Master Transmit Flowchart ..... 80
- Multi-Master Communication ..... 90
- Multi-master Mode ..... 72
- Operation ..... 63
- Repeat Start Condition timing ..... 76
- Restart Condition Flowchart ..... 77
- Slave Mode ..... 64
- Slave Reception ..... 65
- Slave Transmission ..... 65
- SSPBUF ..... 64
- Start Condition Flowchart ..... 75
- Stop Condition Flowchart ..... 88
- Stop Condition Receive or Transmit timing ..... 87
- Stop Condition timing ..... 87
- Waveforms for 7-bit Reception ..... 65
- Waveforms for 7-bit Transmission ..... 66

$I^2C$ Module Address Register, SSPADD ..... 64
$I^2C$ Slave Mode ..... 64
ICEPIC Low-Cost PIC16CXXX In-Circuit Emulator ..... 145
ID Locations ..... 127, 141
In-Circuit Serial Programming (ICSP) ..... 127, 141
INDF ..... 15
INDF Register ..... 13, 14
Indirect Addressing ..... 25
- FSR Register ..... 11

Instruction Format ..... 143
Instruction Set ..... 143
- Summary Table ..... 144

INTCON ..... 15
INTCON Register ..... 18
- GIE Bit ..... 18
- INTE Bit ..... 18
- INTF Bit ..... 18
- PEIE Bit ..... 18
- RBIE Bit ..... 18
- RBIF Bit ..... 18, 30
- T0IE Bit ..... 18
- T0IF Bit ..... 18

Inter-Integrated Circuit ($I^2C$) ..... 53
internal sampling switch (Rss) impedence ..... 123
Interrupt Sources ..... 127, 137
- Block Diagram ..... 137
- Capture Complete (CCP) ..... 48
- Compare Complete (CCP) ..... 49
- Interrupt on Change (RB7:RB4 ) ..... 30
- RB0/INT Pin, External ..... 7, 8, 138
- TMR0 Overflow ..... 40, 138
- TMR1 Overflow ..... 41, 43
- TMR2 to PR2 Match ..... 46
- TMR2 to PR2 Match (PWM) ..... 45, 50
- USART Receive/Transmit Complete ..... 97

Interrupts, Context Saving During ..... 138
Interrupts, Enable Bits
- A/D Converter Enable (ADIE Bit) ..... 19
- CCP1 Enable (CCP1IE Bit) ..... 19, 48
- CCP2 Enable (CCP2IE Bit) ..... 21
- Global Interrupt Enable (GIE Bit) ..... 18, 137
- Interrupt on Change (RB7:RB4) Enable (RBIE Bit) ..... 18, 138
- Peripheral Interrupt Enable (PEIE Bit) ..... 18
- PSP Read/Write Enable (PSPIE Bit) ..... 19
- RB0/INT Enable (INTE Bit) ..... 18
- SSP Enable (SSPIE Bit) ..... 19
- TMR0 Overflow Enable (T0IE Bit) ..... 18
- TMR1 Overflow Enable (TMR1IE Bit) ..... 19
- TMR2 to PR2 Match Enable (TMR2IE Bit) ..... 19
- USART Receive Enable (RCIE Bit) ..... 19
- USART Transmit Enable (TXIE Bit) ..... 19