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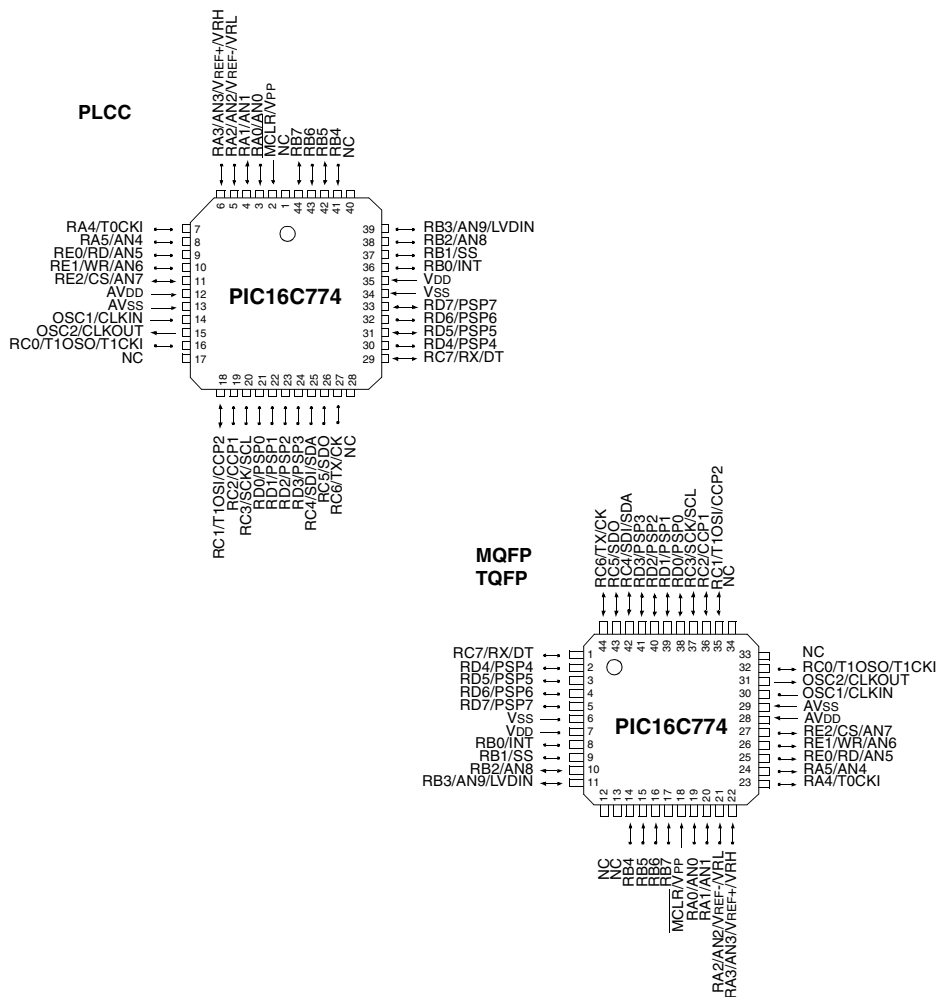
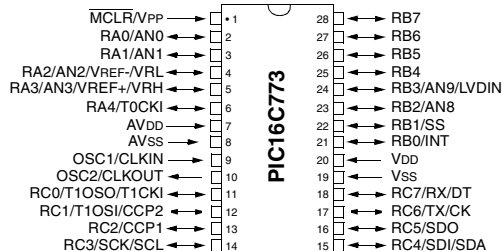
Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 6x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc773-i-so

PIC16C77X

Pin Diagrams

300 mil. SDIP, SOIC, Windowed Cerdip, SSOP



PIC16C77X

FIGURE 1-2: PIC16C77A BLOCK DIAGRAM

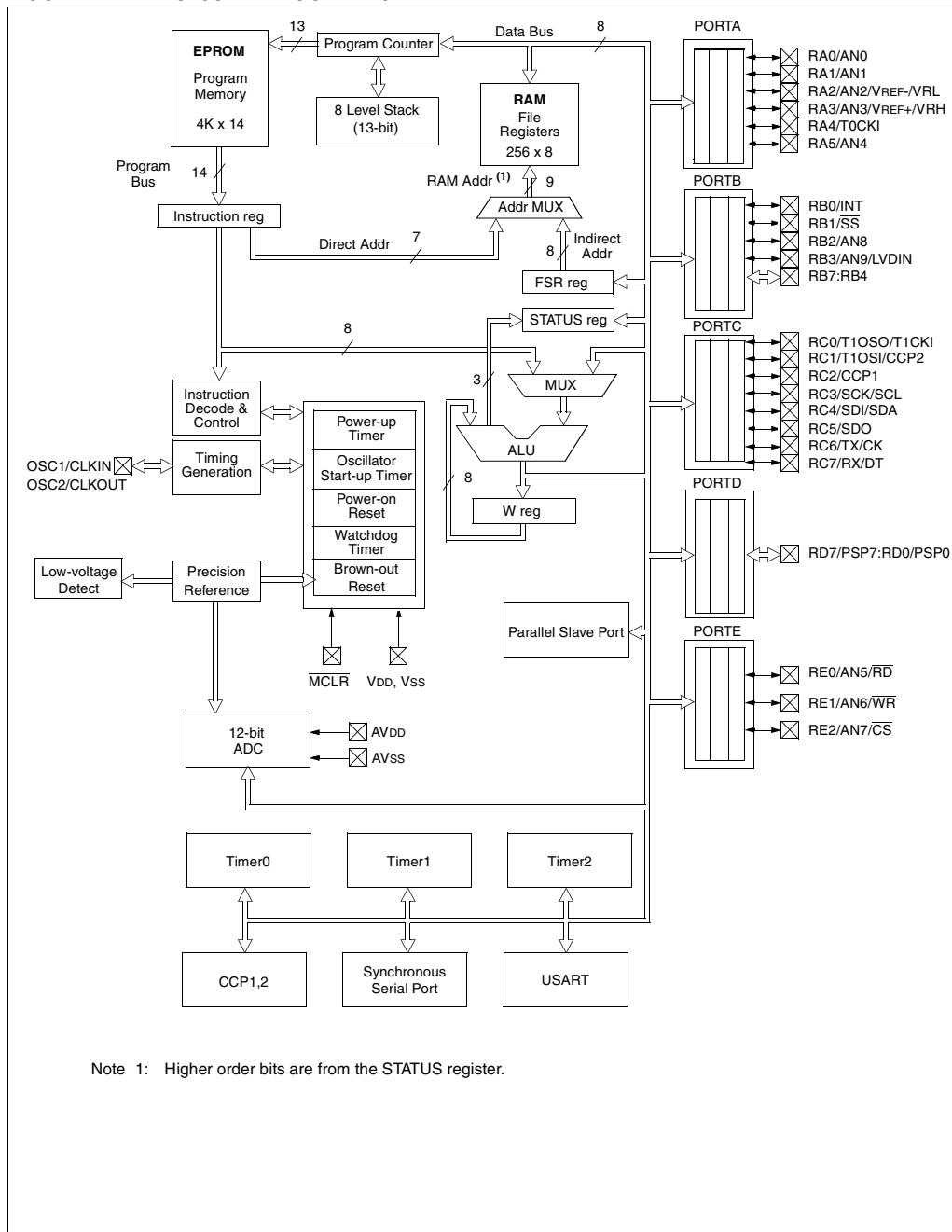


TABLE 1-2 PIC16C774 PINOUT DESCRIPTION (Cont.'d)

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
RC0/T1OSO/T1CKI	15	16	32	I/O	ST	<p>PORTC is a bi-directional I/O port.</p> <p>RC0 can also be the Timer1 oscillator output or a Timer1 clock input.</p> <p>RC1 can also be the Timer1 oscillator input or Capture2 input/Compare2 output/PWM2 output.</p> <p>RC2 can also be the Capture1 input/Compare1 output/PWM1 output.</p> <p>RC3 can also be the synchronous serial clock input/output for both SPI and I²C modes.</p> <p>RC4 can also be the SPI Data In (SPI mode) or data I/O (I²C mode).</p> <p>RC5 can also be the SPI Data Out (SPI mode).</p> <p>RC6 can also be the USART Asynchronous Transmit or Synchronous Clock.</p> <p>RC7 can also be the USART Asynchronous Receive or Synchronous Data.</p>
RC1/T1OSI/CCP2	16	18	35	I/O	ST	
RC2/CCP1	17	19	36	I/O	ST	
RC3/SCK/SCL	18	20	37	I/O	ST	
RC4/SDI/SDA	23	25	42	I/O	ST	
RC5/SDO	24	26	43	I/O	ST	
RC6/TX/CK	25	27	44	I/O	ST	
RC7/RX/DT	26	29	1	I/O	ST	
RD0/PSP0	19	21	38	I/O	ST/TTL ⁽³⁾	<p>PORTD is a bi-directional I/O port or parallel slave port when interfacing to a microprocessor bus.</p>
RD1/PSP1	20	22	39	I/O	ST/TTL ⁽³⁾	
RD2/PSP2	21	23	40	I/O	ST/TTL ⁽³⁾	
RD3/PSP3	22	24	41	I/O	ST/TTL ⁽³⁾	
RD4/PSP4	27	30	2	I/O	ST/TTL ⁽³⁾	
RD5/PSP5	28	31	3	I/O	ST/TTL ⁽³⁾	
RD6/PSP6	29	32	4	I/O	ST/TTL ⁽³⁾	
RD7/PSP7	30	33	5	I/O	ST/TTL ⁽³⁾	
RE0/RD [−] /AN5	8	9	25	I/O	ST/TTL ⁽³⁾	<p>PORTE is a bi-directional I/O port.</p> <p>RE0 can also be read control for the parallel slave port, or analog input5.</p> <p>RE1 can also be write control for the parallel slave port, or analog input6.</p> <p>RE2 can also be select control for the parallel slave port, or analog input7.</p>
RE1/WR [−] /AN6	9	10	26	I/O	ST/TTL ⁽³⁾	
RE2/CS [−] /AN7	10	11	27	I/O	ST/TTL ⁽³⁾	
AVss	12	13	29	P		Ground reference for A/D converter
AVDD	11	12	28	P		Positive supply for A/D converter
Vss	31	34	6	P	—	Ground reference for logic and I/O pins.
VDD	32	35	7	P	—	Positive supply for logic and I/O pins.
NC	—	1,17,28,40	12,13,33,34		—	These pins are not internally connected. These pins should be left unconnected.

Legend: I = input O = output I/O = input/output P = power
 — = Not used TTL = TTL input ST = Schmitt Trigger input

- Note 1: This buffer is a Schmitt Trigger input when configured for the multiplexed function.
 2: This buffer is a Schmitt Trigger input when used in serial programming mode.
 3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).
 4: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

2.2.2.6 PIE2 REGISTER

This register contains the individual enable bits for the CCP2, SSP bus collision, and low voltage detect interrupts.

FIGURE 2-8: PIE2 REGISTER (ADDRESS 8Dh)

R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	R/W-0
LVDIE	—	—	—	BCLIE	—	—	CCP2IE
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7 **LVDIE:** Low-voltage Detect Interrupt Enable bit
1 = LVD Interrupt is enabled
0 = LVD Interrupt is disabled

bit 6-4: **Unimplemented:** Read as '0'

bit 3: **BCLIE:** Bus Collision Interrupt Enable bit
1 = Bus Collision interrupt is enabled
0 = Bus Collision interrupt is disabled

bit 2-1: **Unimplemented:** Read as '0'

bit 0: **CCP2IE:** CCP2 Interrupt Enable bit
1 = Enables the CCP2 interrupt
0 = Disables the CCP2 interrupt

2.3 PCL and PCLATH

The program counter (PC) specifies the address of the instruction to fetch for execution. The PC is 13 bits wide. The low byte is called the PCL register. This register is readable and writable. The high byte is called the PCH register. This register contains the PC<12:8> bits and is not directly readable or writable. All updates to the PCH register go through the PCLATH register.

2.3.1 STACK

The stack allows a combination of up to 8 program calls and interrupts to occur. The stack contains the return address from this branch in program execution.

Midrange devices have an 8 level deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not modified when the stack is PUSHed or POPed.

After the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

2.4 Program Memory Paging

PIC16C77X devices are capable of addressing a continuous 8K word block of program memory. The CALL and GOTO instructions provide only 11 bits of address to allow branching within any 2K program memory page. When doing a CALL or GOTO instruction the upper 2 bits of the address are provided by PCLATH<4:3>. When doing a CALL or GOTO instruction, the user must ensure that the page select bits are programmed so that the desired program memory page is addressed. If a return from a CALL instruction (or interrupt) is executed, the entire 13-bit PC is pushed onto the stack. Therefore, manipulation of the PCLATH<4:3> bits are not required for the return instructions (which POPs the address from the stack).

3.5 PORTE and TRISE Register

This section is applicable to the 40/44-pin devices only.

PORTE has three pins RE0/RD/AN5, RE1/WR/AN6 and RE2/CS/AN7, which are individually configurable as inputs or outputs. These pins have Schmitt Trigger input buffers.

I/O PORTE becomes control inputs for the microprocessor port when bit PSPMODE (TRISE<4>) is set. In this mode, the user must make sure that the TRISE<2:0> bits are set (pins are configured as digital inputs). Ensure ADCON1 is configured for digital I/O. In this mode the input buffers are TTL.

Figure 3-12 shows the TRISE register, which also controls the parallel slave port operation.

PORTE pins are multiplexed with analog inputs. When selected as an analog input, these pins will read as '0's.

TRISE controls the direction of the RE pins, even when they are being used as analog inputs. The user must make sure to keep the pins configured as inputs when using them as analog inputs.

Note: On a Power-on Reset these pins are configured as analog inputs.

FIGURE 3-11: PORTE BLOCK DIAGRAM (IN I/O PORT MODE)

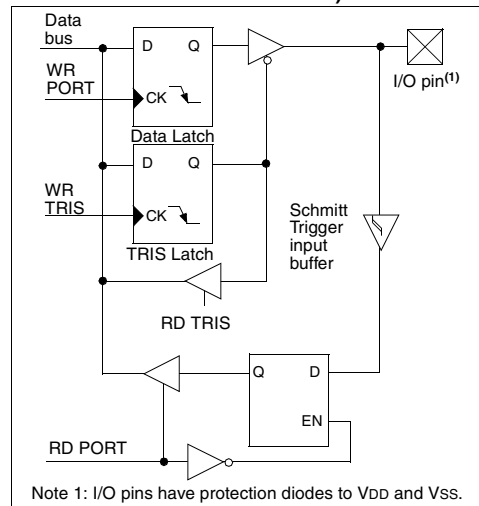


FIGURE 3-12: TRISE REGISTER (ADDRESS 89h)

R-0	R-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1
IBF	OBF	IBOV	PSPMODE	—	bit2	bit1	bit0
bit7							bit0
<p>bit 7 : IBF: Input Buffer Full Status bit 1 = A word has been received and is waiting to be read by the CPU 0 = No word has been received</p> <p>bit 6 : OBF: Output Buffer Full Status bit 1 = The output buffer still holds a previously written word 0 = The output buffer has been read</p> <p>bit 5 : IBOV: Input Buffer Overflow Detect bit (in microprocessor mode) 1 = A write occurred when a previously input word has not been read (must be cleared in software) 0 = No overflow occurred</p> <p>bit 4 : PSPMODE: Parallel Slave Port Mode Select bit 1 = Parallel slave port mode 0 = General purpose I/O mode</p> <p>bit 3 : Unimplemented: Read as '0'</p> <p>PORTE Data Direction Bits</p> <p>bit 2 : Bit2: Direction Control bit for pin RE2/CS/AN7 1 = Input 0 = Output</p> <p>bit 1 : Bit1: Direction Control bit for pin RE1/WR/AN6 1 = Input 0 = Output</p> <p>bit 0 : Bit0: Direction Control bit for pin RE0/RD/AN5 1 = Input 0 = Output</p>							
<p>R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset</p>							

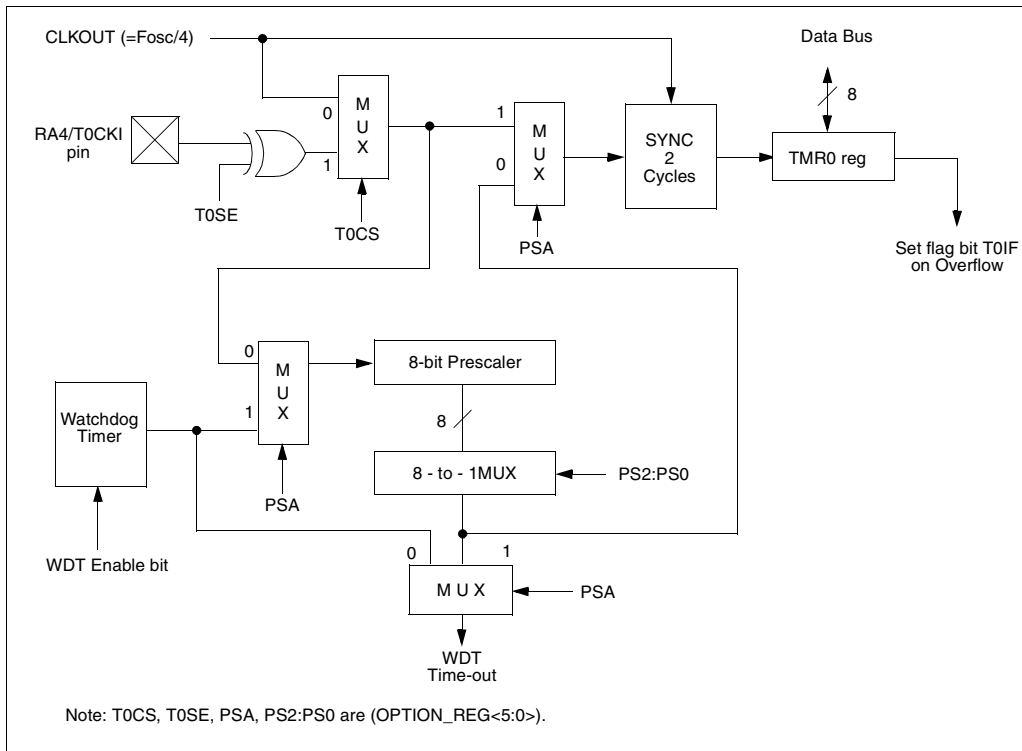
4.3 Timer0 Interrupt

The prescaler assignment is fully under software control, i.e., it can be changed “on the fly” during program execution.

Note: To avoid an unintended device RESET, a specific instruction sequence (shown in the PICmicro™ Mid-Range Reference Manual, DS33023) must be executed when changing the prescaler assignment from Timer0 to the WDT. This sequence must be followed even if the WDT is disabled.

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets bit T0IF (INTCON<2>). The interrupt can be masked by clearing bit T0IE (INTCON<5>). Bit T0IF must be cleared in software by the Timer0 module interrupt service routine before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from SLEEP since the timer is shut off during SLEEP.

FIGURE 4-2: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER

**TABLE 4-1 REGISTERS ASSOCIATED WITH TIMER0**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
01h,101h	TMR0	Timer0 module's register								xxxxx xxxxx	uuuuu uuuuu
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
81h,181h	OPTION_REG	RBPƯ	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer0.

5.0 TIMER1 MODULE

The Timer1 module timer/counter has the following features:

- 16-bit timer/counter
(Two 8-bit registers; TMR1H and TMR1L)
- Readable and writable (Both registers)
- Internal or external clock select
- Interrupt on overflow from FFFFh to 0000h
- Reset from CCP module trigger

Timer1 has a control register, shown in Figure 5-1. Timer1 can be enabled/disabled by setting/clearing control bit TMR1ON (T1CON<0>).

Figure 5-3 is a simplified block diagram of the Timer1 module.

Additional information on timer modules is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

5.1 Timer1 Operation

Timer1 can operate in one of these modes:

- As a timer
- As a synchronous counter
- As an asynchronous counter

The operating mode is determined by the clock select bit, TMR1CS (T1CON<1>).

In timer mode, Timer1 increments every instruction cycle. In counter mode, it increments on every rising edge of the external clock input.

When the Timer1 oscillator is enabled (T1OSCEN is set), the RC1/T1OSI and RC0/T1OSO/T1CKI pins become inputs. That is, the TRISC<1:0> value is ignored.

Timer1 also has an internal "reset input". This reset can be generated by the CCP module (Section 7.0).

FIGURE 5-1: T1CON: TIMER1 CONTROL REGISTER (ADDRESS 10h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-6: **Unimplemented:** Read as '0'

bit 5-4: **T1CKPS1:T1CKPS0:** Timer1 Input Clock Prescale Select bits

11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3: **T1OSCEN:** Timer1 Oscillator Enable Control bit

1 = Oscillator is enabled
0 = Oscillator is shut off
Note: The oscillator inverter and feedback resistor are turned off to eliminate power drain

bit 2: **T1SYNC:** Timer1 External Clock Input Synchronization Control bit

TMR1CS = 1
1 = Do not synchronize external clock input
0 = Synchronize external clock input

TMR1CS = 0
This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

bit 1: **TMR1CS:** Timer1 Clock Source Select bit

1 = External clock from pin RC0/T1OSO/T1CKI (on the rising edge)
0 = Internal clock (Fosc/4)

bit 0: **TMR1ON:** Timer1 On bit

1 = Enables Timer1
0 = Stops Timer1

8.2.2 GENERAL CALL ADDRESS SUPPORT

The addressing procedure for the I²C bus is such that the first byte after the START condition usually determines which device will be the slave addressed by the master. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge.

The general call address is one of eight addresses reserved for specific purposes by the I²C protocol. It consists of all 0's with R/W = 0

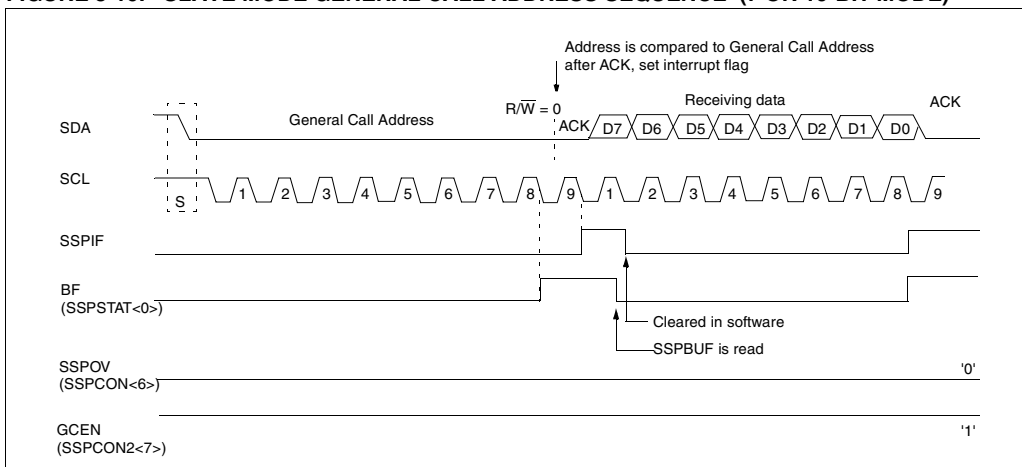
The general call address is recognized when the General Call Enable bit (GCEN) is enabled (SSPCON2<7> is set). Following a start-bit detect, 8-bits are shifted into SSPSR and the address is compared against SSPADD, and is also compared to the general call address, fixed in hardware.

If the general call address matches, the SSPSR is transferred to the SSPBUF, the BF flag is set (eighth bit), and on the falling edge of the ninth bit (ACK bit) the SSPIF flag is set.

When the interrupt is serviced. The source for the interrupt can be checked by reading the contents of the SSPBUF to determine if the address was device specific or a general call address.

In 10-bit mode, the SSPADD is required to be updated for the second half of the address to match, and the UA bit is set (SSPSTAT<1>). If the general call address is sampled when GCEN is set while the slave is configured in 10-bit address mode, then the second half of the address is not necessary, the UA bit will not be set, and the slave will begin receiving data after the acknowledge (Figure 8-16).

FIGURE 8-16: SLAVE MODE GENERAL CALL ADDRESS SEQUENCE (7 OR 10-BIT MODE)



8.2.13 ACKNOWLEDGE SEQUENCE TIMING

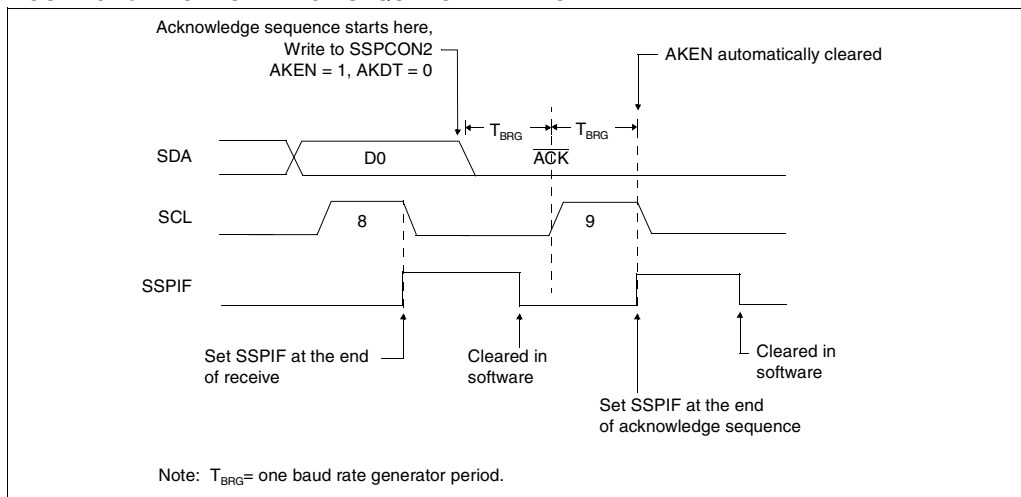
An acknowledge sequence is enabled by setting the acknowledge sequence enable bit, **AKEN** (**SSPCON2<4>**). When this bit is set, the **SCL** pin is pulled low and the contents of the acknowledge data bit is presented on the **SDA** pin. If the user wishes to generate an acknowledge, then the **AKDT** bit should be cleared. If not, the user should set the **AKDT** bit before starting an acknowledge sequence. The baud rate generator then counts for one rollover period (T_{BRG}), and the **SCL** pin is de-asserted (pulled high). When the **SCL** pin is sampled high (clock arbitration), the baud

rate generator counts for T_{BRG} . The **SCL** pin is then pulled low. Following this, the **AKEN** bit is automatically cleared, the baud rate generator is turned off, and the **SSP** module then goes into **IDLE** mode. (Figure 8-29)

8.2.13.13 WCOL STATUS FLAG

If the user writes the **SSPBUF** when an acknowledge sequence is in progress, then **WCOL** is set and the contents of the buffer are unchanged (the write doesn't occur).

FIGURE 8-29: ACKNOWLEDGE SEQUENCE WAVEFORM



8.2.15 CLOCK ARBITRATION

Clock arbitration occurs when the master, during any receive, transmit, or repeated start/stop condition, deasserts the SCL pin (SCL allowed to float high). When the SCL pin is allowed to float high, the baud rate generator (BRG) is suspended from counting until the SCL pin is actually sampled high. When the SCL pin is sampled high, the baud rate generator is reloaded with the contents of SSPADD<6:0> and begins counting. This ensures that the SCL high time will always be at least one BRG rollover count in the event that the clock is held low by an external device (Figure 8-33).

8.2.16 SLEEP OPERATION

While in sleep mode, the I²C module can receive addresses or data, and when an address match or complete byte transfer occurs wake the processor from sleep (if the SSP interrupt is enabled).

8.2.17 EFFECTS OF A RESET

A reset disables the SSP module and terminates the current transfer.

FIGURE 8-33: CLOCK ARBITRATION TIMING IN MASTER TRANSMIT MODE

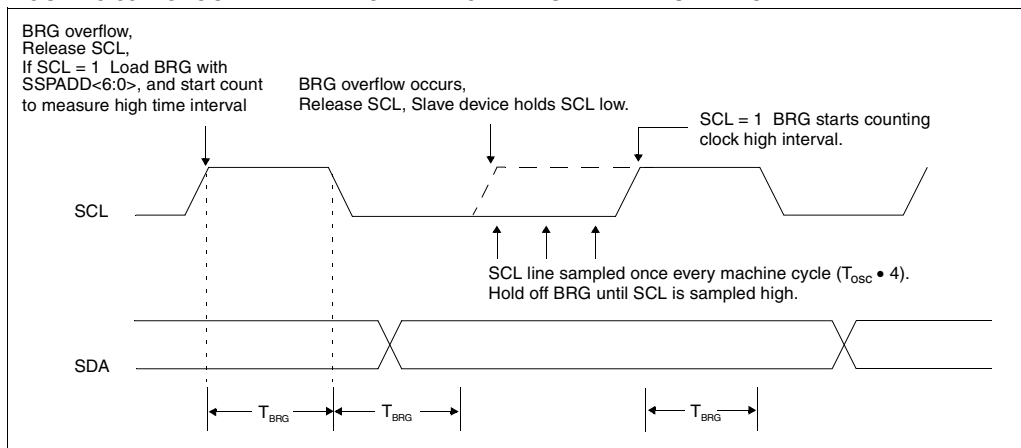


FIGURE 8-36: BUS COLLISION DURING START CONDITION (SCL = 0)

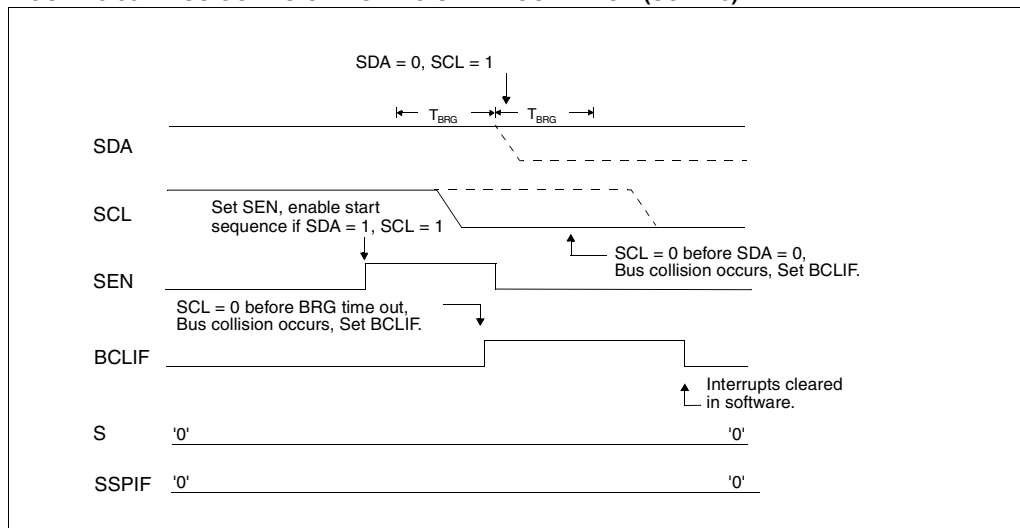
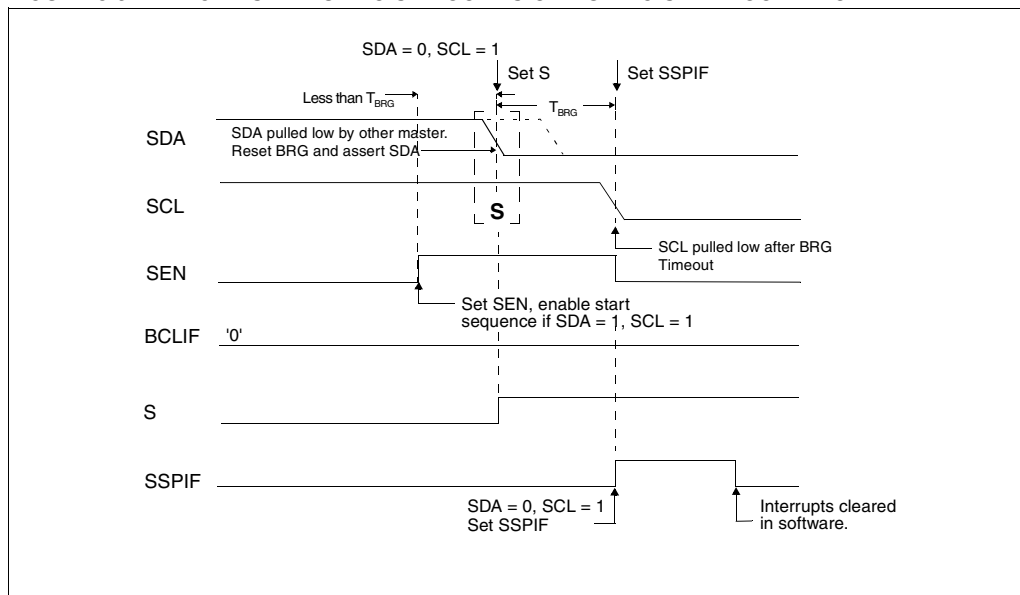


FIGURE 8-37: BRG RESET DUE TO SDA COLLISION DURING START CONDITION



8.2.18.17 BUS COLLISION DURING A STOP CONDITION

Bus collision occurs during a STOP condition if:

- After the SDA pin has been de-asserted and allowed to float high, SDA is sampled low after the BRG has timed out.
- After the SCL pin is de-asserted, SCL is sampled low before SDA goes high.

The STOP condition begins with SDA asserted low. When SDA is sampled low, the SCL pin is allow to float. When the pin is sampled high (clock arbitration), the baud rate generator is loaded with SSPADD<6:0> and counts down to 0. After the BRG times out SDA is sampled. If SDA is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data '0'. If the SCL pin is sampled low before SDA is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data '0' (Figure 8-40).

FIGURE 8-40: BUS COLLISION DURING A STOP CONDITION (CASE 1)

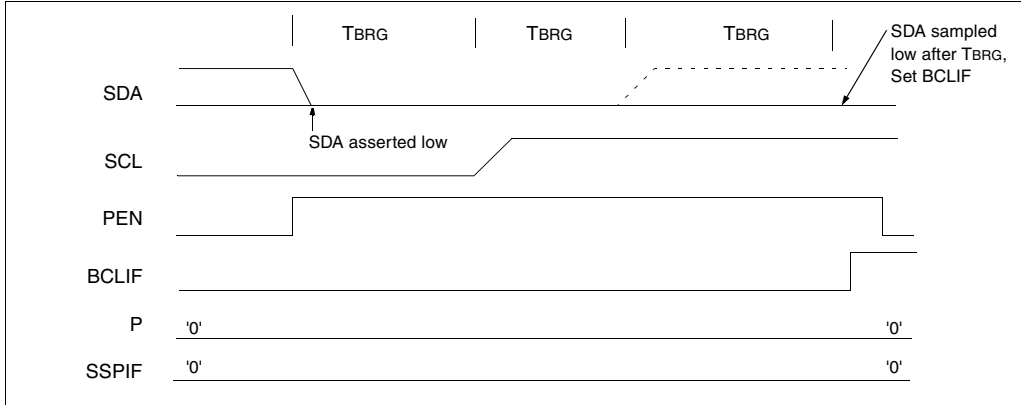
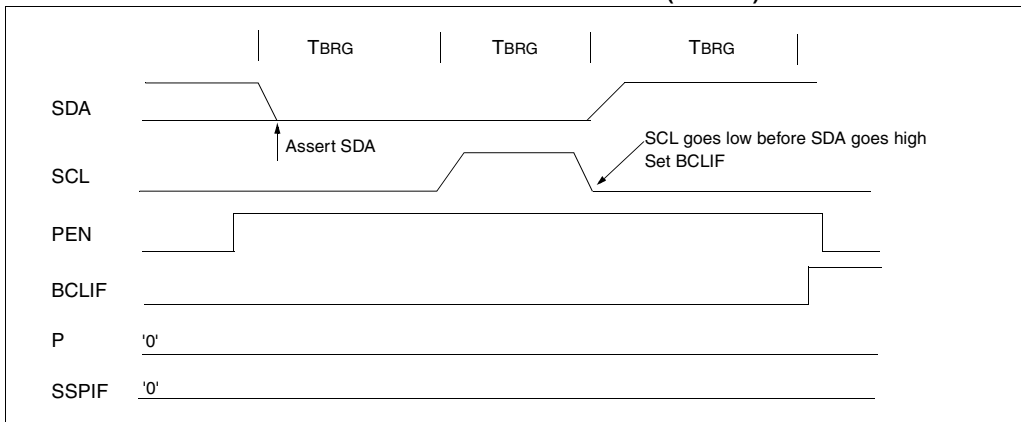


FIGURE 8-41: BUS COLLISION DURING A STOP CONDITION (CASE 2)



The value that is in the ADRESH and ADRESL registers are not modified for a Power-on Reset. The ADRESH and ADRESL registers will contain unknown data after a Power-on Reset.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine acquisition time, see Section 11.6. After this acquisition time has elapsed the A/D conversion can be started. The following steps should be followed for doing an A/D conversion:

11.2 Configuring the A/D Module

11.3 Configuring Analog Port Pins

The ADCON1 and TRIS registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bit set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS3:CHS0 bits and the TRIS bits.

Note 1: When reading the PORTA or PORTE register, all pins configured as analog input channels will read as cleared (a low level). When reading the PORTB register, all pins configured as analog input channels will read as set (a high level). Pins configured as digital inputs, will convert an analog input. Analog levels on a digitally configured input will not affect the conversion accuracy.

Note 2: Analog levels on any pin that is defined as a digital input (including the ANx pins), may cause the input buffer to consume current that is out of the devices specification.

11.3.1 CONFIGURING THE REFERENCE VOLTAGES

The VCFG bits in the ADCON1 register configure the A/D module reference inputs. The reference high input can come from an internal reference (VRH) or (VRL), an external reference (VREF+), or AVDD. The low reference input can come from an internal reference (VRL), an external reference (VREF-), or AVSS. If an external reference is chosen for the reference high or reference low inputs, the port pin that multiplexes the incoming external references is configured as an analog input, regardless of the values contained in the A/D port configuration bits (PCFG3:PCFG0).

After the A/D module has been configured as desired, and the analog input channels have their corresponding TRIS bits selected for port inputs, the selected channel must be acquired before conversion is started. The A/D conversion cycle can be initiated by setting the GO/DONE bit. The A/D conversion begins, and lasts for 13TAD. The following steps should be followed for performing an A/D conversion:

1. Configure the A/D module
 - Configure analog pins / voltage reference / and digital I/O (ADCON1)
 - Select A/D input channel (ADCON0)
 - Select A/D conversion clock (ADCON0)
 - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if required)
 - Clear ADIF bit
 - Set ADIE bit
 - Set PEIE bit
 - Set GIE bit
3. Wait the required acquisition time (3TAD)
4. Start conversion
 - Set GO/DONE bit (ADCON0)
5. Wait 13TAD until A/D conversion is complete, by either:
 - Polling for the GO/DONE bit to be cleared
 OR
 - Waiting for the A/D interrupt
6. Read A/D Result registers (ADRESH and ADRESL), clear ADIF if required.
7. For next conversion, go to step 1, step 2 or step 3 as required.

Clearing the GO/DONE bit during a conversion will abort the current conversion. The ADRESH and ADRESL registers **WILL** be updated with the partially completed A/D conversion value. That is, the ADRESH and ADRESL registers **WILL** contain the value of the current incomplete conversion.

Note: Do not set the ADON bit and the GO/DONE bit in the same instruction. Doing so will cause the GO/DONE bit to be automatically cleared.

15.5 AC Characteristics: PIC16C77X (Commercial, Industrial)

15.5.1 TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST (I²C specifications only)
4. Ts (I²C specifications only)

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	RD
cs	CS	rw	RD or WR
di	SDI	sc	SSK
do	SDO	ss	SS
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	MCLR	wr	WR

Uppercase letters and their meanings:

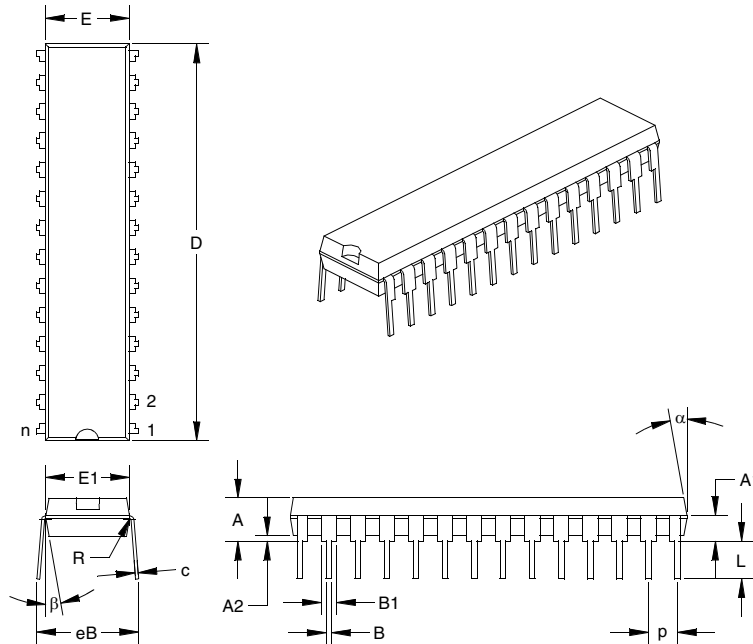
S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
I²C only			
AA	output access	High	High
BUF	Bus free	Low	Low

TCC:ST (I²C specifications only)

CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

17.2 K04-070 28-Lead Skinny Plastic Dual In-line (SP) – 300 mil

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		28			28	
Pitch	p		0.100			2.54	
Lower Lead Width	B	0.016	0.019	0.022	0.41	0.48	0.56
Upper Lead Width	B1†	0.040	0.053	0.065	1.02	1.33	1.65
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Top to Seating Plane	A	0.140	0.150	0.160	3.56	3.81	4.06
Top of Lead to Seating Plane	A1	0.070	0.090	0.110	1.78	2.29	2.79
Base to Seating Plane	A2	0.015	0.020	0.025	0.38	0.51	0.64
Tip to Seating Plane	L	0.125	0.130	0.135	3.18	3.30	3.43
Package Length	D‡	1.345	1.365	1.385	34.16	34.67	35.18
Molded Package Width	E‡	0.280	0.288	0.295	7.11	7.30	7.49
Radius to Radius Width	E1	0.270	0.283	0.295	6.86	7.18	7.49
Overall Row Spacing	eB	0.320	0.350	0.380	8.13	8.89	9.65
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter.

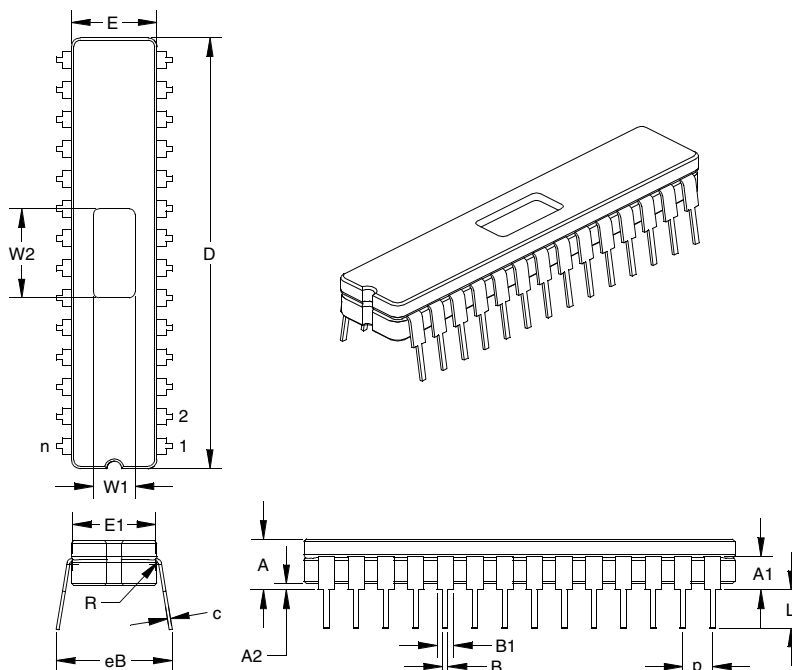
† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

PIC16C77X

17.3 K04-080 28-Lead Ceramic Dual In-line with Window (JW) – 300 mil

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



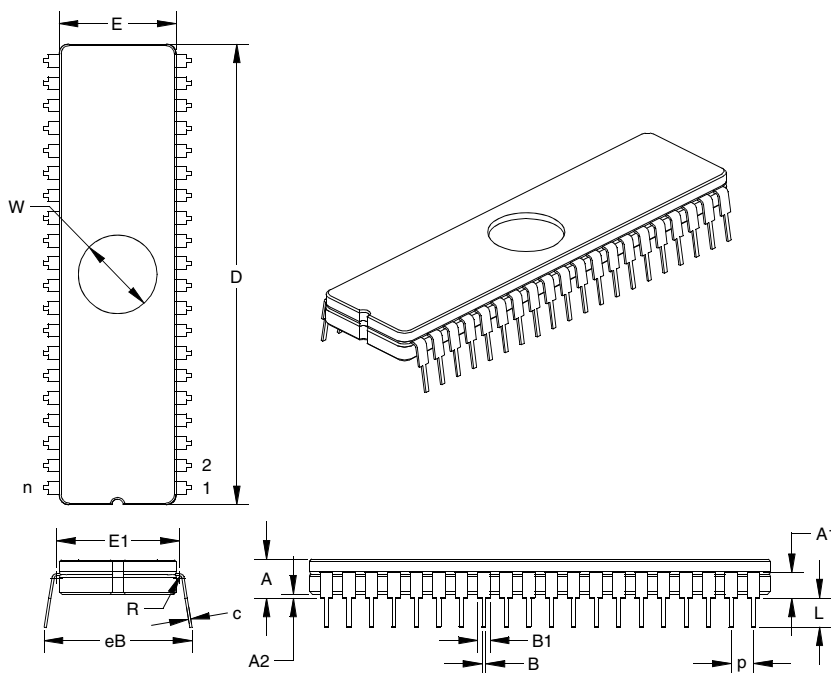
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		28			28	
Pitch	p	0.098	0.100	0.102	2.49	2.54	2.59
Lower Lead Width	B	0.016	0.019	0.021	0.41	0.47	0.53
Upper Lead Width	B1	0.050	0.058	0.065	1.27	1.46	1.65
Shoulder Radius	R	0.010	0.013	0.015	0.25	0.32	0.38
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Top to Seating Plane	A	0.170	0.183	0.195	4.32	4.64	4.95
Top of Lead to Seating Plane	A1	0.107	0.125	0.143	2.72	3.18	3.63
Base to Seating Plane	A2	0.015	0.023	0.030	0.00	0.57	0.76
Tip to Seating Plane	L	0.135	0.140	0.145	3.43	3.56	3.68
Package Length	D	1.430	1.458	1.485	36.32	37.02	37.72
Package Width	E	0.285	0.290	0.295	7.24	7.37	7.49
Radius to Radius Width	E1	0.255	0.270	0.285	6.48	6.86	7.24
Overall Row Spacing	eB	0.345	0.385	0.425	8.76	9.78	10.80
Window Width	W1	0.130	0.140	0.150	0.13	0.14	0.15
Window Length	W2	0.290	0.300	0.310	0.29	0.3	0.31

* Controlling Parameter.

PIC16C77X

17.7 K04-014 40-Lead Ceramic Dual In-line with Window (JW) – 600 mil

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.600			15.24	
Number of Pins	n		40			40	
Pitch	p	0.098	0.100	0.102	2.49	2.54	2.59
Lower Lead Width	B	0.016	0.020	0.023	0.41	0.50	0.58
Upper Lead Width	B1	0.050	0.053	0.055	1.27	1.33	1.40
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.008	0.011	0.014	0.20	0.28	0.36
Top to Seating Plane	A	0.190	0.205	0.220	4.83	5.21	5.59
Top of Lead to Seating Plane	A1	0.117	0.135	0.153	2.97	3.43	3.89
Base to Seating Plane	A2	0.030	0.045	0.060	0.00	1.14	1.52
Tip to Seating Plane	L	0.135	0.140	0.145	3.43	3.56	3.68
Package Length	D	2.040	2.050	2.060	51.82	52.07	52.32
Package Width	E	0.514	0.520	0.526	13.06	13.21	13.36
Radius to Radius Width	E1	0.560	0.580	0.600	14.22	14.73	15.24
Overall Row Spacing	eB	0.610	0.660	0.710	15.49	16.76	18.03
Window Diameter	W	0.340	0.350	0.360	8.64	8.89	9.14

* Controlling Parameter.

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