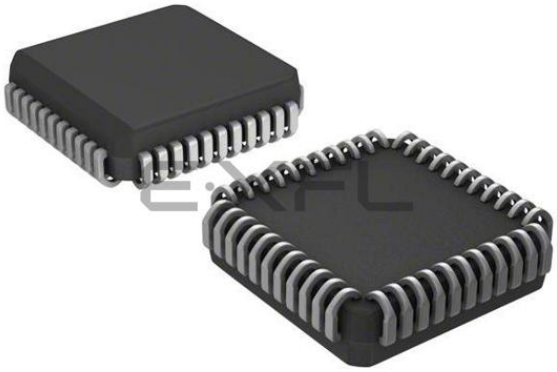

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc774-i-l

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although STATUS bits may be affected).

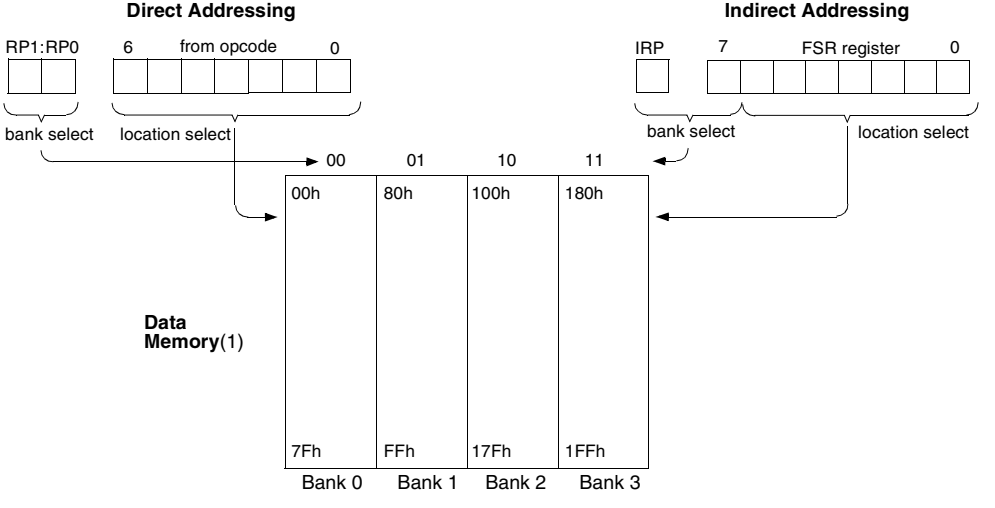
A simple program to clear RAM locations 20h-2Fh using indirect addressing is shown in Example 2-1.

EXAMPLE 2-1: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```
        movlw   0x20  ;initialize pointer
        movwf   FSR   ;  to RAM
NEXT    clrf    INDF  ;clear INDF register
        incf    FSR   ;inc pointer
        btfss   FSR,4 ;all done?
        goto    NEXT  ;NO, clear next
CONTINUE
        :             ;YES, continue
```

An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 2-11.

FIGURE 2-11: DIRECT/INDIRECT ADDRESSING



Note 1: For register file map detail see Figure 2-2.

3.2 PORTB and the TRISB Register

PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (=1) will make the corresponding PORTB pin an input, i.e., put the corresponding output driver in a hi-impedance mode. Clearing a TRISB bit (=0) will make the corresponding PORTB pin an output, i.e., put the contents of the output latch on the selected pin.

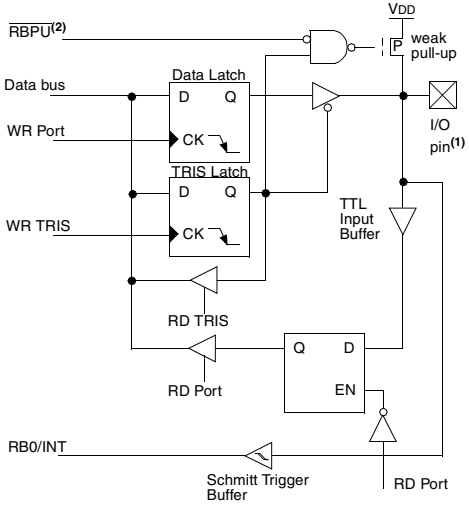
EXAMPLE 3-1: INITIALIZING PORTB

```
BCF     STATUS, RP0  ;
CLRF    PORTB        ; Initialize PORTB by
                     ; clearing output
                     ; data latches
BSF     STATUS, RP0  ; Select Bank 1
MOVLW   0xCF         ; Value used to
                     ; initialize data
                     ; direction
MOVWF   TRISB        ; Set RB<3:0> as inputs
                     ; RB<5:4> as outputs
                     ; RB<7:6> as inputs
```

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit $\overline{\text{RBPU}}$ (OPTION_REG<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

The RB0 pin is multiplexed with the external interrupt (RB0/INT).

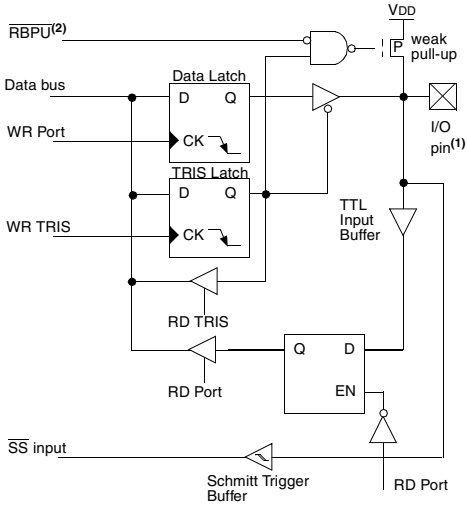
FIGURE 3-4: BLOCK DIAGRAM OF RB0 PIN



Note 1: I/O pins have diode protection to VDD and VSS.
2: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the $\overline{\text{RBPU}}$ bit (OPTION_REG<7>).

The RB1 pin is multiplexed with the SSP module slave select (RB1/$\overline{\text{SS}}$).

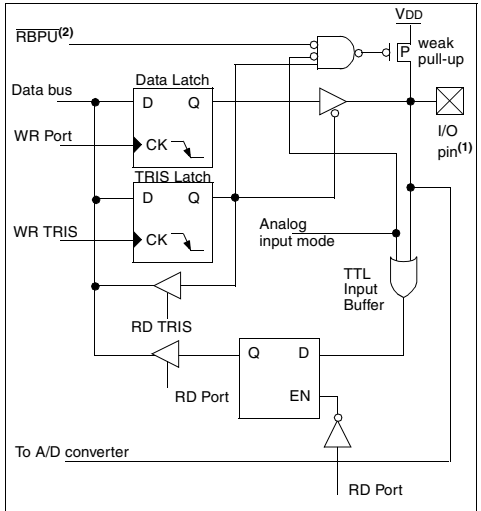
FIGURE 3-5: BLOCK DIAGRAM OF RB1/$\overline{\text{SS}}$ PIN



Note 1: I/O pins have diode protection to VDD and VSS.
2: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the $\overline{\text{RBPU}}$ bit (OPTION_REG<7>).

The RB2 pin is multiplexed with analog channel 8 (RB2/AN8).

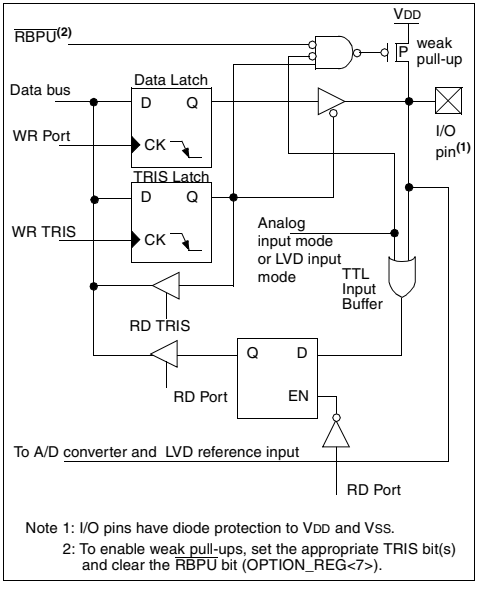
FIGURE 3-6: BLOCK DIAGRAM OF RB2/AN8 PIN



Note 1: I/O pins have diode protection to VDD and VSS.
2: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the $\overline{\text{RBPU}}$ bit (OPTION_REG<7>).

The RB3 pin is multiplexed with analog channel 9 and the low voltage detect input (RB3/AN9/LVDIN)

FIGURE 3-7: BLOCK DIAGRAM OF RB3/AN9/LVDIN PIN



Note 1: I/O pins have diode protection to VDD and VSS.
2: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the RBPU bit (OPTION_REG<7>).

Four of PORTB's pins, RB7:RB4, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e. any RB7:RB4 pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

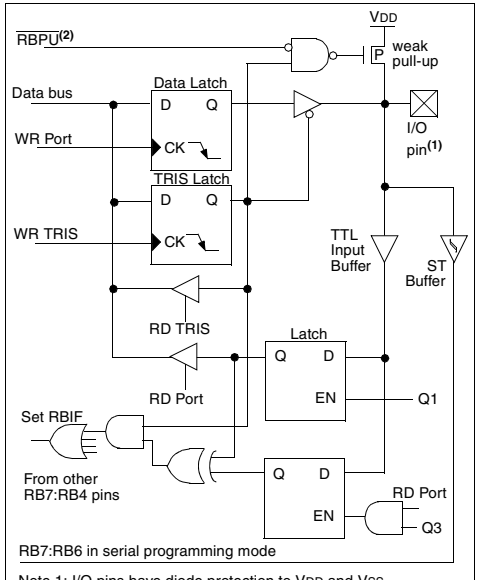
This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

a) Any read or write of PORTB. This will end the mismatch condition.
b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition, and allow flag bit RBIF to be cleared.

The interrupt on change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt on change feature.

FIGURE 3-8: BLOCK DIAGRAM OF RB7:RB4 PINS



Note 1: I/O pins have diode protection to VDD and VSS.
2: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the RBPU bit (OPTION_REG<7>).

3.3 PORTC and the TRISC Register

PORTC is an 8-bit wide bi-directional port. The corresponding data direction register is TRISC. Setting a TRISC bit (=1) will make the corresponding PORTC pin an input, i.e., put the corresponding output driver in a hi-impedance mode. Clearing a TRISC bit (=0) will make the corresponding PORTC pin an output, i.e., put the contents of the output latch on the selected pin.

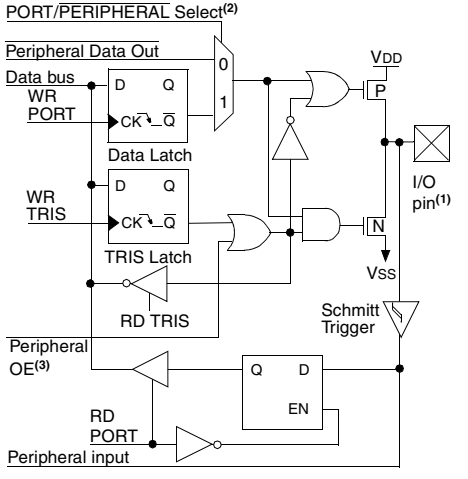
PORTC is multiplexed with several peripheral functions (Table 3-5). PORTC pins have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify-write instructions (`BSF, BCF, XORWF`) with TRISC as destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

EXAMPLE 3-1: INITIALIZING PORTC

```
BCF     STATUS, RP0   ; Select Bank 0
CLRF    PORTC         ; Initialize PORTC by
                      ; clearing output
                      ; data latches
BSF     STATUS, RP0   ; Select Bank 1
MOVLW   0xCF          ; Value used to
                      ; initialize data
                      ; direction
MOVWF   TRISC         ; Set RC<3:0> as inputs
                      ; RC<5:4> as outputs
                      ; RC<7:6> as inputs
```

FIGURE 3-9: PORTC BLOCK DIAGRAM (PERIPHERAL OUTPUT OVERRIDE)

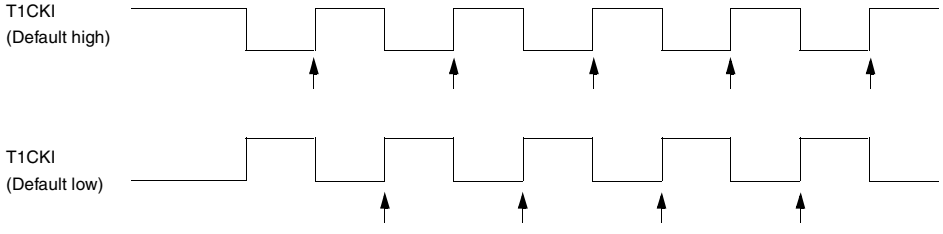


Note 1: I/O pins have diode protection to VDD and VSS.
2: Port/Peripheral select signal selects between port data and peripheral output.
3: Peripheral OE (output enable) is only activated if peripheral select is active.

5.1.1 TIMER1 COUNTER OPERATION

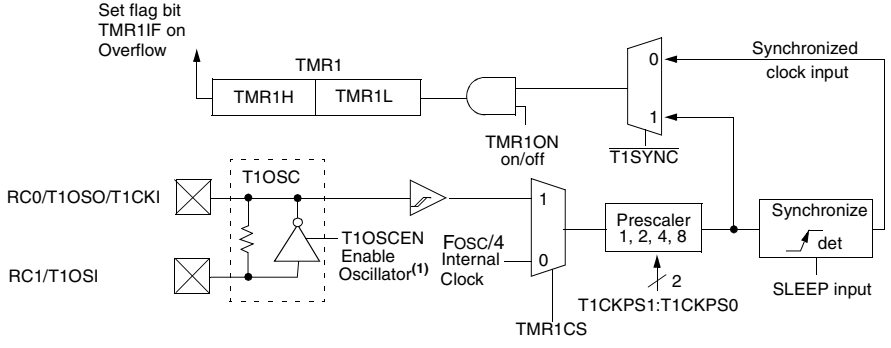
In this mode, Timer1 is being incremented via an external source. Increments occur on a rising edge. After Timer1 is enabled in counter mode, the module must first have a falling edge before the counter begins to increment.

FIGURE 5-2: TIMER1 INCREMENTING EDGE



Note: Arrows indicate counter increments.

FIGURE 5-3: TIMER1 BLOCK DIAGRAM



Note 1: When the T1OSCEN bit is cleared, the inverter and feedback resistor are turned off. This eliminates power drain.

7.3.3 SET-UP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Set the PWM period by writing to the PR2 register.
2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
3. Make the CCP1 pin an output by clearing the TRISC<2> bit.
4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
5. Configure the CCP1 module for PWM operation.

TABLE 7-4 EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 20 MHz

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	5.5

TABLE 7-5 REGISTERS ASSOCIATED WITH PWM AND TIMER2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
92h	PR2	Timer2 module's period register								1111 1111	1111 1111
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/Compare/PWM register1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM register1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by PWM and Timer2.
Note 1: Bits PSPIE and PSPIF are reserved on the 28-pin, always maintain these bits clear.

8.1.4 MASTER MODE

The master can initiate the data transfer at any time because it controls the SCK. The master determines when the slave (Processor 2, Figure 8-5) is to broadcast data by the software protocol.

In master mode the data is transmitted/received as soon as the SSPBUF register is written to. If the SPI module is only going to receive, the SDO output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPBUF register as if a normal received byte (interrupts and status bits appropriately set). This could be useful in receiver applications as a "line activity monitor".

The clock polarity is selected by appropriately programming bit CKP (SSPCON<4>). This then would give waveforms for SPI communication as shown in Figure 8-6, Figure 8-8, and Figure 8-9 where the MSb is transmitted first. In master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- FOSC/4 (or TCY)
- FOSC/16 (or 4 • TCY)
- FOSC/64 (or 16 • TCY)
- Timer2 output/2

This allows a maximum bit clock frequency (at 20 MHz) of 8.25 MHz.

Figure 8-6 shows the waveforms for Master mode. When CKE = 1, the SDO data is valid before there is a clock edge on SCK. The change of the input sample is shown based on the state of the SMP bit. The time when the SSPBUF is loaded with the received data is shown.

FIGURE 8-6: SPI MODE WAVEFORM (MASTER MODE)

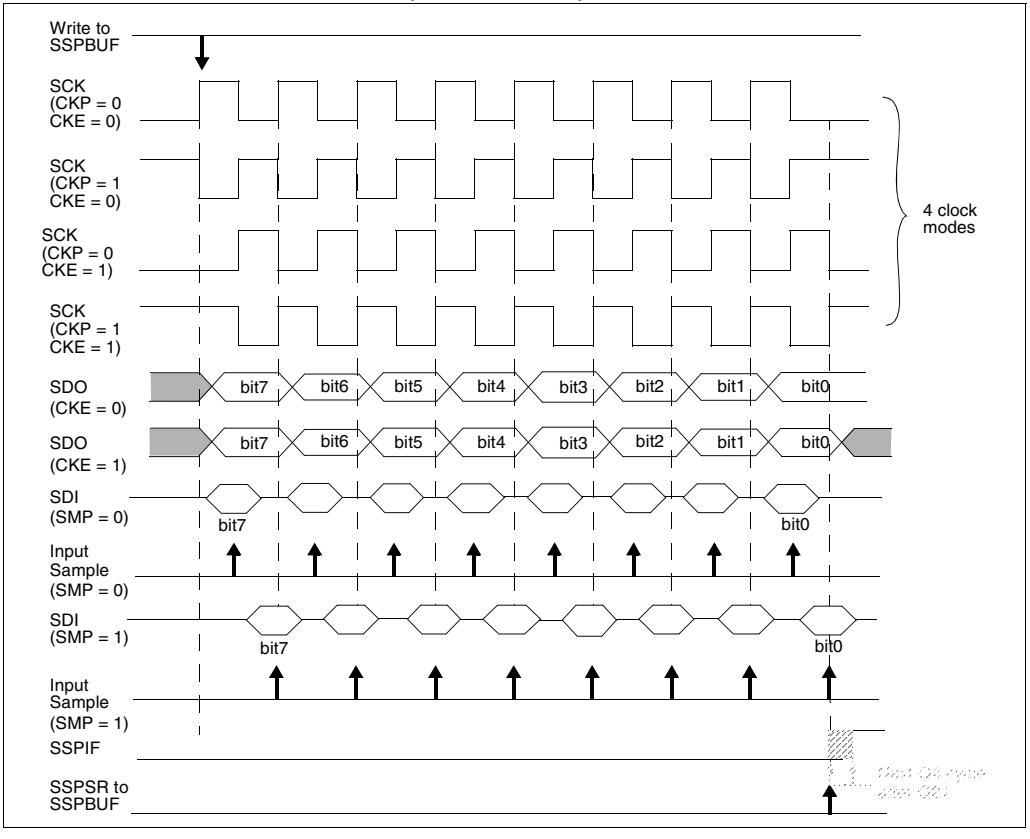
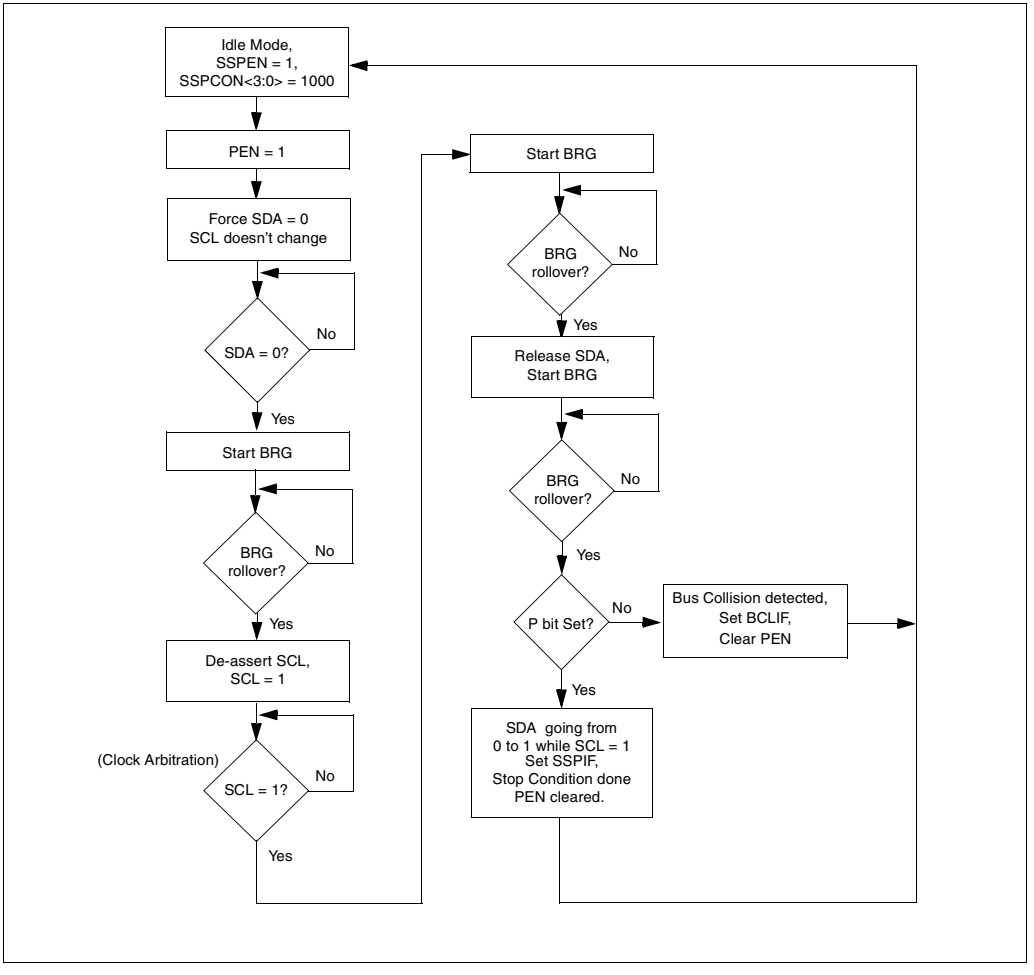


FIGURE 8-32: STOP CONDITION FLOWCHART



8.2.18 MULTI -MASTER COMMUNICATION, BUS COLLISION, AND BUS ARBITRATION

Multi-Master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDA pin, arbitration takes place when the master outputs a '1' on SDA by letting SDA float high and another master asserts a '0'. When the SCL pin floats high, data should be stable. If the expected data on SDA is a '1' and the data sampled on the SDA pin = '0', then a bus collision has taken place. The master will set the Bus Collision Interrupt Flag, BCLIF and reset the I^2C port to its IDLE state. (Figure 8-34).

If a transmit was in progress when the bus collision occurred, the transmission is halted, the BF flag is cleared, the SDA and SCL lines are de-asserted, and the SSPBUF can be written to. When the user services the bus collision interrupt service routine, and if the I^2C bus is free, the user can resume communication by asserting a START condition.

If a START, Repeated Start, STOP, or Acknowledge condition was in progress when the bus collision occurred, the condition is aborted, the SDA and SCL lines are de-asserted, and the respective control bits in the SSPCON2 register are cleared. When the user services the bus collision interrupt service routine, and if the I^2C bus is free, the user can resume communication by asserting a START condition.

The Master will continue to monitor the SDA and SCL pins, and if a STOP condition occurs, the SSPIF bit will be set.

A write to the SSPBUF will start the transmission of data at the first data bit, regardless of where the transmitter left off when bus collision occurred.

In multi-master mode, the interrupt generation on the detection of start and stop conditions allows the determination of when the bus is free. Control of the I^2C bus can be taken when the P bit is set in the SSPSTAT register, or the bus is idle and the S and P bits are cleared.

FIGURE 8-34: BUS COLLISION TIMING FOR TRANSMIT AND ACKNOWLEDGE

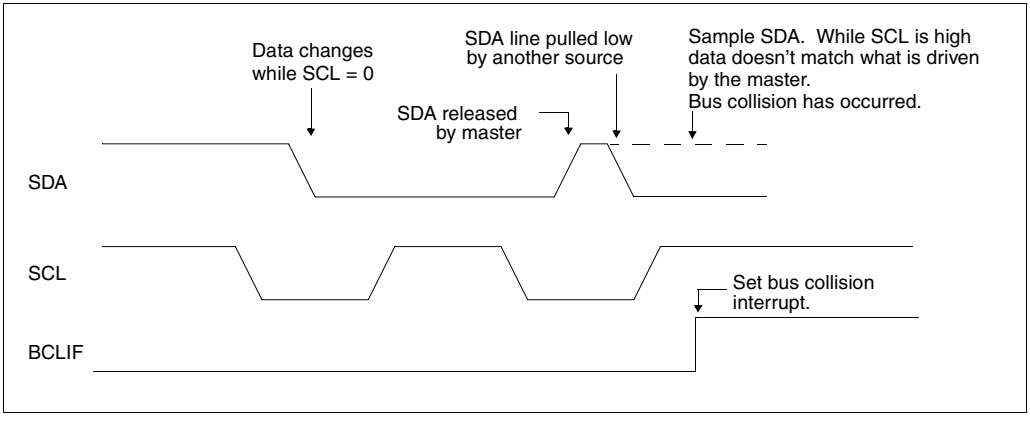


FIGURE 8-36: BUS COLLISION DURING START CONDITION (SCL = 0)

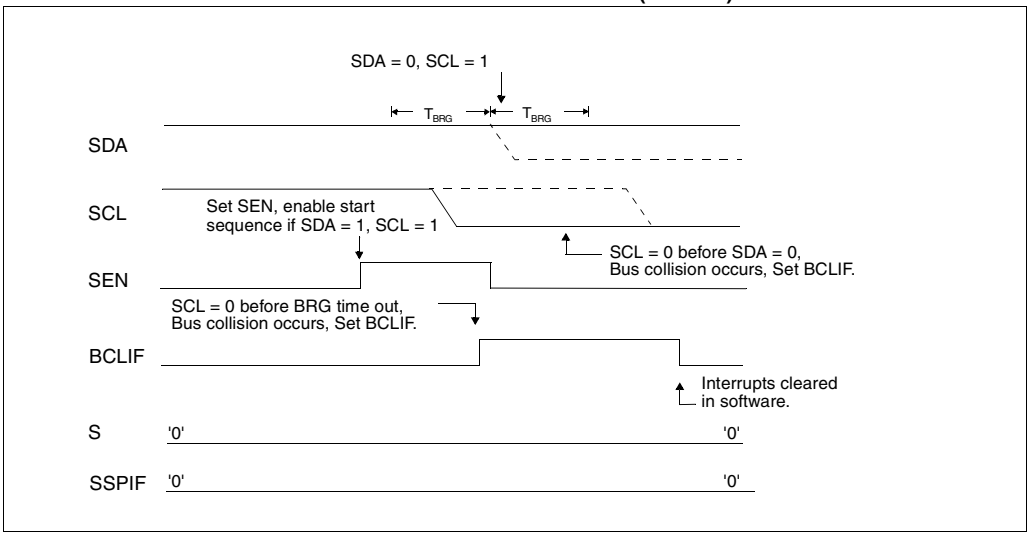


FIGURE 8-37: BRG RESET DUE TO SDA COLLISION DURING START CONDITION

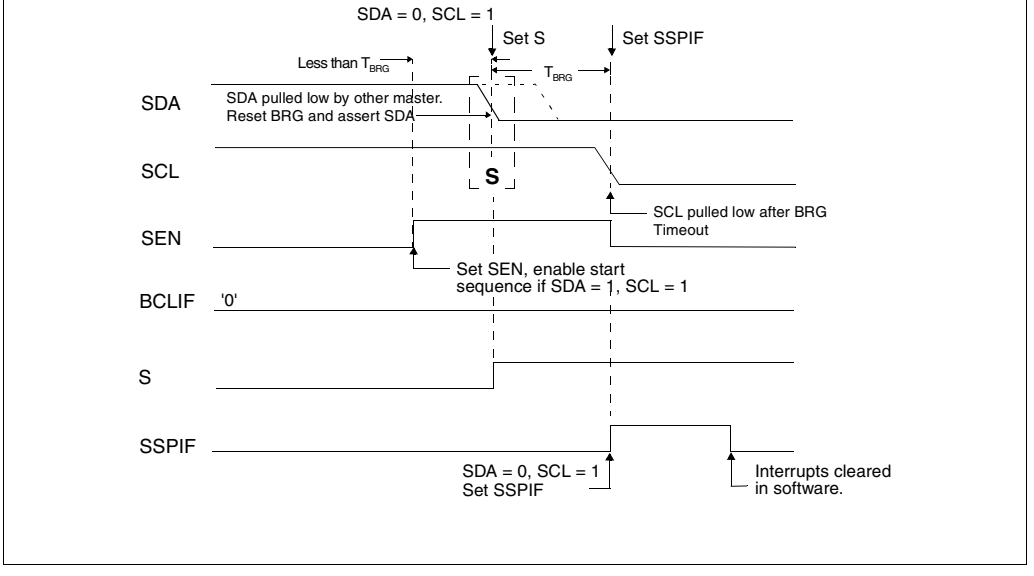


FIGURE 9-4: ASYNCHRONOUS TRANSMISSION

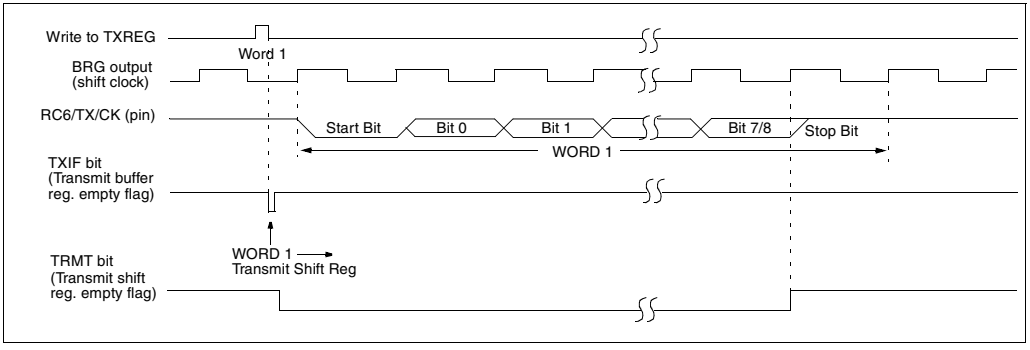
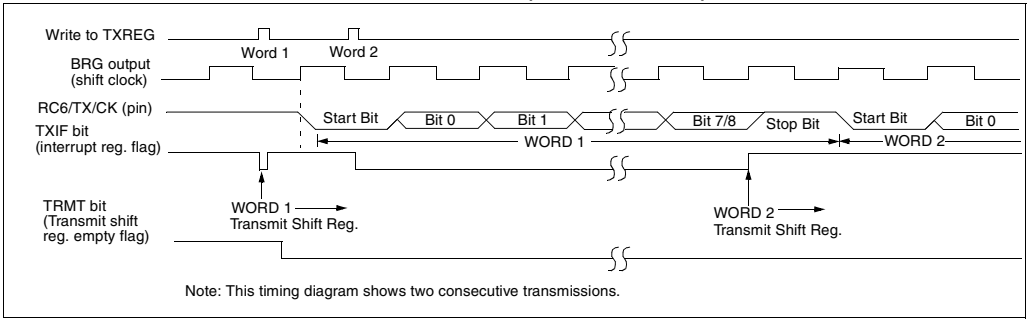


FIGURE 9-5: ASYNCHRONOUS TRANSMISSION (BACK TO BACK)



Note: This timing diagram shows two consecutive transmissions.

TABLE 9-6 REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Ch	PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
19h	TXREG	USART Transmit Register								0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Asynchronous Transmission.
Note 1: Bits PSPIE and PSPIF are reserved on the 28-pin devices, always maintain these bits clear.

NOTES:

11.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The analog-to-digital (A/D) converter module has six inputs for the PIC16C773 and ten for the PIC16C774.

The analog-to-digital converter (A/D) allows conversion of an analog input signal to a corresponding 12-bit digital number. The A/D module has up to 10 analog inputs, which are multiplexed into one sample and hold. The output of the sample and hold is the input into the converter, which generates the result via successive approximation. The analog reference voltages are software selectable to either the device's analog positive and negative supply voltages (AV_{DD}/AV_{SS}), the voltage level on the V_{REF+} and V_{REF-} pins, or internal voltage references if available (VRH, VRL).

The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode. To operate in sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The A/D module has four registers. These registers are:

- A/D Result Register Low ADRESL
- A/D Result Register High ADRESH
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)

A device reset forces all registers to their reset state. This forces the A/D module to be turned off and any conversion is aborted.

11.1 Control Registers

The ADCON0 register, shown in Figure 11-1, controls the operation of the A/D module. The ADCON1 register, shown in Figure 11-2, configures the functions of the port pins, the voltage reference configuration and the result format. The port pins can be configured as analog inputs or as digital I/O.

The combination of the ADRESH and ADRESL registers contain the result of the A/D conversion. The register pair is referred to as the ADRES register. When the A/D conversion is complete, the result is loaded into ADRES, the GO/$\overline{\text{DONE}}$ bit (ADCON0<2>) is cleared, and the A/D interrupt flag ADIF is set. The block diagram of the A/D module is shown in Figure 11-3.

FIGURE 11-1: ADCON0 REGISTER (ADDRESS 1Fh).

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	CHS3	ADON
bit7							bit 0

R =	Readable bit
W =	Writable bit
- n =	Value at POR reset

bit 7:6 **ADCS1:ADCS0:** A/D Conversion Clock Select bits
00 = Fosc/2
01 = Fosc/8
10 = Fosc/32
11 = FRC (clock derived from an RC oscillator = 1 MHz max)

bit 5:3,1 **CHS3:CHS0:** Analog Channel Select bits
0000 = channel 00 (AN0)
0001 = channel 01 (AN1)
0010 = channel 02 (AN2)
0011 = channel 03 (AN3)
0100 = channel 04 (AN4) (Reserved on 28-pin devices, do not use)
0101 = channel 05 (AN5) (Reserved on 28-pin devices, do not use)
0110 = channel 06 (AN6) (Reserved on 28-pin devices, do not use)
0111 = channel 07 (AN7) (Reserved on 28-pin devices, do not use)
1000 = channel 08 (AN8)
1001 = channel 09 (AN9)
1010, 1011, 1100, 1101, 1110,1111 are reserved, do not select.

bit 2: **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.
This bit is automatically cleared by hardware when the A/D conversion has completed.
0 = A/D conversion completed/not in progress

bit 0: **ADON:** A/D On bit
1 = A/D converter module is operating
0 = A/D converter is shutoff and consumes no operating current

11.6 A/D Sample Requirements

11.6.1 RECOMMENDED SOURCE IMPEDANCE

The maximum recommended impedance for analog sources is 2.5 kΩ. This value is calculated based on the maximum leakage current of the input pin. The leakage current is 100 nA max., and the analog input voltage cannot be vary by more than 1/4 LSb or 250 mV due to leakage. This places a requirement on the input impedance of 250 μV/100 nA = 2.5 kΩ.

11.6.2 SAMPLING TIME CALCULATION

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 11-8. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), see Figure 11-8. **The maximum recommended impedance for analog sources is 2.5 kΩ.** After the analog input channel is selected (changed) this sampling must be done before the conversion can be started.

To calculate the minimum sampling time, Equation 11-6 may be used. This equation assumes that 1/4 LSb error is used (16384 steps for the A/D). The 1/4 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

The CHOLD is assumed to be 25 pF for the 12-bit A/D.

FIGURE 11-6: A/D SAMPLING TIME EQUATION

$$V_{HOLD} = (V_{REF} - V_{REF}/16384) = (V_{REF}) \bullet (1 - e^{(-T_C/C\ (R_{IC} + R_{SS} + R_S))}) \quad \text{~~VREF~~}(1 - 1/16384) = \text{~~VREF~~} \bullet (1 - e^{(-T_C/C\ (R_{IC} + R_{SS} + R_S))})$$

$$T_C = -C_{HOLD}\ (1k\Omega + R_{SS} + R_S)\ \ln(1/16384)$$

Figure 11-7 shows the calculation of the minimum time required to charge CHOLD. This calculation is based on the following system assumptions:

CHOLD = 25 pF

RS = 2.5 kΩ

1/4 LSb error

VDD = 5V → RSS = 10 kΩ (worst case)

Temp (system Max.) = 50°C

Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (**CHOLD**) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 2.5 kΩ. This is required to meet the pin leakage specification.

4: After a conversion has completed, 2 TAD time must be waited before sampling can begin again. During this time the holding capacitor is not connected to the selected A/D input channel.

12.8 Time-out Sequence

On power-up the time-out sequence is as follows: First PWRT time-out is invoked by the POR pulse. When the PWRT delay expires the Oscillator Start-up Timer is activated. The total time-out will vary based on oscillator configuration and the status of the PWRT. For example, in RC mode with the PWRT disabled, there will be no time-out at all. Figure 12-7, Figure 12-8, Figure 12-9 and Figure 12-10 depict time-out sequences on power-up.

Since the time-outs occur from the POR pulse, if $\overline{MCLR}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{MCLR}$ high will begin execution immediately (Figure 12-9). This is useful for testing purposes or to synchronize more than one PICmicro microcontroller operating in parallel.

Table 12-5 shows the reset conditions for some special function registers, while Table 12-6 shows the reset conditions for all the registers.

12.9 Power Control/Status Register (PCON)

The Power Control/Status Register, PCON has two status bits that provide indication of which power-up type reset occurred.

Bit0 is Brown-out Reset Status bit, $\overline{BOR}$. Bit $\overline{BOR}$ is set on a Power-on Reset. It must then be set by the user and checked on subsequent resets to see if bit $\overline{BOR}$ cleared, indicating a BOR occurred. However, if the brown-out circuitry is disabled, the $\overline{BOR}$ bit is a "Don't Care" bit and is considered unknown upon a POR.

Bit1 is $\overline{POR}$ (Power-on Reset Status bit). It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

TABLE 12-3 TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out	Wake-up from SLEEP
	$\overline{PWRTE}$ = 0	$\overline{PWRTE}$ = 1		
XT, HS, LP	72 ms + 1024TOSC	1024TOSC	72 ms + 1024TOSC	1024TOSC
RC	72 ms	—	72 ms	—

TABLE 12-4 STATUS BITS AND THEIR SIGNIFICANCE

$\overline{POR}$	$\overline{BOR}$	$\overline{TO}$	$\overline{PD}$	
0	1	1	1	Power-on Reset
0	x	0	x	Illegal, $\overline{TO}$ is set on $\overline{POR}$
0	x	x	0	Illegal, $\overline{PD}$ is set on $\overline{POR}$
1	0	1	1	Brown-out Reset
1	1	0	1	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	$\overline{MCLR}$ Reset during normal operation
1	1	1	0	$\overline{MCLR}$ Reset during SLEEP or interrupt wake-up from SLEEP

TABLE 12-5 RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	---- --01
$\overline{MCLR}$ Reset during normal operation	000h	000u uuuu	---- --uu
$\overline{MCLR}$ Reset during SLEEP	000h	0001 0uuu	---- --uu
WDT Reset	000h	0000 1uuu	---- --uu
WDT Wake-up	PC + 1	uuu0 0uuu	---- --uu
Brown-out Reset	000h	0001 1uuu	---- --u0
Interrupt wake-up from SLEEP	PC + 1(1)	uuu1 0uuu	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.
Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

TABLE 12-6 INITIALIZATION CONDITIONS FOR ALL REGISTERS

Register	Devices		Power-on Reset, Brown-out Reset	MCLR Resets WDT Reset	Wake-up via WDT or Interrupt
W	773	774	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	773	774	N/A	N/A	N/A
TMR0	773	774	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	773	774	0000h	0000h	PC + 1(2)
STATUS	773	774	0001 1xxx	000q quuu(3)	uuuq quuu(3)
FSR	773	774	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	773	774	--0x 0000	--0u 0000	--uu uuuu
PORTB	773	774	xxxx 11xx	uuuu 11uu	uuuu uuuu
PORTC	773	774	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTD	773	774	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTE	773	774	---- -000	---- -000	---- -uuu
PCLATH	773	774	---0 0000	---0 0000	---u uuuu
INTCON	773	774	0000 000x	0000 000u	uuuu uuuu(1)
PIR1	773	774	r000 0000	r000 0000	ruuu uuuu(1)
	773	774	0000 0000	0000 0000	uuuu uuuu(1)
PIR2	773	774	0--- 0--0	0--- 0--0	u--- u--u(1)
TMR1L	773	774	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	773	774	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	773	774	--00 0000	--uu uuuu	--uu uuuu
TMR2	773	774	0000 0000	0000 0000	uuuu uuuu
T2CON	773	774	-000 0000	-000 0000	-uuu uuuu
SSPBUF	773	774	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSPCON	773	774	0000 0000	0000 0000	uuuu uuuu
CCPR1L	773	774	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H	773	774	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	773	774	--00 0000	--00 0000	--uu uuuu
RCSTA	773	774	0000 000x	0000 000x	uuuu uuuu
TXREG	773	774	0000 0000	0000 0000	uuuu uuuu
RCREG	773	774	0000 0000	0000 0000	uuuu uuuu
CCPR2L	773	774	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR2H	773	774	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP2CON	773	774	--00 0000	--00 0000	--uu uuuu
ADRESH	773	774	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	773	774	0000 0000	0000 0000	uuuu uuuu
OPTION_REG	773	774	1111 1111	1111 1111	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

Note 1: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 12-5 for reset value for specific condition.

12.12 Watchdog Timer (WDT)

The Watchdog Timer is as a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run, even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a SLEEP instruction.

During normal operation, a WDT time-out generates a device RESET (Watchdog Timer Reset). If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation (Watchdog Timer Wake-up). The $\overline{TO}$ bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

The WDT can be permanently disabled by clearing configuration bit WDTE (Section 12.1).

WDT time-out period values may be found in the Electrical Specifications section under parameter #31. Values for the WDT prescaler may be assigned using the OPTION_REG register.

Note:	The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

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Note:	When a CLRWDT instruction is executed and the prescaler is assigned to the WDT, the prescaler count will be cleared, but the prescaler assignment is not changed.

FIGURE 12-12: WATCHDOG TIMER BLOCK DIAGRAM

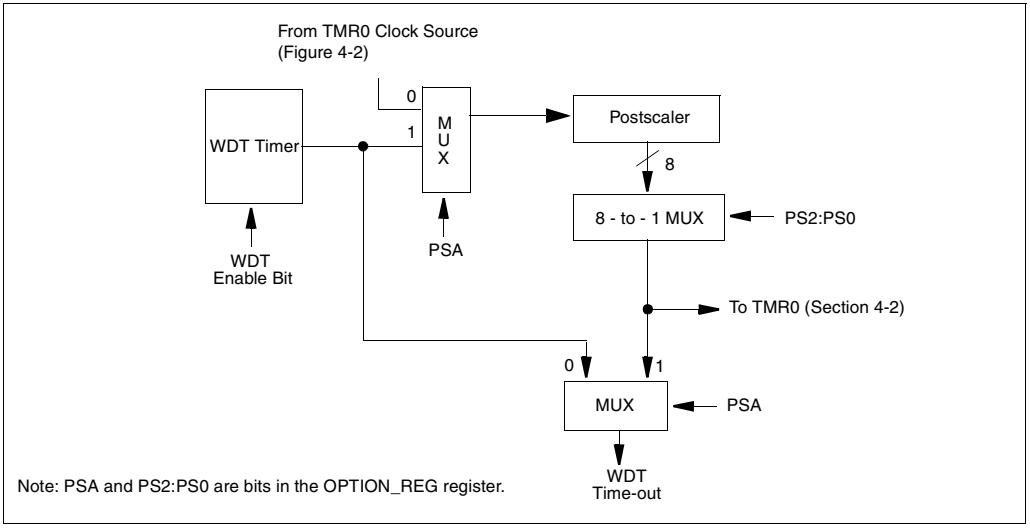


FIGURE 12-13: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits	**(1)**	BODEN(1)	CP1	CP0	$\overline{PWRTE}$(1)	WDTE	FOSC1	FOSC0
81h,181h	OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer.
Note 1: See Figure 12-1 for the full description of the configuration word bits.

FIGURE 15-2: BROWN-OUT RESET CHARACTERISTICS

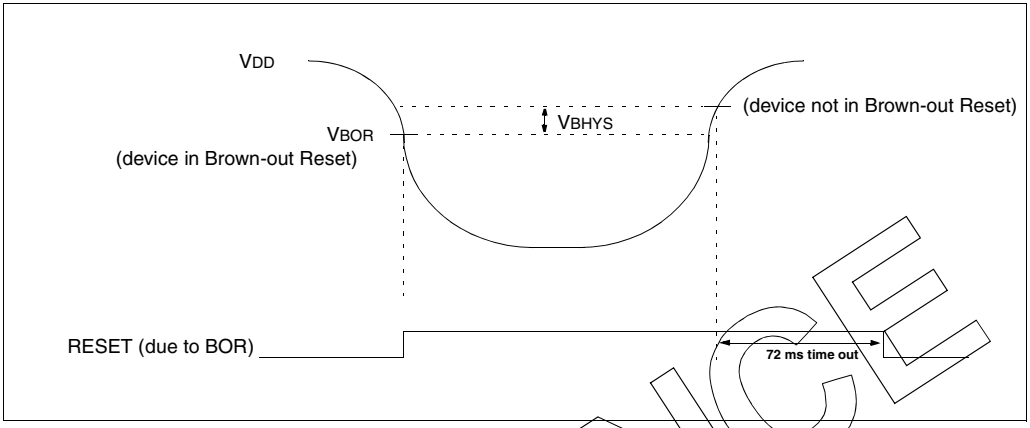


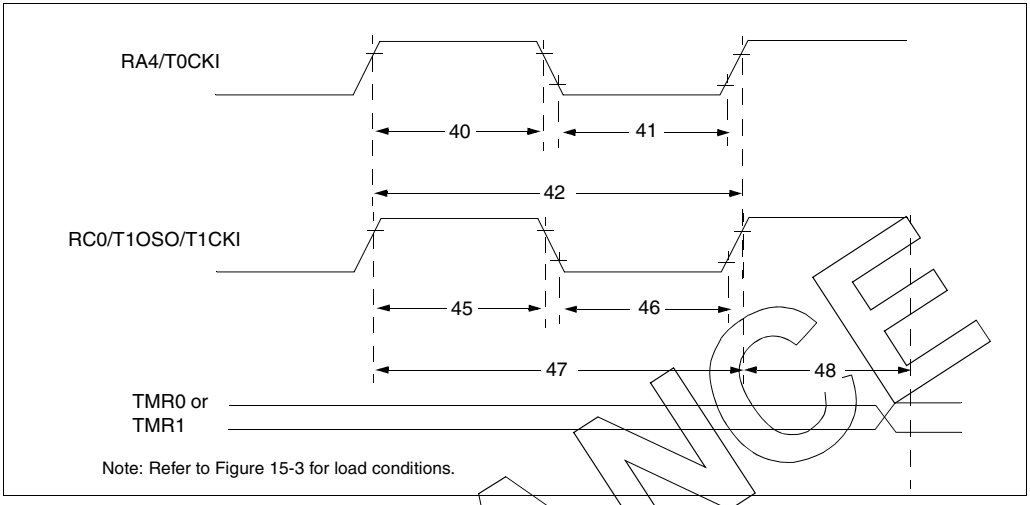
TABLE 15-4 ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS								
	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC spec Section 15.1 and Section 15.2.							
Param No.	**Characteristic**		**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D005	BOR Voltage	BORV1:0 = 11	VBOR	2.5	2.58	2.66	V	
		BORV1:0 = 10		2.7	2.78	2.86		
		BORV1:0 = 01		4.2	4.33	4.46		
		BORV1:0 = 00		4.5	4.64	4.78		
D006*	BOR Voltage Drift Temperature coefficient		TCVOUT	—	15	50	ppm/°C	
D006A*	BOR Voltage Drift with respect to VDD Regulation		ΔVBOR/ ΔVDD	—	—	50	μV/V	
D007	Brown-out Hysteresis		VBHYS	TBD	—	100	mV	
D022A	Supply Current		ΔIBOR	—	10	20	μA	

* These parameters are characterized but not tested.

Note 1: Production tested at TAMB = 25°C. Specifications over temp limits ensured by characterization.

FIGURE 15-11: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS



Note: Refer to Figure 15-3 for load conditions.

TABLE 15-12 TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	Must also meet parameter 42
				With Prescaler	10	—	—	ns	
41*	Tt0L	T0CKI Low Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	Must also meet parameter 42
				With Prescaler	10	—	—	ns	
42*	Tt0P	T0CKI Period		No Prescaler	TCY + 40	—	—	ns	
				With Prescaler	Greater of: 20 or TCY + 40 / N	—	—	ns	N = prescale value (2, 4, ..., 256)
45*	Tt1H	T1CKI High Time	Synchronous, Prescaler = 1		0.5TCY + 20	—	—	ns	Must also meet parameter 47
			Synchronous, Prescaler = 2,4,8	PIC16**C**77X	15	—	—	ns	
				PIC16**LC**77X	25	—	—	ns	
			Asynchronous	PIC16**C**77X	30	—	—	ns	
				PIC16**LC**77X	50	—	—	ns	
46*	Tt1L	T1CKI Low Time	Synchronous, Prescaler = 1		0.5TCY + 20	—	—	ns	Must also meet parameter 47
			Synchronous, Prescaler = 2,4,8	PIC16**C**77X	15	—	—	ns	
				PIC16**LC**77X	25	—	—	ns	
			Asynchronous	PIC16**C**77X	30	—	—	ns	
				PIC16**LC**77X	50	—	—	ns	
47*	Tt1P	T1CKI input period	Synchronous	PIC16**C**77X	Greater of: 30 OR TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4, 8)
				PIC16**LC**77X	Greater of: 50 OR TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous	PIC16**C**77X	60	—	—	ns	
				PIC16**LC**77X	100	—	—	ns	
	Ft1	Timer1 oscillator input frequency range (oscillator enabled by setting bit T1OSCEN)			DC	—	50	kHz	
48	TCKEZtmr1	Delay from external clock edge to timer increment			2Tosc	—	7Tosc	—	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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