



Welcome to E-XFL.COM

# What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

# Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

# Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	7KB (4K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc774-l

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

### 2.2.2.8 PCON REGISTER

The Power Control (PCON) register contains a flag bit to allow differentiation between a Power-on Reset (POR) to an external  $\overline{\text{MCLR}}$  Reset or WDT Reset. Those devices with brown-out detection circuitry contain an additional bit to differentiate a Brown-out Reset condition from a Power-on Reset condition.

Note: BOR is unknown on Power-on Reset. It must then be set by the user and checked on subsequent resets to see if BOR is clear, indicating a brown-out has occurred. The BOR status bit is a don't care and is not necessarily predictable if the brown-out circuit is disabled (by clearing the BODEN bit in the Configuration word).





# 3.6 Parallel Slave Port

The Parallel Slave Port is implemented on the 40/44-pin devices only.

PORTD operates as an 8-bit wide Parallel Slave Port, or microprocessor port when control bit PSPMODE (TRISE<4>) is set. In slave mode it is asynchronously readable and writable by the external world through  $\overline{\text{RD}}$  control input pin RE0/ $\overline{\text{RD}}$  and  $\overline{\text{WR}}$  control input pin RE1/ $\overline{\text{WR}}$ .

It can directly interface to an 8-bit microprocessor data bus. The external microprocessor can read or write the PORTD latch as an 8-bit latch. Setting bit PSPMODE enables port pin RE0/RD to be the RD input, RE1/WR to be the WR input and RE2/CS to be the CS (chip select) input. For this functionality, the corresponding data direction bits of the TRISE register (TRISE<2:0>) must be configured as inputs (set). The configuration bits, PCFG3:PCFG0 (ADCON1<3:0>) must be configured to make pins RE2:RE0 as digital I/O.

A write to the PSP occurs when both the  $\overline{CS}$  and  $\overline{WR}$  lines are first detected low. A read from the PSP occurs when both the  $\overline{CS}$  and  $\overline{RD}$  lines are first detected low.

### FIGURE 3-13: PORTD AND PORTE BLOCK DIAGRAM (PARALLEL SLAVE PORT)





# FIGURE 3-14: PARALLEL SLAVE PORT WRITE WAVEFORMS



# FIGURE 3-15: PARALLEL SLAVE PORT READ WAVEFORMS

# TABLE 3-11 REGISTERS ASSOCIATED WITH PARALLEL SLAVE PORT

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
08h	PORTD	Port dat	ta latch w	hen writte	en: Port pins v	vhen read	I			xxxx xxxx	uuuu uuuu
09h	PORTE	—	—	—	—	—	RE2	RE1	RE0	xxx	uuu
89h	TRISE	IBF	OBF	IBOV	PSPMODE	_	PORTE I	Data Direc	tion Bits	0000 -111	0000 -111
0Ch	PIR1	PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
9Fh	ADCON1	ADFM	VCFG2	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the Parallel Slave Port.

# 6.0 TIMER2 MODULE

The Timer2 module timer has the following features:

- 8-bit timer (TMR2 register)
- 8-bit period register (PR2)
- · Readable and writable (Both registers)
- Software programmable prescaler (1:1, 1:4, 1:16)
- Software programmable postscaler (1:1 to 1:16)
- Interrupt on TMR2 match of PR2
- SSP module optional use of TMR2 output to generate clock shift

Timer2 has a control register, shown in Figure 6-1. Timer2 can be shut off by clearing control bit TMR2ON (T2CON<2>) to minimize power consumption.

Figure 6-2 is a simplified block diagram of the Timer2 module.

Additional information on timer modules is available in the PICmicro<sup>™</sup> Mid-Range Reference Manual, (DS33023).

# 6.1 <u>Timer2 Operation</u>

Timer2 can be used as the PWM time-base for PWM mode of the CCP module.

The TMR2 register is readable and writable, and is cleared on any device reset.

The input clock (Fosc/4) has a prescale option of 1:1, 1:4 or 1:16, selected by control bits T2CKPS1:T2CKPS0 (T2CON<1:0>).

The match output of TMR2 goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling inclusive) to generate a TMR2 interrupt (latched in flag bit TMR2IF, (PIR1<1>)).

The prescaler and postscaler counters are cleared when any of the following occurs:

- a write to the TMR2 register
- · a write to the T2CON register
- any device reset (Power-on Reset, MCLR reset, Watchdog Timer reset, or Brown-out Reset)

TMR2 is not cleared when T2CON is written.

# FIGURE 6-1: T2CON: TIMER2 CONTROL REGISTER (ADDRESS 12h)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
_	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	R = Readable bit
bit7							bit0	<ul> <li>W = Writable bit</li> <li>U = Unimplemented bit, read as '0'</li> <li>n = Value at POR reset</li> </ul>
bit 7:	Unimplem	ented: Rea	d as '0'					
bit 6-3:	TOUTPS3: 0000 = 1:1 0001 = 1:2 • • 1111 = 1:1	TOUTPS0: Postscale Postscale 6 Postscale	Timer2 Ou	tput Postsca	ale Select bi	ts		
bit 2:	<b>TMR2ON</b> : 1 = Timer2 0 = Timer2	Timer2 On I is on is off	bit					
bit 1-0:	<b>T2CKPS1:</b> 00 = Presc 01 = Presc 1x = Presc	T2CKPS0: caler is 1 caler is 4 caler is 16	Timer2 Clo	ock Prescale	Select bits			

# 7.3 PWM Mode

In Pulse Width Modulation (PWM) mode, the CCP1 pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORTC data latch, the TRISC<2> bit must be cleared to make the CCP1 pin an output.

Note:	Clearing the CCP1CON register will force
	the CCP1 PWM output latch to the default
	low level. This is not the PORTC I/O data
	latch.

Figure 7-4 shows a simplified block diagram of the CCP module in PWM mode.

For a step by step procedure on how to set up the CCP module for PWM operation, see Section 7.3.3.

### FIGURE 7-4: SIMPLIFIED PWM BLOCK DIAGRAM



A PWM output (Figure 7-5) has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/ period).

### FIGURE 7-5: PWM OUTPUT



### 7.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

PWM period = [(PR2) + 1] • 4 • TOSC • (TMR2 prescale value)

PWM frequency is defined as 1 / [PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

Note:	The Timer2 postscaler (see Section 6.0) is
	not used in the determination of the PWM
	frequency. The postscaler could be used to
	have a servo update rate at a different fre-
	quency than the PWM output.

### 7.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available: the CCPR1L contains the eight MSbs and the CCP1CON<5:4> contains the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle in time:

#### PWM duty cycle = (CCPR1L:CCP1CON<5:4>) • Tosc • (TMR2 prescale value)

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2 concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

Maximum PWM resolution (bits) for a given PWM frequency:

$$= \frac{\log\left(\frac{FOSC}{FPWM}\right)}{\log(2)} \quad \text{bits}$$

**Note:** If the PWM duty cycle value is longer than the PWM period the CCP1 pin will not be cleared.

For an example PWM period and duty cycle calculation, see the PICmicro<sup>™</sup> Mid-Range Reference Manual, (DS33023).

#### 7.3.3 SET-UP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

- 1. Set the PWM period by writing to the PR2 register.
- 2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
- 3. Make the CCP1 pin an output by clearing the TRISC<2> bit.
- 4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
- 5. Configure the CCP1 module for PWM operation.

# TABLE 7-4 EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 20 MHz

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	5.5

### TABLE 7-5 REGISTERS ASSOCIATED WITH PWM AND TIMER2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
87h	TRISC	PORTC D	ata Directio	n Register						1111 1111	1111 1111
11h	TMR2	Timer2 mo	dule's registe	ər						0000 0000	0000 0000
92h	PR2	Timer2 mo	dule's perioc	l register						1111 1111	1111 1111
12h	T2CON	_	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/Co	Capture/Compare/PWM register1 (LSB)								uuuu uuuu
16h	CCPR1H	Capture/Co	Capture/Compare/PWM register1 (MSB)								uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by PWM and Timer2.

Note 1: Bits PSPIE and PSPIF are reserved on the 28-pin, always maintain these bits clear.

# 8.2 MSSP I<sup>2</sup>C Operation

The MSSP module in I<sup>2</sup>C mode fully implements all master and slave functions (including general call support) and provides interrupts on start and stop bits in hardware to determine a free bus (multi-master function). The MSSP module implements the standard mode specifications as well as 7-bit and 10-bit addressing.

Refer to Application Note AN578, "Use of the SSP Module in the I<sup>2</sup>C Multi-Master Environment."

A "glitch" filter is on the SCL and SDA pins when the pin is an input. This filter operates in both the 100 kHz and 400 kHz modes. In the 100 kHz mode, when these pins are an output, there is a slew rate control of the pin that is independent of device frequency.





### FIGURE 8-11: I<sup>2</sup>C MASTER MODE BLOCK DIAGRAM



Two pins are used for data transfer. These are the SCL pin, which is the clock, and the SDA pin, which is the data. The SDA and SCL pins that are automatically configured when the  $l^2C$  mode is enabled. The SSP module functions are enabled by setting SSP Enable bit SSPEN (SSPCON<5>).

The MSSP module has six registers for  ${\rm I}^2 C$  operation. They are the:

- SSP Control Register (SSPCON)
- SSP Control Register2 (SSPCON2)
- SSP Status Register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- SSP Shift Register (SSPSR) Not directly accessible
- SSP Address Register (SSPADD)

The SSPCON register allows control of the I<sup>2</sup>C operation. Four mode selection bits (SSPCON<3:0>) allow one of the following I<sup>2</sup>C modes to be selected:

- I<sup>2</sup>C Slave mode (7-bit address)
- I<sup>2</sup>C Slave mode (10-bit address)
- I<sup>2</sup>C Master mode, clock = OSC/4 (SSPADD +1)

Before selecting any  $I^2C$  mode, the SCL and SDA pins must be programmed to inputs by setting the appropriate TRIS bits. Selecting an  $I^2C$  mode, by setting the SSPEN bit, enables the SCL and SDA pins to be used as the clock and data lines in  $I^2C$  mode.

### 8.2.5 MASTER MODE

Master mode of operation is supported by interrupt generation on the detection of the START and STOP conditions. The STOP (P) and START (S) bits are cleared from a reset or when the MSSP module is disabled. Control of the  $l^2C$  bus may be taken when the P bit is set, or the bus is idle with both the S and P bits clear.

In master mode, the SCL and SDA lines are manipulated by the MSSP hardware.

The following events will cause SSP Interrupt Flag bit, SSPIF, to be set (SSP Interrupt if enabled):

- START condition
- STOP condition
- Data transfer byte transmitted/received
- Acknowledge transmit
- Repeated Start



# FIGURE 8-17: SSP BLOCK DIAGRAM (I<sup>2</sup>C MASTER MODE)



FIGURE 8-23: REPEATED START CONDITION FLOWCHART (PAGE 1)

### 8.2.12 I<sup>2</sup>C MASTER MODE RECEPTION

Master mode reception is enabled by programming the receive enable bit, RCEN (SSPCON2<3>).

Note:	The SSP Module must be in an IDLE
	STATE before the RCEN bit is set, or the
	RCEN bit will be disregarded.

The baud rate generator begins counting, and on each rollover, the state of the SCL pin changes (high to low/ low to high) and data is shifted into the SSPSR. After the falling edge of the eighth clock, the receive enable flag is automatically cleared, the contents of the SSPSR are loaded into the SSPBUF, the BF flag is set, the SSPIF is set, and the baud rate generator is suspended from counting, holding SCL low. The SSP is now in IDLE state, awaiting the next command. When the buffer is read by the CPU, the BF flag is automatically cleared. The user can then send an acknowledge bit at the end of reception, by setting the acknowledge sequence enable bit, AKEN (SSPCON2<4>).

#### 8.2.12.10 BF STATUS FLAG

In receive operation, BF is set when an address or data byte is loaded into SSPBUF from SSPSR. It is cleared when SSPBUF is read.

#### 8.2.12.11 SSPOV STATUS FLAG

In receive operation, SSPOV is set when 8 bits are received into the SSPSR, and the BF flag is already set from a previous reception.

### 8.2.12.12 WCOL STATUS FLAG

If the user writes the SSPBUF when a receive is already in progress (i.e. SSPSR is still shifting in a data byte), then WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

# 10.0 VOLTAGE REFERENCE MODULE AND LOW-VOLTAGE DETECT

The Voltage Reference module provides reference voltages for the Brown-out Reset circuitry, the Low-voltage Detect circuitry and the A/D converter. The source for the reference voltages comes from the bandgap reference circuit. The bandgap circuit is energized anytime the reference voltage is required by the other sub-modules, and is powered down when not in use. The control registers for this module are LVDCON and REFCON, as shown in Figure 10-1 and Figure 10-2.

#### U-0 U-0 R-0 R/W-0 R/W-0 **R/W-1** R/W-0 **R/W-1** BGST LVDEN LV3 LV2 LV1 LV0 R = Readable bit W = Writable bit U = Unimplemented bit, bit7 bit0 read as '0' - n =Value at POR reset bit 7-6: Unimplemented: Read as '0' bit 5: BGST: Bandgap Stable Status Flag bit 1 = Indicates that the bandgap voltage is stable, and LVD interrupt is reliable 0 = Indicates that the bandgap voltage is not stable, and LVD interrupt should not be enabled LVDEN: Low-voltage Detect Power Enable bit bit 4: 1 = Enables LVD, powers up bandgap circuit and reference generator 0 = Disables LVD, powers down bandgap circuit if unused by BOR or VRH/VRL bit 3-0: LV3:LV0: Low Voltage Detection Limit bits (1) 1111 = External analog input is used 1110 = 4.5V1101 = 4.2V1100 = 4.0V 1011 = 3.8V1010 = 3.6V1001 = 3.5V1000 = 3.3V0111 = 3.0V 0110 = 2.8V 0101 = 2.7V 0100 = 2.5VNote 1: These are the minimum trip points for the LVD, see Table 15-3 for the trip point tolerances. Selection of an unused setting may result in an inadvertant interrupt.

# FIGURE 10-1: LVDCON: LOW-VOLTAGE DETECT CONTROL REGISTER

# 11.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The analog-to-digital (A/D) converter module has six inputs for the PIC16C773 and ten for the PIC16C774.

The analog-to-digital converter (A/D) allows conversion of an analog input signal to a corresponding 12-bit digital number. The A/D module has up to 10 analog inputs, which are multiplexed into one sample and hold. The output of the sample and hold is the input into the converter, which generates the result via successive approximation. The analog reference voltages are software selectable to either the device's analog positive and negative supply voltages (AVDD/AVSS), the voltage level on the VREF+ and VREF- pins, or internal voltage references if available (VRH, VRL).

The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode. To operate in sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The A/D module has four registers. These registers are:

- A/D Result Register Low ADRESL
- A/D Result Register High ADRESH
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)

A device reset forces all registers to their reset state. This forces the A/D module to be turned off and any conversion is aborted.

### 11.1 Control Registers

The ADCON0 register, shown in Figure 11-1, controls the operation of the A/D module. The ADCON1 register, shown in Figure 11-2, configures the functions of the port pins, the voltage reference configuration and the result format. The port pins can be configured as analog inputs or as digital I/O.

The combination of the ADRESH and ADRESL registers contain the result of the A/D conversion. The register pair is referred to as the ADRES register. When the A/D conversion is complete, the result is loaded into ADRES, the GO/DONE bit (ADCON0<2>) is cleared, and the A/D interrupt flag ADIF is set. The block diagram of the A/D module is shown in Figure 11-3.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	CHS3	ADON	R =	Readable bit		
bit7							bit 0	• n =	Value at POR reset		
bit 7:6	ADCS1:ADCS0: A/D Conversion Clock Select bits 00 = Fosc/2 01 = Fosc/8 10 = Fosc/32 11 = FRC (clock derived from an RC oscillator = 1 MHz max)										
bit 5:3,1	bit 5:3,1 <b>CHS3:CHS0:</b> Analog Channel Select bits 0000 = channel 00 (AN0) 0001 = channel 01 (AN1) 0010 = channel 02 (AN2) 0011 = channel 03 (AN3) 0100 = channel 04 (AN4) (Reserved on 28-pin devices, do not use) 0101 = channel 05 (AN5) (Reserved on 28-pin devices, do not use) 0110 = channel 06 (AN6) (Reserved on 28-pin devices, do not use) 0111 = channel 07 (AN7) (Reserved on 28-pin devices, do not use) 0111 = channel 07 (AN7) (Reserved on 28-pin devices, do not use) 0110 = channel 08 (AN8) 1000 = channel 08 (AN8) 1001 = channel 09 (AN9)										
bit 2:	<b>GO/DONE:</b> A/D Conversion Status bit 1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle. This bit is automatically cleared by hardware when the A/D conversion has completed. 0 = A/D conversion completed/not in progress										
bit 0:	<b>ADON:</b> A/ 1 = A/D cc 0 = A/D cc	D On bit onverter m onverter is	odule is o shutoff ar	perating nd consum	nes no operatir	ng current					

# FIGURE 11-1: ADCON0 REGISTER (ADDRESS 1Fh).

# 11.10 A/D Operation During Sleep

The A/D module can operate during SLEEP mode. This requires that the A/D clock source be configured for RC (ADCS1:ADCS0 = 11b). With the RC clock source selected, when the GO/DONE bit is set the A/D module waits one instruction cycle before starting the conversion cycle. This allows the SLEEP instruction to be executed, which eliminates all digital switching noise during the sample and conversion. When the conversion cycle is completed the GO/DONE bit is cleared, and the result loaded into the ADRESH and ADRESL registers. If the A/D interrupt is enabled, the device will wake-up from SLEEP. If the A/D interrupt is not enabled, the ADON bit will remain set.

When the A/D clock source is another clock option (not RC), a SLEEP instruction causes the present conversion to be aborted and the A/D module is turned off, though the ADON bit will remain set.

Turning off the A/D places the A/D module in its lowest current consumption state.

Note:	For the A/D module to operate in SLEEP,
	the A/D clock source must be configured to
	RC (ADCS1:ADCS0 = $11b$ ).

### 11.11 Connection Considerations

Since the analog inputs employ ESD protection, they have diodes to VDD and Vss. This requires that the analog input must be between VDD and Vss. If the input voltage exceeds this range by greater than 0.3V (either direction), one of the diodes becomes forward biased and it may damage the device if the input current specification is exceeded.

An external RC filter is sometimes added for anti-aliasing of the input signal. The R component should be selected to ensure that the total source impedance is kept under the 2.5 k $\Omega$  recommended specification. Any external components connected (via hi-impedance) to an analog input pin (capacitor, zener diode, etc.) should have very little leakage current at the pin.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
1Eh	ADRESH	A/D High B	yte Result	Register				·		xxxx xxxx	uuuu uuuu
9Eh	ADRESL	A/D Low By	/te Result	Register						xxxx xxxx	uuuu uuuu
9Bh	REFCON	VRHEN	VRLEN	VRHOEN	VRLOEN	_	_	_	_	0000	0000
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	CHS3	ADON	0000 0000	0000 0000
9Fh	ADCON1	ADFM	VCFG2	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	0000 0000	0000 0000
05h	PORTA	—	_	PORTA5 <sup>(2)</sup>	PORTA Data	Latch wher	n written: POR	TA<4:0> pins	when read	0x 0000	0u 0000
06h	PORTB	PORTB Da	ta Latch w	hen written:	PORTB pins w	hen read				xxxx 11xx	uuuu 11uu
09h <sup>(2)</sup>	PORTE	—	_	-	_	—	RE2	RE1	RE0	000	000
85h	TRISA	— — bit5 <sup>(2)</sup> PORTA Data Direction Register								11 1111	11 1111
86h	TRISB	PORTB Da	ta Directio	n Register						1111 1111	1111 1111
89h(2)	TRISE	IBE	OBE	IBOV	PSPMODE	_	PORTE Data	Direction Bit	•	0000 -111	0000 -111

### TABLE 11-3 SUMMARY OF A/D REGISTERS

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used for A/D conversion.

Note 1: Bits PSPIE and PSPIF are reserved on the 28-pin devices, always maintain these bits clear.

2: These bits/registers are not implemented on the 28-pin devices, read as '0'.

				<u> </u>	
Register	Devices		Power-on Reset, Brown-out Reset	MCLR Resets WDT Reset	Wake-up via WDT or Interrupt
TRISA	773	774	1 1111	1 1111	u uuuu
THIOA	773	774	11 1111	11 1111	uu uuuu
TRISB	773	774	1111 1111	1111 1111	uuuu uuuu
TRISC	773	774	1111 1111	1111 1111	uuuu uuuu
TRISD	773	774	1111 1111	1111 1111	uuuu uuuu
TRISE	773	774	0000 -111	0000 -111	uuuu -uuu
PIE1	773	774	r000 0000	r000 0000	ruuu uuuu
	773	774	0000 0000	0000 0000	uuuu uuuu
PIE2	773	774	00	00	u uu
PCON	773	774	dd	uu	uu
PR2	773	774	1111 1111	1111 1111	1111 1111
SSPADD	773	774	0000 0000	0000 0000	uuuu uuuu
SSPSTAT	773	774	0000 0000	0000 0000	uuuu uuuu
TXSTA	773	774	0000 -010	0000 -010	uuuu -uuu
SPBRG	773	774	0000 0000	0000 0000	uuuu uuuu
REFCON	773	774	0000	0000	uuuu
LVDCON	773	774	00 0101	00 0101	uu uuuu
ADRESL	773	774	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON1	773	774	0000 000	0000 0000	uuuu uuuu

TABLE 12-6	INITIALIZATION	CONDITIONS FOR	ALL REGISTERS	(Cont.'d)
------------	----------------	----------------	---------------	-----------

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

Note 1: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 12-5 for reset value for specific condition.

### FIGURE 12-7: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD)



# 13.0 INSTRUCTION SET SUMMARY

Each PIC16CXXX instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16CXX instruction set summary in Table 13-2 lists **byte-oriented**, **bit-oriented**, and **literal and control** operations. Table 13-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an eight or eleven bit constant or literal value.

### TABLE 13-1 OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
PC	Program Counter
TO	Time-out bit
PD	Power-down bit

The instruction set is highly orthogonal and is grouped into three basic categories:

- · Byte-oriented operations
- Bit-oriented operations
- · Literal and control operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1  $\mu$ s. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2  $\mu$ s. Table 13-2 lists the instructions recognized by the MPASM assembler.

Figure 13-1 shows the general formats that the instructions can have.

Note:	To maintain upward compatibility with								
	future PIC16CXXX products, do not use								
	He OPTION and TRIS instructions.								

All examples use the following format to represent a hexadecimal number:

0xhh

where h signifies a hexadecimal digit.

### FIGURE 13-1: GENERAL FORMAT FOR INSTRUCTIONS



A description of each instruction is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

# TABLE 13-2 PIC16CXXX INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode				Status	Notes
				MSb			LSb	Affected	
BYTE-ORIE	NTED I	FILE REGISTER OPERATIONS							
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	С	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	С	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENT	ED FIL	E REGISTER OPERATIONS							
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
LITERAL AN	ND COI	NTROL OPERATIONS							
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	TO,PD	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into standby mode	1	00	0000	0110	0011	TO,PD	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

### 15.5.2 TIMING DIAGRAMS AND SPECIFICATIONS



# TABLE 15-5 EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter	Sym	Characteristic	Min	Typt	Max	Units	Conditions
NO.			<u> </u>				
	Fosc	External CLKIN Frequency	>dC>	$\langle \rightarrow \rangle$	4	MHz	XT and RC osc mode
		(Note 1)	DC.	[ ≻`	4	MHz	HS osc mode (-04)
			DC	~ —	20	MHz	HS osc mode (-20)
		$\sim$	DC	_	200	kHz	LP osc mode
		Oscillator Frequency	DC	_	4	MHz	RC osc mode
	$\langle \langle \rangle$	(Note 1)	0.1	_	4	MHz	XT osc mode
		$\land \land \land \land \checkmark$	4	—	20	MHz	HS osc mode
			5	—	200	kHz	LP osc mode
1	Tosc	External CLKIN Period	250	_	-	ns	XT and RC osc mode
		(Note 1)	250	_	—	ns	HS osc mode (-04)
			50	—	—	ns	HS osc mode (-20)
	$\sim$		5	_	—	μs	LP osc mode
		Oscillator Period	250	_	—	ns	RC osc mode
		(Note 1)	250	_	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (-04)
			50	—	250	ns	HS osc mode (-20)
			5	—	—	μs	LP osc mode
2	Тсү	Instruction Cycle Time (Note 1)	200	Тсү	DC	ns	TCY = 4/FOSC
3*	TosL,	External Clock in (OSC1) High or	100	—	-	ns	XT oscillator
	TosH	Low Time	2.5	—	—	μs	LP oscillator
			15	—	—	ns	HS oscillator
4*	TosR,	External Clock in (OSC1) Rise or	—	—	25	ns	XT oscillator
	TosF	Fall Time	_	—	50	ns	LP oscillator
			_	_	15	ns	HS oscillator

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TcY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

# 17.7 K04-014 40-Lead Ceramic Dual In-line with Window (JW) – 600 mil

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*		MILLIMETERS			
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.600			15.24	
Number of Pins	n		40			40	
Pitch	р	0.098	0.100	0.102	2.49	2.54	2.59
Lower Lead Width	В	0.016	0.020	0.023	0.41	0.50	0.58
Upper Lead Width	B1	0.050	0.053	0.055	1.27	1.33	1.40
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	с	0.008	0.011	0.014	0.20	0.28	0.36
Top to Seating Plane	A	0.190	0.205	0.220	4.83	5.21	5.59
Top of Lead to Seating Plane	A1	0.117	0.135	0.153	2.97	3.43	3.89
Base to Seating Plane	A2	0.030	0.045	0.060	0.00	1.14	1.52
Tip to Seating Plane	L	0.135	0.140	0.145	3.43	3.56	3.68
Package Length	D	2.040	2.050	2.060	51.82	52.07	52.32
Package Width	E	0.514	0.520	0.526	13.06	13.21	13.36
Radius to Radius Width E1		0.560	0.580	0.600	14.22	14.73	15.24
Overall Row Spacing	eB	0.610	0.660	0.710	15.49	16.76	18.03
Window Diameter V		0.340	0.350	0.360	8.64	8.89	9.14

\* Controlling Parameter.

#### Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not
  mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

# QUALITY MANAGEMENT SYSTEM CERTIFIED BY DNV = ISO/TS 16949=

#### Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, KEELoo, KEELoo logo, MPLAB, PIC, PICmicro, PICSTART, PIC<sup>32</sup> logo, rfPIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MTP, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

Analog-for-the-Digital Age, Application Maestro, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniscient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICtail, REAL ICE, rfLAB, Select Mode, SQI, Serial Quad I/O, Total Endurance, TSHARC, UniWinDriver, WiperLock, ZENA and Z-Scale are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

GestIC and ULPP are registered trademarks of Microchip Technology Germany II GmbH & Co. & KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 1999-2013, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.

ISBN: 9781620769263

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELC0® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

# Worldwide Sales and Service

### AMERICAS

Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tei: 480-792-7200 Fax: 480-792-7277 Technical Support: http://www.microchip.com/ support Web Address: www.microchip.com

Atlanta Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455

Boston Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088

Chicago Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075

**Cleveland** Independence, OH Tel: 216-447-0464 Fax: 216-447-0643

**Dallas** Addison, TX Tel: 972-818-7423 Fax: 972-818-2924

Detroit Farmington Hills, MI Tel: 248-538-2250 Fax: 248-538-2260

Indianapolis Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453

Los Angeles Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608

Santa Clara Santa Clara, CA Tel: 408-961-6444 Fax: 408-961-6445

Toronto Mississauga, Ontario, Canada Tel: 905-673-0699 Fax: 905-673-6509

### ASIA/PACIFIC

Asia Pacific Office Suites 3707-14, 37th Floor Tower 6, The Gateway Harbour City, Kowloon Hong Kong Tel: 852-2401-1200 Fax: 852-2401-3431 Australia - Sydney

Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

**China - Beijing** Tel: 86-10-8569-7000 Fax: 86-10-8528-2104

**China - Chengdu** Tel: 86-28-8665-5511 Fax: 86-28-8665-7889

China - Chongqing Tel: 86-23-8980-9588 Fax: 86-23-8980-9500

**China - Hangzhou** Tel: 86-571-2819-3187 Fax: 86-571-2819-3189

**China - Hong Kong SAR** Tel: 852-2943-5100 Fax: 852-2401-3431

China - Nanjing Tel: 86-25-8473-2460 Fax: 86-25-8473-2470

**China - Qingdao** Tel: 86-532-8502-7355 Fax: 86-532-8502-7205

**China - Shanghai** Tel: 86-21-5407-5533 Fax: 86-21-5407-5066

**China - Shenyang** Tel: 86-24-2334-2829 Fax: 86-24-2334-2393

**China - Shenzhen** Tel: 86-755-8864-2200 Fax: 86-755-8203-1760

**China - Wuhan** Tel: 86-27-5980-5300 Fax: 86-27-5980-5118

China - Xian Tel: 86-29-8833-7252 Fax: 86-29-8833-7256

**China - Xiamen** Tel: 86-592-2388138 Fax: 86-592-2388130

**China - Zhuhai** Tel: 86-756-3210040 Fax: 86-756-3210049

### ASIA/PACIFIC

India - Bangalore Tel: 91-80-3090-4444 Fax: 91-80-3090-4123

India - New Delhi Tel: 91-11-4160-8631 Fax: 91-11-4160-8632

India - Pune Tel: 91-20-2566-1512 Fax: 91-20-2566-1513

Japan - Osaka Tel: 81-6-6152-7160 Fax: 81-6-6152-9310

Japan - Tokyo Tel: 81-3-6880- 3770 Fax: 81-3-6880-3771

Korea - Daegu Tel: 82-53-744-4301 Fax: 82-53-744-4302

Korea - Seoul Tel: 82-2-554-7200 Fax: 82-2-558-5932 or 82-2-558-5934

Malaysia - Kuala Lumpur Tel: 60-3-6201-9857 Fax: 60-3-6201-9859

Malaysia - Penang Tel: 60-4-227-8870 Fax: 60-4-227-4068

Philippines - Manila Tel: 63-2-634-9065 Fax: 63-2-634-9069

Singapore Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan - Hsin Chu Tel: 886-3-5778-366 Fax: 886-3-5770-955

Taiwan - Kaohsiung Tel: 886-7-213-7828 Fax: 886-7-330-9305

Taiwan - Taipei Tel: 886-2-2508-8600 Fax: 886-2-2508-0102

**Thailand - Bangkok** Tel: 66-2-694-1351 Fax: 66-2-694-1350

### EUROPE

Austria - Wels Tel: 43-7242-2244-39 Fax: 43-7242-2244-393

**Denmark - Copenhagen** Tel: 45-4450-2828 Fax: 45-4485-2829

France - Paris Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

**Germany - Munich** Tel: 49-89-627-144-0 Fax: 49-89-627-144-44

Italy - Milan Tel: 39-0331-742611 Fax: 39-0331-466781

Netherlands - Drunen Tel: 31-416-690399 Fax: 31-416-690340

**Spain - Madrid** Tel: 34-91-708-08-90 Fax: 34-91-708-08-91

**UK - Wokingham** Tel: 44-118-921-5869 Fax: 44-118-921-5820