Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	15376
Total RAM Bits	423936
Number of I/O	496
Number of Gates	1250000
Voltage - Supply	2.3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	680-LBGA
Supplier Device Package	680-FPSBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx1200b-04fe680c

ispXPGA® Family

Includes High-Performance, Low-Cost "E-Series"

February 2010

Data Sheet DS1026

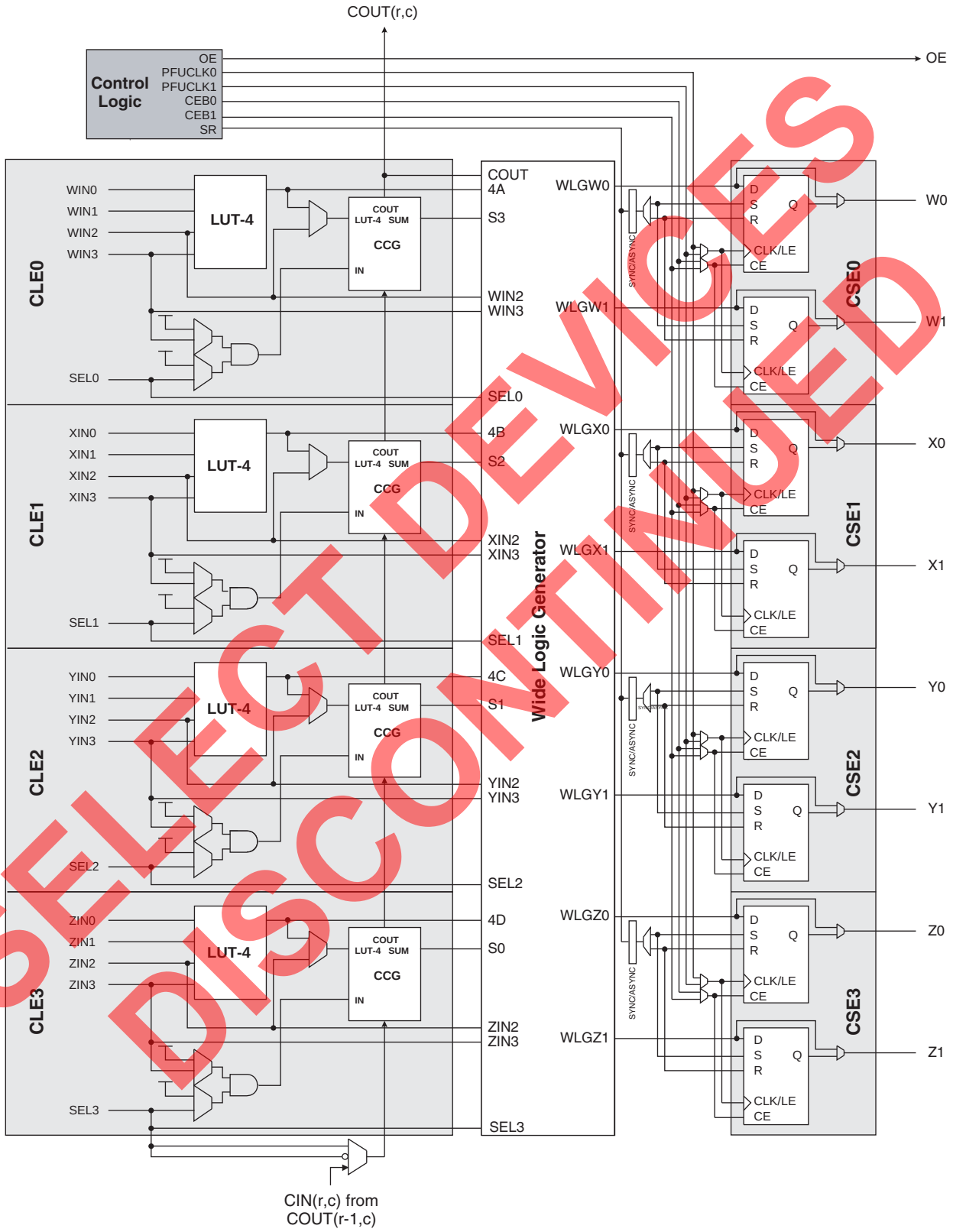
- **Non-volatile, Infinitely Reconfigurable**
  - Instant-on - Powers up in microseconds via on-chip E²CMOS® based memory
  - No external configuration memory
  - Excellent design security, no bit stream to intercept
  - Reconfigure SRAM based logic in milliseconds
- **High Logic Density for System-level Integration**
  - 139K to 1.25M functional gates
  - 160 to 496 I/O
  - 1.8V, 2.5V, and 3.3V V_{CC} operation
  - Up to 414Kb sysMEM™ embedded memory
- **High Performance Programmable Function Unit (PFU)**
  - Four LUT-4 per PFU supports wide and narrow functions
  - Dual flip-flops per LUT-4 for extensive pipelining
  - Dedicated logic for adders, multipliers, multiplexers, and counters
- **Flexible Memory Resources**
  - Multiple sysMEM Embedded RAM Blocks
    - Single port, Dual port, and FIFO operation
  - 64-bit distributed memory in each PFU
    - Single port, Double port, FIFO, and Shift Register operation
- **Flexible Programming, Reconfiguration, and Testing**
  - Supports IEEE 1532 and 1149.1
  - Microprocessor configuration interface
  - Program E²CMOS while operating from SRAM
- **Eight sysCLOCK™ Phase Locked Loops (PLLs) for Clock Management**
  - True PLL technology
  - 10MHz to 320MHz operation
  - Clock multiplication and division
  - Phase adjustment
  - Shift clocks in 250ps steps
- **sysIO™ for High System Performance**
  - High speed memory support through SSTL and HSTL
  - Advanced buses supported through PCI, GTL+, LVDS, BLVDS, and LVPECL
  - Standard logic supported through LVTTL, LVCMOS 3.3, 2.5 and 1.8
  - 5V tolerant I/O for LVCMOS 3.3 and LVTTL interfaces
  - Programmable drive strength for series termination
  - Programmable bus maintenance
- **Two Options Available**
  - High-performance sysHSI (standard part number)
  - Low-cost, no sysHSI ("E-Series")
- **sysHSI™ Capability for Ultra Fast Serial Communications**
  - Up to 800Mbps performance
  - Up to 20 channels per device
  - Built in Clock Data Recovery (CDR) and Serialization and De-serialization (SERDES)

Table 1. ispXPGA Family Selection Guide

	ispXPGA 125/E	ispXPGA 200/E	ispXPGA 500/E	ispXPGA 1200/E[3]
Functional Gates	139K	210K	476K	1.25M
PFUs	484	676	1764	3844
LUT-4s	1936	2704	7056	15376
Logic FFs	3.8K	5.4K	14.1K	30.7K
sysMEM Memory	92K	111K	184K	414K
Distributed Memory	30K	43K	112K	246K
EBR	20	24	40	90
sysHSI Channels[1]	4	8	12	20
User I/O	160/176	160/208	336	496
Packaging	256 fpBGA 516 fpBGA[2]	256 fpBGA 516 fpBGA[2]	516 fpBGA[2] 900 fpBGA	680 fpSBGA 900 fpBGA

1. "E-Series" does not support sysHSI.
2. FH516 package was converted to F516 via PCN #09A-08.
3. Discontinued via PCN #03A-10.

Figure 2. ispXPGA PFU



The second type of interface implemented is the terminated, single-ended interface standard. This group of interfaces includes different versions of SSTL and HSTL interfaces along with CTT, and GTL+. Usage of these particular I/O interfaces requires an additional V_{REF} signal. At the system level a termination voltage, V_{TT}, is also required. Typically an output will be terminated to V_{TT} at the receiving end of the transmission line it is driving.

The third type of interface standards are the differential standards LVDS, BLVDS, and LVPECL. The differential standards require two I/O pins to create the differential pair. The logic level is determined by the difference in the two signals. Table 6 lists how these interface standards are implemented in the ispXPGA devices.

For more information on sysIO capability, refer to TN1000, sysIO Usage Guidelines for Lattice Devices.

Figure 19. sysIO Banks per Device

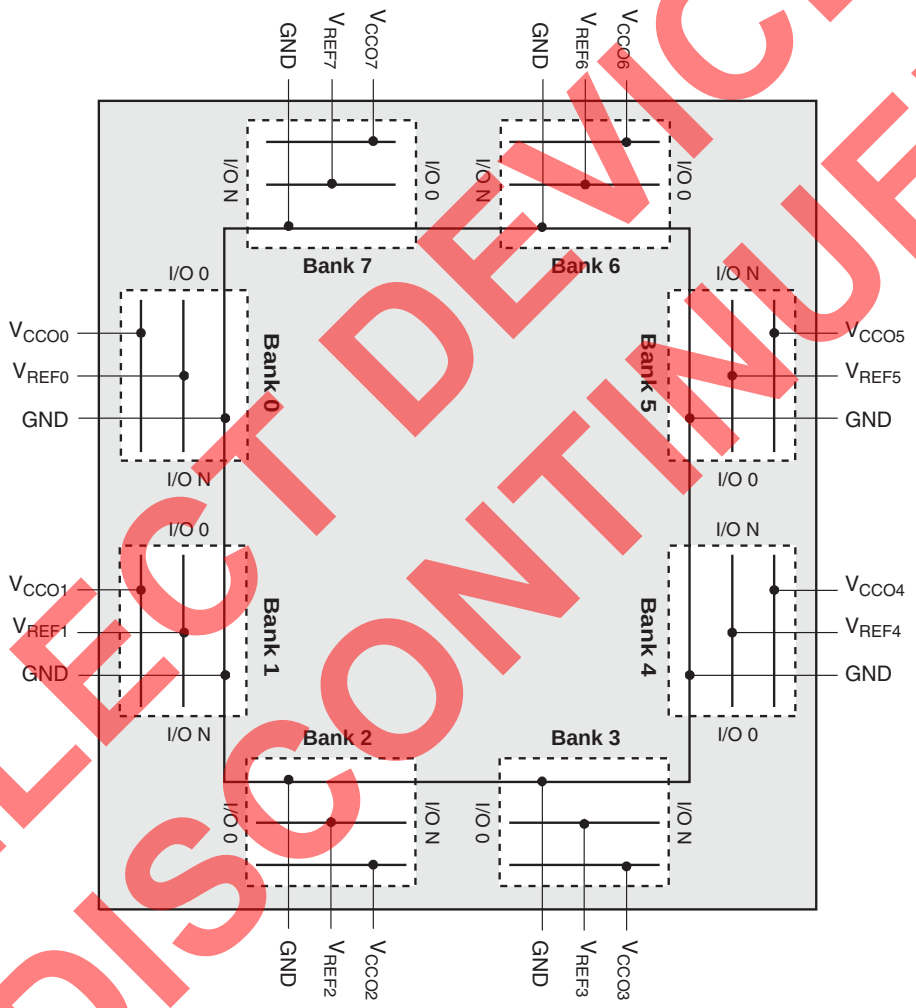


Table 4. Number of I/Os per Bank

Device	Max. Number of I/Os per Bank (N)
XPGA 1200	62
XPGA 500	42
XPGA 200	26
XPGA 125	22

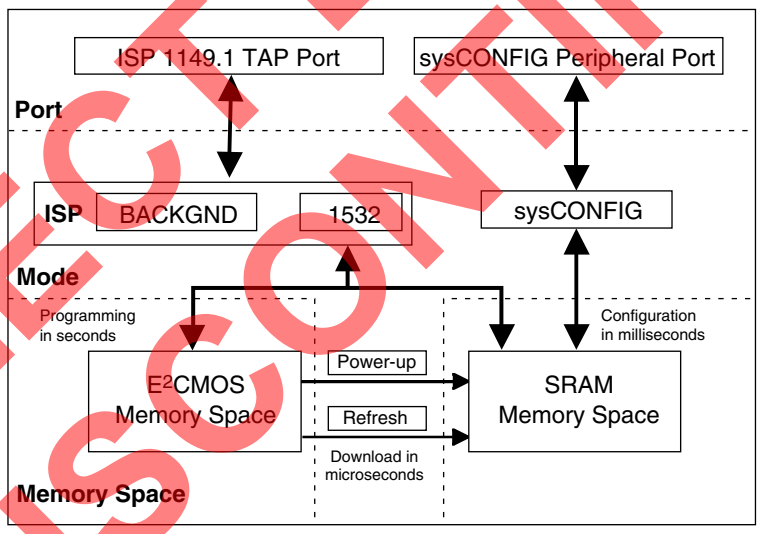
Configuration and Programming

The ispXPGA family of devices takes a unique approach to FPGA configuration memory. It contains two types of memory, Static RAM and non-volatile E²CMOS cells. The static RAM is used to control the functionality of the device during normal operation and the E²CMOS memory cells are used to load the SRAM. The E²CMOS memory module can be thought of as the hard drive for the ispXPGA configuration and the SRAM as the working configuration memory. There is a one-to-one relationship between SRAM memory and the E²CMOS cells. The SRAM can be configured either from the E²CMOS memory or from an external source, as shown in Figure 21.

Figure 21 shows the different ports and modes that are used in the configuration and programming of the ispXPGA devices. There are two possible ports that can be used for configuration of the SRAM memory: the ISP port which supports the IEEE 1149.1 Test Access Port (TAP) Std., accommodates bit-wide configuration. The sysCONFIG port allows byte-wide configuration of the SRAM configuration memory. When programming the E²CMOS memory, only the 1149.1 TAP can be used.

Configuration and programming done through the 1149.1 Test Access Port (TAP) supports both the IEEE Std. 1149.1 Boundary Scan TAP specification and the IEEE Std. 1532 In-System Configuration specification. To configure or program the device using the 1149.1 TAP the device must be in the ISP mode. To configure the SRAM memory using the sysCONFIG Port, the device must be in the sysCONFIG mode. Upon power-up, the device's SRAM memory can be configured either from the E²CMOS memory or from an external source through the sysCONFIG mode. Additionally, the SRAM can be re-configured from the E²CMOS memory by executing a "REFRESH." See TN1026, ispXP Configuration Usage Guidelines, for more in depth information on the different programming modes, timing and wake-up.

Figure 21. ispXP Block Diagram



Supports IEEE 1149.1 Boundary Scan Testability

All ispXPGA devices have boundary scan cells and supports the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal boundary scan registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board level testing.

Security Scheme

A programmable security scheme is provided on the ispXPGA devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, the security scheme prevents read-back of the programmed

sysIO Recommended Operating Conditions

Standard	V_{CCO} (V)[1]			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.0	3.3	3.6	-	-	-
LVCMOS 2.5	2.3	2.5	2.7	-	-	-
LVCMOS 1.8[2]	1.65	1.8	1.95	-	-	-
LVTTL	3.0	3.3	3.6	-	-	-
PCI 3.3	3.0	3.3	3.6	-	-	-
AGP-1X	3.15	3.3	3.45	-	-	-
SSTL 2	2.3	2.5	2.7	1.15	1.25	1.35
SSTL 3	3.0	3.3	3.6	1.3	1.5	1.7
CTT 3.3	3.0	3.3	3.6	1.35	1.5	1.65
CTT 2.5	2.3	2.5	2.7	1.35	1.5	1.65
HSTL Class I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL Class III	1.4	1.5	1.6	-	0.9	-
GTL+	-	-	-	0.882	1.0	1.122
LVDS	2.3	2.5	2.7	-	-	-
LVPECL	3.0	3.3	3.6	-	-	-
BLVDS	2.3	2.5	2.7	-	-	-

1. Inputs independent of V_{CCO}.
2. Design tool default setting.

ispXPGA 200B/C & ispXPGA 200EB/EC PFU Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Set								
t_{LASSRO}	Asynchronous Set/Reset to Output	—	1.09	—	1.17	—	1.35	ns
$t_{LASSRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{LASSRR}	Asynchronous Set/Reset Recovery	—	0.51	—	0.55	—	0.63	ns
t_{LSSR_S}	Synchronous Set/Reset Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{LSSR_H}	Synchronous Set/Reset Hold Time	0.03	—	0.03	—	0.03	—	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.
2. $t_{LCTHRUL}$ quoted bit by bit.

Timing v.0.3

ispXPGA 200B/C & ispXPGA 200EB/EC PIC Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Register/Latch Delays								
t_{IO_CO}	Register Clock to Output Delay	—	0.93	—	1.00	—	1.15	ns
t_{IO_S}	Register Setup Time (Data before Clock)	0.05	—	0.05	—	0.06	—	ns
t_{IO_H}	Register Hold Time (Data after Clock)	0.06	—	0.06	—	0.07	—	ns
t_{IOCE_S}	Register Clock Enable Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{IOCE_H}	Register Clock Enable Hold Time	0.13	—	0.13	—	0.15	—	ns
t_{IO_GO}	Latch Gate to Output Delay	—	0.72	—	0.77	—	0.89	ns
t_{IOL_S}	Latch Setup Time	0.05	—	0.05	—	0.06	—	ns
t_{IOL_H}	Latch Hold Time	0.06	—	0.06	—	0.07	—	ns
t_{IOLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns
t_{IOASRO}	Asynchronous Set/Reset to Output	—	1.04	—	1.12	—	1.29	ns
$t_{IOASRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{IOASRR}	Asynchronous Set/Reset Recovery Time	—	0.23	—	0.25	—	0.29	ns
Input/Output Delays								
t_{IOBUF}	Output Buffer Delay	—	0.97	—	1.04	—	1.20	ns
t_{IOIN}	Input Buffer Delay	—	0.60	—	0.64	—	0.74	ns
t_{IOEN}	Output Enable Delay	—	0.53	—	0.57	—	0.66	ns
t_{IODIS}	Output Disable Delay	—	-0.13	—	-0.12	—	-0.10	ns
t_{IOFT}	Feed-thru Delay	—	0.19	—	0.20	—	0.23	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 500B/C & ispXPGA 500EB/EC External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Conditions	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{CO}	Global Clock Input to Output	PIO Output Register	—	6.4	—	6.9	—	7.9	ns
t_S	Global Clock Input Setup	PIO Input Register without input delay	-2.9	—	-2.7	—	-2.3	—	ns
t_H	Global Clock Input Hold	PIO Input Register without input delay	3.6	—	3.9	—	4.5	—	ns
t_{SINDLY}	Global Clock Input Setup	PIO Input Register with input delay	3.3	—	3.6	—	4.1	—	ns
t_{HINDLY}	Global Clock Input Hold	PIO Input Register with input delay	0.0	—	0.0	—	0.0	—	
t_{COPLL}	Global Clock Input to Output	PIO Output Register using PLL without delay	—	3.2	—	3.4	—	3.9	ns
t_{SPLL}	Global Clock Input Setup	PIO Input Register without input delay using PLL without delay	0.1	—	0.2	—	0.3	—	ns
t_{HPLL}	Global Clock Input Hold	PIO Input Register without input delay using PLL without delay	0.8	—	0.9	—	1.0	—	ns
$t_{SINDLYPLL}$	Global Clock Input Setup	PIO Input Register with input delay using PLL without delay	6.7	—	7.2	—	8.3	—	ns
$t_{HINDLYPLL}$	Global Clock Input Hold	PIO Input Register with input delay using PLL without delay	-4.3	—	-4.0	—	-3.4	—	ns

1. Only available for ispXPGA 500B and ispXPGA 500EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 500B/C & ispXPGA 500EB/EC Timing Adders

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	5.21	—	5.60	—	6.44	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

ispXPGA 1200B/C & ispXPGA 1200EB/EC Timing Adders (Cont.)

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LVCMOS_33_4mA_out	Using 3.3V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_33_5.33mA_out	Using 3.3V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_33_8mA_out	Using 3.3V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_33_12mA_out	Using 3.3V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_33_16mA_out	Using 3.3V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_33_24mA_out	Using 3.3V CMOS Standard, 24mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_out	Using AGP 1x Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
CTT25_out	Using CTT 2.5V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
CTT33_out	Using CTT 3.3V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
GTL+_out	Using GTL+	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_out	Using HSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_out	Using HSTL 2.5V, Class III	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVDS_out	Using Low Voltage Differential Signaling (LVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
BLVDS_out	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVPECL_out	Using Low Voltage PECL	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
PCI_out	Using PCI Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL2_I_out	Using SSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL2_II_out	Using SSTL 2.5V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_out	Using SSTL 3.3V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL3_II_out	Using SSTL 3.3V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

1. Only available for ispXPGA 1200B and ispXPGA 1200EB (2.5V/3.3V) devices.

Timing v.2.1

ispXPGA Logic Signal Connections: 256-Ball fpBGA

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
C2	BK0_IO2	HSI0A_SOUTP	1P/HSI0	BK0_IO0	HSI0A_SOUTP	0P
-	GND (Bank 0)	-	-	-	-	-
D2	BK0_IO3	HSI0A_SOUTN	1N/HSI0	BK0_IO1	HSI0A_SOUTN	0N
B1	BK0_IO6	HSI0A_SINP	3P/HSI0	BK0_IO4	HSI0A_SINP	2P/HSI0
-	-	-	-	GND (Bank 0)	-	-
C1	BK0_IO7	HSI0A_SINN	3N/HSI0	BK0_IO5	HSI0A_SINN	2N/HSI0
D3	BK0_IO8	-	4P/HSI0	BK0_IO6	-	3P/HSI0
E3	BK0_IO9	VREF0	4N/HSI0	BK0_IO7	VREF0	3N/HSI0
D1	BK0_IO10	HSI0B_SOUTP	5P/HSI0	BK0_IO8	HSI0B_SOUTP	4P/HSI0
-	GND (Bank 0)	-	-	-	-	-
E1	BK0_IO11	HSI0B_SOUTN	5N/HSI0	BK0_IO9	HSI0B_SOUTN	4N/HSI0
E2	BK0_IO12	-	6P/HSI0	BK0_IO10	-	5P/HSI0
F2	BK0_IO13	-	6N/HSI0	BK0_IO11	-	5N/HSI0
F1	BK0_IO14	HSI0B_SINP	7P/HSI0	BK0_IO12	HSI0B_SINP	6P/HSI0
-	-	-	-	GND (Bank 0)	-	-
G1	BK0_IO15	HSI0B_SINN	7N/HSI0	BK0_IO13	HSI0B_SINN	6N/HSI0
F3	BK0_IO18	PLL_FBK0	9P	BK0_IO14	PLL_FBK0	7P/HSI0
-	GND (Bank 0)	-	-	-	-	-
G2	BK0_IO19	PLL_RST1	9N	BK0_IO15	PLL_RST1	7N/HSI0
E4	BK0_IO20	-	10P	BK0_IO16	-	8P/HSI0
F4	BK0_IO21	PLL_FBK1	10N	BK0_IO17	PLL_FBK1	8N/HSI0
H1	BK0_IO22	PLL_RST0	11P	BK0_IO18	PLL_RST0	9P
-	-	-	-	GND (Bank 0)	-	-
J1	BK0_IO23	-	11N	BK0_IO19	-	9N
H2	BK0_IO24	CLK_OUT0	12P	BK0_IO20	CLK_OUT0	10P
G3	BK0_IO25	CLK_OUT1	12N	BK0_IO21	CLK_OUT1	10N
-	GND (Bank 0)	-	-	-	-	-
G4	GCLK0	-	LVDS Pair0P	GCLK0	-	LVDS Pair0P
H4	GCLK1	-	LVDS Pair0N	GCLK1	-	LVDS Pair0N
H3	VCCP0	-	-	VCCP0	-	-
J4	GNDP0	-	-	GNDP0	-	-
J2	GCLK2	-	LVDS Pair1P	GCLK2	-	LVDS Pair1P
J3	GCLK3	-	LVDS Pair1N	GCLK3	-	LVDS Pair1N
-	GND (Bank 1)	-	-	-	-	-
H5	BK1_IO0	CLK_OUT2	13P	BK1_IO0	CLK_OUT2	11P
J5	BK1_IO1	CLK_OUT3	13N	BK1_IO1	CLK_OUT3	11N
K1	BK1_IO2	SS_CLKOUT0P	14P	BK1_IO2	SS_CLKOUT0P	12P
-	-	-	-	GND (Bank 1)	-	-
L1	BK1_IO3	SS_CLKOUT0N	14N	BK1_IO3	SS_CLKOUT0N	12N
K4	BK1_IO4	PLL_FBK2	15P	BK1_IO4	PLL_FBK2	13P
L4	BK1_IO5	PLL_FBK3	15N	BK1_IO5	PLL_FBK3	13N
K3	BK1_IO6	SS_CLKIN0P	16P	BK1_IO6	SS_CLKIN0P	14P

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
M15	BK4_IO5	-	54N/HSI2	BK4_IO5	-	46N
M14	BK4_IO8	-	56P/HSI2	BK4_IO6	-	47P
M13	BK4_IO9	VREF4	56N/HSI2	BK4_IO7	VREF4	47N
-	GND (Bank 4)	-	-	-	-	-
L13	BK4_IO12	PLL_RST4	58P/HSI2	BK4_IO8	PLL_RST4	48P
L14	BK4_IO13	PLL_RST5	58N/HSI2	BK4_IO9	PLL_RST5	48N
N16	BK4_IO14	HSI2B_SOUTP	59P/HSI2	BK4_IO10	-	49P
M16	BK4_IO15	HSI2B_SOUTN	59N/HSI2	BK4_IO11	-	49N
-	-	-	-	GND (Bank 4)	-	-
L15	BK4_IO18	SS_CLKIN1P	61P	BK4_IO14	SS_CLKIN1P	51P
-	GND (Bank 4)	-	-	-	-	-
K15	BK4_IO19	SS_CLKIN1N	61N	BK4_IO15	SS_CLKIN1N	51N
K14	BK4_IO20	PLL_FBK4	62P	BK4_IO16	PLL_FBK4	52P
K13	BK4_IO21	PLL_FBK5	62N	BK4_IO17	PLL_FBK5	52N
L16	BK4_IO22	SS_CLKOUT1P	63P	BK4_IO18	SS_CLKOUT1P	53P
-	-	-	-	GND (Bank 4)	-	-
K16	BK4_IO23	SS_CLKOUT1N	63N	BK4_IO19	SS_CLKOUT1N	53N
J13	BK4_IO24	CLK_OUT4	64P	BK4_IO20	CLK_OUT4	54P
J12	BK4_IO25	CLK_OUT5	64N	BK4_IO21	CLK_OUT5	54N
-	GND (Bank 4)	-	-	-	-	-
J14	GCLK4	-	LVDS Pair2P	GCLK4	-	LVDS Pair2P
H14	GCLK5	-	LVDS Pair2N	GCLK5	-	LVDS Pair2N
J15	VCCP1	-	-	VCCP1	-	-
H15	GNDP1	-	-	GNDP1	-	-
J16	GCLK6	-	LVDS Pair3P	GCLK6	-	LVDS Pair3P
H16	GCLK7	-	LVDS Pair3N	GCLK7	-	LVDS Pair3N
-	GND (Bank 5)	-	-	-	-	-
H12	BK5_IO0	CLK_OUT6	65P	BK5_IO0	CLK_OUT6	55P
H13	BK5_IO1	CLK_OUT7	65N	BK5_IO1	CLK_OUT7	55N
G14	BK5_IO2	-	66P	BK5_IO2	-	56P
-	-	-	-	GND (Bank 5)	-	-
G15	BK5_IO3	PLL_RST7	66N	BK5_IO3	PLL_RST7	56N
G13	BK5_IO6	PLL_RST6	68P	BK5_IO6	PLL_RST6	58P/HSI1
-	GND (Bank 5)	-	-	-	-	-
F13	BK5_IO7	PLL_FBK7	68N	BK5_IO7	PLL_FBK7	58N/HSI1
G16	BK5_IO10	HSI3A_SINP	70P	BK5_IO8	HSI1A_SINP	59P/HSI1
-	-	-	-	GND (Bank 5)	-	-
F16	BK5_IO11	HSI3A_SINN	70N/HSI3	BK5_IO9	HSI1A-SINN	59N/HSI1
F14	BK5_IO12	-	71P/HSI3	BK5_IO10	-	60P/HSI1
F15	BK5_IO13	-	71N/HSI3	BK5_IO11	-	60N/HSI1
E16	BK5_IO14	HSI3A_SOUTP	72P/HSI3	BK5_IO12	HSI1A_SOUTP	61P/HSI1
-	GND (Bank 5)	-	-	-	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AE3	BK1_IO33	-	37N/HSI2	NC	-	-	NC	-	-
AG1	BK1_IO34	-	38P/HSI2	NC	-	-	NC	-	-
AH1	BK1_IO35	-	38N/HSI2	NC	-	-	NC	-	-
AG2	BK1_IO36	-	39P/HSI2	NC	-	-	NC	-	-
AF3	BK1_IO37	-	39N/HSI2	NC	-	-	NC	-	-
AJ1	BK1_IO38	-	40P/HSI2	NC	-	-	NC	-	-
-	GND (Bank 1)	-	-	-	-	-	-	-	-
AH2	BK1_IO39	-	40N/HSI2	NC	-	-	NC	-	-
AG3	BK1_IO40	-	41P	BK1_IO24	-	25P/HSI1	NC	-	-
AF4	BK1_IO41	-	41N	BK1_IO25	-	25N/HSI1	NC	-	-
AK2	TCK	-	-	TCK	-	-	TCK	-	-
AJ3	TMS	-	-	TMS	-	-	TMS	-	-
AG5	TOE	-	-	TOE	-	-	TOE	-	-
AH4	BK2_IO0	-	42P	BK2_IO0	-	26P	BK2_IO0	-	22P
AK3	BK2_IO1	-	42N	BK2_IO1	-	26N	BK2_IO1	-	22N
AJ4	BK2_IO2	-	43P	BK2_IO2	-	27P	BK2_IO2	-	23P
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-	-	-	-
AH5	BK2_IO3	-	43N	BK2_IO3	-	27N	BK2_IO3	-	23N
AK4	BK2_IO4	-	44P	BK2_IO4	-	28P	BK2_IO4	-	24P
-	-	-	-	-	-	-	GND (Bank 2)	-	-
AJ5	BK2_IO5	-	44N	BK2_IO5	-	28N	BK2_IO5	-	24N
AG7	BK2_IO6	-	45P	BK2_IO6	-	29P	BK2_IO6	-	25P
AH6	BK2_IO7	-	45N	BK2_IO7	-	29N	BK2_IO7	-	25N
AK5	BK2_IO8	-	46P	NC	-	-	NC	-	-
AJ6	BK2_IO9	-	46N	NC	-	-	NC	-	-
AG8	BK2_IO10	-	47P	NC	-	-	NC	-	-
-	GND (Bank 2)	-	-	-	-	-	-	-	-
AH7	BK2_IO11	-	47N	NC	-	-	NC	-	-
AK6	BK2_IO12	-	48P	NC	-	-	NC	-	-
AJ7	BK2_IO13	-	48N	NC	-	-	NC	-	-
AH8	BK2_IO14	-	49P	NC	-	-	NC	-	-
AG10	BK2_IO15	-	49N	NC	-	-	NC	-	-
AK7	BK2_IO16	-	50P	NC	-	-	NC	-	-
AJ8	BK2_IO17	-	50N	NC	-	-	NC	-	-
AH9	BK2_IO18	-	51P	NC	-	-	NC	-	-
-	GND (Bank 2)	-	-	-	-	-	-	-	-
AG11	BK2_IO19	-	51N	NC	-	-	NC	-	-
AK8	BK2_IO20	-	52P	BK2_IO8	-	30P	BK2_IO8	-	26P
AJ9	BK2_IO21	VREF2	52N	BK2_IO9	VREF2	30N	BK2_IO9	VREF2	26N
AH10	BK2_IO22	-	53P	BK2_IO10	-	31P	BK2_IO10	-	27P
-	-	-	-	GND (Bank 2)	-	-	-	-	-
AH11	BK2_IO23	-	53N	BK2_IO11	-	31N	BK2_IO11	-	27N
AJ10	BK2_IO24	-	54P	BK2_IO12		32P	BK2_IO12	-	28P
AK10	BK2_IO25	-	54N	BK2_IO13	-	32N	BK2_IO13	-	28N
AH12	BK2_IO26	-	55P	BK2_IO14	-	33P	BK2_IO14	-	29P
-	GND (Bank 2)	-	-	-	-	-	-	-	-
AJ11	BK2_IO27	-	55N	BK2_IO15	-	33N	BK2_IO15	-	29N
AK11	BK2_IO28	-	56P	NC	-	-	NC	-	-
AJ12	BK2_IO29	-	56N	NC	-	-	NC	-	-
AG13	BK2_IO30	-	57P	BK2_IO16	-	34P	BK2_IO16	-	30P
AH13	BK2_IO31	-	57N	BK2_IO17	-	34N	BK2_IO17	-	30N

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
-	GND (Bank 2)	-	-
K36	BK2_IO19	-	71N
H38	BK2_IO20	-	72P
J38	BK2_IO21	-	72N
J39	BK2_IO22	-	73P
L36	BK2_IO23	-	73N
K38	BK2_IO24	-	74P
M36	BK2_IO25	-	74N
L37	BK2_IO26	-	75P
-	GND (Bank 2)	-	-
K39	BK2_IO27	-	75N
L38	BK2_IO28	-	76P
P35	BK2_IO29	-	76N
N36	BK2_IO30	-	77P
M37	BK2_IO31	-	77N
L39	BK2_IO32	-	78P
M38	BK2_IO33	-	78N
M39	BK2_IO34	-	79P
-	GND (Bank 2)	-	-
P36	BK2_IO35	-	79N
R36	BK2_IO36	-	80P
N37	BK2_IO37	-	80N
P38	BK2_IO38	-	81P
T35	BK2_IO39	-	81N
R37	BK2_IO40	-	82P
R38	BK2_IO41	-	82N
P39	BK2_IO42	-	83P
-	GND (Bank 2)	-	-
R39	BK2_IO43	-	83N
T38	BK2_IO44	-	84P
T36	BK2_IO45	-	84N
T37	BK2_IO46	-	85P
U36	BK2_IO47	-	85N
U37	BK2_IO48	-	86P
T39	BK2_IO49	-	86N
V36	BK2_IO50	-	87P
-	GND (Bank 2)	-	-
U38	BK2_IO51	-	87N
U39	BK2_IO52	-	88P
V38	BK2_IO53	-	88N
V37	BK2_IO54	-	89P
W36	BK2_IO55	-	89N
W35	BK2_IO56	-	90P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
V39	BK2_IO57	-	90N
W37	BK2_IO58	-	91P
-	GND (Bank 2)	-	-
W38	BK2_IO59	-	91N
W39	BK2_IO60	-	92P
AA39	BK2_IO61	-	92N
-	GND (Bank 2)	-	-
-	GND (Bank 3)	-	-
AA38	BK3_IO0	-	93P
Y35	BK3_IO1	-	93N
AA37	BK3_IO2	-	94P
-	GND (Bank 3)	-	-
AA35	BK3_IO3	-	94N
AB39	BK3_IO4	-	95P
AB38	BK3_IO5	-	95N
AA36	BK3_IO6	-	96P
AB37	BK3_IO7	-	96N
AC39	BK3_IO8	-	97P
AC38	BK3_IO9	-	97N
AB36	BK3_IO10	-	98P
-	GND (Bank 3)	-	-
AC37	BK3_IO11	-	98N
AC36	BK3_IO12	-	99P
AD39	BK3_IO13	-	99N
AD37	BK3_IO14	-	100P
AD36	BK3_IO15	-	100N
AD35	BK3_IO16	-	101P
AE38	BK3_IO17	-	101N
AD38	BK3_IO18	-	102P
-	GND (Bank 3)	-	-
AE39	BK3_IO19	-	102N
AF38	BK3_IO20	-	103P
AF37	BK3_IO21	-	103N
AF39	BK3_IO22	-	104P
AE36	BK3_IO23	-	104N
AF36	BK3_IO24	-	105P
AG38	BK3_IO25	-	105N
AG39	BK3_IO26	-	106P
-	GND (Bank 3)	-	-
AG37	BK3_IO27	-	106N
AH37	BK3_IO28	-	107P
AH38	BK3_IO29	-	107N
AG36	BK3_IO30	-	108P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
-	GND (Bank 4)	-	-
AW26	BK4_IO43	-	145N
AV25	BK4_IO44	-	146P
AT24	BK4_IO45	-	146N
AU24	BK4_IO46	-	147P
AU25	BK4_IO47	-	147N
AW25	BK4_IO48	PLL_RST4	148P
AW24	BK4_IO49	PLL_RST5	148N
AU23	BK4_IO50	-	149P
-	GND (Bank 4)	-	-
AT23	BK4_IO51	-	149N
AV24	BK4_IO52	-	150P
AW23	BK4_IO53	-	150N
AV23	BK4_IO54	SS_CLKIN1P	151P
AU22	BK4_IO55	SS_CLKIN1N	151N
AR21	BK4_IO56	PLL_FBK4	152P
AT22	BK4_IO57	PLL_FBK5	152N
AV22	BK4_IO58	SS_CLKOUT1P	153P
-	GND (Bank 4)	-	-
AV21	BK4_IO59	SS_CLKOUT1N	153N
AT21	BK4_IO60	CLK_OUT4	154P
AU21	BK4_IO61	CLK_OUT5	154N
-	GND (Bank 4)	-	-
AT19	GCLK4	-	LVDS Pair2P
AU19	GCLK5	-	LVDS Pair2N
AW22	VCCP1	-	-
AR20	GNDP1	-	-
AU18	GCLK6	-	LVDS Pair3P
AT18	GCLK7	-	LVDS Pair3N
-	GND (Bank 5)	-	-
AV17	BK5_IO0	CLK_OUT6	155P
AV18	BK5_IO1	CLK_OUT7	155N
AW21	BK5_IO2	PLL_FBK6	156P
-	GND (Bank 5)	-	-
AV19	BK5_IO3	PLL_FBK7	156N
AR19	BK5_IO4	-	157P/HSI7
AW19	BK5_IO5	-	157N/HSI7
AW18	BK5_IO6	PLL_RST6	158P/HSI7
AW17	BK5_IO7	PLL_RST7	158N/HSI7
AT17	BK5_IO8	-	159P/HSI7
AV16	BK5_IO9	-	159N/HSI7
AU17	BK5_IO10	HSI7A_SINP	160P/HSI7
-	GND (Bank 5)	-	-

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
AT16	BK5_IO11	HSI7A_SINN	160N/HSI7
AW16	BK5_IO12	-	161P/HSI7
AU16	BK5_IO13	-	161N/HSI7
AV14	BK5_IO14	HSI7A_SOUTP	162P/HSI7
AV15	BK5_IO15	HSI7A_SOUTN	162N/HSI7
AU15	BK5_IO16	-	163P/HSI7
AW15	BK5_IO17	-	163N/HSI7
AT15	BK5_IO18	HSI7B_SINP	164P/HSI7
-	GND (Bank 5)	-	-
AR16	BK5_IO19	HSI7B_SINN	164N/HSI7
AW14	BK5_IO20	-	165P/HSI8
AW13	BK5_IO21	-	165N/HSI8
AR14	BK5_IO22	HSI7B_SOUTP	166P/HSI8
AT14	BK5_IO23	HSI7B_SOUTN	166N/HSI8
AT13	BK5_IO24	-	167P/HSI8
AV13	BK5_IO25	-	167N/HSI8
AU12	BK5_IO26	HSI8A_SINP	168P/HSI8
-	GND (Bank 5)	-	-
AU13	BK5_IO27	HSI8A_SINN	168N/HSI8
AV12	BK5_IO28	-	169P/HSI8
AT12	BK5_IO29	-	169N/HSI8
AR12	BK5_IO30	HSI8A_SOUTP	170P/HSI8
AT11	BK5_IO31	HSI8A_SOUTN	170N/HSI8
AW12	BK5_IO32	-	171P/HSI8
AU11	BK5_IO33	-	171N/HSI8
AV9	BK5_IO34	HSI8B_SINP	172P/HSI8
-	GND (Bank 5)	-	-
AV10	BK5_IO35	HSI8B_SINN	172N/HSI8
AW10	BK5_IO36	-	173P/HSI9
AW9	BK5_IO37	-	173N/HSI9
AT10	BK5_IO38	HSI8B_SOUTP	174P/HSI9
AU9	BK5_IO39	HSI8B_SOUTN	174N/HSI9
AT9	BK5_IO40	-	175P/HSI9
AR10	BK5_IO41	-	175N/HSI9
AU8	BK5_IO42	HSI9A_SINP	176P/HSI9
-	GND (Bank 5)	-	-
AV8	BK5_IO43	HSI9A_SINN	176N/HSI9
AW8	BK5_IO44	-	177P/HSI9
AW7	BK5_IO45	-	177N/HSI9
AU7	BK5_IO46	HSI9A_SOUTP	178P/HSI9
AT8	BK5_IO47	HSI9A_SOUTN	178N/HSI9
AV7	BK5_IO48	-	179P/HSI9
AW6	BK5_IO49	VREF5	179N/HSI9

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AJ12	BK2_IO43	-	83N	BK2_IO23	-	53N
AD13	BK2_IO44	-	84P	BK2_IO24	-	54P
AE13	BK2_IO45	-	84N	BK2_IO25	-	54N
AK13	BK2_IO46	-	85P	BK2_IO26	-	55P
-	-	-	-	GND (Bank 2)	-	-
AJ13	BK2_IO47	-	85N	BK2_IO27	-	55N
AG13	BK2_IO48	-	86P	BK2_IO28	-	56P
AH13	BK2_IO49	-	86N	BK2_IO29	-	56N
AE14	BK2_IO50	-	87P	BK2_IO30	-	57P
-	GND (Bank 2)	-	-	-	-	-
AF14	BK2_IO51	-	87N	BK2_IO31	-	57N
AG14	BK2_IO52	-	88P	BK2_IO32	-	58P
AH14	BK2_IO53	-	88N	BK2_IO33	-	58N
AJ14	BK2_IO54	-	89P	BK2_IO34	-	59P
-	-	-	-	GND (Bank 2)	-	-
AK14	BK2_IO55	-	89N	BK2_IO35	-	59N
AE15	BK2_IO56	-	90P	BK2_IO36	-	60P
AF15	BK2_IO57	-	90N	BK2_IO37	-	60N
AG15	BK2_IO58	-	91P	BK2_IO38	-	61P
-	GND (Bank 2)	-	-	-	-	-
AH15	BK2_IO59	-	91N	BK2_IO39	-	61N
AJ15	BK2_IO60	-	92P	BK2_IO40	-	62P
AK15	BK2_IO61	-	92N	BK2_IO41	-	62N
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-
AK16	BK3_IO0	-	93P	BK3_IO0	-	63P
AJ16	BK3_IO1	-	93N	BK3_IO1	-	63N
AH16	BK3_IO2	-	94P	BK3_IO2	-	64P
-	GND (Bank 3)	-	-	-	-	-
AG16	BK3_IO3	-	94N	BK3_IO3	-	64N
AF16	BK3_IO4	-	95P	BK3_IO4	-	65P
AE16	BK3_IO5	-	95N	BK3_IO5	-	65N
AK17	BK3_IO6	-	96P	BK3_IO6	-	66P
-	-	-	-	GND (Bank 3)	-	-
AJ17	BK3_IO7	-	96N	BK3_IO7	-	66N
AH17	BK3_IO8	-	97P	BK3_IO8	-	67P
AG17	BK3_IO9	-	97N	BK3_IO9	-	67N
AF17	BK3_IO10	-	98P	BK3_IO10	-	68P
-	GND (Bank 3)	-	-	-	-	-
AE17	BK3_IO11	-	98N	BK3_IO11	-	68N
AH18	BK3_IO12	-	99P	BK3_IO12	-	69P
AG18	BK3_IO13	-	99N	BK3_IO13	-	69N

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
K30	BK5_IO22	HSI7B_SOUTP	166P/HSI8	BK5_IO22	HSI4B_SOUTP	116P/HSI4
-	-	-	-	GND (Bank 5)	-	-
K29	BK5_IO23	HSI7B_SOUTN	166N/HSI8	BK5_IO23	HSI4B_SOUTN	116N/HSI4
L28	BK5_IO24	-	167P/HSI8	BK5_IO24	-	117P/HSI5
L27	BK5_IO25	-	167N/HSI8	BK5_IO25	-	117N/HSI5
L26	BK5_IO26	HSI8A_SINP	168P/HSI8	BK5_IO26	HSI5A_SINP	118P/HSI5
-	GND (Bank 5)	-	-	-	-	-
L25	BK5_IO27	HSI8A_SINN	168N/HSI8	BK5_IO27	HSI5A_SINN	118N/HSI5
K27	BK5_IO28	-	169P/HSI8	BK5_IO28	-	119P/HSI5
K26	BK5_IO29	-	169N/HSI8	BK5_IO29	-	119N/HSI5
J30	BK5_IO30	HSI8A_SOUTP	170P/HSI8	BK5_IO30	HSI5A_SOUTP	120P/HSI5
-	-	-	-	GND (Bank 5)	-	-
J29	BK5_IO31	HSI8A_SOUTN	170N/HSI8	BK5_IO31	HSI5A_SOUTN	120N/HSI5
J26	BK5_IO32	-	171P/HSI8	NC	-	-
J27	BK5_IO33	-	171N/HSI8	NC	-	-
H30	BK5_IO34	HSI8B_SINP	172P/HSI8	NC	-	-
-	GND (Bank 5)	-	-	-	-	-
H29	BK5_IO35	HSI8B_SINN	172N/HSI8	NC	-	-
J25	BK5_IO36	-	173P/HSI9	NC	-	-
J24	BK5_IO37	-	173N/HSI9	NC	-	-
G30	BK5_IO38	HSI8B_SOUTP	174P/HSI9	NC	-	-
G29	BK5_IO39	HSI8B_SOUTN	174N/HSI9	NC	-	-
H27	BK5_IO40	-	175P/HSI9	NC	-	-
H28	BK5_IO41	-	175N/HSI9	NC	-	-
F30	BK5_IO42	HSI9A_SINP	176P/HSI9	NC	-	-
-	GND (Bank 5)	-	-	-	-	-
F29	BK5_IO43	HSI9A_SINN	176N/HSI9	NC	-	-
G27	BK5_IO44	-	177P/HSI9	NC	-	-
G28	BK5_IO45	-	177N/HSI9	NC	-	-
E30	BK5_IO46	HSI9A_SOUTP	178P/HSI9	NC	-	-
E29	BK5_IO47	HSI9A_SOUTN	178N/HSI9	NC	-	-
H26	BK5_IO48	-	179P/HSI9	BK5_IO33	-	121N/HSI5
H25	BK5_IO49	VREF5	179N/HSI9	BK5_IO32	VREF5	121P/HSI5
D30	BK5_IO50	HSI9B_SINP	180P/HSI9	BK5_IO34	HSI5B_SINP	122P/HSI5
-	GND (Bank 5)	-	-	-	-	-
D29	BK5_IO51	HSI9B_SINN	180N/HSI9	BK5_IO35	HSI5B_SINN	122N/HSI5
F28	BK5_IO52	-	181P	BK5_IO36	-	123P/HSI5
F27	BK5_IO53	-	181N	BK5_IO37	-	123N/HSI5
C30	BK5_IO54	HSI9B_SOUTP	182P	BK5_IO38	HSI5B_SOUTP	124P/HSI5
-	-	-	-	GND (Bank 5)	-	-
C29	BK5_IO55	HSI9B_SOUTN	182N	BK5_IO39	HSI5B_SOUTN	124N/HSI5
G26	BK5_IO56	-	183P	NC	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
D21	BK6_IO29	-	200N	NC	-	-
A21	BK6_IO30	-	201P	NC	-	-
B21	BK6_IO31	-	201N	NC	-	-
F20	BK6_IO32	DATA7	202P	BK6_IO18	DATA7	135P
-	-	-	-	GND (Bank 6)	-	-
E20	BK6_IO33	DATA6	202N	BK6_IO19	DATA6	135N
D20	BK6_IO34	-	203P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-
C20	BK6_IO35		203N	NC	-	-
F19	BK6_IO36	DATA5	204P	BK6_IO22	DATA5	137P
E19	BK6_IO37	DATA4	204N	BK6_IO23	DATA4	137N
B20	BK6_IO38	-	205P	NC	-	-
A20	BK6_IO39	-	205N	NC	-	-
D19	BK6_IO40	-	206P	NC	-	-
C19	BK6_IO41	-	206N	NC	-	-
A19	BK6_IO42	-	207P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-
B19	BK6_IO43	-	207N	NC	-	-
G18	BK6_IO44	-	208P	BK6_IO24	-	138P
F18	BK6_IO45	-	208N	BK6_IO25	-	138N
A18	BK6_IO46	-	209P	BK6_IO32	-	142P
B18	BK6_IO47	-	209N	BK6_IO33	-	142N
D18	BK6_IO48	-	210P	BK6_IO34	-	143P
-	-	-	-	GND (Bank 6)	-	-
C18	BK6_IO49	-	210N	BK6_IO35	-	143N
F17	BK6_IO50	DATA3	211P	BK6_IO26	DATA3	139P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
E17	BK6_IO51	DATA2	211N	BK6_IO27	DATA2	139N
D17	BK6_IO52	-	212P	BK6_IO28	-	140P
C17	BK6_IO53	-	212N	BK6_IO29	-	140N
B17	BK6_IO54	DATA1	213P	BK6_IO30	DATA1	141P
A17	BK6_IO55	DATA0	213N	BK6_IO31	DATA0	141N
F16	BK6_IO56	-	214P	BK6_IO36	-	144P
E16	BK6_IO57	-	214N	BK6_IO37	-	144N
D16	BK6_IO58	-	215P	BK6_IO38	-	145P
-	GND (Bank 6)	-	-	-	-	-
C16	BK6_IO59	-	215N	BK6_IO39	-	145N
B16	BK6_IO60	-	216P	BK6_IO40	-	146P
A16	BK6_IO61	-	216N	BK6_IO41	-	146N
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-
A15	BK7_IO0	-	217P	BK7_IO0	-	147P

"E-Series" Industrial (Cont.)

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX1200EB-04F900I[2]	1.25M	2.5/3.3	-4	fpBGA	900
LFX1200EB-03F900I[2]	1.25M	2.5/3.3	-3	fpBGA	900
LFX1200EC-03F900I[2]	1.25M	1.8	-3	fpBGA	900
LFX1200EB-04FE680I[2]	1.25M	2.5/3.3	-4	fpSBGA	680
LFX1200EB-03FE680I[2]	1.25M	2.5/3.3	-3	fpSBGA	680
LFX1200EC-03FE680I[2]	1.25M	1.8	-3	fpSBGA	680

1. FH516 package was converted to F516 via PCN #09A-08.
2. Discontinued via PCN #03A-10.

Lead-Free Packaging

Commercial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125B-05FN256C	139K	2.5/3.3	-5	Lead-Free fpBGA	256
LFX125B-04FN256C	139K	2.5/3.3	-4	Lead-Free fpBGA	256
LFX125B-03FN256C	139K	2.5/3.3	-3	Lead-Free fpBGA	256
LFX125C-04FN256C	139K	1.8	-4	Lead-Free fpBGA	256
LFX125C-03FN256C	139K	1.8	-3	Lead-Free fpBGA	256
LFX200B-05FN256C	210K	2.5/3.3	-5	Lead-Free fpBGA	256
LFX200B-04FN256C	210K	2.5/3.3	-4	Lead-Free fpBGA	256
LFX200B-03FN256C	210K	2.5/3.3	-3	Lead-Free fpBGA	256
LFX200C-04FN256C	210K	1.8	-4	Lead-Free fpBGA	256
LFX200C-03FN256C	210K	1.8	-3	Lead-Free fpBGA	256
LFX500B-05FN900C	476K	2.5/3.3	-5	Lead-Free fpBGA	900
LFX500B-04FN900C	476K	2.5/3.3	-4	Lead-Free fpBGA	900
LFX500B-03FN900C	476K	2.5/3.3	-3	Lead-Free fpBGA	900
LFX500C-04FN900C	476K	1.8	-4	Lead-Free fpBGA	900
LFX500C-03FN900C	476K	1.8	-3	Lead-Free fpBGA	900

"E-Series" Commercial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125EB-05FN256C	139K	2.5/3.3	-5	Lead-Free fpBGA	256
LFX125EB-04FN256C	139K	2.5/3.3	-4	Lead-Free fpBGA	256
LFX125EB-03FN256C	139K	2.5/3.3	-3	Lead-Free fpBGA	256
LFX125EC-04FN256C	139K	1.8	-4	Lead-Free fpBGA	256
LFX125EC-03FN256C	139K	1.8	-3	Lead-Free fpBGA	256
LFX200EB-05FN256C	210K	2.5/3.3	-5	Lead-Free fpBGA	256
LFX200EB-04FN256C	210K	2.5/3.3	-4	Lead-Free fpBGA	256
LFX200EB-03FN256C	210K	2.5/3.3	-3	Lead-Free fpBGA	256
LFX200EC-04FN256C	210K	1.8	-4	Lead-Free fpBGA	256
LFX200EC-03FN256C	210K	1.8	-3	Lead-Free fpBGA	256
LFX500EB-05FN900C	476K	2.5/3.3	-5	Lead-Free fpBGA	900
LFX500EB-04FN900C	476K	2.5/3.3	-4	Lead-Free fpBGA	900
LFX500EB-03FN900C	476K	2.5/3.3	-3	Lead-Free fpBGA	900