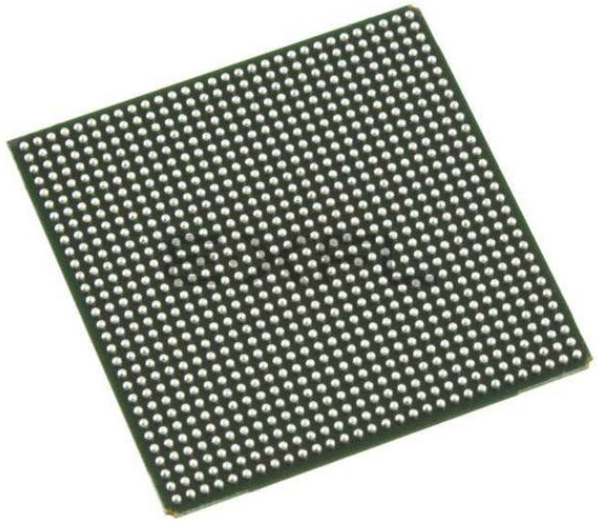
Lattice Semiconductor Corporation - LFX1200C-03F900C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	15376
Total RAM Bits	423936
Number of I/O	496
Number of Gates	1250000
Voltage - Supply	1.65V ~ 1.95V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx1200c-03f900c

Product Line	Ordering Part Number	Product Status	Reference PCN
LFX500B	LFX500B-03F516C	**Discontinued**	PCN#09-10
	LFX500B-04F516C		
	LFX500B-05F516C		
	LFX500B-03F900C		
	LFX500B-03FN900C		
	LFX500B-04F900C		
	LFX500B-04FN900C		
	LFX500B-05F900C		
	LFX500B-05FN900C		
LFX500C	LFX500C-03F516C	**Discontinued**	PCN#09-10
	LFX500C-04F516C		
	LFX500C-03F900C		
	LFX500C-03FN900C		
	LFX500C-04F900C		
	LFX500C-04FN900C		
LFX1200B	LFX1200B-03FE680C	**Discontinued**	PCN#03A-10
	LFX1200B-04FE680C		
	LFX1200B-05FE680C		
	LFX1200B-03F900C		
	LFX1200B-04F900C		
	LFX1200B-05F900C		
LFX1200C	LFX1200C-03FE680C	**Discontinued**	PCN#03A-10
	LFX1200C-04FE680C		
	LFX1200C-03F900C		
	LFX1200C-04F900C		
LFX125EB	LFX125EB-03F256C	Active / Orderable	
	LFX125EB-03FN256C		
	LFX125EB-04F256C		
	LFX125EB-04FN256C		
	LFX125EB-05F256C		
	LFX125EB-05FN256C		
	LFX125EB-03F256I		
	LFX125EB-03FN256I		
	LFX125EB-04F256I		
	LFX125EB-04FN256I		
	LFX125EB-03F516C	**Discontinued**	PCN#09-10
	LFX125EB-04F516C		
	LFX125EB-05F516C		
	LFX125EB-03F516I		
	LFX125EB-04F516I		
LFX125EC	LFX125EC-03F256C	**Discontinued**	PCN#09-10
	LFX125EC-03FN256C		
	LFX125EC-04F256C		
	LFX125EC-04FN256C		
	LFX125EC-03F256I		
	LFX125EC-03FN256I		

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Internet: http://www.latticesemi.com

Product Line	Ordering Part Number	Product Status	Reference PCN
LFX125EC (Cont'd)	LFX125EC-03F516C	**Discontinued**	PCN#09-10
	LFX125EC-04F516C		
	LFX125EC-03F516I		
LFX200EB	LFX200EB-03F256C	Active / Orderable	
	LFX200EB-03FN256C		
	LFX200EB-04F256C		
	LFX200EB-04FN256C		
	LFX200EB-05F256C		
	LFX200EB-05FN256C		
	LFX200EB-03F256I		
	LFX200EB-03FN256I		
	LFX200EB-04F256I		
	LFX200EB-04FN256I		
	LFX200EB-03F516C	**Discontinued**	PCN#09-10
	LFX200EB-04F516C		
	LFX200EB-05F516C		
	LFX200EB-03F516I		
	LFX200EB-04F516I		
LFX200EC	LFX200EC-03F256C	**Discontinued**	PCN#09-10
	LFX200EC-03FN256C		
	LFX200EC-04F256C		
	LFX200EC-04FN256C		
	LFX200EC-03F256I		
	LFX200EC-03FN256I		
	LFX200EC-03F516C		
	LFX200EC-04F516C		
	LFX200EC-03F516I		
LFX500EB	LFX500EB-03F516C	**Discontinued**	PCN#09-10
	LFX500EB-04F516C		
	LFX500EB-05F516C		
	LFX500EB-03F516I		
	LFX500EB-04F516I		
	LFX500EB-03F900C		
	LFX500EB-03FN900C		
	LFX500EB-04F900C		
	LFX500EB-04FN900C		
	LFX500EB-05F900C		
	LFX500EB-05FN900C		
	LFX500EB-03F900I		
	LFX500EB-03FN900I		
	LFX500EB-04F900I		
	LFX500EB-04FN900I		
LFX500EC	LFX500EC-03F516C	**Discontinued**	PCN#09-10
	LFX500EC-04F516C		
	LFX500EC-03F516I		

ispXPGA Family Overview

The ispXPGA family of devices provides the ideal vehicle for the creation of high-performance logic designs that are both non-volatile and infinitely re-programmable. Other FPGA solutions force a compromise, being either re-programmable or non-volatile. This family couples this capability with a mainstream architecture containing the features required for today's system-level design.

The ispXPGA family is available in two options. The standard device supports sysHSI capability for ultra fast serial communications while the lower-cost "E-Series" supports the same high-performance FPGA fabric without the sysHSI Block.

Electrically Erasable CMOS (E^2CMOS) memory cells provide the ispXPGA family with non-volatile capability. These allow logic to be functional microseconds after power is applied, allowing easy interfacing in many applications. This capability also means that expensive external configuration memories are not required and that designs can be secured from unauthorized read back. Internal SRAM cells allow the device to be infinitely reconfigured if desired. Both the SRAM and E^2CMOS cells can be programmed and verified through the IEEE 1532 industry standard. Additionally, the SRAM cells can be configured and read-back through the sysCONFIG™ peripheral port.

The family spans the density and I/O range required for the majority of today's logic designs, 139K to 1.25M functional gates and 160 to 496 I/O. The devices are available for operation from 1.8V, 2.5V, and 3.3V power supplies, providing easy integration into the overall system.

System-level design needs are met through the incorporation of sysMEM dual-port memory blocks, sysIO advanced I/O support, and sysCLOCK Phase Locked Loops (PLLs). High-speed serial communications are supported through multiple sysHSI blocks, which provide clock data recovery (CDR) and serialization/de-serialization (SERDES).

The ispLEVER™ design tool from Lattice allows easy implementation of designs using the ispXPGA product. Synthesis library support is available for major logic synthesis tools. The ispLEVER tool takes the output from these common synthesis packages and place and routes the design in the ispXPGA product. The tool supports floor planning and the management of other constraints within the device. The tool also provides outputs to common timing analysis tools for timing analysis.

To increase designer productivity, Lattice provides a variety of pre-designed modules referred to as IP cores for the ispXPGA product. These IP cores allow designers to concentrate on the unique portions of their design while using pre-designed blocks to implement standard functions such as bus interfaces, standard communication interfaces, and memory controllers.

Through the use of advanced technology and innovative architecture the ispXPGA FPGA devices provide designers with excellent speed performance. Although design dependent, many typical designs can run at over 150MHz. Certain designs can run at over 300MHz. Table 2 details the performance of several building blocks commonly used by logic designers.

Table 2. ispXPGA Speed Performance for Typical Building Blocks

Function	Performance
8:1 Asynch MUX	150 MHz
1:32 Asynch Demultiplexer	125 MHz
8 x 8 2-LL Pipelined Multiplier	225 MHz
32-bit Up/Down Counter	290 MHz
32-bit Shift Register	360 MHz

sysCLOCK PLL Description

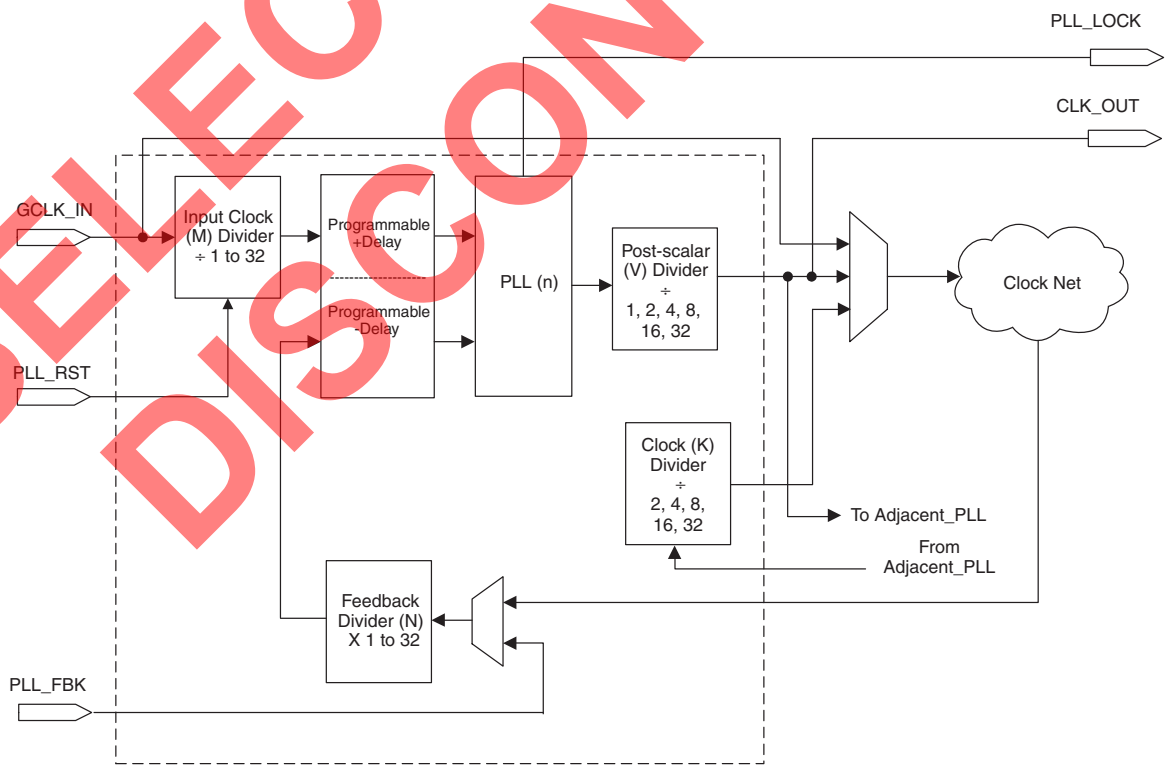
The sysCLOCK PLL circuitry consists of Phase-Lock Loops (PLLs) and the various dividers, reset, and feedback signals associated with the PLLs. This feature gives the user the ability to synthesize clock frequencies and generate multiple clock signals for routing within the device. Furthermore, it can generate clock signals that are aligned either at the board level or the device level.

The ispXPGA devices provide up to eight PLLs. Each PLL receives its input clock from its associated global clock pin, and its output is routed to the associated global clock net. For example, PLL0 receives its clock input from the GCLK0 global clock pin and provides output to the CLK0 global clock net. The PLL also has the ability to output a secondary clock that is a division of the primary clock output. When using the secondary clock, the secondary clock will be routed to the neighboring global clock net. For example, PLL0 will drive its primary clock output on the CLK0 global clock net and its secondary clock output will drive the CLK1 global clock net. Additionally, each PLL has a set of PLL_RST, PLL_FBK, and PLL_LOCK signals. The PLL_RST signal can be generated through routing or a dedicated dual-function I/O pin. The PLL_FBK signal can be generated through a dedicated dual-function I/O pin or internally from the Global Clock net associated with the PLL. The PLL_LOCK signal feeds routing directly from the sysCLOCK PLL circuit. Figure 17 illustrates how the PLL_RST and PLL_FBK signals are generated.

Each PLL has four dividers associated with it, M, N, V, and K. The M divider is used to divide the clock signal, while the N divider is used to multiply the clock signal. The V divider allows the VCO frequency to operate at higher frequencies than the clock output, thereby increasing the frequency range. The K divider is only used when a secondary clock output is needed. This divider divides the primary clock output and feeds to the adjacent global clock net. Different combinations of these dividers allow the user to synthesize clock frequencies. Figure 16 shows the ispXPGA PLL block diagram.

The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. This operates by inserting delay on the input or feedback lines of the PLL. For more information on the PLL, please refer to TN1003, sysCLOCK PLL Usage and Design Guidelines.

Figure 16. ispXPGA PLL Block Diagram



ispXPGA 125B/C & ispXPGA 125EB/EC Timing Adders

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	4.28	—	4.6	—	5.29	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

ispXPGA 200B/C & ispXPGA 200EB/EC EBR Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Synchronous Write								
t_{EBSWAD_S}	Address Setup Delay	0.59	—	0.61	—	0.70	—	ns
t_{EBSWAD_H}	Address Hold Delay	-0.40	—	-0.39	—	-0.33	—	ns
$t_{EBSWCPW}$	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t_{EBSWWE_S}	Write Enable Setup Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{EBSWWE_H}	Write Enable Hold Time	0.16	—	0.16	—	0.18	—	ns
t_{EBSWD_S}	Data Setup Time	0.27	—	0.28	—	0.32	—	ns
t_{EBSWD_H}	Data Hold Time	-0.27	—	-0.26	—	-0.22	—	ns
Synchronous Read								
t_{EBSR_CO}	Clock to Data Delay	—	2.04	—	2.19	—	2.52	ns
t_{EBSRAD_S}	Address Setup Delay	0.10	—	0.10	—	0.12	—	ns
t_{EBSRAD_H}	Address Hold Delay	-0.07	—	-0.07	—	-0.06	—	ns
$t_{EBSRCPW}$	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t_{EBSRCE_S}	Clock Enable Setup Time	-1.76	—	-1.71	—	-1.45	—	ns
t_{EBSRCE_H}	Clock Enable Hold Time	1.64	—	1.69	—	1.94	—	ns
t_{EBSRWE_S}	Write Enable Setup Time	-0.18	—	-0.17	—	-0.14	—	ns
t_{EBSRWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{EBSRWEEN}$	Write Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBSRWEDIS}$	Write Enable to Data Disable Time	—	0.99	—	1.02	—	1.17	ns
t_{EBSREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBSRDIS}$	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns
Asynchronous Read								
$t_{EBARADO}$	Address to New Valid Data Delay	—	2.39	—	2.46	—	2.83	ns
t_{EBARAD_H}	Address to Previous Valid Data Delay	—	2.10	—	2.17	—	2.50	ns
$t_{EBARWEEN}$	Write Enable to Data Enable Time	—	1.01	—	1.04	—	1.20	ns
$t_{EBARWEDIS}$	Write Enable to Data Disable Time	—	0.98	—	1.01	—	1.16	ns
t_{EBAREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBARDIS}$	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 500B/C & ispXPGA 500EB/EC Timing Adders (Cont.)

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LVCMOS_33_4mA_out	Using 3.3V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_33_5.33mA_out	Using 3.3V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_33_8mA_out	Using 3.3V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_33_12mA_out	Using 3.3V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_33_16mA_out	Using 3.3V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_33_24mA_out	Using 3.3V CMOS Standard, 24mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_out	Using AGP 1x Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
CTT25_out	Using CTT 2.5V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
CTT33_out	Using CTT 3.3V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
GTL+_out	Using GTL+	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_out	Using HSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_out	Using HSTL 2.5V, Class III	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVDS_out	Using Low Voltage Differential Signaling (LVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
BLVDS_out	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVPECL_out	Using Low Voltage PECL	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
PCI_out	Using PCI Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL2_I_out	Using SSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL2_II_out	Using SSTL 2.5V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_out	Using SSTL 3.3V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL3_II_out	Using SSTL 3.3V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

1. Only available for ispXPGA 500B and ispXPGA 500EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 1200B/C & ispXPGA 1200EB/EC PFU Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Functional Delays								
LUTs								
t_{LUT4}	4-Input LUT Delay	—	0.41	—	0.44	—	0.51	ns
t_{LUT5}	5-Input LUT Delay	—	0.73	—	0.79	—	0.91	ns
t_{LUT6}	6-Input LUT Delay	—	0.86	—	0.93	—	1.07	ns
Shift Register (LUT)								
t_{LSR_S}	Shift Register Setup Time	-0.64	—	-0.62	—	-0.53	—	ns
t_{LSR_H}	Shift Register Hold Time	0.61	—	0.63	—	0.72	—	ns
t_{LSR_CO}	Shift Register Clock to Output Delay	—	0.70	—	0.75	—	0.86	ns
Arithmetic Functions								
$t_{LCTHRUR}$	MC (Macro Cell) Carry In to MC Carry Out Delay (Ripple)	—	0.08	—	0.09	—	0.10	ns
$t_{LCTHRUL}$[2]	MC Carry In to MC Carry Out Delay (Look Ahead)	—	0.05	—	0.05	—	0.06	ns
t_{LSTHRU}	MC Sum In to MC Sum Out Delay	—	0.42	—	0.45	—	0.52	ns
$t_{LSINCOUT}$	MC Sum In to MC Carry Out Delay	—	0.29	—	0.31	—	0.36	ns
$t_{LCINSOUTR}$	MC Carry In to MC Sum Out Delay (Ripple)	—	0.36	—	0.39	—	0.45	ns
$t_{LCINSOUTL}$	MC Carry In to MC Sum Out Delay (Look Ahead)	—	0.26	—	0.28	—	0.32	ns
Feed-thru								
t_{LFT}	PFU Feed-Thru Delay	—	0.15	—	0.16	—	0.18	ns
Distributed RAM								
t_{LRAM_CO}	Clock to RAM Output	—	1.24	—	1.33	—	1.53	ns
t_{LRAMAD_S}	Address Setup Time	-0.41	—	-0.40	—	-0.34	—	ns
t_{LRAMD_S}	Data Setup Time	0.21	—	0.22	—	0.25	—	ns
t_{LRAMWE_S}	Write Enable Setup Time	0.45	—	0.46	—	0.53	—	ns
t_{LRAMAD_H}	Address Hold Time	0.58	—	0.60	—	0.69	—	ns
t_{LRAMD_H}	Data Hold Time	0.11	—	0.11	—	0.13	—	ns
t_{LRAMWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{LRAMCPW}$	Clock Pulse Width (High or Low)	2.91	—	3.00	—	3.45	—	ns
$t_{LRAMADO}$	Address to Output Delay	—	0.86	—	0.93	—	1.07	ns
Register/Latch Delays								
Registers								
t_{L_CO}	Register Clock to Output Delay	—	0.58	—	0.62	—	0.71	ns
t_{L_S}	Register Setup Time (Data before Clock)	0.14	—	0.14	—	0.16	—	ns
t_{L_H}	Register Hold Time (Data after Clock)	-0.12	—	-0.12	—	-0.10	—	ns
t_{LCE_S}	Register Clock Enable Setup Time	-0.11	—	-0.11	—	-0.09	—	ns
t_{LCE_H}	Register Clock Enable Hold Time	0.11	—	0.11	—	0.13	—	ns
Latches								
t_{L_GO}	Latch Gate to Output Delay	—	0.09	—	0.10	—	0.12	ns
t_{LL_S}	Latch Setup Time	0.14	—	0.14	—	0.16	—	ns
t_{LL_H}	Latch Hold Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{LLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns

ispXPGA 1200B/C & ispXPGA 1200EB/EC Timing Adders

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	5.58	—	6.0	—	6.90	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

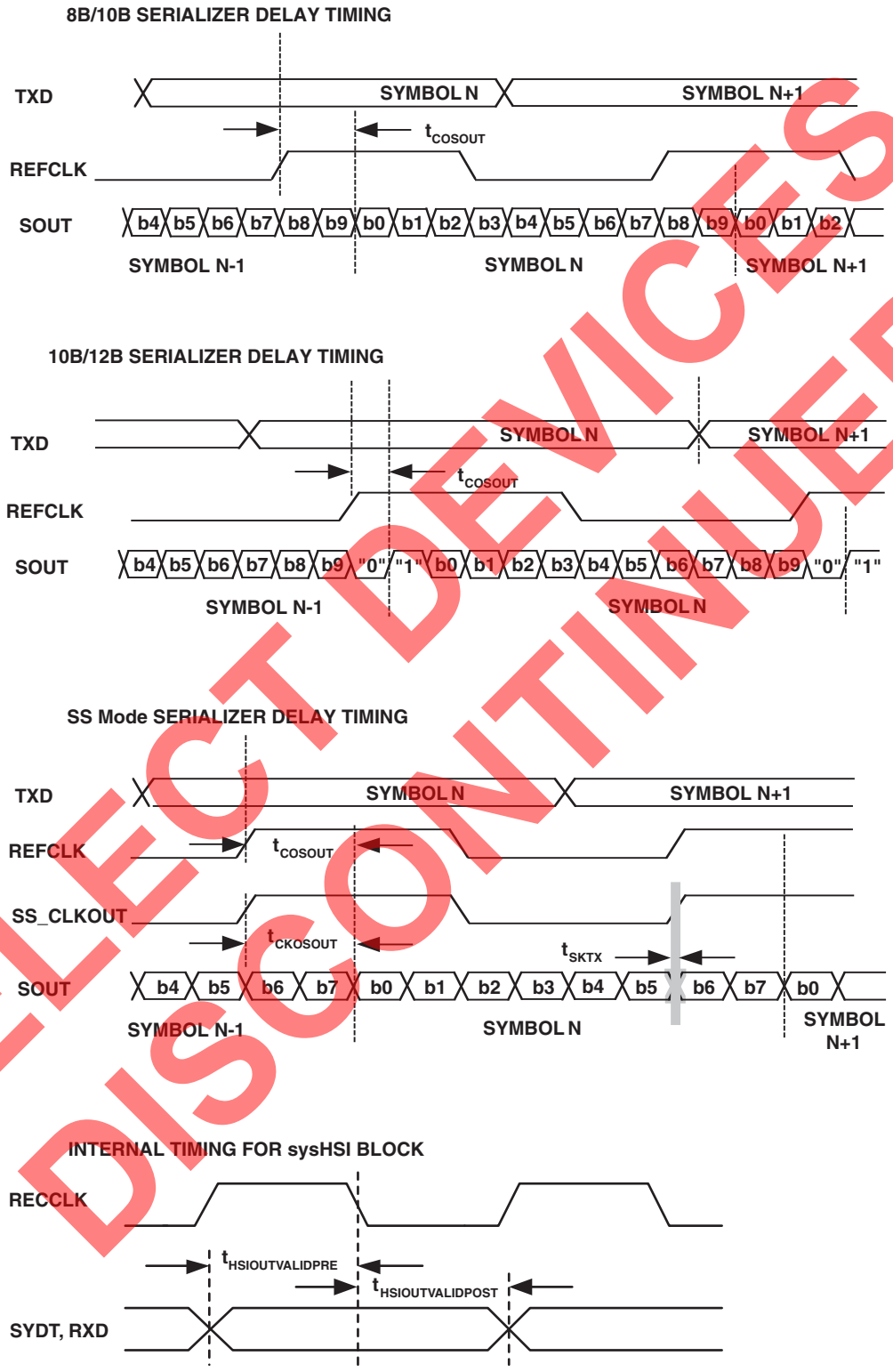
ispXPGA 1200B/C & ispXPGA 1200EB/EC Timing Adders (Cont.)

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LVCMOS_33_4mA_out	Using 3.3V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_33_5.33mA_out	Using 3.3V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_33_8mA_out	Using 3.3V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_33_12mA_out	Using 3.3V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_33_16mA_out	Using 3.3V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_33_24mA_out	Using 3.3V CMOS Standard, 24mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_out	Using AGP 1x Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
CTT25_out	Using CTT 2.5V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
CTT33_out	Using CTT 3.3V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
GTL+_out	Using GTL+	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_out	Using HSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_out	Using HSTL 2.5V, Class III	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVDS_out	Using Low Voltage Differential Signaling (LVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
BLVDS_out	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVPECL_out	Using Low Voltage PECL	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
PCI_out	Using PCI Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL2_I_out	Using SSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL2_II_out	Using SSTL 2.5V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_out	Using SSTL 3.3V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL3_II_out	Using SSTL 3.3V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

1. Only available for ispXPGA 1200B and ispXPGA 1200EB (2.5V/3.3V) devices.

Timing v.2.1

Serializer Timing



ispXP sysCONFIG Port Timing Specifications

Symbol	Timing Parameter	Min.	Typ.	Max.	Units
sysCONFIG Write Cycle Timing					
t_{SUCS}	Input setup time of CS to CCLK rise	10	—	—	ns
t_{HCS}	Hold time of CS to CCLK Rise	0	—	—	ns
t_{SUWD}	Input setup time of write data to CCLK rise	12	—	—	ns
t_{HWD}	Hold time of write data to CCLK rise	0	—	—	ns
t_{PRGM}	Low time to reset device SRAM	5	—	50	ns
t_{WINIT}	INIT pulse width	—	—	5	ms
t_{IODISS}	User I/O disable	—	—	30	ns
t_{IOENSS}	User I/O enable	—	—	30	ns
t_{WH}	Write clock High pulse width	12	—	—	ns
t_{WL}	Write clock Low pulse width	12	—	—	ns
f_{MAXW}	Write f_{MAX}	—	—	33	MHz
sysCONFIG Read Cycle Timing					
t_{HREAD}	Hold time of READ to CCLK rise	0	—	—	ns
t_{SUREAD}	Input setup time of READ High to CCLK rise	30	—	—	ns
t_{RH}	READ clock high pulse width	12	—	—	ns
t_{RL}	READ clock low pulse width	15	—	—	ns
f_{MAXR}	Read f_{MAX}	—	—	33	MHz
t_{CORD}	Clock to out for read data	—	—	25	ns

Boundary Scan Timing

Parameter	Description	Min.	Max.	Units
t_{BTCP}	TCK [BSCAN] Clock Pulse Width	40	—	ns
t_{BTCPH}	TCK [BSCAN] Clock Pulse Width High	20	—	ns
t_{BTCPL}	TCK [BSCAN] Clock Pulse Width Low	20	—	ns
t_{BTS}	TCK [BSCAN] Setup Time	8	—	ns
t_{BTH}	TCK [BSCAN] Hold Time	10	—	ns
t_{BTRF}	TCK [BSCAN] Rise/Fall Time	50	—	mV/ns
t_{BTCO}	TAP Controller Falling Edge of Clock to Valid Output	—	18	ns
$t_{BTCODIS}$	TAP Controller Falling Edge of Clock to Valid Disable	—	18	ns
t_{BTCOEN}	TAP Controller Falling Edge of Clock to Valid Enable	—	18	ns
t_{BTCRS}	BSCAN Test Capture Register Setup Time	8	—	ns
t_{BTCRH}	BSCAN Test Capture Register Hold Time	25	—	ns
t_{BUTCO}	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	45	ns
$t_{BTUODIS}$	BSCAN Test Update Register, Falling Edge of Clock to Valid Disable	—	20	ns
$t_{BTUPOEN}$	BSCAN Test Update Register, Falling Edge of Clock to Valid Enable	—	20	ns

ispXPGA Power Supply and NC Connections[1] (Continued)

Signal	680-Ball fpBGA[3]	900-Ball fpBGA[3]
NC[2]	A3, B29, AW3, AV3, AW11, AV11, AV29, AW29, AW37, B3, AV37, C39, C38, AU39, AU38, AJ39, AJ38, N38, N39, C2, C1, AU1, AU2, AJ2, AJ1, N2, N1, B11, A11, A37, B37, A29	**LFX500:** A8, A9, A10, A11, A19, A20, A21, A22, B8, B9, B10, B11, B19, B20, B21, B22, C1, C2, C11, C12, C19, C20, C23, D3, D10, D11, D12, D19, D20, D21, D22, D23, E3, E5, E6, E10, E11, E12, E21, E22, E25, E26, E28, E29, E30, F1, F2, F6, F9, F10, F11, F12, F21, F22, F25, F26, F29, F30, G1, G2, G3, G4, G7, G8, G9, G10, G11, G12, G14, G15, G16, G17, G19, G20, G21, G22, G23, G24, G25, G26, G27, G28, G29, G30, H1, H2, H3, H4, H5, H6, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, H17, H18, H19, H20, H21, H22, H23, H24, H27, H28, H29, H30, J1, J2, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, K6, K7, K8, K9, K10, K12, K13, K14, K15, K16, K17, K18, K19, K21, K22, K23, K24, K25, L7, L8, L9, L22, L23, L24, M7, M8, M9, M10, M21, M22, M23, M24, N8, N9, N10, N21, N22, N23, P7, P8, P9, P10, P21, P22, P23, P24, R8, R9, R10, R21, R22, R23, R24, R25, T6, T7, T8, T9, T10, T21, T22, T23, T24, T25, U7, U8, U9, U10, U21, U22, U23, U24, V8, V9, V10, V21, V22, V23, W7, W8, W9, W10, W21, W22, W23, W24, W25, W26, Y3, Y4, Y5, Y6, Y7, Y8, Y9, Y22, Y23, Y24, Y25, Y26, Y27, Y28, AA4, AA5, AA6, AA7, AA8, AA9, AA10, AA12, AA13, AA14, AA15, AA16, AA17, AA18, AA19, AA21, AA22, AA23, AA24, AA25, AA26, AA27, AB1, AB2, AB4, AB5, AB6, AB7, AB8, AB9, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB18, AB19, AB20, AB21, AB22, AB23, AB24, AB25, AB26, AB27, AC1, AC2, AC3, AC4, AC5, AC6, AC7, AC8, AC9, AC10, AC11, AC12, AC13, AC14, AC15, AC16, AC17' AC18' AC19, AC20, AC21, AC22, AC23, AC24, AC27, AC28, AC29, AC30, AD1, AD2, AD7, AD8, AD9, AD10, AD11, AD12, AD14, AD15, AD16, AD17, AD19, AD20, AD21, AD22, AD23, AD24, AD29, AD30, AE6, AE9, AE10, AE11, AE12, AE19, AE20, AE21, AE22, AE25, AE29, AE30, AF5, AF6, AF10, AF11, AF12, AF19, AF20, AF21, AF22, AF25, AF26, AG10, AG11, AG12, AG19, AG20, AG21, AG22, AH11, AH12, AH19, AH20, AJ8, AJ9, AJ10, AJ11, AJ20, AJ21, AJ22, AK8, AK9, AK10, AK11, AK20, AK21, AK22 **LFX1200:** AA22, AA23, AA24, AA25, AB23, AC24, T21, T22, T23, T24, T25, U21, U22, U23, U24, V21, V22, V23, W21, W22, W23, W24, Y22, Y23, Y24, AA16, AA17, AA18, AA19, AA21, AB16, AB17, AB18, AB19, AB20, AB21, AB22, AC16, AC17, AC18, AC19, AC20, AC21, AC22, AC23, AD16, AD17, AD19, AD20, AD22, AD23, AD24, AE22, AE25, AF25, AF26, AA10, AA12, AA13, AA14, AA15, AB10, AB11, AB12, AB13, AB14, AB15, AB9, AC10, AC11, AC12, AC13, AC14, AC15, AC8, AC9, AD11, AD12, AD14, AD15, AD7, AD8, AD9, AE6, AE9, AF5, AF6, H24, J23, K22, K23, K24, K25, L22, L23, L24, M21, M22, M23, M24, N21, N22, N23, P21, P22, P23, P24, R21, R22, R23, R24, R25, AA6, AA7, AA8, AA9, AB8, AC7, T10, T6, T7, T8, T9, U10, U7, U8, U9, V10, V8, V9, W10, W7, W8, W9, Y7, Y8, Y9, H5, H6, H7, J8, K6, K7, K8, K9, L7, L8, L9, M10, M7, M8, M9, N10, N8, N9, P10, P7, P8, P9, R10, R8, R9, E25, E26, F22, F25, G16, G17, G19, G20, G22, G23, G24, H16, H17, H18, H19, H20, H21, H22, H23, J16, J17, J18, J19, J20, J21, J22, K16, K17, K18, K19, K21, E5, E6, F6, F9, G11, G12, G14, G15, G7, G8, G9, H10, H11, H12, H13, H14, H15, H8, H9, J10, J11, J12, J13, J14, J15, J9, K10, K12, K13, K14, K15

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, V_{CC} or GND.
3. Balls for GND, V_{CC} and V_{CCOx} are connected within the substrate to their respective common signals. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
AH39	BK3_IO31	-	108N
AK39	BK3_IO32	-	109P
AK38	BK3_IO33	-	109N
AF35	BK3_IO34	-	110P
-	GND (Bank 3)	-	-
AJ37	BK3_IO35	-	110N
AH36	BK3_IO36	-	111P
AM39	BK3_IO37	-	111N
AL38	BK3_IO38	-	112P
AL39	BK3_IO39	-	112N
AJ36	BK3_IO40	-	113P
AH35	BK3_IO41	-	113N
AL37	BK3_IO42	-	114P
-	GND (Bank 3)	-	-
AN38	BK3_IO43	-	114N
AM38	BK3_IO44	-	115P
AK36	BK3_IO45	-	115N
AM37	BK3_IO46	-	116P
AN37	BK3_IO47	-	116N
AN39	BK3_IO48	-	117P
AL36	BK3_IO49	VREF3	117N
AK35	BK3_IO50	-	118P
-	GND (Bank 3)	-	-
AP39	BK3_IO51	-	118N
AM36	BK3_IO52	-	119P
AP38	BK3_IO53	-	119N
AR39	BK3_IO54	-	120P
AN36	BK3_IO55	-	120N
AM35	BK3_IO56	-	121P
AR38	BK3_IO57	-	121N
AP37	BK3_IO58	-	122P
-	GND (Bank 3)	-	-
AT39	BK3_IO59	-	122N
AR37	BK3_IO60	-	123P
AP36	BK3_IO61	-	123N
AT38	GSR	-	-
AP35	DXP	-	-
AT37	DXN	-	-
AU36	BK4_IO0	-	124P
AV36	BK4_IO1	-	124N
AR34	BK4_IO2	-	125P
-	GND (Bank 4)	-	-
AW36	BK4_IO3	-	125N

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
Y5	BK6_IO61	-	216N
-	GND (Bank 6)	-	-
-	GND (Bank 7)	-	-
W3	BK7_IO0	-	217P
W1	BK7_IO1	-	217N
W2	BK7_IO2	-	218P
-	GND (Bank 7)	-	-
W4	BK7_IO3	-	218N
V1	BK7_IO4	-	219P
V2	BK7_IO5	-	219N
V3	BK7_IO6	-	220P
V4	BK7_IO7	-	220N
W5	BK7_IO8	-	221P
U1	BK7_IO9	-	221N
U2	BK7_IO10	-	222P
-	GND (Bank 7)	-	-
U3	BK7_IO11	-	222N
U4	BK7_IO12	-	223P
T1	BK7_IO13	-	223N
T2	BK7_IO14	-	224P
T3	BK7_IO15	-	224N
R1	BK7_IO16	-	225P
R2	BK7_IO17	-	225N
T4	BK7_IO18	-	226P
-	GND (Bank 7)	-	-
P1	BK7_IO19	-	226N
P2	BK7_IO20	-	227P
P3	BK7_IO21	-	227N
R4	BK7_IO22	-	228P
T5	BK7_IO23	-	228N
M1	BK7_IO24	-	229P
M2	BK7_IO25	-	229N
N3	BK7_IO26	-	230P
-	GND (Bank 7)	-	-
P4	BK7_IO27	-	230N
L1	BK7_IO28	-	231P
M3	BK7_IO29	-	231N
L2	BK7_IO30	-	232P
N4	BK7_IO31	-	232N
K1	BK7_IO32	-	233P
K2	BK7_IO33	-	233N
P5	BK7_IO34	-	234P
-	GND (Bank 7)	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AK5	BK2_IO7	-	65N	BK2_IO7	-	45N
AE7	BK2_IO8	-	66P	BK2_IO8	-	46P
AF7	BK2_IO9	-	66N	BK2_IO9	-	46N
AG7	BK2_IO10	-	67P	BK2_IO10	-	47P
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
AH7	BK2_IO11	-	67N	BK2_IO11	-	47N
AE8	BK2_IO12	VREF2	68P	BK2_IO21	VREF2	52N
AF8	BK2_IO13	-	68N	BK2_IO20	-	52P
AJ6	BK2_IO14	-	69P	BK2_IO12	-	48P
AK6	BK2_IO15	-	69N	BK2_IO13	-	48N
AG8	BK2_IO16	-	70P	BK2_IO14	-	49P
AH8	BK2_IO17	-	70N	BK2_IO15	-	49N
AJ7	BK2_IO18	-	71P	BK2_IO16	-	50P
-	GND (Bank 2)	-	-	-	-	-
AK7	BK2_IO19	-	71N	BK2_IO17	-	50N
AF9	BK2_IO20	-	72P	BK2_IO18	-	51P
-	-	-	-	GND (Bank 2)	-	-
AG9	BK2_IO21	-	72N	BK2_IO19	-	51N
AJ8	BK2_IO22	-	73P	NC	-	-
AK8	BK2_IO23	-	73N	NC	-	-
AD10	BK2_IO24	-	74P	NC	-	-
AE10	BK2_IO25	-	74N	NC	-	-
AJ9	BK2_IO26	-	75P	NC	-	-
-	GND (Bank 2)	-	-	-	-	-
AK9	BK2_IO27	-	75N	NC	-	-
AF10	BK2_IO28	-	76P	NC	-	-
AG10	BK2_IO29	-	76N	NC	-	-
AK10	BK2_IO30	-	77P	NC	-	-
AJ10	BK2_IO31	-	77N	NC	-	-
AE11	BK2_IO32	-	78P	NC	-	-
AF11	BK2_IO33	-	78N	NC	-	-
AG11	BK2_IO34	-	79P	NC	-	-
-	GND (Bank 2)	-	-	-	-	-
AH11	BK2_IO35	-	79N	NC	-	-
AE12	BK2_IO36	-	80P	NC	-	-
AF12	BK2_IO37	-	80N	NC	-	-
AJ11	BK2_IO38	-	81P	NC	-	-
AK11	BK2_IO39	-	81N	NC	-	-
AG12	BK2_IO40	-	82P	NC	-	-
AH12	BK2_IO41	-	82N	NC	-	-
AK12	BK2_IO42	-	83P	BK2_IO22	-	53P
-	GND (Bank 2)	-	-	-	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
K30	BK5_IO22	HSI7B_SOUTP	166P/HSI8	BK5_IO22	HSI4B_SOUTP	116P/HSI4
-	-	-	-	GND (Bank 5)	-	-
K29	BK5_IO23	HSI7B_SOUTN	166N/HSI8	BK5_IO23	HSI4B_SOUTN	116N/HSI4
L28	BK5_IO24	-	167P/HSI8	BK5_IO24	-	117P/HSI5
L27	BK5_IO25	-	167N/HSI8	BK5_IO25	-	117N/HSI5
L26	BK5_IO26	HSI8A_SINP	168P/HSI8	BK5_IO26	HSI5A_SINP	118P/HSI5
-	GND (Bank 5)	-	-	-	-	-
L25	BK5_IO27	HSI8A_SINN	168N/HSI8	BK5_IO27	HSI5A_SINN	118N/HSI5
K27	BK5_IO28	-	169P/HSI8	BK5_IO28	-	119P/HSI5
K26	BK5_IO29	-	169N/HSI8	BK5_IO29	-	119N/HSI5
J30	BK5_IO30	HSI8A_SOUTP	170P/HSI8	BK5_IO30	HSI5A_SOUTP	120P/HSI5
-	-	-	-	GND (Bank 5)	-	-
J29	BK5_IO31	HSI8A_SOUTN	170N/HSI8	BK5_IO31	HSI5A_SOUTN	120N/HSI5
J26	BK5_IO32	-	171P/HSI8	NC	-	-
J27	BK5_IO33	-	171N/HSI8	NC	-	-
H30	BK5_IO34	HSI8B_SINP	172P/HSI8	NC	-	-
-	GND (Bank 5)	-	-	-	-	-
H29	BK5_IO35	HSI8B_SINN	172N/HSI8	NC	-	-
J25	BK5_IO36	-	173P/HSI9	NC	-	-
J24	BK5_IO37	-	173N/HSI9	NC	-	-
G30	BK5_IO38	HSI8B_SOUTP	174P/HSI9	NC	-	-
G29	BK5_IO39	HSI8B_SOUTN	174N/HSI9	NC	-	-
H27	BK5_IO40	-	175P/HSI9	NC	-	-
H28	BK5_IO41	-	175N/HSI9	NC	-	-
F30	BK5_IO42	HSI9A_SINP	176P/HSI9	NC	-	-
-	GND (Bank 5)	-	-	-	-	-
F29	BK5_IO43	HSI9A_SINN	176N/HSI9	NC	-	-
G27	BK5_IO44	-	177P/HSI9	NC	-	-
G28	BK5_IO45	-	177N/HSI9	NC	-	-
E30	BK5_IO46	HSI9A_SOUTP	178P/HSI9	NC	-	-
E29	BK5_IO47	HSI9A_SOUTN	178N/HSI9	NC	-	-
H26	BK5_IO48	-	179P/HSI9	BK5_IO33	-	121N/HSI5
H25	BK5_IO49	VREF5	179N/HSI9	BK5_IO32	VREF5	121P/HSI5
D30	BK5_IO50	HSI9B_SINP	180P/HSI9	BK5_IO34	HSI5B_SINP	122P/HSI5
-	GND (Bank 5)	-	-	-	-	-
D29	BK5_IO51	HSI9B_SINN	180N/HSI9	BK5_IO35	HSI5B_SINN	122N/HSI5
F28	BK5_IO52	-	181P	BK5_IO36	-	123P/HSI5
F27	BK5_IO53	-	181N	BK5_IO37	-	123N/HSI5
C30	BK5_IO54	HSI9B_SOUTP	182P	BK5_IO38	HSI5B_SOUTP	124P/HSI5
-	-	-	-	GND (Bank 5)	-	-
C29	BK5_IO55	HSI9B_SOUTN	182N	BK5_IO39	HSI5B_SOUTN	124N/HSI5
G26	BK5_IO56	-	183P	NC	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
G25	BK5_IO57	-	183N	NC	-	-
F26	BK5_IO58	-	184P	NC	-	-
-	GND (Bank 5)	-	-	-	-	-
E28	BK5_IO59	-	184N	NC	-	-
E27	BK5_IO60	-	185P	BK5_IO40	-	125P
D28	BK5_IO61	-	185N	BK5_IO41	-	125N
C27	CFG0	-	-	CFG0	-	-
B28	DONE	-	-	DONE	-	-
A28	PROGRAMb	-	-	PROGRAMb	-	-
D26	BK6_IO0	INITb	186P	BK6_IO0	INITb	126P
C26	BK6_IO1	CCLK	186N	BK6_IO1	CCLK	126N
B27	BK6_IO2	-	187P	BK6_IO2	-	127P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
A27	BK6_IO3	-	187N	BK6_IO3	-	127N
D25	BK6_IO4	CSb	188P	BK6_IO4	CSb	128P
C25	BK6_IO5	Read	188N	BK6_IO5	READ	128N
B26	BK6_IO6	-	189P	BK6_IO6	-	129P
A26	BK6_IO7	-	189N	BK6_IO7	-	129N
F24	BK6_IO8	-	190P	BK6_IO8	-	130P
E24	BK6_IO9	-	190N	BK6_IO9	-	130N
A25	BK6_IO10	-	191P	BK6_IO10	-	131P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
B25	BK6_IO11	-	191N	BK6_IO11	-	131N
D24	BK6_IO12	VREF6	192P	BK6_IO21	VREF6	136N
C24	BK6_IO13	-	192N	BK6_IO20	-	136P
A24	BK6_IO14	-	193P	BK6_IO12	-	132P
B24	BK6_IO15	-	193N	BK6_IO13	-	132N
F23	BK6_IO16	-	194P	BK6_IO14	-	133P
E23	BK6_IO17	-	194N	BK6_IO15	-	133N
A23	BK6_IO18	-	195P	BK6_IO16	-	134P
-	GND (Bank 6)	-	-	-	-	-
B23	BK6_IO19	-	195N	BK6_IO17	-	134N
C23	BK6_IO20	-	196P	NC	-	-
D23	BK6_IO21	-	196N	NC	-	-
E22	BK6_IO22	-	197P	NC	-	-
D22	BK6_IO23	-	197N	NC	-	-
G21	BK6_IO24	-	198P	NC	-	-
F21	BK6_IO25	-	198N	NC	-	-
B22	BK6_IO26	-	199P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-
A22	BK6_IO27	-	199N	NC	-	-
E21	BK6_IO28	-	200P	NC	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
B15	BK7_IO1	-	217N	BK7_IO1	-	147N
C15	BK7_IO2	-	218P	BK7_IO2	-	148P
-	GND (Bank 7)	-	-		-	-
D15	BK7_IO3	-	218N	BK7_IO3	-	148N
E15	BK7_IO4	-	219P	BK7_IO4	-	149P
F15	BK7_IO5	-	219N	BK7_IO5	-	149N
A14	BK7_IO6	-	220P	BK7_IO6	-	150P
-	-	-	-	GND (Bank 7)	-	-
B14	BK7_IO7	-	220N	BK7_IO7	-	150N
C14	BK7_IO8	-	221P	BK7_IO8	-	151P
D14	BK7_IO9	-	221N	BK7_IO9	-	151N
E14	BK7_IO10	-	222P	BK7_IO10	-	152P
-	GND (Bank 7)	-	-	-	-	-
F14	BK7_IO11	-	222N	BK7_IO11	-	152N
C13	BK7_IO12	-	223P	BK7_IO12	-	153P
D13	BK7_IO13	-	223N	BK7_IO13	-	153N
B13	BK7_IO14	-	224P	BK7_IO14	-	154P
-	-	-	-	GND (Bank 7)	-	-
A13	BK7_IO15	-	224N	BK7_IO15	-	154N
F13	BK7_IO16	-	225P	BK7_IO16	-	155P
G13	BK7_IO17	-	225N	BK7_IO17	-	155N
A12	BK7_IO18	-	226P	BK7_IO18	-	156P
-	GND (Bank 7)	-	-	-	-	-
B12	BK7_IO19	-	226N	BK7_IO19	-	156N
C12	BK7_IO20	-	227P	NC	-	-
D12	BK7_IO21	-	227N	NC	-	-
A11	BK7_IO22	-	228P	NC	-	-
B11	BK7_IO23	-	228N	NC	-	-
E12	BK7_IO24	-	229P	NC	-	-
F12	BK7_IO25	-	229N	NC	-	-
C11	BK7_IO26	-	230P	NC	-	-
-	GND (Bank 7)	-	-	-	-	-
D11	BK7_IO27	-	230N	NC	-	-
E11	BK7_IO28	-	231P	NC	-	-
F11	BK7_IO29	-	231N	NC	-	-
B10	BK7_IO30	-	232P	NC	-	-
A10	BK7_IO31	-	232N	NC	-	-
D10	BK7_IO32	-	233P	NC	-	-
E10	BK7_IO33	-	233N	NC	-	-
A9	BK7_IO34	-	234P	NC	-	-
-	GND (Bank 7)	-	-	-	-	-
B9	BK7_IO35	-	234N	NC	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
F10	BK7_IO36	-	235P	NC	-	-
G10	BK7_IO37	-	235N	NC	-	-
A8	BK7_IO38	-	236P	NC	-	-
B8	BK7_IO39	-	236N	NC	-	-
D9	BK7_IO40	-	237P	BK7_IO22	-	158P
-	-	-	-	GND (Bank 7)	-	-
E9	BK7_IO41	-	237N	BK7_IO23	-	158N
A7	BK7_IO42	-	238P	BK7_IO24	-	159P
-	GND (Bank 7)	-	-		-	-
B7	BK7_IO43	-	238N	BK7_IO25	-	159N
C8	BK7_IO44	-	239P	BK7_IO26	-	160P
D8	BK7_IO45	-	239N	BK7_IO27	-	160N
A6	BK7_IO46	-	240P	BK7_IO21	-	157N
B6	BK7_IO47	VREF7	240N	BK7_IO20	VREF7	157P
E8	BK7_IO48	-	241P	BK7_IO28	-	161P
F8	BK7_IO49	-	241N	BK7_IO29	-	161N
C7	BK7_IO50	-	242P	BK7_IO30	-	162P
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-
D7	BK7_IO51	-	242N	BK7_IO31	-	162N
E7	BK7_IO52	-	243P	BK7_IO32	-	163P
F7	BK7_IO53	-	243N	BK7_IO33	-	163N
A5	BK7_IO54	-	244P	BK7_IO34	-	164P
B5	BK7_IO55	-	244N	BK7_IO35	-	164N
C6	BK7_IO56	-	245P	BK7_IO36	-	165P
D6	BK7_IO57	-	245N	BK7_IO37	-	165N
D5	BK7_IO58	-	246P	BK7_IO38	-	166P
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-
C5	BK7_IO59	-	246N	BK7_IO39	-	166N
B4	BK7_IO60	-	247P	BK7_IO40	-	167P
A4	BK7_IO61	-	247N	BK7_IO41	-	167N
A3	TDO	-	-	TDO	-	-
B3	VCCJ	-	-	VCCJ	-	-
C4	TDI	-	-	TDI	-	-

1. If a sysHSI Block is used, the indicated sysHSI reserved pins are unavailable for general purpose I/O use.