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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	15376
Total RAM Bits	423936
Number of I/O	496
Number of Gates	1250000
Voltage - Supply	1.65V ~ 1.95V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	680-LBGA
Supplier Device Package	680-FPSBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx1200c-03fe680c

Architecture Overview

The ispXPGA architecture is a symmetrical architecture consisting of an array of Programmable Function Units (PFUs) enclosed by Input Output Groups (PICs) with columns of sysMEM Embedded Block RAMs (EBRs) distributed throughout the array. Figure 1 illustrates the ispXPGA architecture. Each PIC has two corresponding sysIO blocks, each of which includes one input and output buffer. On two sides of the device, between the PICs and the sysIO blocks, there are sysHSI High-Speed Interface blocks. The symmetrical architecture allows designers to easily implement their designs, since any logic function can be placed in any section of the device.

The PFUs contain the basic building blocks to create logic, memory, arithmetic, and register functions. They are optimized for speed and flexibility allowing complex designs to be implemented quickly and efficiently.

The PICs interface the PFUs and EBRs to the external pins of the device. They allow the signals to be registered quickly to minimize setup times for high-speed designs. They also allow connections directly to the different logic elements for fast access to combinatorial functions.

The sysMEM EBRs are large, fast memory elements that can be configured as RAM, ROM, FIFO, and other storage types. They are designed to facilitate both single and dual-port memory for high-speed applications.

These three components of the architecture are interconnected via a high-speed, flexible routing array. The routing array consists of Variable Length Interconnect (VLI) lines between the PICs, PFUs, and EBRs. There is additional routing available to the PFU for feedback and direct routing of signals to adjacent PFUs or PICs.

The sysIO blocks consist of configurable input and output buffers connected directly to the PICs. These buffers can be configured to interface with 16 different I/O standards. This allows the ispXPGA to interface with other devices without the need for external transceivers.

The sysHSI blocks provide the necessary components to allow the ispXPGA device to transfer data at up to 800Mbps using the LVDS standard. These components include serializing, de-serializing, and clock data recovery (CDR) logic.

The sysCLOCK blocks provide clock multiplication/division, clock distribution, delay compensation, and increased performance through the use of PLL circuitry that manipulates the global clocks. There is one sysCLOCK block for each global clock tree in the device.

Configurable Logic Element

The CLE is made up of a four-input Look-up Table (LUT-4), a Carry Chain Generator (CCG), and a two-input AND gate. The LUT-4 creates various combinatorial and memory elements, the CCG creates a single one-bit full adder, and the two-input AND gate can expand the CCG to incorporate Booth Multiplier capability by feeding the output of the AND gate to one of the inputs of the CCG.

Of the five inputs that feed each CLE, two are dedicated inputs into each LUT-4 and the remaining three take on varying functionality. The third and fourth inputs can be used as either inputs to the LUT-4 or as a Feed-Thru to the CSE via the WLG. The fifth input can be a data port when the LUT is configured as Distributed Memory, a select line for multiplexer operation, or a Feed-Thru directly to the CSE via the WLG (Figure 2).

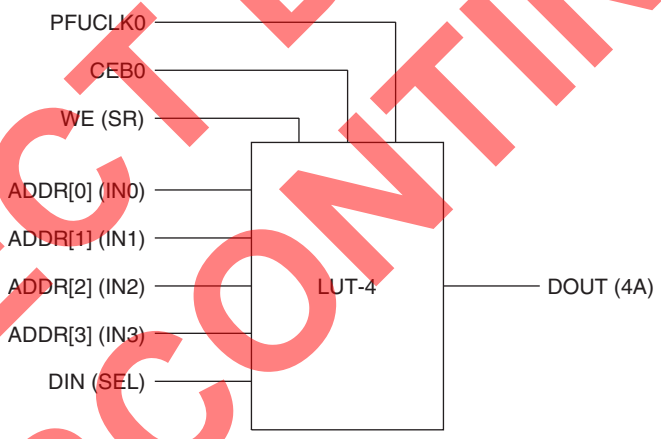
Look-Up Table – Combinatorial Mode

In combinatorial mode, the LUT-4 can implement any logic function up to four inputs. By using the carry chain and the WLG, each LUT-4 can be combined to form the enhanced functions listed in Table 3.

Look-Up Table – Distributed Memory Mode

In the distributed memory mode, the LUT functions as a memory element. The inputs to the LUT function as Address and Data. Each PFU is capable of implementing up to 64 SRAM bits. Both single and double port RAM can be performed in the PFU (Table 3). Furthermore, the distributed memory can be configured as either synchronous or asynchronous memory. Figure 3 illustrates the LUT while in distributed memory mode. When using any LUT in the PFU in memory mode, the Set/Reset signal will be used for Write Enable (WE(SR)) and the CLK0 signal will be used as the clock for synchronous read and write.

Figure 3. LUT in Distributed Memory Mode



Look-Up Table – Shift Register Mode

In the shift register mode, the LUT functions as a 1-bit to 8-bit shift register. This means that each PFU can implement up to four 8-bit shift registers or any cascaded combination. Figure 4 illustrates the LUT when configured in shift register mode.

Memory

The ispXPGA architecture provides a large amount of resources for memory intensive applications. Embedded Block RAMs (EBRs) are available to complement the Distributed Memory that is configured in the PFUs (see Look-Up Table -Distributed Memory Mode in the PFU section above). Each memory element can be configured as RAM or ROM. Additionally, the internal logic of the device can be used to configure the memory elements as FIFO and other storage types. These EBRs are referred to as sysMEM blocks. Refer to Table 1 for memory resources per device.

sysMEM Blocks

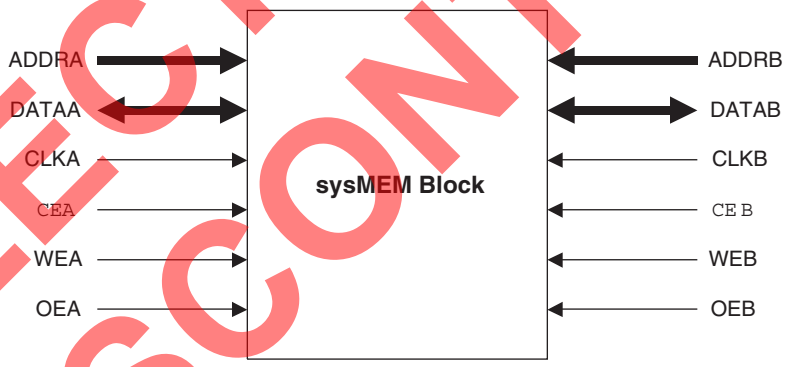
The sysMEM blocks are organized in columns distributed throughout the device. Each EBR contains 4.6K bits of dual-port RAM with dedicated control, address, and data lines for each port. Each column of sysMEM blocks has dedicated address and control lines that can be used by each block separately or cascaded to form larger memory elements. The memory cells are symmetrical and contain two sets of identical control signals. Each port has a read/write clock, clock enable, write enable, and output enable. Figure 12 illustrates the sysMEM block.

The ispXPGA memory block can operate as single-port or dual-port RAM. Supported configurations are:

- 512 x 9 bits single-port (8 bits data / 1 bit parity)
- 256 x 18 bits single-port (16 bits data / 2 bits parity)
- 512 x 9 bits dual-port (8 bits data / 1 bit parity)
- 256 x18 bits dual-port (16 bits data / 2 bits parity)

The data widths of “9” and “18” are ideal for applications where parity is necessary. This allows 9 data bits, 8 data bits plus a parity bit, 18 data bits, or 16 data bits plus two parity bits. The logic for generating and checking the parity must be customized separately.

Figure 12. sysMEM Block Diagram

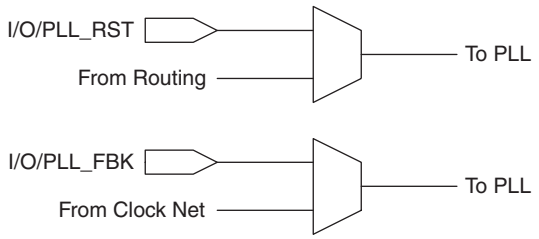


Read and Write Operations

The ispXPGA EBR has fully synchronous read and write operations as well as an asynchronous read operation. These operations allow several different types of memory to be implemented in the device.

Synchronous Read: The Clock Enable ($\overline{CE}$) and Write Enable (WE) signals control the synchronous read operation. When the $\overline{CE}$ signal is low, the clock is enabled. When the WE signal is low the read operation begins. Once the address (ADDR) is present, a rising clock edge (or falling edge depending on polarity) causes the stored data to be available on the DATA port. Figure 13 illustrates the synchronous read timing.

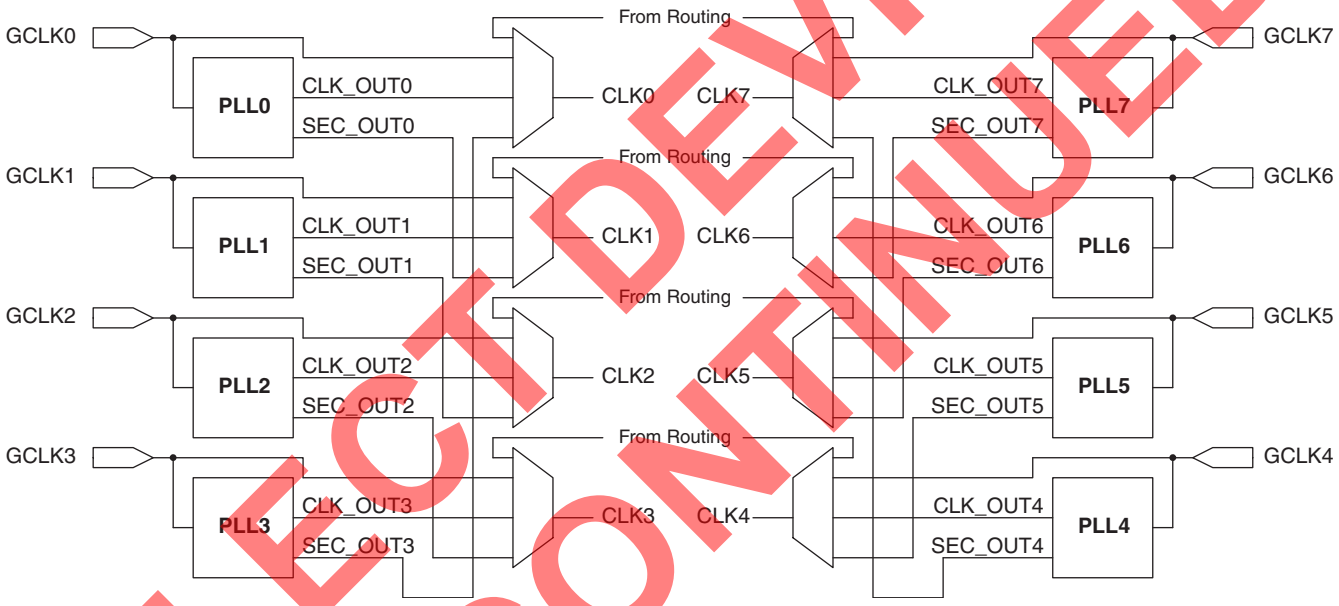
Figure 17. ispXPGA PLL_RST and PLL_FBK Generation



Clock Routing

The Global Clock Lines (GCLK) have two sources, their dedicated pins and the sysCLOCK circuit. Figure 18 illustrates the generation of the Global Clock Lines.

Figure 18. Global Clock Line Generation



sysIO Capability

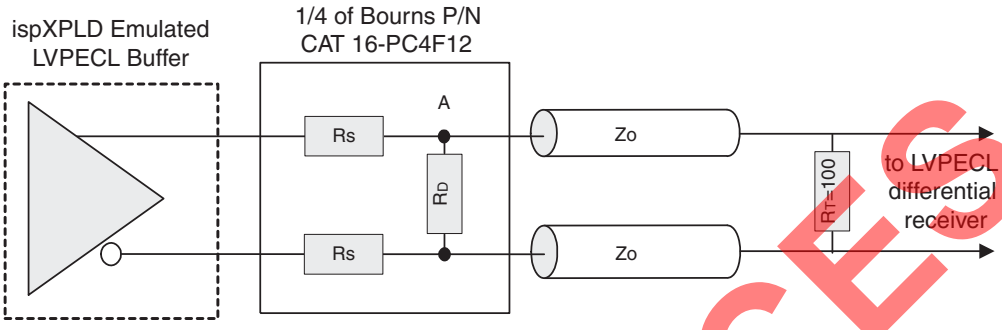
All the ispXPGA devices have eight sysIO banks, where each bank is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage (V_{CCO}) and reference voltage (V_{REF}) resources allowing each bank complete independence from the others. Each I/O is individually configurable based on the bank's V_{CCO} and V_{REF} settings. In addition, each I/O has configurable drive strength, weak pull-up, weak pull-down, or a bus-keeper latch. Table 4 lists the number of I/Os supported per bank in each of the ispXPGA devices. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to V_{CCO} of 3.0V to 3.6V for LVCMOS 3.3, LVTTL and PCI interfaces.

Table 5 lists the sysIO standards with the typical values for V_{CCO}, V_{REF} and V_{TT}.

The TOE, JTAG TAP pins, PROGRAM, CFG0 and DONE pins of the ispXPGA device are the only pins that do not have the sysIO capabilities. The TOE and CFG0 pins operate off the V_{CC} of the device, supporting only the LVCMOS standard corresponding to the device supply voltage. The TAP pins have a separate supply voltage (V_{CCJ}), which determines the LVCMOS standard corresponding to that supply voltage.

There are three classes of I/O interface standards that are implemented in the ispXPGA devices. The first is the unterminated, single-ended interface. It includes the 3.3V LVTTL standard along with the 1.8V, 2.5V, and 3.3V LVCMOS interface standards. Additionally, PCI and AGP-1X are subsets of this type of interface.

Figure 23. LVPECL Driver with Three Resistor Pack



ispXPGA 125B/C & ispXPGA 125EB/EC External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Conditions	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{CO}	Global Clock Input to Output	PIO Output Register	—	5.3	—	5.7	—	6.6	ns
t_{S}	Global Clock Input Setup	PIO Input Register without input delay	-1.9	—	-1.8	—	-1.5	—	ns
t_{H}	Global Clock Input Hold	PIO Input Register without input delay	2.7	—	2.9	—	3.3	—	ns
t_{SINDLY}	Global Clock Input Setup	PIO Input Register with input delay	3.1	—	3.3	—	3.8	—	ns
t_{HINDLY}	Global Clock Input Hold	PIO Input Register with input delay	0.0	—	0.0	—	0.0	—	
t_{COPLL}	Global Clock Input to Output	PIO Output Register using PLL without delay	—	3.6	—	3.9	—	4.5	ns
t_{SPLL}	Global Clock Input Setup	PIO Input Register without input delay using PLL without delay	0	—	0.1	—	0.3	—	ns
t_{HPLL}	Global Clock Input Hold	PIO Input Register without input delay using PLL without delay	0.9	—	1.0	—	1.2	—	ns
$t_{SINDLYPLL}$	Global Clock Input Setup	PIO Input Register with input delay using PLL without delay	5.1	—	5.5	—	6.3	—	ns
$t_{HINDLYPLL}$	Global Clock Input Hold	PIO Input Register with input delay using PLL without delay	-3.0	—	-2.8	—	-2.4	—	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 125B/C & ispXPGA 125EB/EC PFU Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Set								
t_{LASSRO}	Asynchronous Set/Reset to Output	—	1.09	—	1.17	—	1.35	ns
$t_{LASSRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{LASSRR}	Asynchronous Set/Reset Recovery	—	0.51	—	0.55	—	0.63	ns
t_{LSSR_S}	Synchronous Set/Reset Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{LSSR_H}	Synchronous Set/Reset Hold Time	0.03	—	0.03	—	0.03	—	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.
2. $t_{LCTHRUL}$ quoted bit by bit.

Timing v.0.3

ispXPGA 125B/C & ispXPGA 125EB/EC PIC Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Register/Latch Delays								
t_{IO_CO}	Register Clock to Output Delay	—	0.89	—	0.96	—	1.10	ns
t_{IO_S}	Register Setup Time (Data before Clock)	0.05	—	0.05	—	0.06	—	ns
t_{IO_H}	Register Hold Time (Data after Clock)	0.06	—	0.06	—	0.07	—	ns
t_{IOCE_S}	Register Clock Enable Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{IOCE_H}	Register Clock Enable Hold Time	0.13	—	0.13	—	0.15	—	ns
t_{IO_GO}	Latch Gate to Output Delay	—	0.68	—	0.73	—	0.84	ns
t_{IOL_S}	Latch Setup Time	0.05	—	0.05	—	0.06	—	ns
t_{IOL_H}	Latch Hold Time	0.06	—	0.06	—	0.07	—	ns
t_{IOLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns
t_{IOASRO}	Asynchronous Set/Reset to Output	—	1.00	—	1.08	—	1.24	ns
$t_{IOASRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{IOASRR}	Asynchronous Set/Reset Recovery Time	—	0.23	—	0.25	—	0.29	ns
Input/Output Delays								
t_{IOBUF}	Output Buffer Delay	—	0.97	—	1.04	—	1.20	ns
t_{IOIN}	Input Buffer Delay	—	0.57	—	0.61	—	0.70	ns
t_{IOEN}	Output Enable Delay	—	0.53	—	0.57	—	0.66	ns
t_{IODIS}	Output Disable Delay	—	-0.14	—	-0.13	—	-0.11	ns
t_{IOFT}	Feed-thru Delay	—	0.19	—	0.20	—	0.23	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 125B/C & ispXPGA 125EB/EC Timing Adders

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	4.28	—	4.6	—	5.29	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

ispXPGA 200B/C & ispXPGA 200EB/EC PFU Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Set								
t_{LASSRO}	Asynchronous Set/Reset to Output	—	1.09	—	1.17	—	1.35	ns
$t_{LASSRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{LASSRR}	Asynchronous Set/Reset Recovery	—	0.51	—	0.55	—	0.63	ns
t_{LSSR_S}	Synchronous Set/Reset Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{LSSR_H}	Synchronous Set/Reset Hold Time	0.03	—	0.03	—	0.03	—	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.
2. $t_{LCTHRUL}$ quoted bit by bit.

Timing v.0.3

ispXPGA 200B/C & ispXPGA 200EB/EC PIC Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Register/Latch Delays								
t_{IO_CO}	Register Clock to Output Delay	—	0.93	—	1.00	—	1.15	ns
t_{IO_S}	Register Setup Time (Data before Clock)	0.05	—	0.05	—	0.06	—	ns
t_{IO_H}	Register Hold Time (Data after Clock)	0.06	—	0.06	—	0.07	—	ns
t_{IOCE_S}	Register Clock Enable Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{IOCE_H}	Register Clock Enable Hold Time	0.13	—	0.13	—	0.15	—	ns
t_{IO_GO}	Latch Gate to Output Delay	—	0.72	—	0.77	—	0.89	ns
t_{IOL_S}	Latch Setup Time	0.05	—	0.05	—	0.06	—	ns
t_{IOL_H}	Latch Hold Time	0.06	—	0.06	—	0.07	—	ns
t_{IOLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns
t_{IOASRO}	Asynchronous Set/Reset to Output	—	1.04	—	1.12	—	1.29	ns
$t_{IOASRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{IOASRR}	Asynchronous Set/Reset Recovery Time	—	0.23	—	0.25	—	0.29	ns
Input/Output Delays								
t_{IOBUF}	Output Buffer Delay	—	0.97	—	1.04	—	1.20	ns
t_{IOIN}	Input Buffer Delay	—	0.60	—	0.64	—	0.74	ns
t_{IOEN}	Output Enable Delay	—	0.53	—	0.57	—	0.66	ns
t_{IODIS}	Output Disable Delay	—	-0.13	—	-0.12	—	-0.10	ns
t_{IOFT}	Feed-thru Delay	—	0.19	—	0.20	—	0.23	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 1200B/C & ispXPGA 1200EB/EC PFU Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Functional Delays								
LUTs								
t_{LUT4}	4-Input LUT Delay	—	0.41	—	0.44	—	0.51	ns
t_{LUT5}	5-Input LUT Delay	—	0.73	—	0.79	—	0.91	ns
t_{LUT6}	6-Input LUT Delay	—	0.86	—	0.93	—	1.07	ns
Shift Register (LUT)								
t_{LSR_S}	Shift Register Setup Time	-0.64	—	-0.62	—	-0.53	—	ns
t_{LSR_H}	Shift Register Hold Time	0.61	—	0.63	—	0.72	—	ns
t_{LSR_CO}	Shift Register Clock to Output Delay	—	0.70	—	0.75	—	0.86	ns
Arithmetic Functions								
$t_{LCTHRUR}$	MC (Macro Cell) Carry In to MC Carry Out Delay (Ripple)	—	0.08	—	0.09	—	0.10	ns
$t_{LCTHRUL}$[2]	MC Carry In to MC Carry Out Delay (Look Ahead)	—	0.05	—	0.05	—	0.06	ns
t_{LSTHRU}	MC Sum In to MC Sum Out Delay	—	0.42	—	0.45	—	0.52	ns
$t_{LSINCOUT}$	MC Sum In to MC Carry Out Delay	—	0.29	—	0.31	—	0.36	ns
$t_{LCINSOUTR}$	MC Carry In to MC Sum Out Delay (Ripple)	—	0.36	—	0.39	—	0.45	ns
$t_{LCINSOUTL}$	MC Carry In to MC Sum Out Delay (Look Ahead)	—	0.26	—	0.28	—	0.32	ns
Feed-thru								
t_{LFT}	PFU Feed-Thru Delay	—	0.15	—	0.16	—	0.18	ns
Distributed RAM								
t_{LRAM_CO}	Clock to RAM Output	—	1.24	—	1.33	—	1.53	ns
t_{LRAMAD_S}	Address Setup Time	-0.41	—	-0.40	—	-0.34	—	ns
t_{LRAMD_S}	Data Setup Time	0.21	—	0.22	—	0.25	—	ns
t_{LRAMWE_S}	Write Enable Setup Time	0.45	—	0.46	—	0.53	—	ns
t_{LRAMAD_H}	Address Hold Time	0.58	—	0.60	—	0.69	—	ns
t_{LRAMD_H}	Data Hold Time	0.11	—	0.11	—	0.13	—	ns
t_{LRAMWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{LRAMCPW}$	Clock Pulse Width (High or Low)	2.91	—	3.00	—	3.45	—	ns
$t_{LRAMADO}$	Address to Output Delay	—	0.86	—	0.93	—	1.07	ns
Register/Latch Delays								
Registers								
t_{L_CO}	Register Clock to Output Delay	—	0.58	—	0.62	—	0.71	ns
t_{L_S}	Register Setup Time (Data before Clock)	0.14	—	0.14	—	0.16	—	ns
t_{L_H}	Register Hold Time (Data after Clock)	-0.12	—	-0.12	—	-0.10	—	ns
t_{LCE_S}	Register Clock Enable Setup Time	-0.11	—	-0.11	—	-0.09	—	ns
t_{LCE_H}	Register Clock Enable Hold Time	0.11	—	0.11	—	0.13	—	ns
Latches								
t_{L_GO}	Latch Gate to Output Delay	—	0.09	—	0.10	—	0.12	ns
t_{LL_S}	Latch Setup Time	0.14	—	0.14	—	0.16	—	ns
t_{LL_H}	Latch Hold Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{LLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Units
t_{PWH}	Input clock, high time	80% to 80%	1.2	—	ns
t_{PWL}	Input clock, low time	20% to 20%	1.2	—	ns
t_R, t_F	Input Clock, rise and fall time	20% to 80%	—	3.0	ns
t_{INSTB}	Input clock stability, cycle to cycle (peak)		—	+/- 250	ps
f_{MDIVIN}	M Divider input, frequency range		10	320	MHz
$f_{MDIVOUT}$	M Divider output, frequency range		10	320	MHz
f_{NDIVIN}	N Divider input, frequency range		10	320	MHz
$f_{NDIVOUT}$	N Divider output, frequency range		10	320	MHz
f_{VDIVIN}	V Divider input, frequency range		100	400	MHz
$f_{VDIVOUT}$	V Divider output, frequency range		10	320	MHz
$t_{OUTDUTY}$	output clock, duty cycle		40	60	%
$t_{JIT(CC)}$	Output clock, cycle to cycle jitter (peak)	Clean reference[1] 10MHz ð $f_{MDIVOUT}$ ð 40MHz or 100MHz ð f_{VDIVIN} ð 160MHz	—	+/- 600	ps
		Clean reference[1] 40MHz ð $f_{MDIVOUT}$ ð 320MHz and 160MHz ð f_{VDIVIN} ð 400MHz	—	+/- 150	ps
$t_{JIT(PER)}$[2]	Output clock, period jitter (peak)	Clean reference[1] 10MHz ð $f_{MDIVOUT}$ ð 40MHz or 100MHz ð f_{VDIVIN} ð 160MHz	—	+/- 600	ps
		Clean reference[1] 40MHz ð $f_{MDIVOUT}$ ð 320MHz and 160MHz ð f_{VDIVIN} ð 400MHz	—	+/- 150	ps
$t_{CLK\_OUT\_DELAY}$	Input clock to CLK_OUT delay	Internal feedback	—	3.0	ns
t_{PHASE}	Input clock to external feedback delta	External feedback	—	1.5	ns
t_{LOCK}	Time to acquire phase lock after input stable		—	25	us
t_{PLL_DELAY}	Delay increment (Lead/Lag)	Typical = +/- 250ps	+/- 120	+/- 550	ps
t_{RANGE}	Total output delay range (lead/lag)		+/- 0.84	+/- 3.85	ns
t_{PLL_RSTW}	Minimum reset pulse width		1.8	—	ns
t_{CLK_IN}[3]	Global clock input delay		—	1.0	ns
$t_{PLL\_SEC\_DELAY}$	Secondary PLL output delay		—	1.5	ns

1. This condition assures that the output phase jitter will remain within specifications. Jitter spec is based on optimized M, N and V settings determined by the ispLEVER software.
2. Accumulated jitter measured over 10,000 waveform samples
3. Internal timing for reference only.

ispXPGA Power Supply and NC Connections[1]

Signal	256-Ball fpBGA[3]	516-Ball fpBGA[3]
V_{CC}	C3, C14, D4, D13, E5, E12, F6, F11, L6, L11, M5, M12, N4, N13, P3, P14	A9, A22, D4, D27, J1, J30, L11, L12, L15, L16, L19, L20, M11, M20, R11, R20, T11, T20, W11, W20, Y11, Y12, Y15, Y16, Y19, Y20, AB1, AB30, AG4, AG27, AK9, AK22
V_{CCO0}	F5, G5	F4, J4, M4, N11, P4, P11
V_{CCO1}	K5, L5	U4, U11, V11, W4, AB4, AE4
V_{CCO2}	M6, M7	Y13, Y14, AG6, AG9, AG12, AG14
V_{CCO3}	M10, M11	Y17, Y18, AG17, AG19, AG22, AG25
V_{CCO4}	K12, L12	U20, U27, V20, W27, AB27, AE27
V_{CCO5}	G12, F12	F27, J27, M27, N20, P20, P27
V_{CCO6}	E10, E11	D17, D19, D22, D25, L17, L18
V_{CCO7}	E6, E7	D6, D9, D12, D14, L13, L14
V_{CCP}	H3, J15	R4, T30
V_{CCJ}	A2	C4
GND	A1, A16, B2, B15, F7, F8, F9, F10, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L7, L8, L9, L10, R2, R15, T1, T16	A1, A30, B2, B29, C3, C28, M12, M13, M14, M15, M16, M17, M18, M19, N12, N13, N14, N15, N16, N17, N18, N19, P12, P13, P14, P15, P16, P17, P18, P19, R12, R13, R14, R15, R16, R17, R18, R19, T12, T13, T14, T15, T16, T17, T18, T19, U12, U13, U14, U15, U16, U17, U18, U19, V12, V13, V14, V15, V16, V17, V18, V19, W12, W13, W14, W15, W16, W17, W18, W19, AH3, AH28, AJ2, AJ29, AK1, AK30
GND_P	H15, J4	R29, T4
NC[2]	—	**LFX125:** A10, A13, A16, A17, A24, A25, A26, A4, A5, A6, A7, AA1, AA2, AA28, AA29, AA3, AB28, AC1, AC28, AD1, AD27, AD4, AE28, AE29, AE3, AE30, AF27, AF28, AF29, AF3, AF4, AG1, AG10, AG11, AG15, AG2, AG20, AG23, AG24, AG29, AG3, AG8, AH1, AH15, AH19, AH2, AH20, AH23, AH24, AH30, AH7, AH8, AH9, AJ1, AJ12, AJ14, AJ15, AJ19, AJ20, AJ21, AJ23, AJ24, AJ25, AJ27, AJ30, AJ6, AJ7, AJ8, AK11, AK14, AK15, AK20, AK21, AK23, AK24, AK25, AK27, AK5, AK6, AK7, B10, B13, B16, B17, B18, B23, B24, B25, B5, B6, B7, C11, C13, C14, C16, C17, C22, C23, C24, C25, C6, C7, C8, D11, D16, D23, D24, D28, D29, D3, D7, D8, E30, E4, F1, F29, F30, G1, G2, G27, G28, G29, G30, H1, H2, H27, H28, H29, H30, J2, J28, J29, J3, K1, K2, K27, K28, K3, K4, L1, L2, L27, L3, L4, M1, M2, M29, M3, M30, V27, V28, V3, V4, W1, W30, Y1, Y27, Y28, Y3, Y30 **LFX200:** A26, A25, A24, A17, A10, A7, A6, A5, A4, B25, B24, B23, B17, B10, B7, B6, B5, C25, C24, C23, C22, C16, C11, C8, C7, C6, D24, D23, D16, D11, D8, D7, E30, F30, F29, F1, G30, G29, G28, G27, G2, G1, H30, H29, H28, H27, H2, H1, J29, J28, J3, J2, K28, K27, K4, K3, K2, K1, L27, L4, L3, L2, L1, M3, V28, V27, V4, V3, W30, W1, Y30, Y28, Y27, Y3, Y1, AA29, AA28, AA3, AA2, AA1, AD27, AD4, AE28, AE3, AF29, AF28, AF27, AF3, AG29, AG24, AG23, AG20, AG11, AG10, AG8, AG2, AG1, AH30, AH24, AH23, AH20, AH9, AH8, AH7, AH2, AH1, AJ30, AJ27, AJ25, AJ24, AJ23, AJ21, AJ15, AJ12, AJ8, AJ7, AJ6, AJ1, AK27, AK25, AK24, AK23, AK21, AK15, AK11, AK7, AK6, AK5

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, V_{CC} or GND.
3. Balls for GND, V_{CC} and V_{CCOx} are connected within the substrate to their respective common signals. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
M15	BK4_IO5	-	54N/HSI2	BK4_IO5	-	46N
M14	BK4_IO8	-	56P/HSI2	BK4_IO6	-	47P
M13	BK4_IO9	VREF4	56N/HSI2	BK4_IO7	VREF4	47N
-	GND (Bank 4)	-	-	-	-	-
L13	BK4_IO12	PLL_RST4	58P/HSI2	BK4_IO8	PLL_RST4	48P
L14	BK4_IO13	PLL_RST5	58N/HSI2	BK4_IO9	PLL_RST5	48N
N16	BK4_IO14	HSI2B_SOUTP	59P/HSI2	BK4_IO10	-	49P
M16	BK4_IO15	HSI2B_SOUTN	59N/HSI2	BK4_IO11	-	49N
-	-	-	-	GND (Bank 4)	-	-
L15	BK4_IO18	SS_CLKIN1P	61P	BK4_IO14	SS_CLKIN1P	51P
-	GND (Bank 4)	-	-	-	-	-
K15	BK4_IO19	SS_CLKIN1N	61N	BK4_IO15	SS_CLKIN1N	51N
K14	BK4_IO20	PLL_FBK4	62P	BK4_IO16	PLL_FBK4	52P
K13	BK4_IO21	PLL_FBK5	62N	BK4_IO17	PLL_FBK5	52N
L16	BK4_IO22	SS_CLKOUT1P	63P	BK4_IO18	SS_CLKOUT1P	53P
-	-	-	-	GND (Bank 4)	-	-
K16	BK4_IO23	SS_CLKOUT1N	63N	BK4_IO19	SS_CLKOUT1N	53N
J13	BK4_IO24	CLK_OUT4	64P	BK4_IO20	CLK_OUT4	54P
J12	BK4_IO25	CLK_OUT5	64N	BK4_IO21	CLK_OUT5	54N
-	GND (Bank 4)	-	-	-	-	-
J14	GCLK4	-	LVDS Pair2P	GCLK4	-	LVDS Pair2P
H14	GCLK5	-	LVDS Pair2N	GCLK5	-	LVDS Pair2N
J15	VCCP1	-	-	VCCP1	-	-
H15	GNDP1	-	-	GNDP1	-	-
J16	GCLK6	-	LVDS Pair3P	GCLK6	-	LVDS Pair3P
H16	GCLK7	-	LVDS Pair3N	GCLK7	-	LVDS Pair3N
-	GND (Bank 5)	-	-	-	-	-
H12	BK5_IO0	CLK_OUT6	65P	BK5_IO0	CLK_OUT6	55P
H13	BK5_IO1	CLK_OUT7	65N	BK5_IO1	CLK_OUT7	55N
G14	BK5_IO2	-	66P	BK5_IO2	-	56P
-	-	-	-	GND (Bank 5)	-	-
G15	BK5_IO3	PLL_RST7	66N	BK5_IO3	PLL_RST7	56N
G13	BK5_IO6	PLL_RST6	68P	BK5_IO6	PLL_RST6	58P/HSI1
-	GND (Bank 5)	-	-	-	-	-
F13	BK5_IO7	PLL_FBK7	68N	BK5_IO7	PLL_FBK7	58N/HSI1
G16	BK5_IO10	HSI3A_SINP	70P	BK5_IO8	HSI1A_SINP	59P/HSI1
-	-	-	-	GND (Bank 5)	-	-
F16	BK5_IO11	HSI3A_SINN	70N/HSI3	BK5_IO9	HSI1A-SINN	59N/HSI1
F14	BK5_IO12	-	71P/HSI3	BK5_IO10	-	60P/HSI1
F15	BK5_IO13	-	71N/HSI3	BK5_IO11	-	60N/HSI1
E16	BK5_IO14	HSI3A_SOUTP	72P/HSI3	BK5_IO12	HSI1A_SOUTP	61P/HSI1
-	GND (Bank 5)	-	-	-	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
J29	BK5_IO22	HSI4B_SOUTP	116P/HSI4	NC	-	-	NC	-	-
-	GND (Bank 5)	-	-	-	-	-	-	-	-
H29	BK5_IO23	HSI4B_SOUTN	116N/HSI4	NC	-	-	NC	-	-
F30	BK5_IO24	-	117P/HSI5	NC	-	-	NC	-	-
G29	BK5_IO25	-	117N/HSI5	NC	-	-	NC	-	-
H28	BK5_IO26	HSI5A_SINP	118P/HSI5	NC	-	-	NC	-	-
H27	BK5_IO27	HSI5A_SINN	118N/HSI5	NC	-	-	NC	-	-
E30	BK5_IO28	-	119P/HSI5	NC	-	-	NC	-	-
F29	BK5_IO29	-	119N/HSI5	NC	-	-	NC	-	-
G28	BK5_IO30	HSI5A_SOUTP	120P/HSI5	NC	-	-	NC	-	-
-	GND (Bank 5)	-	-	-	-	-	-	-	-
G27	BK5_IO31	HSI5A_SOUTN	120N/HSI5	NC	-	-	NC	-	-
E29	BK5_IO32	VREF5	121P/HSI5	BK5_IO16	VREF5	73P/HSI3	BK5_IO14	VREF5	62P/HSI1
F28	BK5_IO33	-	121N/HSI5	BK5_IO17	-	73N/HSI3	BK5_IO15	-	62N/HSI1
D30	BK5_IO34	HSI5B_SINP	122P/HSI5	BK5_IO18	HSI3B_SINP	74P/HSI3	BK5_IO16	HSI1B_SINP	63P/HSI1
-	-	-	-	-	-	-	GND (Bank 5)	-	-
C30	BK5_IO35	HSI5B_SINN	122N/HSI5	BK5_IO19	HSI3B_SINN	74N/HSI3	BK5_IO17	HSI1B_SINN	63N/HSI1
D29	BK5_IO36	-	123P/HSI5	BK5_IO20		75P/HSI3	NC	-	-
D28	BK5_IO37	-	123N/HSI5	BK5_IO21		75N/HSI3	NC	-	-
E28	BK5_IO38	HSI5B_SOUTP	124P/HSI5	BK5_IO22	HSI3B_SOUTP	76P/HSI3	BK5_IO20	HSI1B_SOUTP	65P/HSI1
-	GND (Bank 5)	-	-	GND (Bank 5)	-	-	-	-	-
E27	BK5_IO39	HSI5B_SOUTN	124N/HSI5	BK5_IO23	HSI3B_SOUTN	76N/HSI3	BK5_IO21	HSI1B_SOUTN	65N/HSI1
C29	BK5_IO40	-	125P	BK5_IO24	-	77P/HSI3	BK5_IO18	-	64P/HSI1
B30	BK5_IO41	-	125N	BK5_IO25	-	77N/HSI3	BK5_IO19	-	64N/HSI1
A29	CFG0	-	-	CFG0	-	-	CFG0	-	-
B28	DONE	-	-	DONE	-	-	DONE	-	-
A28	PROGRAMb	-	-	PROGRAMb	-	-	PROGRAMb	-	-
D26	BK6_IO0	INITb	126P	BK6_IO0	INITb	78P	BK6_IO0	INITb	66P
C27	BK6_IO1	CCLK	126N	BK6_IO1	CCLK	78N	BK6_IO1	CCLK	66N
B27	BK6_IO2	-	127P	BK6_IO2	-	79P	BK6_IO2	-	67P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-	-	-	-
A27	BK6_IO3	-	127N	BK6_IO3	-	79N	BK6_IO3	-	67N
C26	BK6_IO4	CSb	128P	BK6_IO4	CSb	80P	BK6_IO4	CSb	68P
-	-	-	-	-	-	-	GND (Bank 6)	-	-
B26	BK6_IO5	Read	128N	BK6_IO5	Read	80N	BK6_IO5	Read	68N
A26	BK6_IO6	-	129P	NC	-	-	NC	-	-
C25	BK6_IO7	-	129N	NC	-	-	NC	-	-
D24	BK6_IO8	-	130P	NC	-	-	NC	-	-
B25	BK6_IO9	-	130N	NC	-	-	NC	-	-
A25	BK6_IO10	-	131P	NC	-	-	NC	-	-
-	GND (Bank 6)	-	-	-	-	-	-	-	-
C24	BK6_IO11	-	131N	NC	-	-	NC	-	-
D23	BK6_IO12	-	132P	NC	-	-	NC	-	-
B24	BK6_IO13	-	132N	NC	-	-	NC	-	-
C23	BK6_IO14	-	133P	NC	-	-	NC	-	-
A24	BK6_IO15	-	133N	NC	-	-	NC	-	-
C22	BK6_IO16	-	134P	NC	-	-	NC	-	-
B23	BK6_IO17	-	134N	NC	-	-	NC	-	-
B22	BK6_IO18	DATA7	135P	BK6_IO6	DATA7	81P	BK6_IO6	DATA7	69P
-	GND (Bank 6)	-	-	-	-	-	-	-	-
A23	BK6_IO19	DATA6	135N	BK6_IO7	DATA6	81N	BK6_IO7	DATA6	69N

ispXPGA Logic Signal Connections: 680-Ball fpBGA

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
C4	BK0_IO0	-	0P
B4	BK0_IO1	-	0N
E6	BK0_IO2	-	1P
-	GND (Bank 0)	-	-
D6	BK0_IO3	-	1N
A4	BK0_IO4	-	2P
E8	BK0_IO5	-	2N
C5	BK0_IO6	HSI0A_SOUTP	3P
C6	BK0_IO7	HSI0A_SOUTN	3N
A6	BK0_IO8	-	4P
A5	BK0_IO9	-	4N
B6	BK0_IO10	HSI0A_SINP	5P/HSI0
-	GND (Bank 0)	-	-
B5	BK0_IO11	HSI0A_SINN	5N/HSI0
B7	BK0_IO12	VREF0	6P/HSI0
A7	BK0_IO13	-	6N/HSI0
D8	BK0_IO14	HSI0B_SOUTP	7P/HSI0
D7	BK0_IO15	HSI0B_SOUTN	7N/HSI0
D9	BK0_IO16	-	8P/HSI0
E10	BK0_IO17	-	8N/HSI0
C8	BK0_IO18	HSI0B_SINP	9P/HSI0
-	GND (Bank 0)	-	-
C7	BK0_IO19	HSI0B_SINN	9N/HSI0
A8	BK0_IO20	-	10P/HSI0
A9	BK0_IO21	-	10N/HSI0
C9	BK0_IO22	HSI1A_SOUTP	11P/HSI0
B8	BK0_IO23	HSI1A_SOUTN	11N/HSI0
B9	BK0_IO24	-	12P/HSI0
B10	BK0_IO25	-	12N/HSI0
D11	BK0_IO26	HSI1A_SINP	13P/HSI1
-	GND (Bank 0)	-	-
D10	BK0_IO27	HSI1A_SINN	13N/HSI1
A10	BK0_IO28	-	14P/HSI1
C12	BK0_IO29	-	14N/HSI1
D12	BK0_IO30	HSI1B_SOUTP	15P/HSI1
C11	BK0_IO31	HSI1B_SOUTN	15N/HSI1
A12	BK0_IO32	-	16P/HSI1
A13	BK0_IO33	-	16N/HSI1
B13	BK0_IO34	HSI1B_SINP	17P/HSI1
-	GND (Bank 0)	-	-
B12	BK0_IO35	HSI1B_SINN	17N/HSI1
E14	BK0_IO36	-	18P/HSI1

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
C24	BK1_IO7	SS_CLKIN0N	34N
A22	BK1_IO8	-	35P
D22	BK1_IO9	-	35N
A23	BK1_IO10	-	36P
-	GND (Bank 1)	-	-
B25	BK1_IO11	-	36N
D23	BK1_IO12	PLL_RST2	37P
A24	BK1_IO13	PLL_RST3	37N
A25	BK1_IO14	-	38P
E24	BK1_IO15	-	38N
D24	BK1_IO16	-	39P
A26	BK1_IO17	-	39N
D25	BK1_IO18	-	40P
-	GND (Bank 1)	-	-
C25	BK1_IO19	-	40N
B26	BK1_IO20	-	41P/HSI3
B27	BK1_IO21	-	41N/HSI3
D26	BK1_IO22	-	42P/HSI3
A27	BK1_IO23	-	42N/HSI3
A28	BK1_IO24	-	43P/HSI3
E26	BK1_IO25	-	43N/HSI3
C27	BK1_IO26	HSI3A_SOUTP	44P/HSI3
-	GND (Bank 1)	-	-
D27	BK1_IO27	HSI3A_SOUTN	44N/HSI3
B28	BK1_IO28	-	45P/HSI3
A30	BK1_IO29	-	45N/HSI3
C28	BK1_IO30	HSI3A_SINP	46P/HSI3
D28	BK1_IO31	HSI3A_SINN	46N/HSI3
A31	BK1_IO32	-	47P/HSI3
B30	BK1_IO33	-	47N/HSI3
E28	BK1_IO34	HSI3B_SOUTP	48P/HSI3
-	GND (Bank 1)	-	-
D29	BK1_IO35	HSI3B_SOUTN	48N/HSI3
C29	BK1_IO36	-	49P/HSI4
B31	BK1_IO37	-	49N/HSI4
D30	BK1_IO38	HSI3B_SINP	50P/HSI4
E30	BK1_IO39	HSI3B_SINN	50N/HSI4
A32	BK1_IO40	-	51P/HSI4
C31	BK1_IO41	-	51N/HSI4
D31	BK1_IO42	HSI4A_SOUTP	52P/HSI4
-	GND (Bank 1)	-	-
C32	BK1_IO43	HSI4A_SOUTN	52N/HSI4
B32	BK1_IO44	-	53P/HSI4

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
A33	BK1_IO45	-	53N/HSI4
C33	BK1_IO46	HSI4A_SINP	54P/HSI4
B33	BK1_IO47	HSI4A_SINN	54N/HSI4
A34	BK1_IO48	-	55P/HSI4
A35	BK1_IO49	VREF1	55N/HSI4
D32	BK1_IO50	HSI4B_SOUTP	56P/HSI4
-	GND (Bank 1)	-	-
D33	BK1_IO51	HSI4B_SOUTN	56N/HSI4
E32	BK1_IO52	-	57P
C34	BK1_IO53	-	57N
B34	BK1_IO54	HSI4B_SINP	58P
B35	BK1_IO55	HSI4B_SINN	58N
A36	BK1_IO56	-	59P
D34	BK1_IO57	-	59N
C35	BK1_IO58	-	60P
-	GND (Bank 1)	-	-
E34	BK1_IO59	-	60N
B36	BK1_IO60	-	61P
C36	BK1_IO61	-	61N
D39	TCK	-	-
D37	TMS	-	-
D38	TOE	-	-
E37	BK2_IO0	-	62P
F35	BK2_IO1	-	62N
E39	BK2_IO2	-	63P
-	GND (Bank 2)	-	-
F39	BK2_IO3	-	63N
F36	BK2_IO4	-	64P
E38	BK2_IO5	-	64N
G38	BK2_IO6	-	65P
F37	BK2_IO7	-	65N
G36	BK2_IO8	-	66P
G39	BK2_IO9	-	66N
H35	BK2_IO10	-	67P
-	GND (Bank 2)	-	-
F38	BK2_IO11	-	67N
J37	BK2_IO12	VREF2	68P
H36	BK2_IO13	-	68N
G37	BK2_IO14	-	69P
H37	BK2_IO15	-	69N
H39	BK2_IO16	-	70P
K35	BK2_IO17	-	70N
J36	BK2_IO18	-	71P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
AU6	BK5_IO50	HSI9B_SINP	180P/HSI9
-	GND (Bank 5)	-	-
AV6	BK5_IO51	HSI9B_SINN	180N/HSI9
AR8	BK5_IO52	-	181P
AT7	BK5_IO53	-	181N
AU5	BK5_IO54	HSI9B_SOUTP	182P
AV5	BK5_IO55	HSI9B_SOUTN	182N
AW5	BK5_IO56	-	183P
AW4	BK5_IO57	-	183N
AT6	BK5_IO58	-	184P
-	GND (Bank 5)	-	-
AV4	BK5_IO59	-	184N
AR6	BK5_IO60	-	185P
AU4	BK5_IO61	-	185N
AT1	CFG0	-	-
AT3	DONE	-	-
AT2	PROGRAMb	-	-
AP4	BK6_IO0	INITb	186P
AP5	BK6_IO1	CCLK	186N
AR3	BK6_IO2	-	187P
-	GND (Bank 6)	-	-
AR2	BK6_IO3	-	187N
AP3	BK6_IO4	CSb	188P
AR1	BK6_IO5	Read	188N
AP2	BK6_IO6	-	189P
AP1	BK6_IO7	-	189N
AN4	BK6_IO8	-	190P
AM5	BK6_IO9	-	190N
AN3	BK6_IO10	-	191P
-	GND (Bank 6)	-	-
AN2	BK6_IO11	-	191N
AM4	BK6_IO12	VREF6	192P
AM3	BK6_IO13	-	192N
AN1	BK6_IO14	-	193P
AM2	BK6_IO15	-	193N
AL4	BK6_IO16	-	194P
AK5	BK6_IO17	-	194N
AM1	BK6_IO18	-	195P
-	GND (Bank 6)	-	-
AK4	BK6_IO19	-	195N
AL3	BK6_IO20	-	196P
AL2	BK6_IO21	-	196N
AL1	BK6_IO22	-	197P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
AK2	BK6_IO23	-	197N
AK1	BK6_IO24	-	198P
AJ4	BK6_IO25	-	198N
AJ3	BK6_IO26	-	199P
-	GND (Bank 6)	-	-
AH4	BK6_IO27	-	199N
AH3	BK6_IO28	-	200P
AH2	BK6_IO29	-	200N
AH1	BK6_IO30	-	201P
AG4	BK6_IO31	-	201N
AF5	BK6_IO32	DATA7	202P
AG3	BK6_IO33	DATA6	202N
AG2	BK6_IO34	-	203P
-	GND (Bank 6)	-	-
AF4	BK6_IO35	-	203N
AF3	BK6_IO36	DATA5	204P
AG1	BK6_IO37	DATA4	204N
AE2	BK6_IO38	-	205P
AF1	BK6_IO39	-	205N
AF2	BK6_IO40	-	206P
AE1	BK6_IO41	-	206N
AE4	BK6_IO42	-	207P
-	GND (Bank 6)	-	-
AD4	BK6_IO43	-	207N
AD5	BK6_IO44	-	208P
AD3	BK6_IO45	-	208N
AD2	BK6_IO46	-	209P
AD1	BK6_IO47	-	209N
AC4	BK6_IO48	-	210P
AC3	BK6_IO49	-	210N
AC2	BK6_IO50	DATA3	211P
-	GND (Bank 6)	-	-
AC1	BK6_IO51	DATA2	211N
AB3	BK6_IO52	-	212P
AB4	BK6_IO53	-	212N
AB2	BK6_IO54	DATA1	213P
AB1	BK6_IO55	DATA0	213N
AA3	BK6_IO56	-	214P
AA4	BK6_IO57	-	214N
AA5	BK6_IO58	-	215P
-	GND (Bank 6)	-	-
AA2	BK6_IO59	-	215N
AA1	BK6_IO60	-	216P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AB1	BK1_IO35	HSI3B_SOUTN	48N/HSI3	NC	-	-
AC6	BK1_IO36	-	49P/HSI4	NC	-	-
AC5	BK1_IO37	-	49N/HSI4	NC	-	-
AC2	BK1_IO38	HSI3B_SINP	50P/HSI4	NC	-	-
AC1	BK1_IO39	HSI3B_SINN	50N/HSI4	NC	-	-
AC4	BK1_IO40	-	51P/HSI4	NC	-	-
AC3	BK1_IO41	-	51N/HSI4	NC	-	-
AD2	BK1_IO42	HSI4A_SOUTP	52P/HSI4	NC	-	-
-	GND (Bank 1)	-	-	-	-	-
AD1	BK1_IO43	HSI4A_SOUTN	52N/HSI4	NC	-	-
AD3	BK1_IO44	-	53P/HSI4	BK1_IO32	-	37P/HSI3
AD4	BK1_IO45	-	53N/HSI4	BK1_IO33	-	37N
AE2	BK1_IO46	HSI4A_SINP	54P/HSI4	BK1_IO34	-	38P
AE1	BK1_IO47	HSI4A_SINN	54N/HSI4	BK1_IO35	-	38N
AD5	BK1_IO48	-	55P/HSI4	BK1_IO25	-	33N
AD6	BK1_IO49	VREF1	55N/HSI4	BK1_IO24	VREF1	33P
AF2	BK1_IO50	HSI4B_SOUTP	56P/HSI4	BK1_IO26	HSI2B_SOUTP	34P
-	GND (Bank 1)	-	-	-	-	-
AF1	BK1_IO51	HSI4B_SOUTN	56N/HSI4	BK1_IO27	HSI2B_SOUTN	34N
AE3	BK1_IO52	-	57P	BK1_IO28	-	35P
AE4	BK1_IO53	-	57N	BK1_IO29	-	35N
AG1	BK1_IO54	HSI4B_SINP	58P	BK1_IO30	HSI2B_SINP	36P
-	-	-	-	GND (Bank 1)	-	-
AG2	BK1_IO55	HSI4B_SINN	58N	BK1_IO31	HSI2B_SINN	36N
AE5	BK1_IO56	-	59P	BK1_IO36	-	39P
AF4	BK1_IO57	-	59N	BK1_IO37	-	39N
AH1	BK1_IO58	-	60P	BK1_IO38	-	40P
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-
AH2	BK1_IO59	-	60N	BK1_IO39	-	40N
AF3	BK1_IO60	-	61P	BK1_IO40	-	41P
AG3	BK1_IO61	-	61N	BK1_IO41	-	41N
AH4	TCK	-	-	TCK	-	-
AJ3	TMS	-	-	TMS	-	-
AK3	TOE	-	-	TOE	-	-
AG5	BK2_IO0	-	62P	BK2_IO0	-	42P
AH5	BK2_IO1	-	62N	BK2_IO1	-	42N
AJ4	BK2_IO2	-	63P	BK2_IO2	-	43P
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
AK4	BK2_IO3	-	63N	BK2_IO3	-	43N
AG6	BK2_IO4	-	64P	BK2_IO4	-	44P
AH6	BK2_IO5	-	64N	BK2_IO5	-	44N
AJ5	BK2_IO6	-	65P	BK2_IO6	-	45P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
D21	BK6_IO29	-	200N	NC	-	-
A21	BK6_IO30	-	201P	NC	-	-
B21	BK6_IO31	-	201N	NC	-	-
F20	BK6_IO32	DATA7	202P	BK6_IO18	DATA7	135P
-	-	-	-	GND (Bank 6)	-	-
E20	BK6_IO33	DATA6	202N	BK6_IO19	DATA6	135N
D20	BK6_IO34	-	203P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-
C20	BK6_IO35		203N	NC	-	-
F19	BK6_IO36	DATA5	204P	BK6_IO22	DATA5	137P
E19	BK6_IO37	DATA4	204N	BK6_IO23	DATA4	137N
B20	BK6_IO38	-	205P	NC	-	-
A20	BK6_IO39	-	205N	NC	-	-
D19	BK6_IO40	-	206P	NC	-	-
C19	BK6_IO41	-	206N	NC	-	-
A19	BK6_IO42	-	207P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-
B19	BK6_IO43	-	207N	NC	-	-
G18	BK6_IO44	-	208P	BK6_IO24	-	138P
F18	BK6_IO45	-	208N	BK6_IO25	-	138N
A18	BK6_IO46	-	209P	BK6_IO32	-	142P
B18	BK6_IO47	-	209N	BK6_IO33	-	142N
D18	BK6_IO48	-	210P	BK6_IO34	-	143P
-	-	-	-	GND (Bank 6)	-	-
C18	BK6_IO49	-	210N	BK6_IO35	-	143N
F17	BK6_IO50	DATA3	211P	BK6_IO26	DATA3	139P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
E17	BK6_IO51	DATA2	211N	BK6_IO27	DATA2	139N
D17	BK6_IO52	-	212P	BK6_IO28	-	140P
C17	BK6_IO53	-	212N	BK6_IO29	-	140N
B17	BK6_IO54	DATA1	213P	BK6_IO30	DATA1	141P
A17	BK6_IO55	DATA0	213N	BK6_IO31	DATA0	141N
F16	BK6_IO56	-	214P	BK6_IO36	-	144P
E16	BK6_IO57	-	214N	BK6_IO37	-	144N
D16	BK6_IO58	-	215P	BK6_IO38	-	145P
-	GND (Bank 6)	-	-	-	-	-
C16	BK6_IO59	-	215N	BK6_IO39	-	145N
B16	BK6_IO60	-	216P	BK6_IO40	-	146P
A16	BK6_IO61	-	216N	BK6_IO41	-	146N
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-
A15	BK7_IO0	-	217P	BK7_IO0	-	147P