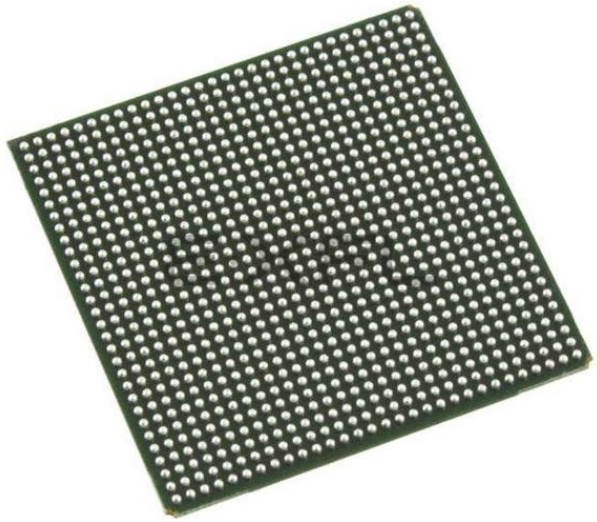
Lattice Semiconductor Corporation - LFX1200C-04F900C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	15376
Total RAM Bits	423936
Number of I/O	496
Number of Gates	1250000
Voltage - Supply	1.65V ~ 1.95V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx1200c-04f900c

Product Line	Ordering Part Number	Product Status	Reference PCN
LFX500EC (Cont'd)	LFX500EC-03F900C	**Discontinued**	PCN#09-10
	LFX500EC-03FN900C		
	LFX500EC-04F900C		
	LFX500EC-04FN900C		
	LFX500EC-03F900I		
	LFX500EC-03FN900I		
LFX1200EB	LFX1200EB-03FE680C	**Discontinued**	PCN#03A-10
	LFX1200EB-04FE680C		
	LFX1200EB-05FE680C		
	LFX1200EB-03FE680I		
	LFX1200EB-04FE680I		
	LFX1200EB-03F900C		
	LFX1200EB-04F900C		
	LFX1200EB-05F900C		
	LFX1200EB-03F900I		
	LFX1200EB-04F900I		
LFX1200EC	LFX1200EC-03FE680C	**Discontinued**	PCN#03A-10
	LFX1200EC-04FE680C		
	LFX1200EC-03FE680I		
	LFX1200EC-03F900C		
	LFX1200EC-04F900C		
	LFX1200EC-03F900I		

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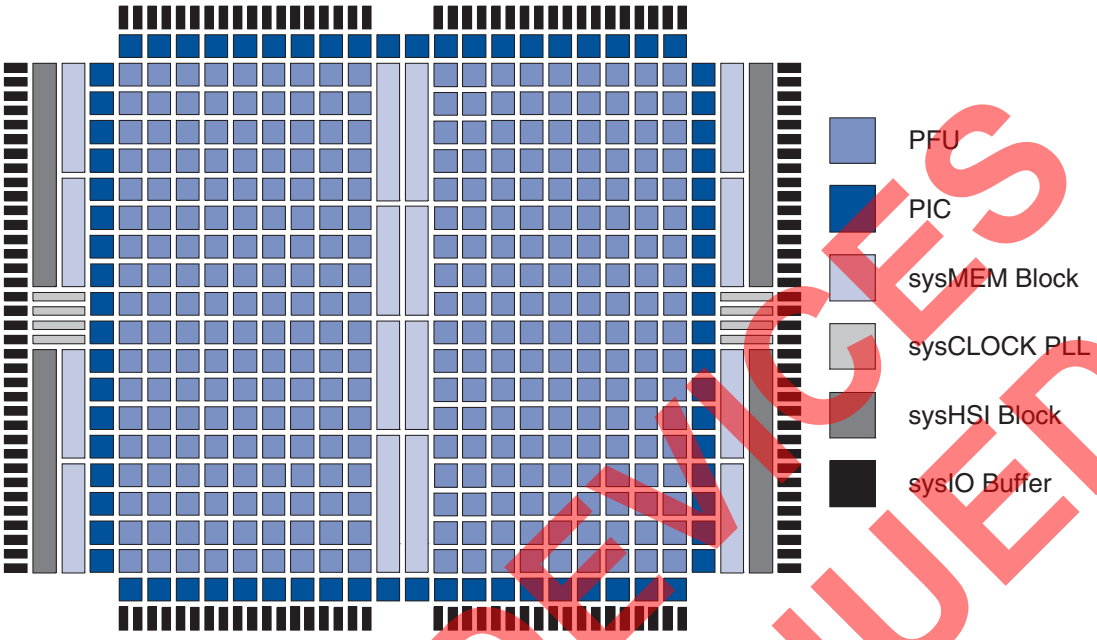
Figure 1. ispXPGA Block Diagram



Programmable Function Unit

The Programmable Function Unit (PFU) is the basic building block of the ispXPGA architecture. The PFUs are arranged in rows and columns in the device with PFU (1,1) referring to (row 1, column 1). Each PFU consists of four Configurable Logic Elements (CLEs), four Configurable Sequential Elements (CSEs), and a Wide Logic Generator (WLG). By utilizing these components, the PFU can implement a variety of functions. Table 3 lists some of the function capabilities of the PFU.

There are 57 inputs to each PFU and nine outputs. The PFU uses 20 inputs for logic, and 37 inputs drive the control logic from which six control signals are derived for the PFU.

Table 3. Function Capability of ispXPGA PFU

Function	Capability
Look-up table	LUT-4, LUT-5, LUT-6
Wide logic functions	Up to 20 input logic functions
Multiplexing	2:1, 4:1, 8:1
Arithmetic logic	Dedicated carry chain and booth multiplication logic
Single-port RAM	16X1, 16X2, 16X4, 32X1, 32X2, 64X1
Double-port RAM	16X1, 16X2, 32X1
Shift register	8-bit shift registers (up to 32-bit shift capability)

Configurable Logic Element

The CLE is made up of a four-input Look-up Table (LUT-4), a Carry Chain Generator (CCG), and a two-input AND gate. The LUT-4 creates various combinatorial and memory elements, the CCG creates a single one-bit full adder, and the two-input AND gate can expand the CCG to incorporate Booth Multiplier capability by feeding the output of the AND gate to one of the inputs of the CCG.

Of the five inputs that feed each CLE, two are dedicated inputs into each LUT-4 and the remaining three take on varying functionality. The third and fourth inputs can be used as either inputs to the LUT-4 or as a Feed-Thru to the CSE via the WLG. The fifth input can be a data port when the LUT is configured as Distributed Memory, a select line for multiplexer operation, or a Feed-Thru directly to the CSE via the WLG (Figure 2).

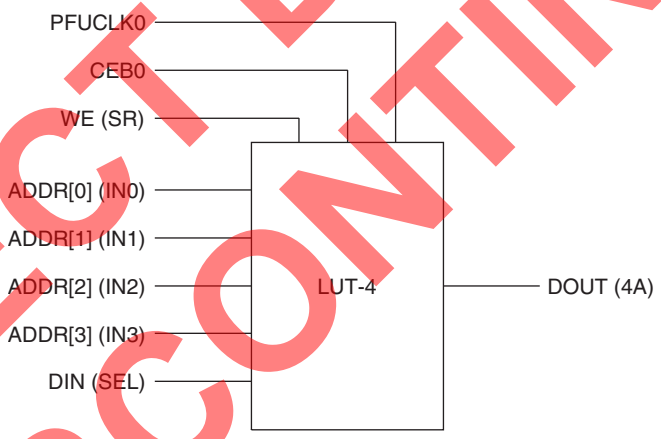
Look-Up Table – Combinatorial Mode

In combinatorial mode, the LUT-4 can implement any logic function up to four inputs. By using the carry chain and the WLG, each LUT-4 can be combined to form the enhanced functions listed in Table 3.

Look-Up Table – Distributed Memory Mode

In the distributed memory mode, the LUT functions as a memory element. The inputs to the LUT function as Address and Data. Each PFU is capable of implementing up to 64 SRAM bits. Both single and double port RAM can be performed in the PFU (Table 3). Furthermore, the distributed memory can be configured as either synchronous or asynchronous memory. Figure 3 illustrates the LUT while in distributed memory mode. When using any LUT in the PFU in memory mode, the Set/Reset signal will be used for Write Enable (WE(SR)) and the CLK0 signal will be used as the clock for synchronous read and write.

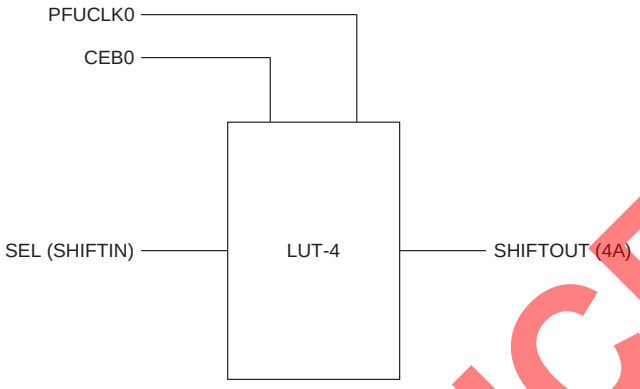
Figure 3. LUT in Distributed Memory Mode



Look-Up Table – Shift Register Mode

In the shift register mode, the LUT functions as a 1-bit to 8-bit shift register. This means that each PFU can implement up to four 8-bit shift registers or any cascaded combination. Figure 4 illustrates the LUT when configured in shift register mode.

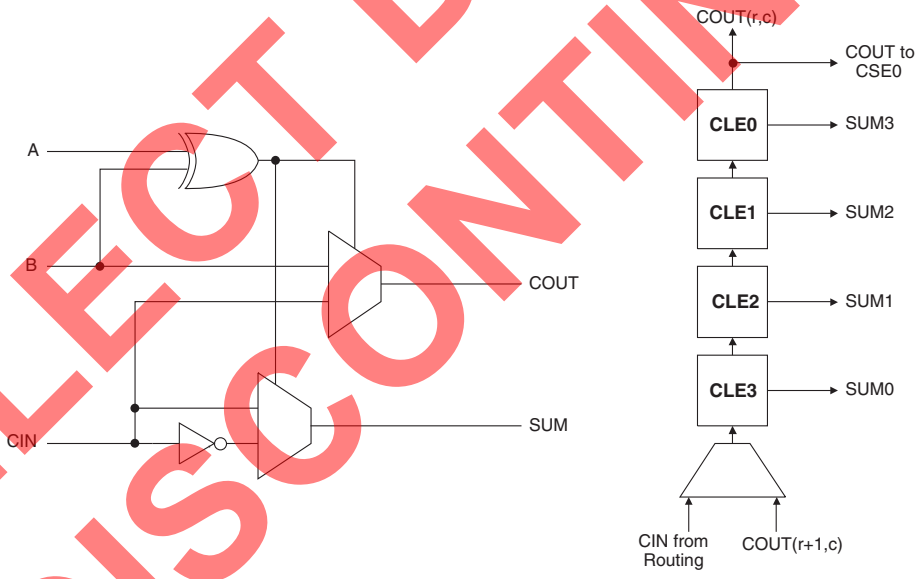
Figure 4. LUT in Shift Register Mode



Carry Chain Generator

The Carry Chain Generator is useful for implementing high-speed arithmetic functions. The CCG consists of a two-input XOR gate whose carryout can be cascaded with the input of the adjacent CCG. As shown in Figure 5, the carryin signal feeds CLE3 of the PFU and is propagated through CLE2 and CLE1 before reaching CLE0. The sum output of the CCG can be fed to the CSE through the WLG. The carryout must propagate to CLE0 for use outside the PFU. The carryout from the PFU can feed the W0 input of CSE0. The CCG also helps to effectively implement wider functions by using its logic elements to expand the capabilities of the LUT-4.

Figure 5. Carry Chain Generator



Wide Logic Generator

The WLG contains the logic necessary to implement wide gate functions. This is made up of a set of multiplexers that are located between the CLE and the CSE. The WLG helps in enhancing the wide gating capability of the PFU. The outputs of each CLE can be cascaded in the WLG to build wide gating functions. Wide multiplexing functions are also possible with a similar use of the WLG. Figure 6 illustrates the WLG.

High Speed Serial Interface Block (sysHSI Block)[1]

The High Speed Serial Interface (sysHSI) allows high speed serial data transfer over a pair of LVDS I/O. The ispXPGA devices have multiple sysHSI blocks.

Each sysHSI block has two SERDES blocks which contain two main sub-blocks, Transmitter (with a serializer) and Receiver (with a deserializer) including Clock/Data Recovery Circuit (CDR). Each SERDES can be used as a full duplex channel. The two SERDES in sysHSI blocks share a common clock and must operate at the same nominal frequency. Figure 20 shows the sysHSI block.

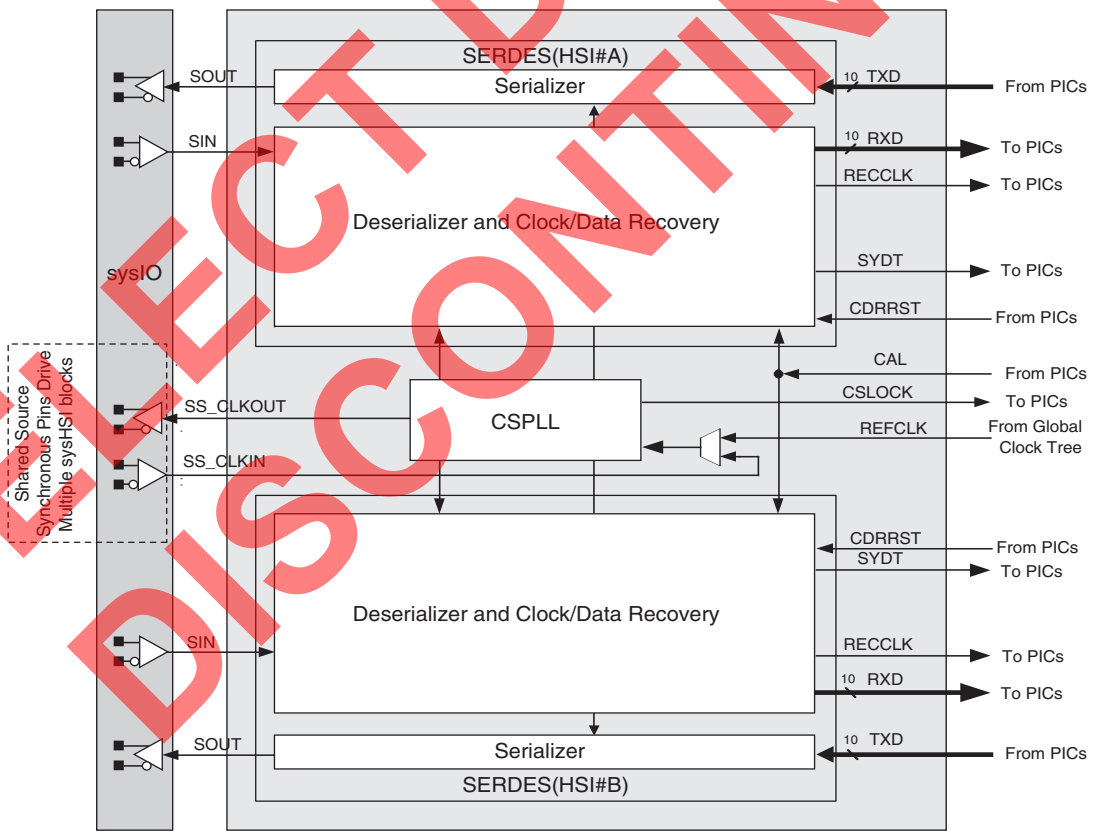
Device features support two data coding modes: 10B/12B and 8B/10B (for use with other encoding schemes, see Lattice's sysHSI technical notes). The encoding and decoding of the 10B/12B standard are performed within the sysHSI block. For the 8B/10B standard, the symbol boundaries are aligned internally but the encoding and decoding are performed outside the sysHSI block.

Each SERDES block receives a single high speed serial data input stream (with embedded clock) from an input, and provide a low speed 10-bit wide data stream and a recovered clock to the device. For transmitting, SERDES converts a 10-bit wide low-speed data stream to a single high-speed data stream with embedded clock for output.

Additionally, multiple sysHSI blocks can be grouped together to form a source synchronous interface of 1-10 channels.

For more information on the SERDES/CDR, refer to TN1020, sysHSI Usage Guidelines.

Figure 20. sysHSI Block Diagram



1. "E-Series" does not support sysHSI.

Absolute Maximum Ratings[1, 2, 3]

	1.8V	2.5V/3.3V
Supply Voltage (V_{CC})	-0.5 to 2.5V	-0.5 to 5.5V
PLL Supply Voltage (V_{CCP})	-0.5 to 2.5V	-0.5 to 5.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V
IEEE 1149.1 TAP Supply Voltage (V_{CCJ})	-0.5 to 4.5V	-0.5 to 4.5V
Input Voltage Applied[4, 5]	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C
Junction Temperature (T_J) with Power Applied	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied (while programming, following the programming specifications).
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to (V_{IH} (MAX) + 2) volts not to exceed 6V is permitted for a duration of <20ns.
5. A maximum of 64 I/Os per device with V_{IN} > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage for 1.8V device[1]	1.65	1.95	V
	Supply Voltage for 2.5V device	2.3	2.7	V
	Supply Voltage for 3.3V device	3.0	3.6	V
V_{CCP}	Supply Voltage for PLL and sysHSI blocks, 1.8V devices[1]	1.65	1.95	V
	Supply Voltage for PLL and sysHSI blocks, 2.5V devices	2.3	2.7	V
	Supply Voltage for PLL and sysHSI blocks, 3.3V devices	3.0	3.6	V
V_{CCJ}	Supply Voltage for IEEE 1149.1 Test Access Port for LVCMOS 1.8V	1.65	1.95	V
	Supply Voltage for IEEE 1149.1 Test Access Port for LVCMOS 2.5V	2.3	2.7	V
	Supply Voltage for IEEE 1149.1 Test Access Port for LVCMOS 3.3V	3.0	3.6	V
T_J (COM)	Junction Temperature Commercial Operation	0	85	C
T_J (IND)	Junction Temperature Industrial Operation	-40	105	C

1. sysHSI specification is valid for V_{CC} and V_{CCP} = 1.7V to 1.9V.

E²CMOS Erase Reprogram Specifications

Parameter	Min	Max	Units
Erase/Reprogram Cycle[1]	1,000	—	Cycles

1. Valid over commercial temperature range.

Hot Socketing Characteristics[1, 2, 3, 4]

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DK}	Input or Tristated I/O Leakage Current	0 ð V_{IN} ð 3.0V	—	+/-50	+/-800	µA

1. Insensitive to sequence of V_{CC} and V_{CCO} when V_{CCO} ð 1.0V. For V_{CCO} > 1.0V, V_{CC} min must be present. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO}, provided (V_{IN} - V_{CCO}) ð 3.6V.
2. LVTTL, LVCMOS only.
3. 0 < V_{CC} ð V_{CC} (MAX), 0 < V_{CCO} ð V_{CCO} (MAX).
4. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until non-volatile cells are active.

sysIO Recommended Operating Conditions

Standard	V_{CCO} (V)[1]			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.0	3.3	3.6	-	-	-
LVCMOS 2.5	2.3	2.5	2.7	-	-	-
LVCMOS 1.8[2]	1.65	1.8	1.95	-	-	-
LVTTL	3.0	3.3	3.6	-	-	-
PCI 3.3	3.0	3.3	3.6	-	-	-
AGP-1X	3.15	3.3	3.45	-	-	-
SSTL 2	2.3	2.5	2.7	1.15	1.25	1.35
SSTL 3	3.0	3.3	3.6	1.3	1.5	1.7
CTT 3.3	3.0	3.3	3.6	1.35	1.5	1.65
CTT 2.5	2.3	2.5	2.7	1.35	1.5	1.65
HSTL Class I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL Class III	1.4	1.5	1.6	-	0.9	-
GTL+	-	-	-	0.882	1.0	1.122
LVDS	2.3	2.5	2.7	-	-	-
LVPECL	3.0	3.3	3.6	-	-	-
BLVDS	2.3	2.5	2.7	-	-	-

1. Inputs independent of V_{CCO}.
2. Design tool default setting.

ispXPGA 200B/C & ispXPGA 200EB/EC External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Conditions	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{CO}	Global Clock Input to Output	PIO Output Register	—	5.5	—	5.9	—	6.8	ns
t_S	Global Clock Input Setup	PIO Input Register without input delay	-2.0	—	-2.0	—	-1.7	—	ns
t_H	Global Clock Input Hold	PIO Input Register without input delay	3.7	—	3.8	—	4.4	—	ns
t_{SINDLY}	Global Clock Input Setup	PIO Input Register with input delay	3.8	—	3.8	—	4.4	—	ns
t_{HINDLY}	Global Clock Input Hold	PIO Input Register with input delay	0.0	—	0.0	—	0.0	—	
t_{COPLL}	Global Clock Input to Output	PIO Output Register using PLL without delay	—	3.3	—	3.6	—	4.2	ns
t_{SPLL}	Global Clock Input Setup	PIO Input Register without input delay using PLL without delay	-0.2	—	-0.2	—	0.1	—	ns
t_{HPLL}	Global Clock Input Hold	PIO Input Register without input delay using PLL without delay	1.5	—	1.5	—	1.8	—	ns
$t_{SINDLYPLL}$	Global Clock Input Setup	PIO Input Register with input delay using PLL without delay	6.3	—	6.3	—	7.3	—	ns
$t_{HINDLYPLL}$	Global Clock Input Hold	PIO Input Register with input delay using PLL without delay	-2.7	—	-2.6	—	-2.2	—	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.

Timing v.0.2

REFCLK and SS_CLKIN Timing

Symbol	Description	Mode	Condition	Min	Max	Unit
$t_{DREFCLK}$	Frequency Deviation Between TX REFCLK and CDRX REFCLK on One Link	8B10B/ 10B12B		-100	100	ppm
$t_{JPPREFCLK}$	REFCLK, SS_CLKIN Peak-to-Peak Period Jitter	All	Random Jitter		0.01	UIPP
$t_{PWREFCLK}$	REFCLK, SS_CLKIN Pulse Width, (80% to 80% or 20% to 20%).	All	40-100MHz	2		ns
			100-200MHz	1		
$t_{RFREFCLK}$	REFCLK, SS_CLKIN Rise/Fall Time (20% to 80% or 80% to 20%)	All			2	ns

Serializer Timing[2]

Symbol	Description	Mode	Condition	Min	Max	Unit
$t_{JPPSOUT}$	SOUT Peak-to-Peak Output Data Jitter	All	f_{CLK} with no jitter		0.25	UIPP
$t_{JPP8B10B}$	SOUT Peak-to-Peak Random Jitter	8B10B	800 Mbps w/K28.7-		130	ps
	SOUT Peak-to-Peak Deterministic Jitter	8B10B	800 Mbps w/K28.5+		160	ps
t_{RFSOUT}	SOUT Output Data Rise/Fall Time (20%, 80%)	LVDS			700	ps
t_{COSOUT}	REFCLK to SOUT Delay	SS/8B10B		$2Bt^{1}$ + 2	$2Bt^{1}$ +10	ns
		10B12B		$1Bt^{1}$ + 2	$1Bt^{1}$ +10	ns
t_{SKTX}	Skew of SOUT with Respect to SS_CLKOUT	SS			300	ps
$t_{CKOSOUT}$	SS_CLKOUT to bit0 of SOUT	SS		$2Bt^{1}$ - t_{SKTX}	$2Bt^{1}$ + t_{SKTX}	ns
$t_{HSITXDDATAS}$	TXD Data Setup Time	All	Note 3	1.5		ns
$t_{HSITXDDATAH}$	TXD Data Hold Time	All	Note 3		1.0	ns

1. Bt: Bit Time Period. High Speed Serial Bit Time.
2. The SIN and SOUT jitter specifications listed above are under the condition that the clock tree that drives the REFCLK to sysHSI Block is in sysCLOCK PLL BYPASS mode.
3. Internal timing for reference only.

Deserializer Timing

Symbol	Description	Mode	Conditions	Min	Max	Units
f_{DSIN}	SIN Frequency Deviation from REFCLK	8B10B/ 10B12B		-100	100	ppm
eo_{SIN}	SIN Eye Opening Tolerance	All	Notes 1, 2	0.45		UIPP
ber	Bit Error Rate	All			10^{-12}	Bits
$t_{HSIOUTVALIDPRE}$	RXD, SYDT Valid Time Before RECCLK Falling Edge	All	Note 3	$t_{RCP}/2$ - 0.7		ns
$t_{HSIOUTVALIDPOST}$	RXD, SYDT Valid Time After RECCLK Falling Edge	All	Note 3	$t_{RCP}/2$ - 0.7		ns
t_{DSIN}	Bit 0 of SIN Delay to RXD Valid at RECCLK Falling edge	All		1.5 t_{RCP} + 4.5Bt + 3	1.5 t_{RCP} + 4.5Bt + 15	ns

1. Eye opening based on jitter frequency of 100KHz.
2. Lower frequency operation assumes maximum eye closure of 800ps.
3. Internal timing for reference only.

ispXPGA Power Supply and NC Connections[1] (Continued)

Signal	680-Ball fpBGA[3]	900-Ball fpBGA[3]
NC[2]	A3, B29, AW3, AV3, AW11, AV11, AV29, AW29, AW37, B3, AV37, C39, C38, AU39, AU38, AJ39, AJ38, N38, N39, C2, C1, AU1, AU2, AJ2, AJ1, N2, N1, B11, A11, A37, B37, A29	**LFX500:** A8, A9, A10, A11, A19, A20, A21, A22, B8, B9, B10, B11, B19, B20, B21, B22, C1, C2, C11, C12, C19, C20, C23, D3, D10, D11, D12, D19, D20, D21, D22, D23, E3, E5, E6, E10, E11, E12, E21, E22, E25, E26, E28, E29, E30, F1, F2, F6, F9, F10, F11, F12, F21, F22, F25, F26, F29, F30, G1, G2, G3, G4, G7, G8, G9, G10, G11, G12, G14, G15, G16, G17, G19, G20, G21, G22, G23, G24, G25, G26, G27, G28, G29, G30, H1, H2, H3, H4, H5, H6, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, H17, H18, H19, H20, H21, H22, H23, H24, H27, H28, H29, H30, J1, J2, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, K6, K7, K8, K9, K10, K12, K13, K14, K15, K16, K17, K18, K19, K21, K22, K23, K24, K25, L7, L8, L9, L22, L23, L24, M7, M8, M9, M10, M21, M22, M23, M24, N8, N9, N10, N21, N22, N23, P7, P8, P9, P10, P21, P22, P23, P24, R8, R9, R10, R21, R22, R23, R24, R25, T6, T7, T8, T9, T10, T21, T22, T23, T24, T25, U7, U8, U9, U10, U21, U22, U23, U24, V8, V9, V10, V21, V22, V23, W7, W8, W9, W10, W21, W22, W23, W24, W25, W26, Y3, Y4, Y5, Y6, Y7, Y8, Y9, Y22, Y23, Y24, Y25, Y26, Y27, Y28, AA4, AA5, AA6, AA7, AA8, AA9, AA10, AA12, AA13, AA14, AA15, AA16, AA17, AA18, AA19, AA21, AA22, AA23, AA24, AA25, AA26, AA27, AB1, AB2, AB4, AB5, AB6, AB7, AB8, AB9, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB18, AB19, AB20, AB21, AB22, AB23, AB24, AB25, AB26, AB27, AC1, AC2, AC3, AC4, AC5, AC6, AC7, AC8, AC9, AC10, AC11, AC12, AC13, AC14, AC15, AC16, AC17' AC18' AC19, AC20, AC21, AC22, AC23, AC24, AC27, AC28, AC29, AC30, AD1, AD2, AD7, AD8, AD9, AD10, AD11, AD12, AD14, AD15, AD16, AD17, AD19, AD20, AD21, AD22, AD23, AD24, AD29, AD30, AE6, AE9, AE10, AE11, AE12, AE19, AE20, AE21, AE22, AE25, AE29, AE30, AF5, AF6, AF10, AF11, AF12, AF19, AF20, AF21, AF22, AF25, AF26, AG10, AG11, AG12, AG19, AG20, AG21, AG22, AH11, AH12, AH19, AH20, AJ8, AJ9, AJ10, AJ11, AJ20, AJ21, AJ22, AK8, AK9, AK10, AK11, AK20, AK21, AK22 **LFX1200:** AA22, AA23, AA24, AA25, AB23, AC24, T21, T22, T23, T24, T25, U21, U22, U23, U24, V21, V22, V23, W21, W22, W23, W24, Y22, Y23, Y24, AA16, AA17, AA18, AA19, AA21, AB16, AB17, AB18, AB19, AB20, AB21, AB22, AC16, AC17, AC18, AC19, AC20, AC21, AC22, AC23, AD16, AD17, AD19, AD20, AD22, AD23, AD24, AE22, AE25, AF25, AF26, AA10, AA12, AA13, AA14, AA15, AB10, AB11, AB12, AB13, AB14, AB15, AB9, AC10, AC11, AC12, AC13, AC14, AC15, AC8, AC9, AD11, AD12, AD14, AD15, AD7, AD8, AD9, AE6, AE9, AF5, AF6, H24, J23, K22, K23, K24, K25, L22, L23, L24, M21, M22, M23, M24, N21, N22, N23, P21, P22, P23, P24, R21, R22, R23, R24, R25, AA6, AA7, AA8, AA9, AB8, AC7, T10, T6, T7, T8, T9, U10, U7, U8, U9, V10, V8, V9, W10, W7, W8, W9, Y7, Y8, Y9, H5, H6, H7, J8, K6, K7, K8, K9, L7, L8, L9, M10, M7, M8, M9, N10, N8, N9, P10, P7, P8, P9, R10, R8, R9, E25, E26, F22, F25, G16, G17, G19, G20, G22, G23, G24, H16, H17, H18, H19, H20, H21, H22, H23, J16, J17, J18, J19, J20, J21, J22, K16, K17, K18, K19, K21, E5, E6, F6, F9, G11, G12, G14, G15, G7, G8, G9, H10, H11, H12, H13, H14, H15, H8, H9, J10, J11, J12, J13, J14, J15, J9, K10, K12, K13, K14, K15

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, V_{CC} or GND.
3. Balls for GND, V_{CC} and V_{CCOx} are connected within the substrate to their respective common signals. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
D16	BK5_IO15	HSI3A_SOUTN	72N/HSI3	BK5_IO13	HSI1A_SOUTN	61N/HSI1
E13	BK5_IO16	VREF5	73P/HSI3	BK5_IO14	VREF5	62P/HSI1
E14	BK5_IO17	-	73N/HSI3	BK5_IO15	-	62N/HSI1
E15	BK5_IO18	HSI3B_SINP	74P/HSI3	BK5_IO16	HSI1B_SINP	63P/HSI1
-	-	-	-	GND (Bank 5)	-	-
D15	BK5_IO19	HSI3B_SINN	74N/HSI3	BK5_IO17	HSI1B_SINN	63N/HSI1
C16	BK5_IO22	HSI3B_SOUTP	76P/HSI3	BK5_IO20	HSI1B_SOUTP	65P/HSI1
-	GND (Bank 5)	-	-	-	-	-
B16	BK5_IO23	HSI3B_SOUTN	76N/HSI3	BK5_IO21	HSI1B_SOUTN	65N/HSI1
D14	BK5_IO24	-	77P/HSI3	BK5_IO18	-	64P/HSI1
C15	BK5_IO25	-	77N/HSI3	BK5_IO19	-	64N/HSI1
C13	CFG0	-	-	CFG0	-	-
A15	DONE	-	-	DONE	-	-
A14	PROGRAMb	-	-	PROGRAMb	-	-
D12	BK6_IO0	INITb	78P	BK6_IO0	INITb	66P
C12	BK6_IO1	CCLK	78N	BK6_IO1	CCLK	66N
B14	BK6_IO2	-	79P	BK6_IO2	-	67P
-	GND (Bank 6)	-	-	-	-	-
B13	BK6_IO3	-	79N	BK6_IO3	-	67N
A13	BK6_IO4	CSb	80P	BK6_IO4	CSb	68P
-	-	-	-	GND (Bank 6)	-	-
A12	BK6_IO5	Read	80N	BK6_IO5	READ	68N
D11	BK6_IO6	DATA7	81P	BK6_IO6	DATA7	69P
C11	BK6_IO7	DATA6	81N	BK6_IO7	DATA6	69N
B12	BK6_IO8	-	82P	BK6_IO8	-	70P
B11	BK6_IO9	VREF6	82N	BK6_IO9	VREF6	70N
D10	BK6_IO10	DATA5	83P	BK6_IO10	DATA5	71P
-	GND (Bank 6)	-	-	-	-	-
C10	BK6_IO11	DATA4	83N	BK6_IO11	DATA4	71N
-	-	-	-	GND (Bank 6)	-	-
A11	BK6_IO14	DATA3	85P	BK6_IO14	DATA3	73P
A10	BK6_IO15	DATA2	85N	BK6_IO15	DATA2	73N
D9	BK6_IO16	-	86P	BK6_IO16	-	74P
C9	BK6_IO17	-	86N	BK6_IO17	-	74N
B10	BK6_IO18	DATA1	87P	BK6_IO18	DATA1	75P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
B9	BK6_IO19	DATA0	87N	BK6_IO19	DATA0	75N
E9	BK6_IO20	-	88P	BK6_IO20	-	76P
E8	BK6_IO21	-	88N	BK6_IO21	-	76N
-	GND (Bank 6)	-	-	-	-	-
-	GND (Bank 7)	-	-	-	-	-
D8	BK7_IO0	-	91P	BK7_IO0	-	77P

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
C8	BK7_IO1	-	91N	BK7_IO1	-	77N
B8	BK7_IO2	-	92P	BK7_IO2	-	78P
B7	BK7_IO3	-	92N	BK7_IO3	-	78N
A9	BK7_IO6	-	94P	BK7_IO4	-	79P
-	GND (Bank 7)	-	-	-	-	-
A8	BK7_IO7	-	94N	BK7_IO5	-	79N
C7	BK7_IO10	-	96P	BK7_IO6	-	80P
D7	BK7_IO11	-	96N	BK7_IO7	-	80N
D6	BK7_IO12	-	97P	BK7_IO8	-	81P
-	-	-	-	GND (Bank 7)	-	-
C6	BK7_IO13	-	97N	BK7_IO9	-	81N
B6	BK7_IO14	-	98P	BK7_IO10	-	82P
-	GND (Bank 7)	-	-	-	-	-
B5	BK7_IO15	-	98N	BK7_IO11	-	82N
A7	BK7_IO16	VREF7	99P	BK7_IO12	VREF7	83P
A6	BK7_IO17	-	99N	BK7_IO13	-	83N
D5	BK7_IO18	-	100P	BK7_IO14	-	84P
C5	BK7_IO19	-	100N	BK7_IO15	-	84N
A5	BK7_IO20	-	101P	BK7_IO16	-	85P
-	-	-	-	GND (Bank 7)	-	-
A4	BK7_IO21	-	101N	BK7_IO17	-	85N
B4	BK7_IO22	-	102P	BK7_IO18	-	86P
-	GND (Bank 7)	-	-	-	-	-
B3	BK7_IO23	-	102N	BK7_IO19	-	86N
A3	TDO	-	-	TDO	-	-
A2	VCCJ	-	-	VCCJ	-	-
C4	TDI	-	-	TDI	-	-

1. Not available for differential pairs.
2. If a sysHSI Block is used, the indicated sysHSI reserved pins are unavailable for general purpose I/O use.

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
-	-	-	-	GND (Bank 0)	-	-	-	-	-
R2	GCLK0	-	LVDS Pair0P	GCLK0	-	LVDS Pair0P	GCLK0	-	LVDS Pair0P
R3	GCLK1	-	LVDS Pair0N	GCLK1	-	LVDS Pair0N	GCLK1	-	LVDS Pair0N
R4	VCCP0	-	-	VCCP0	-	-	VCCP0	-	-
T4	GNDP0	-	-	GNDP0	-	-	GNDP0	-	-
T3	GCLK2	-	LVDS Pair1P	GCLK2	-	LVDS Pair1P	GCLK2	-	LVDS Pair1P
T2	GCLK3	-	LVDS Pair1N	GCLK3	-	LVDS Pair1N	GCLK3	-	LVDS Pair1N
-	-	-	-	GND (Bank 1)	-	-	-	-	-
T1	BK1_IO0	CLK_OUT2	21P	BK1_IO0	CLK_OUT2	13P	BK1_IO0	CLK_OUT2	11P
-	GND (Bank 1)	-	-	-	-	-	-	-	-
U1	BK1_IO1	CLK_OUT3	21N	BK1_IO1	CLK_OUT3	13N	BK1_IO1	CLK_OUT3	11N
U2	BK1_IO2	SS_CLKOUT0P	22P	BK1_IO2	SS_CLKOUT0P	14P	BK1_IO2	SS_CLKOUT0P	12P
-	-	-	-	-	-	-	GND (Bank 1)	-	-
U3	BK1_IO3	SS_CLKOUT0N	22N	BK1_IO3	SS_CLKOUT0N	14N	BK1_IO3	SS_CLKOUT0N	12N
V1	BK1_IO4	PLL_FBK2	23P	BK1_IO4	PLL_FBK2	15P	BK1_IO4	PLL_FBK2	13P
V2	BK1_IO5	PLL_FBK3	23N	BK1_IO5	PLL_FBK3	15N	BK1_IO5	PLL_FBK3	13N
V3	BK1_IO6	-	24P	NC	-	-	NC	-	-
-	GND (Bank 1)	-	-	-	-	-	-	-	-
V4	BK1_IO7	-	24N	NC	-	-	NC	-	-
W1	BK1_IO8	-	25P	NC	-	-	NC	-	-
Y1	BK1_IO9	-	25N	NC	-	-	NC	-	-
W2	BK1_IO10	SS_CLKINOP	26P	BK1_IO6	SS_CLKIN0P	16P	BK1_IO6	SS_CLKIN0P	14P
-	-	-	-	GND (Bank 1)	-	-	-	-	-
W3	BK1_IO11	SS_CLKINON	26N	BK1_IO7	SS_CLKIN0N	16N	BK1_IO7	SS_CLKIN0N	14N
Y2	BK1_IO12		27P	BK1_IO8		17P	BK1_IO8	-	15P
-	-	-	-	-	-	-	GND (Bank 1)	-	-
Y4	BK1_IO13	-	27N	BK1_IO9	-	17N	BK1_IO9	-	15N
Y3	BK1_IO14	-	28P	NC	-	-	NC	-	-
-	GND (Bank 1)	-	-	-	-	-	-	-	-
AA1	BK1_IO15	-	28N	NC	-	-	NC	-	-
AA2	BK1_IO16	-	29P	NC	-	-	NC	-	-
AA3	BK1_IO17	-	29N	NC	-	-	NC	-	-
AB2	BK1_IO18	HSI2A_SOUTP	30P	BK1_IO10	HSI1A_SOUTP	18P/HSI1	BK1_IO10	-	16P
AC2	BK1_IO19	HSI2A_SOUTN	30N	BK1_IO11	HSI1A_SOUTN	18N/HSI1	BK1_IO11	-	16N
AB3	BK1_IO20	PLL_RST2	31P	BK1_IO12	PLL_RST2	19P/HSI1	BK1_IO12	PLL_RST2	17P
AA4	BK1_IO21	PLL_RST3	31N	BK1_IO13	PLL_RST3	19N/HSI1	BK1_IO13	PLL_RST3	17N
AC1	BK1_IO22	HSI2A_SINP	32P	BK1_IO14	HSI1A_SINP	20P/HSI1	NC	-	-
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-	-	-	-
AD1	BK1_IO23	HSI2A_SINN	32N	BK1_IO15	HSI1A_SINN	20N/HSI1	NC	-	-
AE1	BK1_IO24	VREF1	33P/HSI2	BK1_IO16	VREF1	21P/HSI1	BK1_IO14	VREF1	18P
AF1	BK1_IO25		33N/HSI2	BK1_IO17	-	21N/HSI1	BK1_IO15	-	18N
AC3	BK1_IO26	HSI2B_SOUTP	34P/HSI2	BK1_IO18	HSI1B_SOUTP	22P/HSI1	BK1_IO16	-	19P
-	-	-	-	-	-	-	GND (Bank 1)	-	-
AC4	BK1_IO27	HSI2B_SOUTN	34N/HSI2	BK1_IO19	HSI1B_SOUTN	22N/HSI1	BK1_IO17	-	19N
AD2	BK1_IO28	-	35P/HSI2	BK1_IO20	-	23P/HSI1	BK1_IO18	-	20P
AD3	BK1_IO29	-	35N/HSI2	BK1_IO21	-	23N/HSI1	BK1_IO19	-	20N
AE2	BK1_IO30	HSI2B_SINP	36P/HSI2	BK1_IO22	HSI1B_SINP	24P/HSI1	BK1_IO20	-	21P
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-	-	-	-
AF2	BK1_IO31	HSI2B_SINN	36N/HSI2	BK1_IO23	HSI1B_SINN	24N/HSI1	BK1_IO21	-	21N
AD4	BK1_IO32	-	37P/HSI2	NC	-	-	NC	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AE3	BK1_IO33	-	37N/HSI2	NC	-	-	NC	-	-
AG1	BK1_IO34	-	38P/HSI2	NC	-	-	NC	-	-
AH1	BK1_IO35	-	38N/HSI2	NC	-	-	NC	-	-
AG2	BK1_IO36	-	39P/HSI2	NC	-	-	NC	-	-
AF3	BK1_IO37	-	39N/HSI2	NC	-	-	NC	-	-
AJ1	BK1_IO38	-	40P/HSI2	NC	-	-	NC	-	-
-	GND (Bank 1)	-	-	-	-	-	-	-	-
AH2	BK1_IO39	-	40N/HSI2	NC	-	-	NC	-	-
AG3	BK1_IO40	-	41P	BK1_IO24	-	25P/HSI1	NC	-	-
AF4	BK1_IO41	-	41N	BK1_IO25	-	25N/HSI1	NC	-	-
AK2	TCK	-	-	TCK	-	-	TCK	-	-
AJ3	TMS	-	-	TMS	-	-	TMS	-	-
AG5	TOE	-	-	TOE	-	-	TOE	-	-
AH4	BK2_IO0	-	42P	BK2_IO0	-	26P	BK2_IO0	-	22P
AK3	BK2_IO1	-	42N	BK2_IO1	-	26N	BK2_IO1	-	22N
AJ4	BK2_IO2	-	43P	BK2_IO2	-	27P	BK2_IO2	-	23P
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-	-	-	-
AH5	BK2_IO3	-	43N	BK2_IO3	-	27N	BK2_IO3	-	23N
AK4	BK2_IO4	-	44P	BK2_IO4	-	28P	BK2_IO4	-	24P
-	-	-	-	-	-	-	GND (Bank 2)	-	-
AJ5	BK2_IO5	-	44N	BK2_IO5	-	28N	BK2_IO5	-	24N
AG7	BK2_IO6	-	45P	BK2_IO6	-	29P	BK2_IO6	-	25P
AH6	BK2_IO7	-	45N	BK2_IO7	-	29N	BK2_IO7	-	25N
AK5	BK2_IO8	-	46P	NC	-	-	NC	-	-
AJ6	BK2_IO9	-	46N	NC	-	-	NC	-	-
AG8	BK2_IO10	-	47P	NC	-	-	NC	-	-
-	GND (Bank 2)	-	-	-	-	-	-	-	-
AH7	BK2_IO11	-	47N	NC	-	-	NC	-	-
AK6	BK2_IO12	-	48P	NC	-	-	NC	-	-
AJ7	BK2_IO13	-	48N	NC	-	-	NC	-	-
AH8	BK2_IO14	-	49P	NC	-	-	NC	-	-
AG10	BK2_IO15	-	49N	NC	-	-	NC	-	-
AK7	BK2_IO16	-	50P	NC	-	-	NC	-	-
AJ8	BK2_IO17	-	50N	NC	-	-	NC	-	-
AH9	BK2_IO18	-	51P	NC	-	-	NC	-	-
-	GND (Bank 2)	-	-	-	-	-	-	-	-
AG11	BK2_IO19	-	51N	NC	-	-	NC	-	-
AK8	BK2_IO20	-	52P	BK2_IO8	-	30P	BK2_IO8	-	26P
AJ9	BK2_IO21	VREF2	52N	BK2_IO9	VREF2	30N	BK2_IO9	VREF2	26N
AH10	BK2_IO22	-	53P	BK2_IO10	-	31P	BK2_IO10	-	27P
-	-	-	-	GND (Bank 2)	-	-	-	-	-
AH11	BK2_IO23	-	53N	BK2_IO11	-	31N	BK2_IO11	-	27N
AJ10	BK2_IO24	-	54P	BK2_IO12		32P	BK2_IO12	-	28P
AK10	BK2_IO25	-	54N	BK2_IO13	-	32N	BK2_IO13	-	28N
AH12	BK2_IO26	-	55P	BK2_IO14	-	33P	BK2_IO14	-	29P
-	GND (Bank 2)	-	-	-	-	-	-	-	-
AJ11	BK2_IO27	-	55N	BK2_IO15	-	33N	BK2_IO15	-	29N
AK11	BK2_IO28	-	56P	NC	-	-	NC	-	-
AJ12	BK2_IO29	-	56N	NC	-	-	NC	-	-
AG13	BK2_IO30	-	57P	BK2_IO16	-	34P	BK2_IO16	-	30P
AH13	BK2_IO31	-	57N	BK2_IO17	-	34N	BK2_IO17	-	30N

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AJ13	BK2_IO32	-	58P	BK2_IO18	-	35P	BK2_IO18	-	31P
-	-	-	-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
AK12	BK2_IO33	-	58N	BK2_IO19	-	35N	BK2_IO19	-	31N
AK13	BK2_IO34	-	59P	BK2_IO20	-	36P	BK2_IO20	-	32P
-	GND (Bank 2)	-	-	-	-	-	-	-	-
AH14	BK2_IO35	-	59N	BK2_IO21	-	36N	BK2_IO21	-	32N
AJ14	BK2_IO36	-	60P	BK2_IO22	-	37P	NC	-	-
AK14	BK2_IO37	-	60N	BK2_IO23	-	37N	NC	-	-
AG15	BK2_IO38	-	61P	BK2_IO24	-	38P	NC	-	-
AH15	BK2_IO39	-	61N	BK2_IO25	-	38N	NC	-	-
AJ15	BK2_IO40	-	62P	NC	-	-	NC	-	-
AK15	BK2_IO41	-	62N	NC	-	-	NC	-	-
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-	-	-	-
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-	-	-	-
AK16	BK3_IO0	-	63P	BK3_IO0	-	39P	BK3_IO0	-	33P
AJ16	BK3_IO1	-	63N	BK3_IO1	-	39N	BK3_IO1	-	33N
AH16	BK3_IO2	-	64P	BK3_IO2	-	40P	BK3_IO2	-	34P
AG16	BK3_IO3	-	64N	BK3_IO3	-	40N	BK3_IO3	-	34N
AK17	BK3_IO4	-	65P	BK3_IO4	-	41P	BK3_IO4	-	35P
AJ17	BK3_IO5	-	65N	BK3_IO5	-	41N	BK3_IO5	-	35N
AH17	BK3_IO6	-	66P	BK3_IO6	-	42P	BK3_IO6	-	36P
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-	-	-	-
AJ18	BK3_IO7	-	66N	BK3_IO7	-	42N	BK3_IO7	-	36N
AH18	BK3_IO8	-	67P	BK3_IO8	-	43P	BK3_IO8	-	37P
-	-	-	-	-	-	-	GND (Bank 3)	-	-
AG18	BK3_IO9	-	67N	BK3_IO9	-	43N	BK3_IO9	-	37N
AK18	BK3_IO10	-	68P	BK3_IO10	-	44P	BK3_IO10	-	38P
AK19	BK3_IO11	-	68N	BK3_IO11	-	44N	BK3_IO11	-	38N
AJ19	BK3_IO12	-	69P	BK3_IO12	-	45P	NC	-	-
AH19	BK3_IO13	-	69N	BK3_IO13		45N	NC	-	-
AK20	BK3_IO14	-	70P	BK3_IO14	-	46P	NC	-	-
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-	-	-	-
AJ20	BK3_IO15	-	70N	BK3_IO15	-	46N	NC	-	-
AH20	BK3_IO16	-	71P	NC	-	-	NC	-	-
AG20	BK3_IO17	-	71N	NC	-	-	NC	-	-
AK21	BK3_IO18	-	72P	NC	-	-	NC	-	-
AJ21	BK3_IO19	-	72N	NC	-	-	NC	-	-
AH21	BK3_IO20	VREF3	73P	BK3_IO16	VREF3	47P	BK3_IO12	VREF3	39P
AG21	BK3_IO21	-	73N	BK3_IO17	-	47N	BK3_IO13	-	39N
AJ22	BK3_IO22	-	74P	BK3_IO18	-	48P	BK3_IO14	-	40P
-	GND (Bank 3)	-	-	-	-	-	-	-	-
AH22	BK3_IO23	-	74N	BK3_IO19	-	48N	BK3_IO15	-	40N
AK23	BK3_IO24	-	75P	NC	-	-	NC	-	-
AJ23	BK3_IO25	-	75N	NC	-	-	NC	-	-
AH23	BK3_IO26	-	76P	NC	-	-	NC	-	-
AK24	BK3_IO27	-	76N	NC	-	-	NC	-	-
AJ24	BK3_IO28	-	77P	NC	-	-	NC	-	-
AG23	BK3_IO29	-	77N	NC	-	-	NC	-	-
AH24	BK3_IO30	-	78P	NC	-	-	NC	-	-
-	GND (Bank 3)	-	-		-	-	-	-	-
AK25	BK3_IO31	-	78N	NC	-	-	NC	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
D21	BK6_IO20	-	136P	BK6_IO8	-	82P	BK6_IO8	-	70P
C21	BK6_IO21	VREF6	136N	BK6_IO9	VREF6	82N	BK6_IO9	VREF6	70N
B21	BK6_IO22	DATA5	137P	BK6_IO10	DATA5	83P	BK6_IO10	DATA5	71P
-	-	-	-	GND (Bank 6)	-	-	-	-	-
A21	BK6_IO23	DATA4	137N	BK6_IO11	DATA4	83N	BK6_IO11	DATA4	71N
D20	BK6_IO24	-	138P	BK6_IO12	-	84P	BK6_IO12	-	72P
-	-	-	-	-	-	-	GND (Bank 6)	-	-
C20	BK6_IO25	-	138N	BK6_IO13	-	84N	BK6_IO13	-	72N
B20	BK6_IO26	DATA3	139P	BK6_IO14	DATA3	85P	BK6_IO14	DATA3	73P
-	GND (Bank 6)	-	-	-	-	-	-	-	-
A20	BK6_IO27	DATA2	139N	BK6_IO15	DATA2	85N	BK6_IO15	DATA2	73N
C19	BK6_IO28	-	140P	BK6_IO16		86P	BK6_IO16	-	74P
B19	BK6_IO29	-	140N	BK6_IO17		86N	BK6_IO17	-	74N
A19	BK6_IO30	DATA1	141P	BK6_IO18	DATA1	87P	BK6_IO18	DATA1	75P
-	-	-	-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
A18	BK6_IO31	DATA0	141N	BK6_IO19	DATA0	87N	BK6_IO19	DATA0	75N
D18	BK6_IO32	-	142P	BK6_IO20		88P	BK6_IO20	-	76P
C18	BK6_IO33	-	142N	BK6_IO21		88N	BK6_IO21	-	76N
B18	BK6_IO34	-	143P	BK6_IO22		89P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-	-	-	-
C17	BK6_IO35	-	143N	BK6_IO23		89N	NC	-	-
B17	BK6_IO36	-	144P	NC	-	-	NC	-	-
A17	BK6_IO37	-	144N	NC	-	-	NC	-	-
D16	BK6_IO38	-	145P	NC	-	-	NC	-	-
C16	BK6_IO39	-	145N	NC	-	-	NC	-	-
B16	BK6_IO40	-	146P	BK6_IO24	-	90P	NC	-	-
A16	BK6_IO41	-	146N	BK6_IO25	-	90N	NC	-	-
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-	-	-	-
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-	-	-	-
A15	BK7_IO0	-	147P	BK7_IO0	-	91P	BK7_IO0	-	77P
B15	BK7_IO1	-	147N	BK7_IO1	-	91N	BK7_IO1	-	77N
C15	BK7_IO2	-	148P	BK7_IO2	-	92P	BK7_IO2	-	78P
-	-	-	-	-	-	-	GND (Bank 7)	-	-
D15	BK7_IO3	-	148N	BK7_IO3	-	92N	BK7_IO3	-	78N
A14	BK7_IO4	-	149P	BK7_IO4	-	93P	BK7_IO4	-	79P
B14	BK7_IO5	-	149N	BK7_IO5	-	93N	BK7_IO5	-	79N
C14	BK7_IO6	-	150P	BK7_IO6	-	94P	NC	-	-
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-	-	-	-
A13	BK7_IO7	-	150N	BK7_IO7	-	94N	NC	-	-
B13	BK7_IO8	-	151P	BK7_IO8	-	95P	NC	-	-
C13	BK7_IO9	-	151N	BK7_IO9	-	95N	NC	-	-
D13	BK7_IO10	-	152P	BK7_IO10	-	96P	BK7_IO6	-	80P
B12	BK7_IO11	-	152N	BK7_IO11	-	96N	BK7_IO7	-	80N
C12	BK7_IO12	-	153P	BK7_IO12	-	97P	BK7_IO8	-	81P
-	-	-	-	-	-	-	GND (Bank 7)	-	-
A12	BK7_IO13	-	153N	BK7_IO13		97N	BK7_IO9	-	81N
A11	BK7_IO14	-	154P	BK7_IO14	-	98P	BK7_IO10	-	82P
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-	-	-	-
B11	BK7_IO15	-	154N	BK7_IO15	-	98N	BK7_IO11	-	82N
C11	BK7_IO16	-	155P	NC	-	-	NC	-	-
D11	BK7_IO17	-	155N	NC	-	-	NC	-	-

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
AH39	BK3_IO31	-	108N
AK39	BK3_IO32	-	109P
AK38	BK3_IO33	-	109N
AF35	BK3_IO34	-	110P
-	GND (Bank 3)	-	-
AJ37	BK3_IO35	-	110N
AH36	BK3_IO36	-	111P
AM39	BK3_IO37	-	111N
AL38	BK3_IO38	-	112P
AL39	BK3_IO39	-	112N
AJ36	BK3_IO40	-	113P
AH35	BK3_IO41	-	113N
AL37	BK3_IO42	-	114P
-	GND (Bank 3)	-	-
AN38	BK3_IO43	-	114N
AM38	BK3_IO44	-	115P
AK36	BK3_IO45	-	115N
AM37	BK3_IO46	-	116P
AN37	BK3_IO47	-	116N
AN39	BK3_IO48	-	117P
AL36	BK3_IO49	VREF3	117N
AK35	BK3_IO50	-	118P
-	GND (Bank 3)	-	-
AP39	BK3_IO51	-	118N
AM36	BK3_IO52	-	119P
AP38	BK3_IO53	-	119N
AR39	BK3_IO54	-	120P
AN36	BK3_IO55	-	120N
AM35	BK3_IO56	-	121P
AR38	BK3_IO57	-	121N
AP37	BK3_IO58	-	122P
-	GND (Bank 3)	-	-
AT39	BK3_IO59	-	122N
AR37	BK3_IO60	-	123P
AP36	BK3_IO61	-	123N
AT38	GSR	-	-
AP35	DXP	-	-
AT37	DXN	-	-
AU36	BK4_IO0	-	124P
AV36	BK4_IO1	-	124N
AR34	BK4_IO2	-	125P
-	GND (Bank 4)	-	-
AW36	BK4_IO3	-	125N

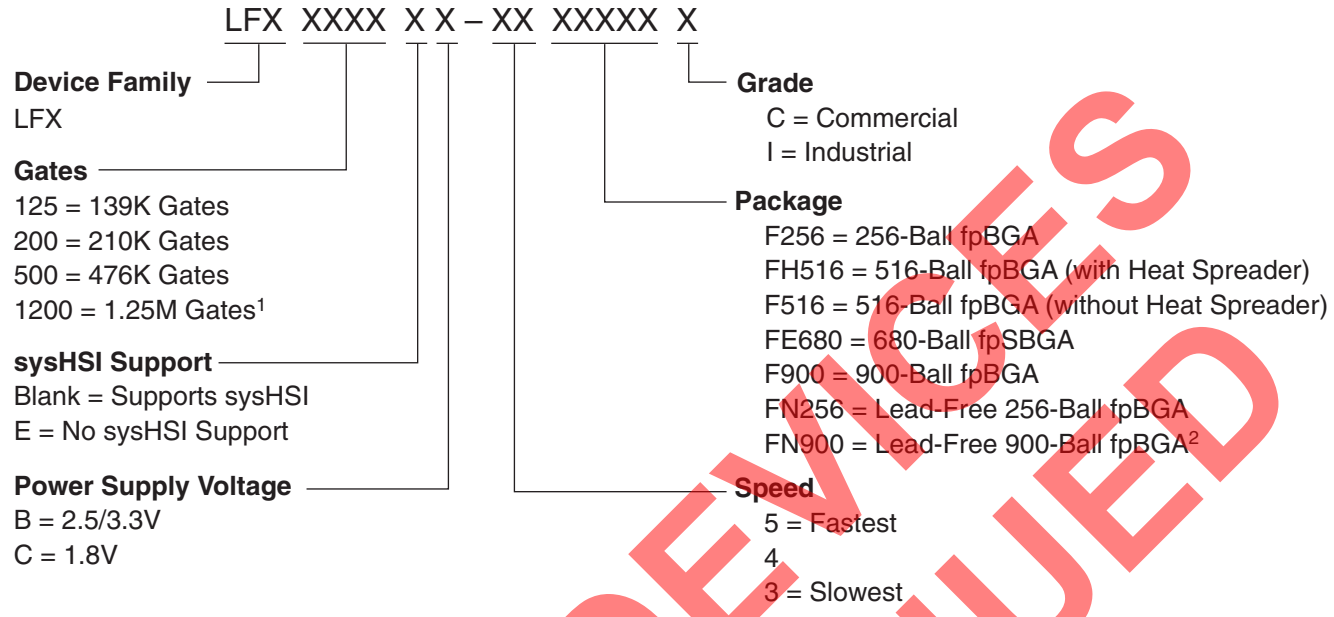
ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
AU6	BK5_IO50	HSI9B_SINP	180P/HSI9
-	GND (Bank 5)	-	-
AV6	BK5_IO51	HSI9B_SINN	180N/HSI9
AR8	BK5_IO52	-	181P
AT7	BK5_IO53	-	181N
AU5	BK5_IO54	HSI9B_SOUTP	182P
AV5	BK5_IO55	HSI9B_SOUTN	182N
AW5	BK5_IO56	-	183P
AW4	BK5_IO57	-	183N
AT6	BK5_IO58	-	184P
-	GND (Bank 5)	-	-
AV4	BK5_IO59	-	184N
AR6	BK5_IO60	-	185P
AU4	BK5_IO61	-	185N
AT1	CFG0	-	-
AT3	DONE	-	-
AT2	PROGRAMb	-	-
AP4	BK6_IO0	INITb	186P
AP5	BK6_IO1	CCLK	186N
AR3	BK6_IO2	-	187P
-	GND (Bank 6)	-	-
AR2	BK6_IO3	-	187N
AP3	BK6_IO4	CSb	188P
AR1	BK6_IO5	Read	188N
AP2	BK6_IO6	-	189P
AP1	BK6_IO7	-	189N
AN4	BK6_IO8	-	190P
AM5	BK6_IO9	-	190N
AN3	BK6_IO10	-	191P
-	GND (Bank 6)	-	-
AN2	BK6_IO11	-	191N
AM4	BK6_IO12	VREF6	192P
AM3	BK6_IO13	-	192N
AN1	BK6_IO14	-	193P
AM2	BK6_IO15	-	193N
AL4	BK6_IO16	-	194P
AK5	BK6_IO17	-	194N
AM1	BK6_IO18	-	195P
-	GND (Bank 6)	-	-
AK4	BK6_IO19	-	195N
AL3	BK6_IO20	-	196P
AL2	BK6_IO21	-	196N
AL1	BK6_IO22	-	197P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AJ18	BK3_IO14	-	100P	BK3_IO14	-	70P
-	-	-	-	GND (Bank 3)	-	-
AK18	BK3_IO15	-	100N	BK3_IO15	-	70N
AE18	BK3_IO16	-	101P	BK3_IO16	-	71P
AD18	BK3_IO17	-	101N	BK3_IO17	-	71N
AJ19	BK3_IO18	-	102P	BK3_IO18	-	72P
-	GND (Bank 3)	-	-	-	-	-
AK19	BK3_IO19	-	102N	BK3_IO19	-	72N
AH19	BK3_IO20	-	103P	NC	-	-
AG19	BK3_IO21	-	103N	NC	-	-
AK20	BK3_IO22	-	104P	NC	-	-
AJ20	BK3_IO23	-	104N	NC	-	-
AF19	BK3_IO24	-	105P	NC	-	-
AE19	BK3_IO25	-	105N	NC	-	-
AH20	BK3_IO26	-	106P	NC	-	-
-	GND (Bank 3)	-	-	-	-	-
AG20	BK3_IO27	-	106N	NC	-	-
AF20	BK3_IO28	-	107P	NC	-	-
AE20	BK3_IO29	-	107N	NC	-	-
AJ21	BK3_IO30	-	108P	NC	-	-
AK21	BK3_IO31	-	108N	NC	-	-
AG21	BK3_IO32	-	109P	NC	-	-
AF21	BK3_IO33	-	109N	NC	-	-
AK22	BK3_IO34	-	110P	NC	-	-
-	GND (Bank 3)	-	-	-	-	-
AJ22	BK3_IO35	-	110N	NC	-	-
AE21	BK3_IO36	-	111P	NC	-	-
AD21	BK3_IO37	-	111N	NC	-	-
AG22	BK3_IO38	-	112P	NC	-	-
AF22	BK3_IO39	-	112N	NC	-	-
AG23	BK3_IO40	-	113P	BK3_IO22	-	74P
-	-	-	-	GND (Bank 3)	-	-
AH23	BK3_IO41	-	113N	BK3_IO23	-	74N
AJ23	BK3_IO42	-	114P	BK3_IO24	-	75P
-	GND (Bank 3)	-	-	-	-	-
AK23	BK3_IO43	-	114N	BK3_IO25	-	75N
AF23	BK3_IO44	-	115P	BK3_IO26	-	76P
AE23	BK3_IO45	-	115N	BK3_IO27	-	76N
AJ24	BK3_IO46	-	116P	BK3_IO28	-	77P
AK24	BK3_IO47	-	116N	BK3_IO29	-	77N
AH24	BK3_IO48	-	117P	BK3_IO21	-	73N
AG24	BK3_IO49	VREF3	117N	BK3_IO20	VREF3	73P

Part Number Description



1. Discontinued via PCN #03A-10.
2. Select products only. See Ordering Information tables below for specific support.

Ordering Information

Conventional Packaging

Commercial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125B-05F256C	139K	2.5/3.3	-5	fpBGA	256
LFX125B-04F256C	139K	2.5/3.3	-4	fpBGA	256
LFX125B-03F256C	139K	2.5/3.3	-3	fpBGA	256
LFX125C-04F256C	139K	1.8	-4	fpBGA	256
LFX125C-03F256C	139K	1.8	-3	fpBGA	256
LFX125B-05F516C	139K	2.5/3.3	-5	fpBGA	516
LFX125B-04F516C	139K	2.5/3.3	-4	fpBGA	516
LFX125B-03F516C	139K	2.5/3.3	-3	fpBGA	516
LFX125C-04F516C	139K	1.8	-4	fpBGA	516
LFX125C-03F516C	139K	1.8	-3	fpBGA	516
LFX125B-05FH516C[1]	139K	2.5/3.3	-5	fpBGA	516
LFX125B-04FH516C[1]	139K	2.5/3.3	-4	fpBGA	516
LFX125B-03FH516C[1]	139K	2.5/3.3	-3	fpBGA	516
LFX125C-04FH516C[1]	139K	1.8	-4	fpBGA	516
LFX125C-03FH516C[1]	139K	1.8	-3	fpBGA	516
LFX200B-05F256C	210K	2.5/3.3	-5	fpBGA	256
LFX200B-04F256C	210K	2.5/3.3	-4	fpBGA	256
LFX200B-03F256C	210K	2.5/3.3	-3	fpBGA	256
LFX200C-04F256C	210K	1.8	-4	fpBGA	256
LFX200C-03F256C	210K	1.8	-3	fpBGA	256