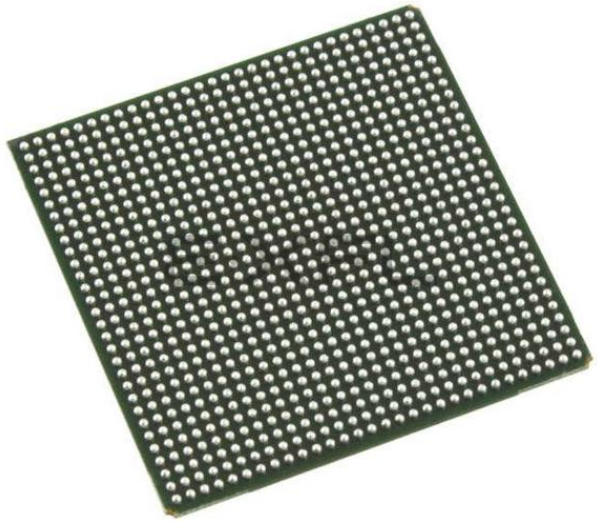
Lattice Semiconductor Corporation - LFX1200EB-03F900C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	15376
Total RAM Bits	423936
Number of I/O	496
Number of Gates	1250000
Voltage - Supply	2.3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx1200eb-03f900c

ispXPGA® Family

Includes High-Performance, Low-Cost "E-Series"

February 2010

Data Sheet DS1026

- **Non-volatile, Infinitely Reconfigurable**
  - Instant-on - Powers up in microseconds via on-chip E²CMOS® based memory
  - No external configuration memory
  - Excellent design security, no bit stream to intercept
  - Reconfigure SRAM based logic in milliseconds
- **High Logic Density for System-level Integration**
  - 139K to 1.25M functional gates
  - 160 to 496 I/O
  - 1.8V, 2.5V, and 3.3V V_{CC} operation
  - Up to 414Kb sysMEM™ embedded memory
- **High Performance Programmable Function Unit (PFU)**
  - Four LUT-4 per PFU supports wide and narrow functions
  - Dual flip-flops per LUT-4 for extensive pipelining
  - Dedicated logic for adders, multipliers, multiplexers, and counters
- **Flexible Memory Resources**
  - Multiple sysMEM Embedded RAM Blocks
    - Single port, Dual port, and FIFO operation
  - 64-bit distributed memory in each PFU
    - Single port, Double port, FIFO, and Shift Register operation
- **Flexible Programming, Reconfiguration, and Testing**
  - Supports IEEE 1532 and 1149.1
  - Microprocessor configuration interface
  - Program E²CMOS while operating from SRAM
- **Eight sysCLOCK™ Phase Locked Loops (PLLs) for Clock Management**
  - True PLL technology
  - 10MHz to 320MHz operation
  - Clock multiplication and division
  - Phase adjustment
  - Shift clocks in 250ps steps
- **sysIO™ for High System Performance**
  - High speed memory support through SSTL and HSTL
  - Advanced buses supported through PCI, GTL+, LVDS, BLVDS, and LVPECL
  - Standard logic supported through LVTTL, LVCMOS 3.3, 2.5 and 1.8
  - 5V tolerant I/O for LVCMOS 3.3 and LVTTL interfaces
  - Programmable drive strength for series termination
  - Programmable bus maintenance
- **Two Options Available**
  - High-performance sysHSI (standard part number)
  - Low-cost, no sysHSI ("E-Series")
- **sysHSI™ Capability for Ultra Fast Serial Communications**
  - Up to 800Mbps performance
  - Up to 20 channels per device
  - Built in Clock Data Recovery (CDR) and Serialization and De-serialization (SERDES)

Table 1. ispXPGA Family Selection Guide

	ispXPGA 125/E	ispXPGA 200/E	ispXPGA 500/E	ispXPGA 1200/E[3]
Functional Gates	139K	210K	476K	1.25M
PFUs	484	676	1764	3844
LUT-4s	1936	2704	7056	15376
Logic FFs	3.8K	5.4K	14.1K	30.7K
sysMEM Memory	92K	111K	184K	414K
Distributed Memory	30K	43K	112K	246K
EBR	20	24	40	90
sysHSI Channels[1]	4	8	12	20
User I/O	160/176	160/208	336	496
Packaging	256 fpBGA 516 fpBGA[2]	256 fpBGA 516 fpBGA[2]	516 fpBGA[2] 900 fpBGA	680 fpSBGA 900 fpBGA

1. "E-Series" does not support sysHSI.
2. FH516 package was converted to F516 via PCN #09A-08.
3. Discontinued via PCN #03A-10.

Architecture Overview

The ispXPGA architecture is a symmetrical architecture consisting of an array of Programmable Function Units (PFUs) enclosed by Input Output Groups (PICs) with columns of sysMEM Embedded Block RAMs (EBRs) distributed throughout the array. Figure 1 illustrates the ispXPGA architecture. Each PIC has two corresponding sysIO blocks, each of which includes one input and output buffer. On two sides of the device, between the PICs and the sysIO blocks, there are sysHSI High-Speed Interface blocks. The symmetrical architecture allows designers to easily implement their designs, since any logic function can be placed in any section of the device.

The PFUs contain the basic building blocks to create logic, memory, arithmetic, and register functions. They are optimized for speed and flexibility allowing complex designs to be implemented quickly and efficiently.

The PICs interface the PFUs and EBRs to the external pins of the device. They allow the signals to be registered quickly to minimize setup times for high-speed designs. They also allow connections directly to the different logic elements for fast access to combinatorial functions.

The sysMEM EBRs are large, fast memory elements that can be configured as RAM, ROM, FIFO, and other storage types. They are designed to facilitate both single and dual-port memory for high-speed applications.

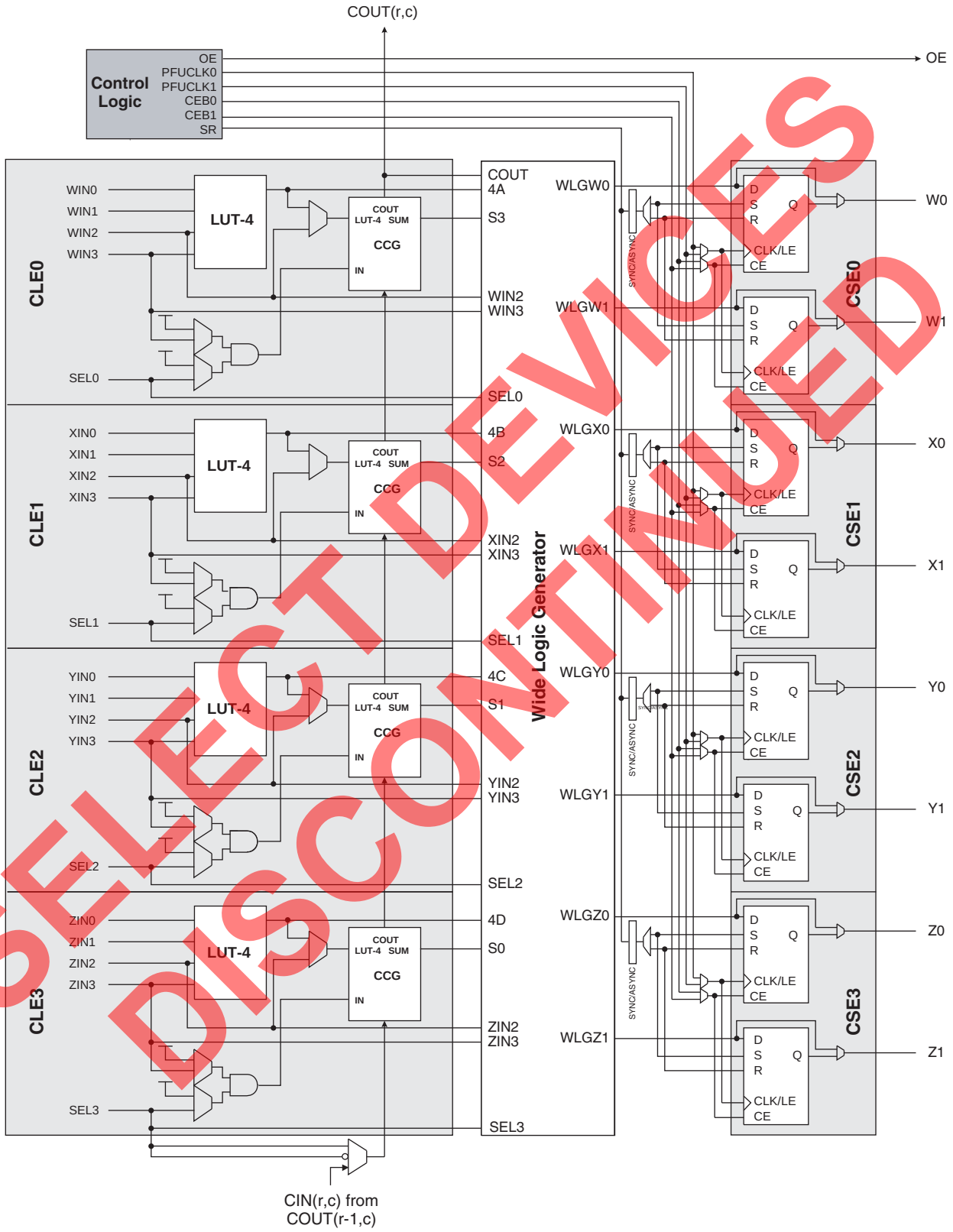
These three components of the architecture are interconnected via a high-speed, flexible routing array. The routing array consists of Variable Length Interconnect (VLI) lines between the PICs, PFUs, and EBRs. There is additional routing available to the PFU for feedback and direct routing of signals to adjacent PFUs or PICs.

The sysIO blocks consist of configurable input and output buffers connected directly to the PICs. These buffers can be configured to interface with 16 different I/O standards. This allows the ispXPGA to interface with other devices without the need for external transceivers.

The sysHSI blocks provide the necessary components to allow the ispXPGA device to transfer data at up to 800Mbps using the LVDS standard. These components include serializing, de-serializing, and clock data recovery (CDR) logic.

The sysCLOCK blocks provide clock multiplication/division, clock distribution, delay compensation, and increased performance through the use of PLL circuitry that manipulates the global clocks. There is one sysCLOCK block for each global clock tree in the device.

Figure 2. ispXPGA PFU



Memory

The ispXPGA architecture provides a large amount of resources for memory intensive applications. Embedded Block RAMs (EBRs) are available to complement the Distributed Memory that is configured in the PFUs (see Look-Up Table -Distributed Memory Mode in the PFU section above). Each memory element can be configured as RAM or ROM. Additionally, the internal logic of the device can be used to configure the memory elements as FIFO and other storage types. These EBRs are referred to as sysMEM blocks. Refer to Table 1 for memory resources per device.

sysMEM Blocks

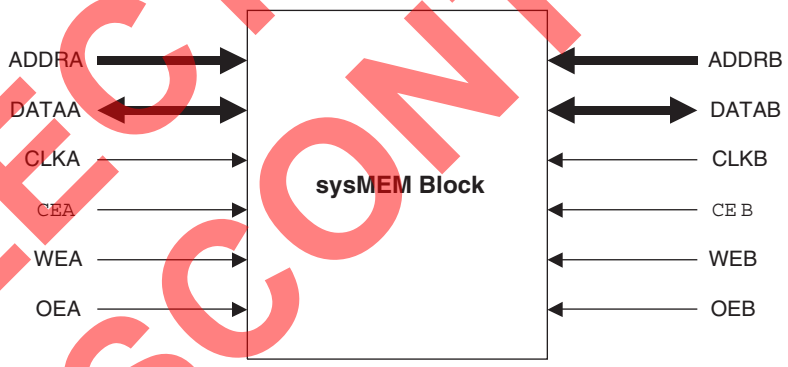
The sysMEM blocks are organized in columns distributed throughout the device. Each EBR contains 4.6K bits of dual-port RAM with dedicated control, address, and data lines for each port. Each column of sysMEM blocks has dedicated address and control lines that can be used by each block separately or cascaded to form larger memory elements. The memory cells are symmetrical and contain two sets of identical control signals. Each port has a read/write clock, clock enable, write enable, and output enable. Figure 12 illustrates the sysMEM block.

The ispXPGA memory block can operate as single-port or dual-port RAM. Supported configurations are:

- 512 x 9 bits single-port (8 bits data / 1 bit parity)
- 256 x 18 bits single-port (16 bits data / 2 bits parity)
- 512 x 9 bits dual-port (8 bits data / 1 bit parity)
- 256 x18 bits dual-port (16 bits data / 2 bits parity)

The data widths of “9” and “18” are ideal for applications where parity is necessary. This allows 9 data bits, 8 data bits plus a parity bit, 18 data bits, or 16 data bits plus two parity bits. The logic for generating and checking the parity must be customized separately.

Figure 12. sysMEM Block Diagram



Read and Write Operations

The ispXPGA EBR has fully synchronous read and write operations as well as an asynchronous read operation. These operations allow several different types of memory to be implemented in the device.

Synchronous Read: The Clock Enable ($\overline{CE}$) and Write Enable (WE) signals control the synchronous read operation. When the $\overline{CE}$ signal is low, the clock is enabled. When the WE signal is low the read operation begins. Once the address (ADDR) is present, a rising clock edge (or falling edge depending on polarity) causes the stored data to be available on the DATA port. Figure 13 illustrates the synchronous read timing.

Absolute Maximum Ratings[1, 2, 3]

	1.8V	2.5V/3.3V
Supply Voltage (V_{CC})	-0.5 to 2.5V	-0.5 to 5.5V
PLL Supply Voltage (V_{CCP})	-0.5 to 2.5V	-0.5 to 5.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V
IEEE 1149.1 TAP Supply Voltage (V_{CCJ})	-0.5 to 4.5V	-0.5 to 4.5V
Input Voltage Applied[4, 5]	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C
Junction Temperature (T_J) with Power Applied	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied (while programming, following the programming specifications).
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to (V_{IH} (MAX) + 2) volts not to exceed 6V is permitted for a duration of <20ns.
5. A maximum of 64 I/Os per device with V_{IN} > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage for 1.8V device[1]	1.65	1.95	V
	Supply Voltage for 2.5V device	2.3	2.7	V
	Supply Voltage for 3.3V device	3.0	3.6	V
V_{CCP}	Supply Voltage for PLL and sysHSI blocks, 1.8V devices[1]	1.65	1.95	V
	Supply Voltage for PLL and sysHSI blocks, 2.5V devices	2.3	2.7	V
	Supply Voltage for PLL and sysHSI blocks, 3.3V devices	3.0	3.6	V
V_{CCJ}	Supply Voltage for IEEE 1149.1 Test Access Port for LVCMOS 1.8V	1.65	1.95	V
	Supply Voltage for IEEE 1149.1 Test Access Port for LVCMOS 2.5V	2.3	2.7	V
	Supply Voltage for IEEE 1149.1 Test Access Port for LVCMOS 3.3V	3.0	3.6	V
T_J (COM)	Junction Temperature Commercial Operation	0	85	C
T_J (IND)	Junction Temperature Industrial Operation	-40	105	C

1. sysHSI specification is valid for V_{CC} and V_{CCP} = 1.7V to 1.9V.

E²CMOS Erase Reprogram Specifications

Parameter	Min	Max	Units
Erase/Reprogram Cycle[1]	1,000	—	Cycles

1. Valid over commercial temperature range.

Hot Socketing Characteristics[1, 2, 3, 4]

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DK}	Input or Tristated I/O Leakage Current	0 ð V_{IN} ð 3.0V	—	+/-50	+/-800	µA

1. Insensitive to sequence of V_{CC} and V_{CCO} when V_{CCO} ð 1.0V. For V_{CCO} > 1.0V, V_{CC} min must be present. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO}, provided (V_{IN} - V_{CCO}) ð 3.6V.
2. LVTTL, LVCMOS only.
3. 0 < V_{CC} ð V_{CC} (MAX), 0 < V_{CCO} ð V_{CCO} (MAX).
4. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until non-volatile cells are active.

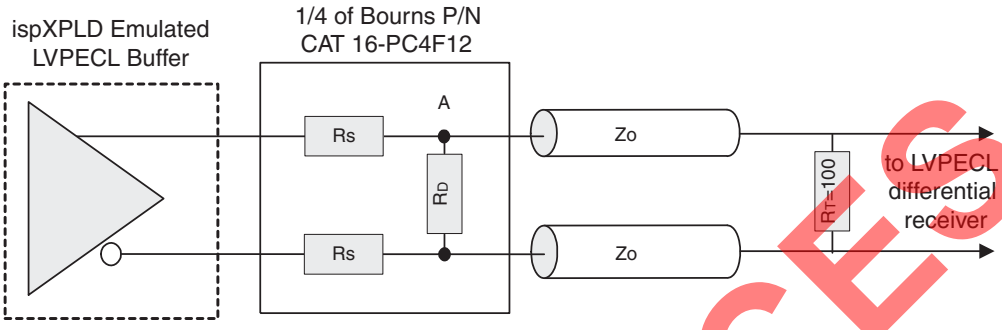
DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{IL}, I_{IH}[1]	Input or I/O Low Leakage	0 ð V_{IN} < (V_{CCO} - 0.2V)	—	—	10	µA
		(V_{CCO} - 0.2V) ð V_{IN} ð 3.6V	—	—	300	µA
I_{IH}[2]	Input High Leakage Current	3.6V < V_{IN} ð 5.5V and 3.0V ð V_{CCO} ð 3.6V	—	—	3	mA
I_{PU}	I/O Active Pull-up Current	0 ð V_{IN} ð 0.7 V_{CCO}	-30	—	-150	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) ð V_{IN} ð V_{IH} (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	V_{IN} = V_{IL} (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	V_{IN} = 0.7 V_{CCO}	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	0 ð V_{IN} ð V_{IH} (MAX)	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive Current	0 ð V_{IN} ð V_{IH} (MAX)	—	—	-150	µA
V_{BHT}	Bus Hold Trip Points		V_{CCO} * 0.35	—	V_{CCO} * 0.65	V
C_1	I/O Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_2	Clock Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_3	Global Input Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. 5V tolerant inputs and I/Os should be placed in banks where 3.0V ð V_{CCO} ð 3.6V. The JTAG and sysCONFIG ports are not included for the 5V tolerant interface.
3. T_A = 25°C, f = 1.0MHz.

Figure 23. LVPECL Driver with Three Resistor Pack



ispXPGA 125B/C & ispXPGA 125EB/EC External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Conditions	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{CO}	Global Clock Input to Output	PIO Output Register	—	5.3	—	5.7	—	6.6	ns
t_{S}	Global Clock Input Setup	PIO Input Register without input delay	-1.9	—	-1.8	—	-1.5	—	ns
t_{H}	Global Clock Input Hold	PIO Input Register without input delay	2.7	—	2.9	—	3.3	—	ns
t_{SINDLY}	Global Clock Input Setup	PIO Input Register with input delay	3.1	—	3.3	—	3.8	—	ns
t_{HINDLY}	Global Clock Input Hold	PIO Input Register with input delay	0.0	—	0.0	—	0.0	—	
t_{COPLL}	Global Clock Input to Output	PIO Output Register using PLL without delay	—	3.6	—	3.9	—	4.5	ns
t_{SPLL}	Global Clock Input Setup	PIO Input Register without input delay using PLL without delay	0	—	0.1	—	0.3	—	ns
t_{HPLL}	Global Clock Input Hold	PIO Input Register without input delay using PLL without delay	0.9	—	1.0	—	1.2	—	ns
$t_{SINDLYPLL}$	Global Clock Input Setup	PIO Input Register with input delay using PLL without delay	5.1	—	5.5	—	6.3	—	ns
$t_{HINDLYPLL}$	Global Clock Input Hold	PIO Input Register with input delay using PLL without delay	-3.0	—	-2.8	—	-2.4	—	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 200B/C & ispXPGA 200EB/EC Timing Adders

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	4.84	—	5.2	—	5.98	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

ispXPGA 200B/C & ispXPGA 200EB/EC Timing Adders (Cont.)

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LVCMOS_33_4mA_out	Using 3.3V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_33_5.33mA_out	Using 3.3V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_33_8mA_out	Using 3.3V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_33_12mA_out	Using 3.3V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_33_16mA_out	Using 3.3V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_33_24mA_out	Using 3.3V CMOS Standard, 24mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_out	Using AGP 1x Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
CTT25_out	Using CTT 2.5V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
CTT33_out	Using CTT 3.3V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
GTL+_out	Using GTL+	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_out	Using HSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_out	Using HSTL 2.5V, Class III	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVDS_out	Using Low Voltage Differential Signaling (LVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
BLVDS_out	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVPECL_out	Using Low Voltage PECL	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
PCI_out	Using PCI Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL2_I_out	Using SSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL2_II_out	Using SSTL 2.5V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_out	Using SSTL 3.3V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL3_II_out	Using SSTL 3.3V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 1200B/C & ispXPGA 1200EB/EC Timing Adders

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	5.58	—	6.0	—	6.90	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

sysHSI Block AC Specifications

Operating Frequency Ranges

Symbol	Description	Mode	Test Condition	Device	-5[1]		-4		-3		Units
					Min.	Max.	Min.	Max.	Min.	Max.	
f_{CLK}	Reference Clock Frequency	SS:CAL		LFX125B/C	50	200	50	200	50	200	MHz
				LFX200B/C	50	188	50	188	50	188	
				LFX500B/C	50	188	50	188	50	188	
				LFX1200B/C	50	175	50	175	50	175	
		10B12B		LFX125B/C	33	67	33	67	33	67	MHz
				LFX200B/C	33	63	33	63	33	63	
				LFX500B/C	33	63	33	63	33	63	
				LFX1200B/C	33	58	33	58	33	58	
		8B10B		LFX125B/C	40	80	40	80	40	80	MHz
				LFX200B/C	40	75	40	75	40	75	
				LFX500B/C	40	75	40	75	40	75	
				LFX1200B/C	40	70	40	70	40	70	
f_{SIN}[2]	Serial Input	SS:CAL	with eoSIN	LFX125B/C	400	800	400	800	400	800	Mbps
				LFX200B/C	400	750	400	750	400	750	
				LFX500B/C	400	750	400	750	400	750	
				LFX1200B/C	400	700	400	700	400	700	
		10B12B	with eoSIN	LFX125B/C	400	800	400	800	400	800	Mbps
				LFX200B/C	400	750	400	750	400	750	
				LFX500B/C	400	750	400	750	400	750	
				LFX1200B/C	400	700	400	700	400	700	
		8B10B	with eoSIN	LFX125B/C	400	800	400	800	400	800	Mbps
				LFX200B/C	400	750	400	750	400	750	
				LFX500B/C	400	750	400	750	400	750	
				LFX1200B/C	400	700	400	700	400	700	
f_{OUT}[2]	Serial Out	LVDS	CL = 5 pF, RL = 100¾ f_{CLK} with no jitter	LFX125B/C	400	800	400	800	400	800	Mbps
				LFX200B/C	400	750	400	750	400	750	
				LFX500B/C	400	750	400	750	400	750	
				LFX1200B/C	400	700	400	700	400	700	

1. Only available for ispXPGA 125B, 200B, 500B and 1200B (2.5V/3.3V) devices.
2. f_{SIN} and f_{SOUT} speeds are supported at V_{CC} and V_{CCP} at 1.7V to 1.9V for ispXPGA 1.8V devices.

LOCKIN Time

Symbol	Description	Mode	Condition	Min	Max	Unit
t_{SCLOCK}	CSPLL Lock Time	All	After input is stabilized		25	µS
$t_{CDRLOCK}$	CDRPLL Lock-in Time	SS	With SS mode sync pattern		1024	t_{RCP}[1]
		10B12B	With 10B12B sync pattern		1024	t_{RCP}
		8B10B	With 8B10B idle pattern		960	t_{RCP}
t_{SYNC}	SyncPat Length	SS		1200		t_{RCP}
t_{CAL}	CAL Duration	SS		1100		t_{RCP}
t_{SUSYNC}	SyncPat Set-up Time to CAL	SS		50		t_{RCP}
t_{HDSYNC}	SyncPat Hold Time from CAL	SS		50		t_{RCP}

1. REFCLK clock period.

ispXPGA Power Supply and NC Connections[1] (Continued)

Signal	680-Ball fpBGA[3]	900-Ball fpBGA[3]
NC[2]	A3, B29, AW3, AV3, AW11, AV11, AV29, AW29, AW37, B3, AV37, C39, C38, AU39, AU38, AJ39, AJ38, N38, N39, C2, C1, AU1, AU2, AJ2, AJ1, N2, N1, B11, A11, A37, B37, A29	**LFX500:** A8, A9, A10, A11, A19, A20, A21, A22, B8, B9, B10, B11, B19, B20, B21, B22, C1, C2, C11, C12, C19, C20, C23, D3, D10, D11, D12, D19, D20, D21, D22, D23, E3, E5, E6, E10, E11, E12, E21, E22, E25, E26, E28, E29, E30, F1, F2, F6, F9, F10, F11, F12, F21, F22, F25, F26, F29, F30, G1, G2, G3, G4, G7, G8, G9, G10, G11, G12, G14, G15, G16, G17, G19, G20, G21, G22, G23, G24, G25, G26, G27, G28, G29, G30, H1, H2, H3, H4, H5, H6, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, H17, H18, H19, H20, H21, H22, H23, H24, H27, H28, H29, H30, J1, J2, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, K6, K7, K8, K9, K10, K12, K13, K14, K15, K16, K17, K18, K19, K21, K22, K23, K24, K25, L7, L8, L9, L22, L23, L24, M7, M8, M9, M10, M21, M22, M23, M24, N8, N9, N10, N21, N22, N23, P7, P8, P9, P10, P21, P22, P23, P24, R8, R9, R10, R21, R22, R23, R24, R25, T6, T7, T8, T9, T10, T21, T22, T23, T24, T25, U7, U8, U9, U10, U21, U22, U23, U24, V8, V9, V10, V21, V22, V23, W7, W8, W9, W10, W21, W22, W23, W24, W25, W26, Y3, Y4, Y5, Y6, Y7, Y8, Y9, Y22, Y23, Y24, Y25, Y26, Y27, Y28, AA4, AA5, AA6, AA7, AA8, AA9, AA10, AA12, AA13, AA14, AA15, AA16, AA17, AA18, AA19, AA21, AA22, AA23, AA24, AA25, AA26, AA27, AB1, AB2, AB4, AB5, AB6, AB7, AB8, AB9, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB18, AB19, AB20, AB21, AB22, AB23, AB24, AB25, AB26, AB27, AC1, AC2, AC3, AC4, AC5, AC6, AC7, AC8, AC9, AC10, AC11, AC12, AC13, AC14, AC15, AC16, AC17' AC18' AC19, AC20, AC21, AC22, AC23, AC24, AC27, AC28, AC29, AC30, AD1, AD2, AD7, AD8, AD9, AD10, AD11, AD12, AD14, AD15, AD16, AD17, AD19, AD20, AD21, AD22, AD23, AD24, AD29, AD30, AE6, AE9, AE10, AE11, AE12, AE19, AE20, AE21, AE22, AE25, AE29, AE30, AF5, AF6, AF10, AF11, AF12, AF19, AF20, AF21, AF22, AF25, AF26, AG10, AG11, AG12, AG19, AG20, AG21, AG22, AH11, AH12, AH19, AH20, AJ8, AJ9, AJ10, AJ11, AJ20, AJ21, AJ22, AK8, AK9, AK10, AK11, AK20, AK21, AK22 **LFX1200:** AA22, AA23, AA24, AA25, AB23, AC24, T21, T22, T23, T24, T25, U21, U22, U23, U24, V21, V22, V23, W21, W22, W23, W24, Y22, Y23, Y24, AA16, AA17, AA18, AA19, AA21, AB16, AB17, AB18, AB19, AB20, AB21, AB22, AC16, AC17, AC18, AC19, AC20, AC21, AC22, AC23, AD16, AD17, AD19, AD20, AD22, AD23, AD24, AE22, AE25, AF25, AF26, AA10, AA12, AA13, AA14, AA15, AB10, AB11, AB12, AB13, AB14, AB15, AB9, AC10, AC11, AC12, AC13, AC14, AC15, AC8, AC9, AD11, AD12, AD14, AD15, AD7, AD8, AD9, AE6, AE9, AF5, AF6, H24, J23, K22, K23, K24, K25, L22, L23, L24, M21, M22, M23, M24, N21, N22, N23, P21, P22, P23, P24, R21, R22, R23, R24, R25, AA6, AA7, AA8, AA9, AB8, AC7, T10, T6, T7, T8, T9, U10, U7, U8, U9, V10, V8, V9, W10, W7, W8, W9, Y7, Y8, Y9, H5, H6, H7, J8, K6, K7, K8, K9, L7, L8, L9, M10, M7, M8, M9, N10, N8, N9, P10, P7, P8, P9, R10, R8, R9, E25, E26, F22, F25, G16, G17, G19, G20, G22, G23, G24, H16, H17, H18, H19, H20, H21, H22, H23, J16, J17, J18, J19, J20, J21, J22, K16, K17, K18, K19, K21, E5, E6, F6, F9, G11, G12, G14, G15, G7, G8, G9, H10, H11, H12, H13, H14, H15, H8, H9, J10, J11, J12, J13, J14, J15, J9, K10, K12, K13, K14, K15

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, V_{CC} or GND.
3. Balls for GND, V_{CC} and V_{CCOx} are connected within the substrate to their respective common signals. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

ispXPGA Logic Signal Connections: 256-Ball fpBGA

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
C2	BK0_IO2	HSI0A_SOUTP	1P/HSI0	BK0_IO0	HSI0A_SOUTP	0P
-	GND (Bank 0)	-	-	-	-	-
D2	BK0_IO3	HSI0A_SOUTN	1N/HSI0	BK0_IO1	HSI0A_SOUTN	0N
B1	BK0_IO6	HSI0A_SINP	3P/HSI0	BK0_IO4	HSI0A_SINP	2P/HSI0
-	-	-	-	GND (Bank 0)	-	-
C1	BK0_IO7	HSI0A_SINN	3N/HSI0	BK0_IO5	HSI0A_SINN	2N/HSI0
D3	BK0_IO8	-	4P/HSI0	BK0_IO6	-	3P/HSI0
E3	BK0_IO9	VREF0	4N/HSI0	BK0_IO7	VREF0	3N/HSI0
D1	BK0_IO10	HSI0B_SOUTP	5P/HSI0	BK0_IO8	HSI0B_SOUTP	4P/HSI0
-	GND (Bank 0)	-	-	-	-	-
E1	BK0_IO11	HSI0B_SOUTN	5N/HSI0	BK0_IO9	HSI0B_SOUTN	4N/HSI0
E2	BK0_IO12	-	6P/HSI0	BK0_IO10	-	5P/HSI0
F2	BK0_IO13	-	6N/HSI0	BK0_IO11	-	5N/HSI0
F1	BK0_IO14	HSI0B_SINP	7P/HSI0	BK0_IO12	HSI0B_SINP	6P/HSI0
-	-	-	-	GND (Bank 0)	-	-
G1	BK0_IO15	HSI0B_SINN	7N/HSI0	BK0_IO13	HSI0B_SINN	6N/HSI0
F3	BK0_IO18	PLL_FBK0	9P	BK0_IO14	PLL_FBK0	7P/HSI0
-	GND (Bank 0)	-	-	-	-	-
G2	BK0_IO19	PLL_RST1	9N	BK0_IO15	PLL_RST1	7N/HSI0
E4	BK0_IO20	-	10P	BK0_IO16	-	8P/HSI0
F4	BK0_IO21	PLL_FBK1	10N	BK0_IO17	PLL_FBK1	8N/HSI0
H1	BK0_IO22	PLL_RST0	11P	BK0_IO18	PLL_RST0	9P
-	-	-	-	GND (Bank 0)	-	-
J1	BK0_IO23	-	11N	BK0_IO19	-	9N
H2	BK0_IO24	CLK_OUT0	12P	BK0_IO20	CLK_OUT0	10P
G3	BK0_IO25	CLK_OUT1	12N	BK0_IO21	CLK_OUT1	10N
-	GND (Bank 0)	-	-	-	-	-
G4	GCLK0	-	LVDS Pair0P	GCLK0	-	LVDS Pair0P
H4	GCLK1	-	LVDS Pair0N	GCLK1	-	LVDS Pair0N
H3	VCCP0	-	-	VCCP0	-	-
J4	GNDP0	-	-	GNDP0	-	-
J2	GCLK2	-	LVDS Pair1P	GCLK2	-	LVDS Pair1P
J3	GCLK3	-	LVDS Pair1N	GCLK3	-	LVDS Pair1N
-	GND (Bank 1)	-	-	-	-	-
H5	BK1_IO0	CLK_OUT2	13P	BK1_IO0	CLK_OUT2	11P
J5	BK1_IO1	CLK_OUT3	13N	BK1_IO1	CLK_OUT3	11N
K1	BK1_IO2	SS_CLKOUT0P	14P	BK1_IO2	SS_CLKOUT0P	12P
-	-	-	-	GND (Bank 1)	-	-
L1	BK1_IO3	SS_CLKOUT0N	14N	BK1_IO3	SS_CLKOUT0N	12N
K4	BK1_IO4	PLL_FBK2	15P	BK1_IO4	PLL_FBK2	13P
L4	BK1_IO5	PLL_FBK3	15N	BK1_IO5	PLL_FBK3	13N
K3	BK1_IO6	SS_CLKIN0P	16P	BK1_IO6	SS_CLKIN0P	14P

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
J29	BK5_IO22	HSI4B_SOUTP	116P/HSI4	NC	-	-	NC	-	-
-	GND (Bank 5)	-	-	-	-	-	-	-	-
H29	BK5_IO23	HSI4B_SOUTN	116N/HSI4	NC	-	-	NC	-	-
F30	BK5_IO24	-	117P/HSI5	NC	-	-	NC	-	-
G29	BK5_IO25	-	117N/HSI5	NC	-	-	NC	-	-
H28	BK5_IO26	HSI5A_SINP	118P/HSI5	NC	-	-	NC	-	-
H27	BK5_IO27	HSI5A_SINN	118N/HSI5	NC	-	-	NC	-	-
E30	BK5_IO28	-	119P/HSI5	NC	-	-	NC	-	-
F29	BK5_IO29	-	119N/HSI5	NC	-	-	NC	-	-
G28	BK5_IO30	HSI5A_SOUTP	120P/HSI5	NC	-	-	NC	-	-
-	GND (Bank 5)	-	-	-	-	-	-	-	-
G27	BK5_IO31	HSI5A_SOUTN	120N/HSI5	NC	-	-	NC	-	-
E29	BK5_IO32	VREF5	121P/HSI5	BK5_IO16	VREF5	73P/HSI3	BK5_IO14	VREF5	62P/HSI1
F28	BK5_IO33	-	121N/HSI5	BK5_IO17	-	73N/HSI3	BK5_IO15	-	62N/HSI1
D30	BK5_IO34	HSI5B_SINP	122P/HSI5	BK5_IO18	HSI3B_SINP	74P/HSI3	BK5_IO16	HSI1B_SINP	63P/HSI1
-	-	-	-	-	-	-	GND (Bank 5)	-	-
C30	BK5_IO35	HSI5B_SINN	122N/HSI5	BK5_IO19	HSI3B_SINN	74N/HSI3	BK5_IO17	HSI1B_SINN	63N/HSI1
D29	BK5_IO36	-	123P/HSI5	BK5_IO20		75P/HSI3	NC	-	-
D28	BK5_IO37	-	123N/HSI5	BK5_IO21		75N/HSI3	NC	-	-
E28	BK5_IO38	HSI5B_SOUTP	124P/HSI5	BK5_IO22	HSI3B_SOUTP	76P/HSI3	BK5_IO20	HSI1B_SOUTP	65P/HSI1
-	GND (Bank 5)	-	-	GND (Bank 5)	-	-	-	-	-
E27	BK5_IO39	HSI5B_SOUTN	124N/HSI5	BK5_IO23	HSI3B_SOUTN	76N/HSI3	BK5_IO21	HSI1B_SOUTN	65N/HSI1
C29	BK5_IO40	-	125P	BK5_IO24	-	77P/HSI3	BK5_IO18	-	64P/HSI1
B30	BK5_IO41	-	125N	BK5_IO25	-	77N/HSI3	BK5_IO19	-	64N/HSI1
A29	CFG0	-	-	CFG0	-	-	CFG0	-	-
B28	DONE	-	-	DONE	-	-	DONE	-	-
A28	PROGRAMb	-	-	PROGRAMb	-	-	PROGRAMb	-	-
D26	BK6_IO0	INITb	126P	BK6_IO0	INITb	78P	BK6_IO0	INITb	66P
C27	BK6_IO1	CCLK	126N	BK6_IO1	CCLK	78N	BK6_IO1	CCLK	66N
B27	BK6_IO2	-	127P	BK6_IO2	-	79P	BK6_IO2	-	67P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-	-	-	-
A27	BK6_IO3	-	127N	BK6_IO3	-	79N	BK6_IO3	-	67N
C26	BK6_IO4	CSb	128P	BK6_IO4	CSb	80P	BK6_IO4	CSb	68P
-	-	-	-	-	-	-	GND (Bank 6)	-	-
B26	BK6_IO5	Read	128N	BK6_IO5	Read	80N	BK6_IO5	Read	68N
A26	BK6_IO6	-	129P	NC	-	-	NC	-	-
C25	BK6_IO7	-	129N	NC	-	-	NC	-	-
D24	BK6_IO8	-	130P	NC	-	-	NC	-	-
B25	BK6_IO9	-	130N	NC	-	-	NC	-	-
A25	BK6_IO10	-	131P	NC	-	-	NC	-	-
-	GND (Bank 6)	-	-	-	-	-	-	-	-
C24	BK6_IO11	-	131N	NC	-	-	NC	-	-
D23	BK6_IO12	-	132P	NC	-	-	NC	-	-
B24	BK6_IO13	-	132N	NC	-	-	NC	-	-
C23	BK6_IO14	-	133P	NC	-	-	NC	-	-
A24	BK6_IO15	-	133N	NC	-	-	NC	-	-
C22	BK6_IO16	-	134P	NC	-	-	NC	-	-
B23	BK6_IO17	-	134N	NC	-	-	NC	-	-
B22	BK6_IO18	DATA7	135P	BK6_IO6	DATA7	81P	BK6_IO6	DATA7	69P
-	GND (Bank 6)	-	-	-	-	-	-	-	-
A23	BK6_IO19	DATA6	135N	BK6_IO7	DATA6	81N	BK6_IO7	DATA6	69N

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
Y5	BK6_IO61	-	216N
-	GND (Bank 6)	-	-
-	GND (Bank 7)	-	-
W3	BK7_IO0	-	217P
W1	BK7_IO1	-	217N
W2	BK7_IO2	-	218P
-	GND (Bank 7)	-	-
W4	BK7_IO3	-	218N
V1	BK7_IO4	-	219P
V2	BK7_IO5	-	219N
V3	BK7_IO6	-	220P
V4	BK7_IO7	-	220N
W5	BK7_IO8	-	221P
U1	BK7_IO9	-	221N
U2	BK7_IO10	-	222P
-	GND (Bank 7)	-	-
U3	BK7_IO11	-	222N
U4	BK7_IO12	-	223P
T1	BK7_IO13	-	223N
T2	BK7_IO14	-	224P
T3	BK7_IO15	-	224N
R1	BK7_IO16	-	225P
R2	BK7_IO17	-	225N
T4	BK7_IO18	-	226P
-	GND (Bank 7)	-	-
P1	BK7_IO19	-	226N
P2	BK7_IO20	-	227P
P3	BK7_IO21	-	227N
R4	BK7_IO22	-	228P
T5	BK7_IO23	-	228N
M1	BK7_IO24	-	229P
M2	BK7_IO25	-	229N
N3	BK7_IO26	-	230P
-	GND (Bank 7)	-	-
P4	BK7_IO27	-	230N
L1	BK7_IO28	-	231P
M3	BK7_IO29	-	231N
L2	BK7_IO30	-	232P
N4	BK7_IO31	-	232N
K1	BK7_IO32	-	233P
K2	BK7_IO33	-	233N
P5	BK7_IO34	-	234P
-	GND (Bank 7)	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
D3	BK0_IO0	-	0P	NC	-	-
E3	BK0_IO1	-	0N	NC	-	-
C2	BK0_IO2	-	1P	NC	-	-
-	GND (Bank 0)	-	-	-	-	-
C1	BK0_IO3	-	1N	NC	-	-
E4	BK0_IO4	-	2P	BK0_IO0	-	0P
F5	BK0_IO5	-	2N	BK0_IO1	-	0N
D2	BK0_IO6	HSI0A_SOUTP	3P	BK0_IO2	HSI0A_SOUTP	1P/HSI0
-	-	-	-	GND (Bank 0)	-	-
D1	BK0_IO7	HSI0A_SOUTN	3N	BK0_IO3	HSI0A_SOUTN	1N/HSI0
F4	BK0_IO8	-	4P	BK0_IO4	-	2P/HSI0
F3	BK0_IO9	-	4N	BK0_IO5	-	2N/HSI0
E2	BK0_IO10	HSI0A_SINP	5P/HSI0	BK0_IO6	HSI0A_SINP	3P/HSI0
-	GND (Bank 0)	-	-	-	-	-
E1	BK0_IO11	HSI0A_SINN	5N/HSI0	BK0_IO7	HSI0A_SINN	3N/HSI0
G6	BK0_IO12	VREF0	6P/HSI0	BK0_IO9	VREF0	4N/HSI0
G5	BK0_IO13	-	6N/HSI0	BK0_IO8	-	4P/HSI0
F1	BK0_IO14	HSI0B_SOUTP	7P/HSI0	NC	-	-
F2	BK0_IO15	HSI0B_SOUTN	7N/HSI0	NC	-	-
G4	BK0_IO16	-	8P/HSI0	NC	-	-
G3	BK0_IO17	-	8N/HSI0	NC	-	-
G2	BK0_IO18	HSI0B_SINP	9P/HSI0	NC	-	-
-	GND (Bank 0)	-	-	-	-	-
G1	BK0_IO19	HSI0B_SINN	9N/HSI0	NC	-	-
H3	BK0_IO20	-	10P/HSI0	NC	-	-
H4	BK0_IO21	-	10N/HSI0	NC	-	-
H1	BK0_IO22	HSI1A_SOUTP	11P/HSI0	NC	-	-
H2	BK0_IO23	HSI1A_SOUTN	11N/HSI0	NC	-	-
J7	BK0_IO24	-	12P/HSI0	NC	-	-
J6	BK0_IO25	-	12N/HSI0	NC	-	-
J1	BK0_IO26	HSI1A_SINP	13P/HSI1	NC	-	-
-	GND (Bank 0)	-	-	-	-	-
J2	BK0_IO27	HSI1A_SINN	13N/HSI1	NC	-	-
J4	BK0_IO28	-	14P/HSI1	NC	-	-
J5	BK0_IO29	-	14N/HSI1	NC	-	-
K1	BK0_IO30	HSI1B_SOUTP	15P/HSI1	BK0_IO10	HSI0B_SOUTP	5P/HSI0
-	-	-	-	GND (Bank 0)	-	-
K2	BK0_IO31	HSI1B_SOUTN	15N/HSI1	BK0_IO11	HSI0B_SOUTN	5N/HSI0
K5	BK0_IO32	-	16P/HSI1	BK0_IO12	-	6P/HSI0
K4	BK0_IO33	-	16N/HSI1	BK0_IO13	-	6N/HSI0
L1	BK0_IO34	HSI1B_SINP	17P/HSI1	BK0_IO14	HSI0B_SINP	7P/HSI0
-	GND (Bank 0)	-	-	-	-	-

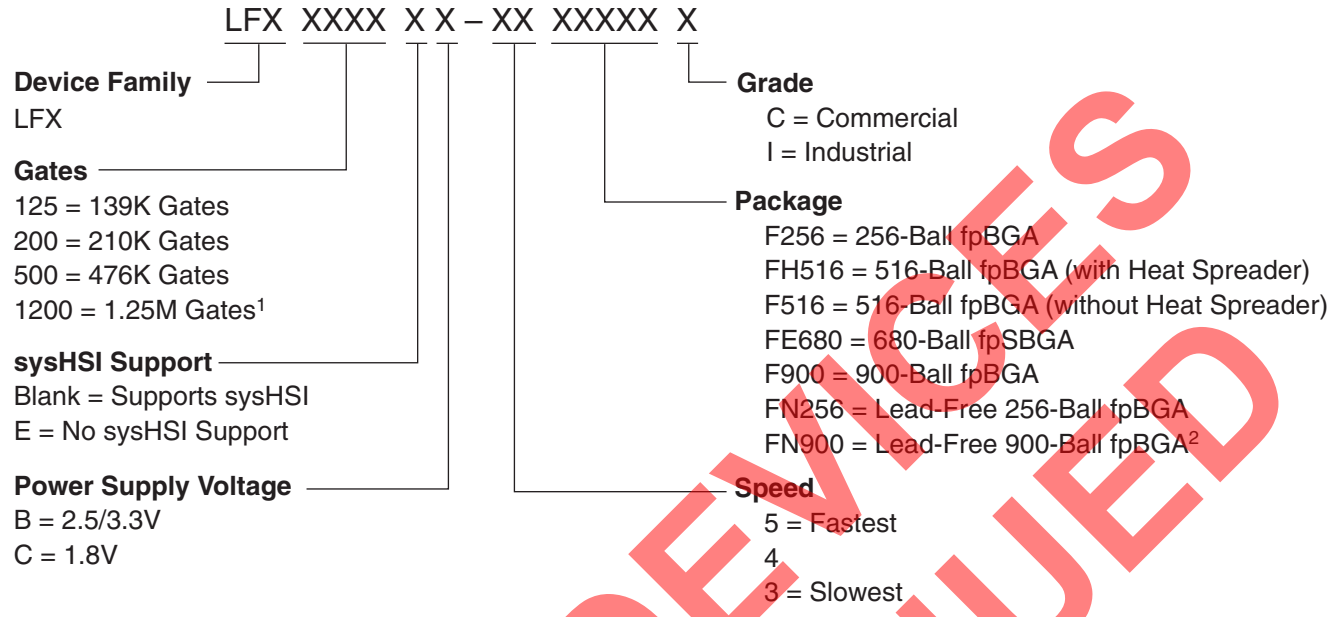
ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
L2	BK0_IO35	HSI1B_SINN	17N/HSI1	BK0_IO15	HSI0B_SINN	7N/HSI0
L6	BK0_IO36	-	18P/HSI1	BK0_IO16	-	8P/HSI0
L5	BK0_IO37	-	18N/HSI1	BK0_IO17	-	8N/HSI0
M1	BK0_IO38	HSI2A_SOUTP	19P/HSI1	BK0_IO18	HSI1A_SOUTP	9P/HSI1
-	-	-	-	GND (Bank 0)	-	-
M2	BK0_IO39	HSI2A_SOUTN	19N/HSI1	BK0_IO19	HSI1A_SOUTN	9N/HSI1
L3	BK0_IO40	-	20P/HSI1	BK0_IO20	-	10P/HSI1
L4	BK0_IO41	-	20N/HSI1	BK0_IO21	-	10N/HSI1
M6	BK0_IO42	HSI2A_SINP	21P/HSI2	BK0_IO22	HSI1A_SINP	11P/HSI1
-	GND (Bank 0)	-	-	-	-	-
M5	BK0_IO43	HSI2A_SINN	21N/HSI2	BK0_IO23	HSI1A_SINN	11N/HSI1
M4	BK0_IO44	-	22P/HSI2	BK0_IO24	-	12P/HSI1
M3	BK0_IO45	-	22N/HSI2	BK0_IO25	-	12N/HSI1
N1	BK0_IO46	HSI2B_SOUTP	23P/HSI2	BK0_IO26	HSI1B_SOUTP	13P/HSI1
-	-	-	-	GND (Bank 0)	-	-
N2	BK0_IO47	HSI2B_SOUTN	23N/HSI2	BK0_IO27	HSI1B_SOUTN	13N/HSI1
N7	BK0_IO48	-	24P/HSI2	BK0_IO28	-	14P/HSI1
N6	BK0_IO49	-	24N/HSI2	BK0_IO29	-	14N/HSI1
P1	BK0_IO50	HSI2B_SINP	25P/HSI2	BK0_IO30	HSI1B_SINP	15P/HSI1
-	GND (Bank 0)	-	-	-	-	-
P2	BK0_IO51	HSI2B_SINN	25N/HSI2	BK0_IO31	HSI1B_SINN	15N/HSI1
N3	BK0_IO52	-	26P/HSI2	BK0_IO32	-	16P/HSI1
N4	BK0_IO53	-	26N/HSI2	BK0_IO33	-	16N/HSI1
P6	BK0_IO54	PLL_RST0	27P/HSI2	BK0_IO38	PLL_RST0	19P
P5	BK0_IO55	PLL_RST1	27N/HSI2	BK0_IO35	PLL_RST1	17N
P3	BK0_IO56	-	28P/HSI2	BK0_IO36	-	18P
P4	BK0_IO57	-	28N/HSI2	BK0_IO39	-	19N
R7	BK0_IO58	PLL_FBK0	29P	BK0_IO34	PLL_FBK0	17P
-	GND (Bank 0)	-	-	GND (Bank 0)	-	-
R6	BK0_IO59	PLL_FBK1	29N	BK0_IO37	PLL_FBK1	18N
R1	BK0_IO60	CLK_OUT0	30P	BK0_IO40	CLK_OUT0	20P
-	-	-	-	GND (Bank 0)	-	-
R2	BK0_IO61	CLK_OUT1	30N	BK0_IO41	CLK_OUT1	20N
-	GND (Bank 0)	-	-	-	-	-
R3	GCLK0	-	LVDS Pair0P	GCLK0	-	LVDS Pair0P
R4	GCLK1	-	LVDS Pair0N	GCLK1	-	LVDS Pair0N
R5	VCCP0	-	-	VCCP0	-	-
T3	GNDP0	-	-	GNDP0	-	-
T4	GCLK2	-	LVDS Pair1P	GCLK2	-	LVDS Pair1P
T5	GCLK3	-	LVDS Pair1N	GCLK3	-	LVDS Pair1N
-	GND (Bank 1)	-	-	-	-	-
T2	BK1_IO0	CLK_OUT2	31P	BK1_IO0	CLK_OUT2	21P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AJ12	BK2_IO43	-	83N	BK2_IO23	-	53N
AD13	BK2_IO44	-	84P	BK2_IO24	-	54P
AE13	BK2_IO45	-	84N	BK2_IO25	-	54N
AK13	BK2_IO46	-	85P	BK2_IO26	-	55P
-	-	-	-	GND (Bank 2)	-	-
AJ13	BK2_IO47	-	85N	BK2_IO27	-	55N
AG13	BK2_IO48	-	86P	BK2_IO28	-	56P
AH13	BK2_IO49	-	86N	BK2_IO29	-	56N
AE14	BK2_IO50	-	87P	BK2_IO30	-	57P
-	GND (Bank 2)	-	-	-	-	-
AF14	BK2_IO51	-	87N	BK2_IO31	-	57N
AG14	BK2_IO52	-	88P	BK2_IO32	-	58P
AH14	BK2_IO53	-	88N	BK2_IO33	-	58N
AJ14	BK2_IO54	-	89P	BK2_IO34	-	59P
-	-	-	-	GND (Bank 2)	-	-
AK14	BK2_IO55	-	89N	BK2_IO35	-	59N
AE15	BK2_IO56	-	90P	BK2_IO36	-	60P
AF15	BK2_IO57	-	90N	BK2_IO37	-	60N
AG15	BK2_IO58	-	91P	BK2_IO38	-	61P
-	GND (Bank 2)	-	-	-	-	-
AH15	BK2_IO59	-	91N	BK2_IO39	-	61N
AJ15	BK2_IO60	-	92P	BK2_IO40	-	62P
AK15	BK2_IO61	-	92N	BK2_IO41	-	62N
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-
AK16	BK3_IO0	-	93P	BK3_IO0	-	63P
AJ16	BK3_IO1	-	93N	BK3_IO1	-	63N
AH16	BK3_IO2	-	94P	BK3_IO2	-	64P
-	GND (Bank 3)	-	-	-	-	-
AG16	BK3_IO3	-	94N	BK3_IO3	-	64N
AF16	BK3_IO4	-	95P	BK3_IO4	-	65P
AE16	BK3_IO5	-	95N	BK3_IO5	-	65N
AK17	BK3_IO6	-	96P	BK3_IO6	-	66P
-	-	-	-	GND (Bank 3)	-	-
AJ17	BK3_IO7	-	96N	BK3_IO7	-	66N
AH17	BK3_IO8	-	97P	BK3_IO8	-	67P
AG17	BK3_IO9	-	97N	BK3_IO9	-	67N
AF17	BK3_IO10	-	98P	BK3_IO10	-	68P
-	GND (Bank 3)	-	-	-	-	-
AE17	BK3_IO11	-	98N	BK3_IO11	-	68N
AH18	BK3_IO12	-	99P	BK3_IO12	-	69P
AG18	BK3_IO13	-	99N	BK3_IO13	-	69N

Part Number Description



1. Discontinued via PCN #03A-10.
2. Select products only. See Ordering Information tables below for specific support.

Ordering Information

Conventional Packaging

Commercial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125B-05F256C	139K	2.5/3.3	-5	fpBGA	256
LFX125B-04F256C	139K	2.5/3.3	-4	fpBGA	256
LFX125B-03F256C	139K	2.5/3.3	-3	fpBGA	256
LFX125C-04F256C	139K	1.8	-4	fpBGA	256
LFX125C-03F256C	139K	1.8	-3	fpBGA	256
LFX125B-05F516C	139K	2.5/3.3	-5	fpBGA	516
LFX125B-04F516C	139K	2.5/3.3	-4	fpBGA	516
LFX125B-03F516C	139K	2.5/3.3	-3	fpBGA	516
LFX125C-04F516C	139K	1.8	-4	fpBGA	516
LFX125C-03F516C	139K	1.8	-3	fpBGA	516
LFX125B-05FH516C[1]	139K	2.5/3.3	-5	fpBGA	516
LFX125B-04FH516C[1]	139K	2.5/3.3	-4	fpBGA	516
LFX125B-03FH516C[1]	139K	2.5/3.3	-3	fpBGA	516
LFX125C-04FH516C[1]	139K	1.8	-4	fpBGA	516
LFX125C-03FH516C[1]	139K	1.8	-3	fpBGA	516
LFX200B-05F256C	210K	2.5/3.3	-5	fpBGA	256
LFX200B-04F256C	210K	2.5/3.3	-4	fpBGA	256
LFX200B-03F256C	210K	2.5/3.3	-3	fpBGA	256
LFX200C-04F256C	210K	1.8	-4	fpBGA	256
LFX200C-03F256C	210K	1.8	-3	fpBGA	256

"E-Series" Commercial (Cont.)

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX500EC-03F900C	476K	1.8	-3	fpBGA	900
LFX1200EB-05F900C[2]	1.25M	2.5/3.3	-5	fpBGA	900
LFX1200EB-04F900C[2]	1.25M	2.5/3.3	-4	fpBGA	900
LFX1200EB-03F900C[2]	1.25M	2.5/3.3	-3	fpBGA	900
LFX1200EC-04F900C[2]	1.25M	1.8	-4	fpBGA	900
LFX1200EC-03F900C[2]	1.25M	1.8	-3	fpBGA	900
LFX1200EB-05FE680C[2]	1.25M	2.5/3.3	-5	fpSBGA	680
LFX1200EB-04FE680C[2]	1.25M	2.5/3.3	-4	fpSBGA	680
LFX1200EB-03FE680C[2]	1.25M	2.5/3.3	-3	fpSBGA	680
LFX1200EC-04FE680C[2]	1.25M	1.8	-4	fpSBGA	680
LFX1200EC-03FE680C[2]	1.25M	1.8	-3	fpSBGA	680

1. FH516 package was converted to F516 via PCN #09A-08.
2. Discontinued via PCN #03A-10.

"E-Series" Industrial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125EB-04F256I	139K	2.5/3.3	-4	fpBGA	256
LFX125EB-03F256I	139K	2.5/3.3	-3	fpBGA	256
LFX125EC-03F256I	139K	1.8	-3	fpBGA	256
LFX125EB-04F516I	139K	2.5/3.3	-4	fpBGA	516
LFX125EB-03F516I	139K	2.5/3.3	-3	fpBGA	516
LFX125EC-03F516I	139K	1.8	-3	fpBGA	516
LFX125EB-04FH516I[1]	139K	2.5/3.3	-4	fpBGA	516
LFX125EB-03FH516I[1]	139K	2.5/3.3	-3	fpBGA	516
LFX125EC-03FH516I[1]	139K	1.8	-3	fpBGA	516
LFX200EB-04F256I	210K	2.5/3.3	-4	fpBGA	256
LFX200EB-03F256I	210K	2.5/3.3	-3	fpBGA	256
LFX200EC-03F256I	210K	1.8	-3	fpBGA	256
LFX200EB-04F516I	210K	2.5/3.3	-4	fpBGA	516
LFX200EB-03F516I	210K	2.5/3.3	-3	fpBGA	516
LFX200EC-03F516I	210K	1.8	-3	fpBGA	516
LFX200EB-04FH516I[1]	210K	2.5/3.3	-4	fpBGA	516
LFX200EB-03FH516I[1]	210K	2.5/3.3	-3	fpBGA	516
LFX200EC-03FH516I[1]	210K	1.8	-3	fpBGA	516
LFX500EB-04F516I	476K	2.5/3.3	-4	fpBGA	516
LFX500EB-03F516I	476K	2.5/3.3	-3	fpBGA	516
LFX500EC-03F516I	476K	1.8	-3	fpBGA	516
LFX500EB-04FH516I[1]	476K	2.5/3.3	-4	fpBGA	516
LFX500EB-03FH516I[1]	476K	2.5/3.3	-3	fpBGA	516
LFX500EC-03FH516I[1]	476K	1.8	-3	fpBGA	516
LFX500EB-04F900I	476K	2.5/3.3	-4	fpBGA	900
LFX500EB-03F900I	476K	2.5/3.3	-3	fpBGA	900
LFX500EC-03F900I	476K	1.8	-3	fpBGA	900