Lattice Semiconductor Corporation - LFX1200EB-03FE680I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	15376
Total RAM Bits	423936
Number of I/O	496
Number of Gates	1250000
Voltage - Supply	2.3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	680-LBGA
Supplier Device Package	680-FPSBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx1200eb-03fe680i

Product Line	Ordering Part Number	Product Status	Reference PCN
LFX500EC (Cont'd)	LFX500EC-03F900C	**Discontinued**	PCN#09-10
	LFX500EC-03FN900C		
	LFX500EC-04F900C		
	LFX500EC-04FN900C		
	LFX500EC-03F900I		
	LFX500EC-03FN900I		
LFX1200EB	LFX1200EB-03FE680C	**Discontinued**	PCN#03A-10
	LFX1200EB-04FE680C		
	LFX1200EB-05FE680C		
	LFX1200EB-03FE680I		
	LFX1200EB-04FE680I		
	LFX1200EB-03F900C		
	LFX1200EB-04F900C		
	LFX1200EB-05F900C		
	LFX1200EB-03F900I		
	LFX1200EB-04F900I		
LFX1200EC	LFX1200EC-03FE680C	**Discontinued**	PCN#03A-10
	LFX1200EC-04FE680C		
	LFX1200EC-03FE680I		
	LFX1200EC-03F900C		
	LFX1200EC-04F900C		
	LFX1200EC-03F900I		

5555 N.E. Moore Ct. ● Hillsboro, Oregon 97124-6421 ● Phone (503) 268-8000 ● FAX (503) 268-8347
Internet: http://www.latticesemi.com

Figure 2. ispXPGA PFU

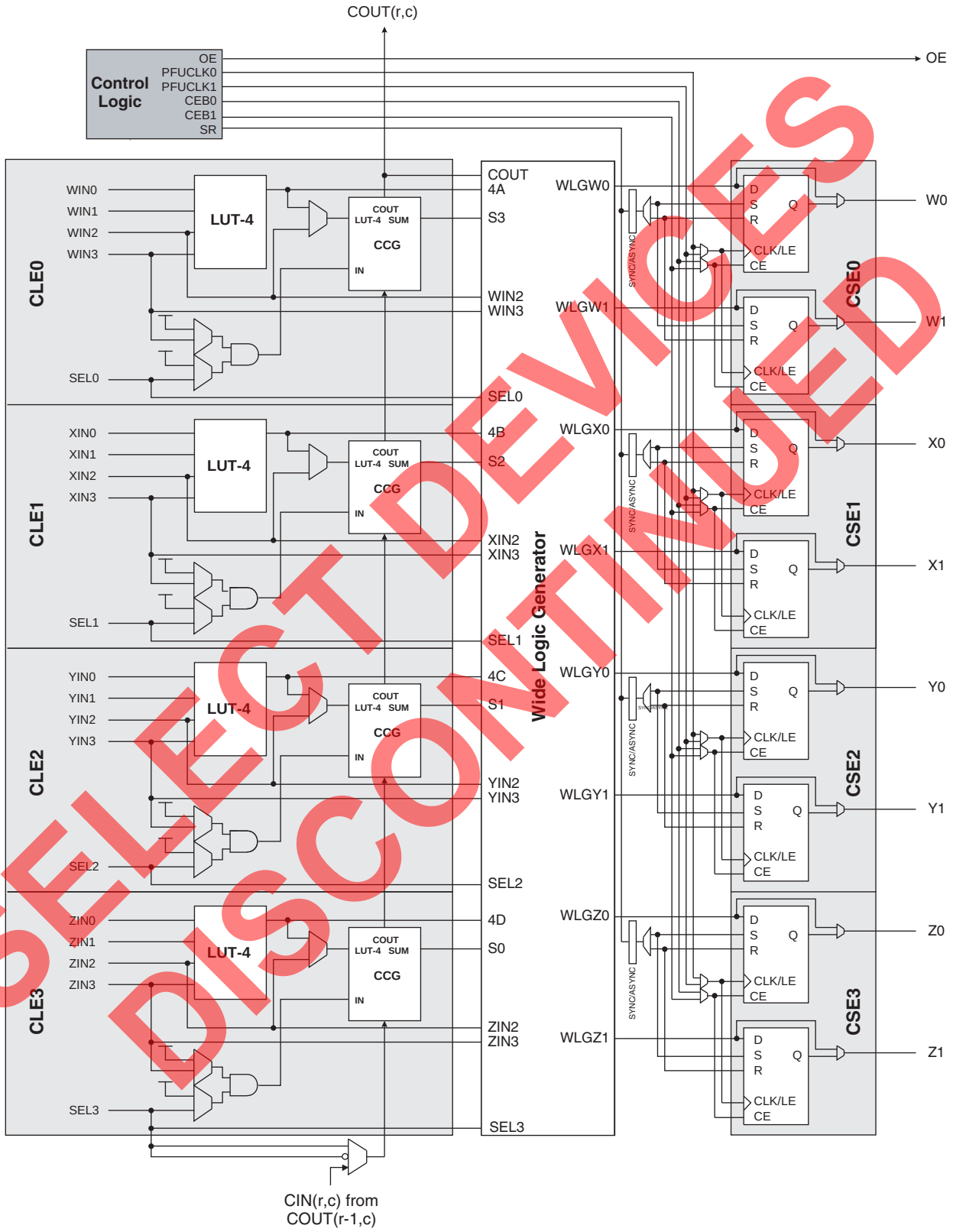
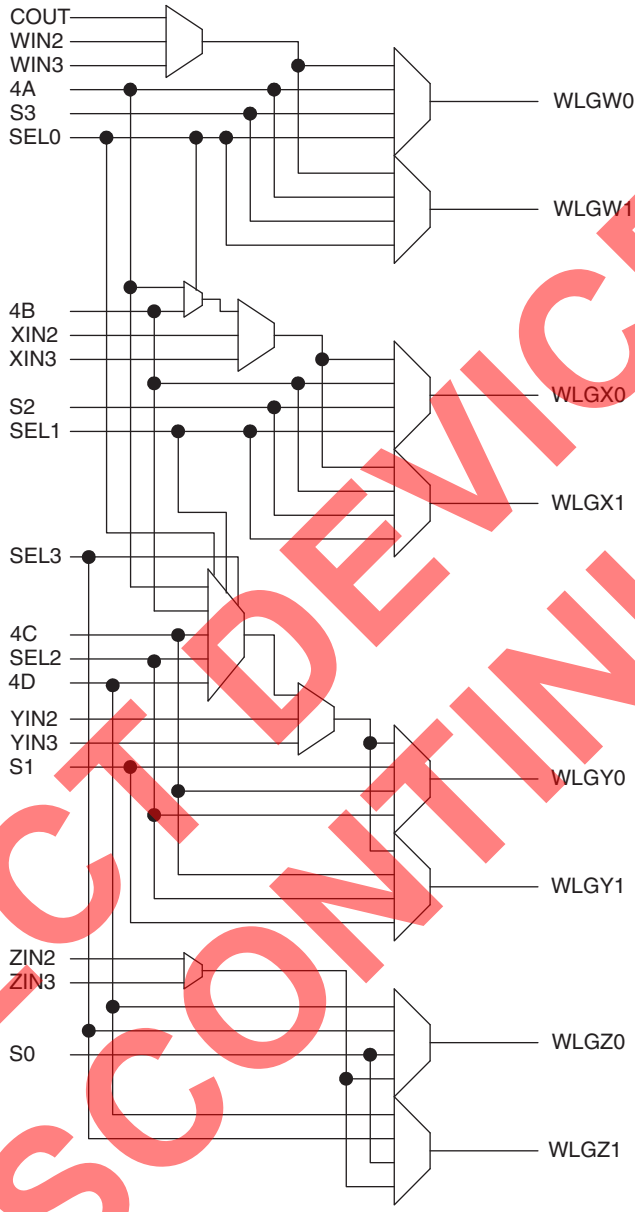


Figure 6. ispXPGA Wide Logic Generator



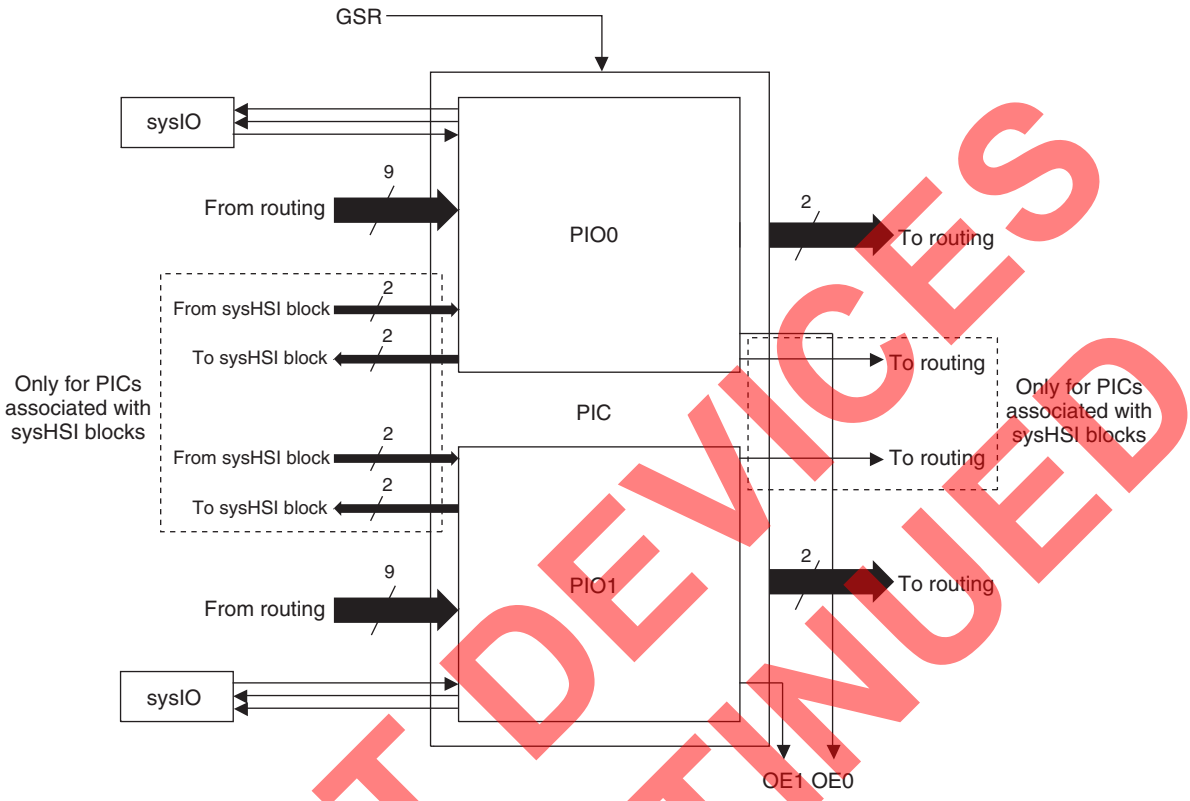
Configurable Sequential Element

There are two registers in each CSE for a total of eight registers in each PFU. This high register count assists in implementing efficient pipelined applications with no utilization penalty. Each register can be configured as a latch or D type flip-flop with either synchronous or asynchronous set or reset. Figure 2 shows the signals that feed the register's D inputs. Feed-through signals in the architecture ensure that registers are efficiently utilized even if the accompanying LUT is occupied.

Control Logic

The control signals available to the registers in a PFU are Clock, Clock Enable, and Set/Reset. Figure 7 shows the various options available to generate the clock signal. As can be seen, the clock signal is the output of a 12:1 MUX with true and compliment versions available from the 12:1 MUX. Each CSE can chose whether it uses the true or complement form of the clock. Figure 8 shows the Set/Reset selection for each PFU in the ispXPGA. A common

Figure 10. ispXPGA PIC



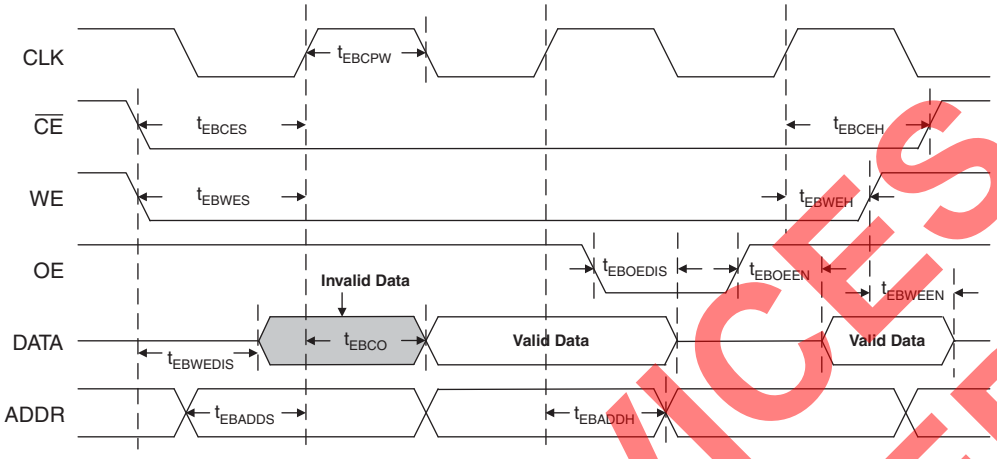
Programmable Input/Output

The PIO is the building block of a PIC. The PIO has a total of 11 inputs and five outputs. Nine of the 11 inputs are generated from routing. The inputs from routing are the PIO Input (IN), Feed-Thru (FT), Clock (CLK), Input Clock Enable (ICE), Input Set/Reset (ISR), Output Clock Enable (OCEN), Output Set/Reset (OSR), PIO Output Enable (OEN), and PIO Input Enable (IEN). The remaining inputs are the sysIO input buffer signal and the Global Set/Reset signal. Three of the five outputs (OUT0, OUT1, and OE) feed routing. The last two outputs feed the sysIO buffer directly as the output and output enable of the sysIO output buffer.

PIOs associated with sysHSI blocks contain two additional inputs and outputs to support the sysHSI block. The two inputs come from the sysHSI block associated with the PIO, and the two outputs feed the sysHSI block. One of the inputs routes directly through the PIO to routing, while the other is multiplexed with the Feed-Thru, register bypass, and Q output of the register to form the OUT1 output of the PIO. The outputs to the sysHSI block are the same signals as the outputs which feed the sysIO buffers (sysIO Output and sysIO Output Enable).

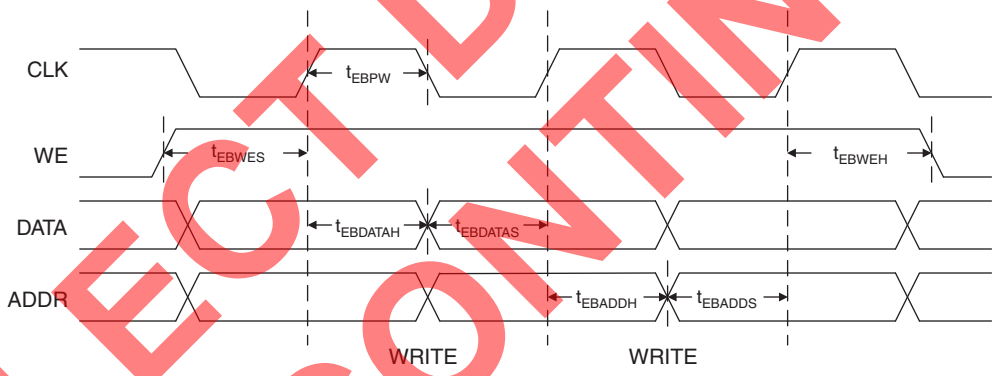
Each PIO has an input register, an output register, and an output enable register as shown in Figure 11. The input register path of the PIO has a 'delay' option, which slows the data-flow. A two-input OR function of the Global Set/Reset (GSR) and Set/Reset (ISR or OSR) signals creates the set/reset term for the respective registers. Each PIO has two pairs of set/reset and clock enable signals. One is exclusive to the input register, whereas the other is common for both the output and output enable registers. The clock (CLK) is common to all registers in a PIO, and the polarity of the clock is controllable. The input, output, and the output enable registers can be configured as a latch or D-type flip-flop. Each PIO is capable of generating an output enable signal, which in turn becomes a PIC output.

Figure 13. EBR Synchronous Read Timing Diagram



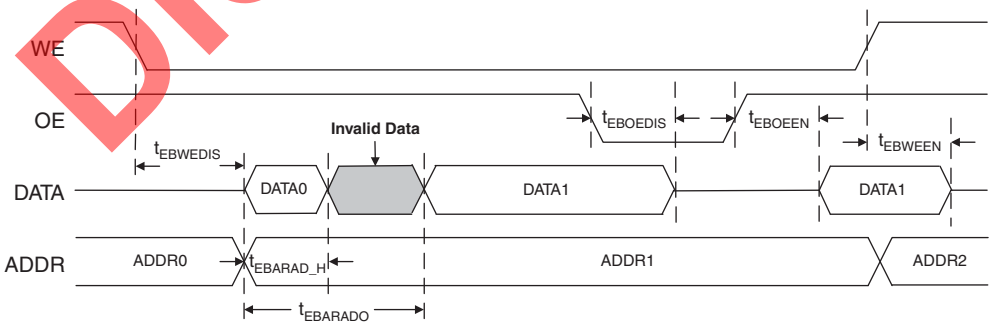
Synchronous Write: The WE signal controls the synchronous write operation. When the WE signal is high, the write operation begins. Once the address and data are present and the Output Enable (OE) is active, a rising clock edge (or falling edge depending on polarity) causes the data to be stored into the EBR. Figure 14 illustrates the synchronous write timing.

Figure 14. EBR Synchronous Write Timing Diagram



Asynchronous Read: The WE signal controls the asynchronous read operation. When the WE signal is low, the read operation begins. Shortly after the address is present, the stored data is available on the DATA port. Figure 15 illustrates the asynchronous read timing. For more information about the EBR, refer to TN1028 ispXPGA Memory Usage Guidelines.

Figure 15. EBR Asynchronous Read Timing Diagram



sysIO Differential Standards DC Electrical Characteristics[1]

Parameter	Description	Test Conditions	Min.	Typ.	Max.
LVDS[2]					
V_{INP}, V_{INM}	Input voltage		0V	—	2.4V
V_{THD}	Differential input threshold	0.2V ð V_{CM} ð 1.8V	+/-100mV	—	—
I_{IN}	Input current	Power on	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	—	1.38V	1.60V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	0.9V	1.03V	—
V_{OD}	Output Voltage Differential	$\|V_{OP} - V_{OM}\|$, R_T = 100 ohm	250mV	350mV	450mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50mV
V_{OS}	Output Voltage Offset	$\|V_{OP} + V_{OM}\|/2$, R_T = 100 ohm	1.125V	1.25V	1.375V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50mV
I_{OSD}	Output short circuit current	V_{OD} = 0V Driver outputs shorted	—	—	24mA
BLVDS[1]					
V_{INP}, V_{INM}	Input voltage		0V	—	2.4V
V_{THD}	Differential input threshold	0.2V ð V_{CM} ð 1.8V	+/-100mV	—	—
I_{IN}	Input current	Power on	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 27Ω	—	1.4V	1.80V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 27Ω	0.95V	1.1V	—
V_{OD}	Output Voltage Differential	$\|V_{OP} - V_{OM}\|$, RT = 27Ω	240mV	300mV	460mV
ΔV_{OD}	Change in V_{OD} Between H and L				27mV
V_{OS}	Output Voltage Offset	$\|V_{OP} + V_{OM}\|$ /2, RT = 27Ω	1.1V	1.3V	1.5V
ΔV_{OS}	Change in V_{OS} Between H and L				27mV
I_{OSD}	Output Short Circuit Current	V_{OD} = 0. Driver Outputs Shorted.		36mA	65mA

1. Refer to TN1000, sysIO Usage Guidelines for Lattice Devices.
2. V_{OP} and V_{OM} are the two outputs of the LVDS/BLVDS output buffer.

LVPECL[1]								
DC Parameter	**Parameter Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
V_{CCO}		**3.0**		**3.3**		**3.6**		**V**
V_{IH}	Input Voltage High	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	Input Voltage Low	0.86	2.125	0.86	2.125	0.86	2.125	V
V_{OH}	Output Voltage High	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	Output Voltage Low	0.96	1.27	1.06	1.43	1.3	1.57	V
V_{DIFF}[2]	Differential Input threshold	0.3	—	0.3	—	0.3	—	V

1. These values are valid at the output of the source termination pack as shown above with 100-ohm differential load only (see Figure 23). The V_{OH} levels are 200mV below the standard LVPECL levels and are compatible with devices tolerant of the lower common mode ranges.
2. Valid for 0.2 ð V_{CM} ð 1.8V.

ispXPGA 125B/C & ispXPGA 125EB/EC PFU Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Set								
t_{LASSRO}	Asynchronous Set/Reset to Output	—	1.09	—	1.17	—	1.35	ns
$t_{LASSRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{LASSRR}	Asynchronous Set/Reset Recovery	—	0.51	—	0.55	—	0.63	ns
t_{LSSR_S}	Synchronous Set/Reset Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{LSSR_H}	Synchronous Set/Reset Hold Time	0.03	—	0.03	—	0.03	—	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.
2. $t_{LCTHRUL}$ quoted bit by bit.

Timing v.0.3

ispXPGA 125B/C & ispXPGA 125EB/EC PIC Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Register/Latch Delays								
t_{IO_CO}	Register Clock to Output Delay	—	0.89	—	0.96	—	1.10	ns
t_{IO_S}	Register Setup Time (Data before Clock)	0.05	—	0.05	—	0.06	—	ns
t_{IO_H}	Register Hold Time (Data after Clock)	0.06	—	0.06	—	0.07	—	ns
t_{IOCE_S}	Register Clock Enable Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{IOCE_H}	Register Clock Enable Hold Time	0.13	—	0.13	—	0.15	—	ns
t_{IO_GO}	Latch Gate to Output Delay	—	0.68	—	0.73	—	0.84	ns
t_{IOL_S}	Latch Setup Time	0.05	—	0.05	—	0.06	—	ns
t_{IOL_H}	Latch Hold Time	0.06	—	0.06	—	0.07	—	ns
t_{IOLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns
t_{IOASRO}	Asynchronous Set/Reset to Output	—	1.00	—	1.08	—	1.24	ns
$t_{IOASRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{IOASRR}	Asynchronous Set/Reset Recovery Time	—	0.23	—	0.25	—	0.29	ns
Input/Output Delays								
t_{IOBUF}	Output Buffer Delay	—	0.97	—	1.04	—	1.20	ns
t_{IOIN}	Input Buffer Delay	—	0.57	—	0.61	—	0.70	ns
t_{IOEN}	Output Enable Delay	—	0.53	—	0.57	—	0.66	ns
t_{IODIS}	Output Disable Delay	—	-0.14	—	-0.13	—	-0.11	ns
t_{IOFT}	Feed-thru Delay	—	0.19	—	0.20	—	0.23	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 500B/C & ispXPGA 500EB/EC External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Conditions	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{CO}	Global Clock Input to Output	PIO Output Register	—	6.4	—	6.9	—	7.9	ns
t_S	Global Clock Input Setup	PIO Input Register without input delay	-2.9	—	-2.7	—	-2.3	—	ns
t_H	Global Clock Input Hold	PIO Input Register without input delay	3.6	—	3.9	—	4.5	—	ns
t_{SINDLY}	Global Clock Input Setup	PIO Input Register with input delay	3.3	—	3.6	—	4.1	—	ns
t_{HINDLY}	Global Clock Input Hold	PIO Input Register with input delay	0.0	—	0.0	—	0.0	—	
t_{COPLL}	Global Clock Input to Output	PIO Output Register using PLL without delay	—	3.2	—	3.4	—	3.9	ns
t_{SPLL}	Global Clock Input Setup	PIO Input Register without input delay using PLL without delay	0.1	—	0.2	—	0.3	—	ns
t_{HPLL}	Global Clock Input Hold	PIO Input Register without input delay using PLL without delay	0.8	—	0.9	—	1.0	—	ns
$t_{SINDLYPLL}$	Global Clock Input Setup	PIO Input Register with input delay using PLL without delay	6.7	—	7.2	—	8.3	—	ns
$t_{HINDLYPLL}$	Global Clock Input Hold	PIO Input Register with input delay using PLL without delay	-4.3	—	-4.0	—	-3.4	—	ns

1. Only available for ispXPGA 500B and ispXPGA 500EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 1200B/C & ispXPGA 1200EB/EC PFU Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Set								
t_{LASSRO}	Asynchronous Set/Reset to Output	—	1.09	—	1.17	—	1.35	ns
$t_{LASSRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{LASSRR}	Asynchronous Set/Reset Recovery	—	0.51	—	0.55	—	0.63	ns
t_{LSSR_S}	Synchronous Set/Reset Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{LSSR_H}	Synchronous Set/Reset Hold Time	0.03	—	0.03	—	0.03	—	ns

1. Only available for ispXPGA 1200B and ispXPGA 1200EB (2.5V/3.3V) devices.
2. $t_{LCTHRUL}$ quoted bit by bit.

Timing v.2.1

ispXPGA 1200B/C & ispXPGA 1200EB/EC PIC Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Register/Latch Delays								
t_{IO_CO}	Register Clock to Output Delay	—	1.01	—	1.09	—	1.25	ns
t_{IO_S}	Register Setup Time (Data before Clock)	0.05	—	0.05	—	0.06	—	ns
t_{IO_H}	Register Hold Time (Data after Clock)	0.06	—	0.06	—	0.07	—	ns
t_{IOCE_S}	Register Clock Enable Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{IOCE_H}	Register Clock Enable Hold Time	0.13		0.13	—	0.15	—	ns
t_{IO_GO}	Latch Gate to Output Delay	—	0.85	—	0.91	—	1.05	ns
t_{IOL_S}	Latch Setup Time	0.05	—	0.05	—	0.06	—	ns
t_{IOL_H}	Latch Hold Time	0.06	—	0.06	—	0.07	—	ns
t_{IOLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns
t_{IOASRO}	Asynchronous Set/Reset to Output	—	1.17	—	1.26	—	1.45	ns
$t_{IOASRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{IOASRR}	Asynchronous Set/Reset Recovery Time	—	0.23	—	0.25	—	0.29	ns
Input/Output Delays								
t_{IOBUF}	Output Buffer Delay	—	0.99	—	1.06	—	1.22	ns
t_{IOIN}	Input Buffer Delay	—	0.71	—	0.76	—	0.87	ns
t_{IOEN}	Output Enable Delay	—	0.52	—	0.56	—	0.64	ns
t_{IODIS}	Output Disable Delay	—	-0.11	—	-0.10	—	-0.09	ns
t_{IOFT}	Feed-thru Delay	—	0.19	—	0.20	—	0.23	ns

1. Only available for ispXPGA 1200B and ispXPGA 1200EB (2.5V/3.3V) devices.

Timing v.2.1

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Units
t_{PWH}	Input clock, high time	80% to 80%	1.2	—	ns
t_{PWL}	Input clock, low time	20% to 20%	1.2	—	ns
t_R, t_F	Input Clock, rise and fall time	20% to 80%	—	3.0	ns
t_{INSTB}	Input clock stability, cycle to cycle (peak)		—	+/- 250	ps
f_{MDIVIN}	M Divider input, frequency range		10	320	MHz
$f_{MDIVOUT}$	M Divider output, frequency range		10	320	MHz
f_{NDIVIN}	N Divider input, frequency range		10	320	MHz
$f_{NDIVOUT}$	N Divider output, frequency range		10	320	MHz
f_{VDIVIN}	V Divider input, frequency range		100	400	MHz
$f_{VDIVOUT}$	V Divider output, frequency range		10	320	MHz
$t_{OUTDUTY}$	output clock, duty cycle		40	60	%
$t_{JIT(CC)}$	Output clock, cycle to cycle jitter (peak)	Clean reference[1] 10MHz ð $f_{MDIVOUT}$ ð 40MHz or 100MHz ð f_{VDIVIN} ð 160MHz	—	+/- 600	ps
		Clean reference[1] 40MHz ð $f_{MDIVOUT}$ ð 320MHz and 160MHz ð f_{VDIVIN} ð 400MHz	—	+/- 150	ps
$t_{JIT(PER)}$[2]	Output clock, period jitter (peak)	Clean reference[1] 10MHz ð $f_{MDIVOUT}$ ð 40MHz or 100MHz ð f_{VDIVIN} ð 160MHz	—	+/- 600	ps
		Clean reference[1] 40MHz ð $f_{MDIVOUT}$ ð 320MHz and 160MHz ð f_{VDIVIN} ð 400MHz	—	+/- 150	ps
$t_{CLK\_OUT\_DELAY}$	Input clock to CLK_OUT delay	Internal feedback	—	3.0	ns
t_{PHASE}	Input clock to external feedback delta	External feedback	—	1.5	ns
t_{LOCK}	Time to acquire phase lock after input stable		—	25	us
t_{PLL_DELAY}	Delay increment (Lead/Lag)	Typical = +/- 250ps	+/- 120	+/- 550	ps
t_{RANGE}	Total output delay range (lead/lag)		+/- 0.84	+/- 3.85	ns
t_{PLL_RSTW}	Minimum reset pulse width		1.8	—	ns
t_{CLK_IN}[3]	Global clock input delay		—	1.0	ns
$t_{PLL\_SEC\_DELAY}$	Secondary PLL output delay		—	1.5	ns

1. This condition assures that the output phase jitter will remain within specifications. Jitter spec is based on optimized M, N and V settings determined by the ispLEVER software.
2. Accumulated jitter measured over 10,000 waveform samples
3. Internal timing for reference only.

Signal Descriptions[1] (Cont.)

Signal Name	Signal Type	Description
HSI*m*A_CDRRST, HSI*m*B_CDRRST	Input	CDR Reset
HSI*m*_CSLOCK, HSI*m*_CSLOCK	Internal Signal	Indicates when the CSPLL circuit is locked
sysHSI Block (Source Synchronous Mode)[6]		
SS_CLKIN0P, SS_CLKIN1P	Input	P-side of differential clock input
SS_CLKIN0N, SS_CLKIN1N	Input	N-side of differential clock input
SS_CLKOUT0P, SS_CLKOUT1P	Output	P-side of differential clock output
SS_CLKOUT0N, SS_CLKOUT1N	Output	N-side of differential clock output
CAL0, CAL1	Input	Initiates source synchronous calibration sequence

1. x is a variable for the I/O number.
2. y is a variable for the I/O Bank.
3. z is a variable for the PLL number.
4. m is a variable for the sysHSI block number.
5. A and B refer to the sysHSI block channels.
6. 0 and 1 refer to Source Synchronous group 0 and 1
7. n is a variable for the GCLK and Input number
8. See Logic Signal Connections Table for differential pairing.

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
C24	BK1_IO7	SS_CLKIN0N	34N
A22	BK1_IO8	-	35P
D22	BK1_IO9	-	35N
A23	BK1_IO10	-	36P
-	GND (Bank 1)	-	-
B25	BK1_IO11	-	36N
D23	BK1_IO12	PLL_RST2	37P
A24	BK1_IO13	PLL_RST3	37N
A25	BK1_IO14	-	38P
E24	BK1_IO15	-	38N
D24	BK1_IO16	-	39P
A26	BK1_IO17	-	39N
D25	BK1_IO18	-	40P
-	GND (Bank 1)	-	-
C25	BK1_IO19	-	40N
B26	BK1_IO20	-	41P/HSI3
B27	BK1_IO21	-	41N/HSI3
D26	BK1_IO22	-	42P/HSI3
A27	BK1_IO23	-	42N/HSI3
A28	BK1_IO24	-	43P/HSI3
E26	BK1_IO25	-	43N/HSI3
C27	BK1_IO26	HSI3A_SOUTP	44P/HSI3
-	GND (Bank 1)	-	-
D27	BK1_IO27	HSI3A_SOUTN	44N/HSI3
B28	BK1_IO28	-	45P/HSI3
A30	BK1_IO29	-	45N/HSI3
C28	BK1_IO30	HSI3A_SINP	46P/HSI3
D28	BK1_IO31	HSI3A_SINN	46N/HSI3
A31	BK1_IO32	-	47P/HSI3
B30	BK1_IO33	-	47N/HSI3
E28	BK1_IO34	HSI3B_SOUTP	48P/HSI3
-	GND (Bank 1)	-	-
D29	BK1_IO35	HSI3B_SOUTN	48N/HSI3
C29	BK1_IO36	-	49P/HSI4
B31	BK1_IO37	-	49N/HSI4
D30	BK1_IO38	HSI3B_SINP	50P/HSI4
E30	BK1_IO39	HSI3B_SINN	50N/HSI4
A32	BK1_IO40	-	51P/HSI4
C31	BK1_IO41	-	51N/HSI4
D31	BK1_IO42	HSI4A_SOUTP	52P/HSI4
-	GND (Bank 1)	-	-
C32	BK1_IO43	HSI4A_SOUTN	52N/HSI4
B32	BK1_IO44	-	53P/HSI4

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
A33	BK1_IO45	-	53N/HSI4
C33	BK1_IO46	HSI4A_SINP	54P/HSI4
B33	BK1_IO47	HSI4A_SINN	54N/HSI4
A34	BK1_IO48	-	55P/HSI4
A35	BK1_IO49	VREF1	55N/HSI4
D32	BK1_IO50	HSI4B_SOUTP	56P/HSI4
-	GND (Bank 1)	-	-
D33	BK1_IO51	HSI4B_SOUTN	56N/HSI4
E32	BK1_IO52	-	57P
C34	BK1_IO53	-	57N
B34	BK1_IO54	HSI4B_SINP	58P
B35	BK1_IO55	HSI4B_SINN	58N
A36	BK1_IO56	-	59P
D34	BK1_IO57	-	59N
C35	BK1_IO58	-	60P
-	GND (Bank 1)	-	-
E34	BK1_IO59	-	60N
B36	BK1_IO60	-	61P
C36	BK1_IO61	-	61N
D39	TCK	-	-
D37	TMS	-	-
D38	TOE	-	-
E37	BK2_IO0	-	62P
F35	BK2_IO1	-	62N
E39	BK2_IO2	-	63P
-	GND (Bank 2)	-	-
F39	BK2_IO3	-	63N
F36	BK2_IO4	-	64P
E38	BK2_IO5	-	64N
G38	BK2_IO6	-	65P
F37	BK2_IO7	-	65N
G36	BK2_IO8	-	66P
G39	BK2_IO9	-	66N
H35	BK2_IO10	-	67P
-	GND (Bank 2)	-	-
F38	BK2_IO11	-	67N
J37	BK2_IO12	VREF2	68P
H36	BK2_IO13	-	68N
G37	BK2_IO14	-	69P
H37	BK2_IO15	-	69N
H39	BK2_IO16	-	70P
K35	BK2_IO17	-	70N
J36	BK2_IO18	-	71P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
AT16	BK5_IO11	HSI7A_SINN	160N/HSI7
AW16	BK5_IO12	-	161P/HSI7
AU16	BK5_IO13	-	161N/HSI7
AV14	BK5_IO14	HSI7A_SOUTP	162P/HSI7
AV15	BK5_IO15	HSI7A_SOUTN	162N/HSI7
AU15	BK5_IO16	-	163P/HSI7
AW15	BK5_IO17	-	163N/HSI7
AT15	BK5_IO18	HSI7B_SINP	164P/HSI7
-	GND (Bank 5)	-	-
AR16	BK5_IO19	HSI7B_SINN	164N/HSI7
AW14	BK5_IO20	-	165P/HSI8
AW13	BK5_IO21	-	165N/HSI8
AR14	BK5_IO22	HSI7B_SOUTP	166P/HSI8
AT14	BK5_IO23	HSI7B_SOUTN	166N/HSI8
AT13	BK5_IO24	-	167P/HSI8
AV13	BK5_IO25	-	167N/HSI8
AU12	BK5_IO26	HSI8A_SINP	168P/HSI8
-	GND (Bank 5)	-	-
AU13	BK5_IO27	HSI8A_SINN	168N/HSI8
AV12	BK5_IO28	-	169P/HSI8
AT12	BK5_IO29	-	169N/HSI8
AR12	BK5_IO30	HSI8A_SOUTP	170P/HSI8
AT11	BK5_IO31	HSI8A_SOUTN	170N/HSI8
AW12	BK5_IO32	-	171P/HSI8
AU11	BK5_IO33	-	171N/HSI8
AV9	BK5_IO34	HSI8B_SINP	172P/HSI8
-	GND (Bank 5)	-	-
AV10	BK5_IO35	HSI8B_SINN	172N/HSI8
AW10	BK5_IO36	-	173P/HSI9
AW9	BK5_IO37	-	173N/HSI9
AT10	BK5_IO38	HSI8B_SOUTP	174P/HSI9
AU9	BK5_IO39	HSI8B_SOUTN	174N/HSI9
AT9	BK5_IO40	-	175P/HSI9
AR10	BK5_IO41	-	175N/HSI9
AU8	BK5_IO42	HSI9A_SINP	176P/HSI9
-	GND (Bank 5)	-	-
AV8	BK5_IO43	HSI9A_SINN	176N/HSI9
AW8	BK5_IO44	-	177P/HSI9
AW7	BK5_IO45	-	177N/HSI9
AU7	BK5_IO46	HSI9A_SOUTP	178P/HSI9
AT8	BK5_IO47	HSI9A_SOUTN	178N/HSI9
AV7	BK5_IO48	-	179P/HSI9
AW6	BK5_IO49	VREF5	179N/HSI9

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AK5	BK2_IO7	-	65N	BK2_IO7	-	45N
AE7	BK2_IO8	-	66P	BK2_IO8	-	46P
AF7	BK2_IO9	-	66N	BK2_IO9	-	46N
AG7	BK2_IO10	-	67P	BK2_IO10	-	47P
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
AH7	BK2_IO11	-	67N	BK2_IO11	-	47N
AE8	BK2_IO12	VREF2	68P	BK2_IO21	VREF2	52N
AF8	BK2_IO13	-	68N	BK2_IO20	-	52P
AJ6	BK2_IO14	-	69P	BK2_IO12	-	48P
AK6	BK2_IO15	-	69N	BK2_IO13	-	48N
AG8	BK2_IO16	-	70P	BK2_IO14	-	49P
AH8	BK2_IO17	-	70N	BK2_IO15	-	49N
AJ7	BK2_IO18	-	71P	BK2_IO16	-	50P
-	GND (Bank 2)	-	-	-	-	-
AK7	BK2_IO19	-	71N	BK2_IO17	-	50N
AF9	BK2_IO20	-	72P	BK2_IO18	-	51P
-	-	-	-	GND (Bank 2)	-	-
AG9	BK2_IO21	-	72N	BK2_IO19	-	51N
AJ8	BK2_IO22	-	73P	NC	-	-
AK8	BK2_IO23	-	73N	NC	-	-
AD10	BK2_IO24	-	74P	NC	-	-
AE10	BK2_IO25	-	74N	NC	-	-
AJ9	BK2_IO26	-	75P	NC	-	-
-	GND (Bank 2)	-	-	-	-	-
AK9	BK2_IO27	-	75N	NC	-	-
AF10	BK2_IO28	-	76P	NC	-	-
AG10	BK2_IO29	-	76N	NC	-	-
AK10	BK2_IO30	-	77P	NC	-	-
AJ10	BK2_IO31	-	77N	NC	-	-
AE11	BK2_IO32	-	78P	NC	-	-
AF11	BK2_IO33	-	78N	NC	-	-
AG11	BK2_IO34	-	79P	NC	-	-
-	GND (Bank 2)	-	-	-	-	-
AH11	BK2_IO35	-	79N	NC	-	-
AE12	BK2_IO36	-	80P	NC	-	-
AF12	BK2_IO37	-	80N	NC	-	-
AJ11	BK2_IO38	-	81P	NC	-	-
AK11	BK2_IO39	-	81N	NC	-	-
AG12	BK2_IO40	-	82P	NC	-	-
AH12	BK2_IO41	-	82N	NC	-	-
AK12	BK2_IO42	-	83P	BK2_IO22	-	53P
-	GND (Bank 2)	-	-	-	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AJ12	BK2_IO43	-	83N	BK2_IO23	-	53N
AD13	BK2_IO44	-	84P	BK2_IO24	-	54P
AE13	BK2_IO45	-	84N	BK2_IO25	-	54N
AK13	BK2_IO46	-	85P	BK2_IO26	-	55P
-	-	-	-	GND (Bank 2)	-	-
AJ13	BK2_IO47	-	85N	BK2_IO27	-	55N
AG13	BK2_IO48	-	86P	BK2_IO28	-	56P
AH13	BK2_IO49	-	86N	BK2_IO29	-	56N
AE14	BK2_IO50	-	87P	BK2_IO30	-	57P
-	GND (Bank 2)	-	-	-	-	-
AF14	BK2_IO51	-	87N	BK2_IO31	-	57N
AG14	BK2_IO52	-	88P	BK2_IO32	-	58P
AH14	BK2_IO53	-	88N	BK2_IO33	-	58N
AJ14	BK2_IO54	-	89P	BK2_IO34	-	59P
-	-	-	-	GND (Bank 2)	-	-
AK14	BK2_IO55	-	89N	BK2_IO35	-	59N
AE15	BK2_IO56	-	90P	BK2_IO36	-	60P
AF15	BK2_IO57	-	90N	BK2_IO37	-	60N
AG15	BK2_IO58	-	91P	BK2_IO38	-	61P
-	GND (Bank 2)	-	-	-	-	-
AH15	BK2_IO59	-	91N	BK2_IO39	-	61N
AJ15	BK2_IO60	-	92P	BK2_IO40	-	62P
AK15	BK2_IO61	-	92N	BK2_IO41	-	62N
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-
AK16	BK3_IO0	-	93P	BK3_IO0	-	63P
AJ16	BK3_IO1	-	93N	BK3_IO1	-	63N
AH16	BK3_IO2	-	94P	BK3_IO2	-	64P
-	GND (Bank 3)	-	-	-	-	-
AG16	BK3_IO3	-	94N	BK3_IO3	-	64N
AF16	BK3_IO4	-	95P	BK3_IO4	-	65P
AE16	BK3_IO5	-	95N	BK3_IO5	-	65N
AK17	BK3_IO6	-	96P	BK3_IO6	-	66P
-	-	-	-	GND (Bank 3)	-	-
AJ17	BK3_IO7	-	96N	BK3_IO7	-	66N
AH17	BK3_IO8	-	97P	BK3_IO8	-	67P
AG17	BK3_IO9	-	97N	BK3_IO9	-	67N
AF17	BK3_IO10	-	98P	BK3_IO10	-	68P
-	GND (Bank 3)	-	-	-	-	-
AE17	BK3_IO11	-	98N	BK3_IO11	-	68N
AH18	BK3_IO12	-	99P	BK3_IO12	-	69P
AG18	BK3_IO13	-	99N	BK3_IO13	-	69N

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
G25	BK5_IO57	-	183N	NC	-	-
F26	BK5_IO58	-	184P	NC	-	-
-	GND (Bank 5)	-	-	-	-	-
E28	BK5_IO59	-	184N	NC	-	-
E27	BK5_IO60	-	185P	BK5_IO40	-	125P
D28	BK5_IO61	-	185N	BK5_IO41	-	125N
C27	CFG0	-	-	CFG0	-	-
B28	DONE	-	-	DONE	-	-
A28	PROGRAMb	-	-	PROGRAMb	-	-
D26	BK6_IO0	INITb	186P	BK6_IO0	INITb	126P
C26	BK6_IO1	CCLK	186N	BK6_IO1	CCLK	126N
B27	BK6_IO2	-	187P	BK6_IO2	-	127P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
A27	BK6_IO3	-	187N	BK6_IO3	-	127N
D25	BK6_IO4	CSb	188P	BK6_IO4	CSb	128P
C25	BK6_IO5	Read	188N	BK6_IO5	READ	128N
B26	BK6_IO6	-	189P	BK6_IO6	-	129P
A26	BK6_IO7	-	189N	BK6_IO7	-	129N
F24	BK6_IO8	-	190P	BK6_IO8	-	130P
E24	BK6_IO9	-	190N	BK6_IO9	-	130N
A25	BK6_IO10	-	191P	BK6_IO10	-	131P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
B25	BK6_IO11	-	191N	BK6_IO11	-	131N
D24	BK6_IO12	VREF6	192P	BK6_IO21	VREF6	136N
C24	BK6_IO13	-	192N	BK6_IO20	-	136P
A24	BK6_IO14	-	193P	BK6_IO12	-	132P
B24	BK6_IO15	-	193N	BK6_IO13	-	132N
F23	BK6_IO16	-	194P	BK6_IO14	-	133P
E23	BK6_IO17	-	194N	BK6_IO15	-	133N
A23	BK6_IO18	-	195P	BK6_IO16	-	134P
-	GND (Bank 6)	-	-	-	-	-
B23	BK6_IO19	-	195N	BK6_IO17	-	134N
C23	BK6_IO20	-	196P	NC	-	-
D23	BK6_IO21	-	196N	NC	-	-
E22	BK6_IO22	-	197P	NC	-	-
D22	BK6_IO23	-	197N	NC	-	-
G21	BK6_IO24	-	198P	NC	-	-
F21	BK6_IO25	-	198N	NC	-	-
B22	BK6_IO26	-	199P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-
A22	BK6_IO27	-	199N	NC	-	-
E21	BK6_IO28	-	200P	NC	-	-

Commercial (Cont.)

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX200B-05F516C	210K	2.5/3.3	-5	fpBGA	516
LFX200B-04F516C	210K	2.5/3.3	-4	fpBGA	516
LFX200B-03F516C	210K	2.5/3.3	-3	fpBGA	516
LFX200C-04F516C	210K	1.8	-4	fpBGA	516
LFX200C-03F516C	210K	1.8	-3	fpBGA	516
LFX200B-05FH516C[1]	210K	2.5/3.3	-5	fpBGA	516
LFX200B-04FH516C[1]	210K	2.5/3.3	-4	fpBGA	516
LFX200B-03FH516C[1]	210K	2.5/3.3	-3	fpBGA	516
LFX200C-04FH516C[1]	210K	1.8	-4	fpBGA	516
LFX200C-03FH516C[1]	210K	1.8	-3	fpBGA	516
LFX500B-05F516C	476K	2.5/3.3	-5	fpBGA	516
LFX500B-04F516C	476K	2.5/3.3	-4	fpBGA	516
LFX500B-03F516C	476K	2.5/3.3	-3	fpBGA	516
LFX500C-04F516C	476K	1.8	-4	fpBGA	516
LFX500C-03F516C	476K	1.8	-3	fpBGA	516
LFX500B-05FH516C[1]	476K	2.5/3.3	-5	fpBGA	516
LFX500B-04FH516C[1]	476K	2.5/3.3	-4	fpBGA	516
LFX500B-03FH516C[1]	476K	2.5/3.3	-3	fpBGA	516
LFX500C-04FH516C[1]	476K	1.8	-4	fpBGA	516
LFX500C-03FH516C[1]	476K	1.8	-3	fpBGA	516
LFX500B-05F900C	476K	2.5/3.3	-5	fpBGA	900
LFX500B-04F900C	476K	2.5/3.3	-4	fpBGA	900
LFX500B-03F900C	476K	2.5/3.3	-3	fpBGA	900
LFX500C-04F900C	476K	1.8	-4	fpBGA	900
LFX500C-03F900C	476K	1.8	-3	fpBGA	900
LFX1200B-05F900C[2]	1.25M	2.5/3.3	-5	fpBGA	900
LFX1200B-04F900C[2]	1.25M	2.5/3.3	-4	fpBGA	900
LFX1200B-03F900C[2]	1.25M	2.5/3.3	-3	fpBGA	900
LFX1200C-04F900C[2]	1.25M	1.8	-4	fpBGA	900
LFX1200C-03F900C[2]	1.25M	1.8	-3	fpBGA	900
LFX1200B-05FE680C[2]	1.25M	2.5/3.3	-5	fpSBGA	680
LFX1200B-04FE680C[2]	1.25M	2.5/3.3	-4	fpSBGA	680
LFX1200B-03FE680C[2]	1.25M	2.5/3.3	-3	fpSBGA	680
LFX1200C-04FE680C[2]	1.25M	1.8	-4	fpSBGA	680
LFX1200C-03FE680C[2]	1.25M	1.8	-3	fpSBGA	680

1. FH516 package was converted to F516 via PCN #09A-08.
2. Discontinued via PCN #03A-10.

"E-Series" Industrial (Cont.)

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX1200EB-04F900I[2]	1.25M	2.5/3.3	-4	fpBGA	900
LFX1200EB-03F900I[2]	1.25M	2.5/3.3	-3	fpBGA	900
LFX1200EC-03F900I[2]	1.25M	1.8	-3	fpBGA	900
LFX1200EB-04FE680I[2]	1.25M	2.5/3.3	-4	fpSBGA	680
LFX1200EB-03FE680I[2]	1.25M	2.5/3.3	-3	fpSBGA	680
LFX1200EC-03FE680I[2]	1.25M	1.8	-3	fpSBGA	680

1. FH516 package was converted to F516 via PCN #09A-08.
2. Discontinued via PCN #03A-10.

Lead-Free Packaging

Commercial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125B-05FN256C	139K	2.5/3.3	-5	Lead-Free fpBGA	256
LFX125B-04FN256C	139K	2.5/3.3	-4	Lead-Free fpBGA	256
LFX125B-03FN256C	139K	2.5/3.3	-3	Lead-Free fpBGA	256
LFX125C-04FN256C	139K	1.8	-4	Lead-Free fpBGA	256
LFX125C-03FN256C	139K	1.8	-3	Lead-Free fpBGA	256
LFX200B-05FN256C	210K	2.5/3.3	-5	Lead-Free fpBGA	256
LFX200B-04FN256C	210K	2.5/3.3	-4	Lead-Free fpBGA	256
LFX200B-03FN256C	210K	2.5/3.3	-3	Lead-Free fpBGA	256
LFX200C-04FN256C	210K	1.8	-4	Lead-Free fpBGA	256
LFX200C-03FN256C	210K	1.8	-3	Lead-Free fpBGA	256
LFX500B-05FN900C	476K	2.5/3.3	-5	Lead-Free fpBGA	900
LFX500B-04FN900C	476K	2.5/3.3	-4	Lead-Free fpBGA	900
LFX500B-03FN900C	476K	2.5/3.3	-3	Lead-Free fpBGA	900
LFX500C-04FN900C	476K	1.8	-4	Lead-Free fpBGA	900
LFX500C-03FN900C	476K	1.8	-3	Lead-Free fpBGA	900

"E-Series" Commercial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125EB-05FN256C	139K	2.5/3.3	-5	Lead-Free fpBGA	256
LFX125EB-04FN256C	139K	2.5/3.3	-4	Lead-Free fpBGA	256
LFX125EB-03FN256C	139K	2.5/3.3	-3	Lead-Free fpBGA	256
LFX125EC-04FN256C	139K	1.8	-4	Lead-Free fpBGA	256
LFX125EC-03FN256C	139K	1.8	-3	Lead-Free fpBGA	256
LFX200EB-05FN256C	210K	2.5/3.3	-5	Lead-Free fpBGA	256
LFX200EB-04FN256C	210K	2.5/3.3	-4	Lead-Free fpBGA	256
LFX200EB-03FN256C	210K	2.5/3.3	-3	Lead-Free fpBGA	256
LFX200EC-04FN256C	210K	1.8	-4	Lead-Free fpBGA	256
LFX200EC-03FN256C	210K	1.8	-3	Lead-Free fpBGA	256
LFX500EB-05FN900C	476K	2.5/3.3	-5	Lead-Free fpBGA	900
LFX500EB-04FN900C	476K	2.5/3.3	-4	Lead-Free fpBGA	900
LFX500EB-03FN900C	476K	2.5/3.3	-3	Lead-Free fpBGA	900

"E-Series" Commercial (Cont.)

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX500EC-04FN900C	476K	1.8	-4	Lead-Free fpBGA	900
LFX500EC-03FN900C	476K	1.8	-3	Lead-Free fpBGA	900

"E-Series" Industrial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125EB-04FN256I	139K	2.5/3.3	-4	Lead-Free fpBGA	256
LFX125EB-03FN256I	139K	2.5/3.3	-3	Lead-Free fpBGA	256
LFX125EC-03FN256I	139K	1.8	-3	Lead-Free fpBGA	256
LFX200EB-04FN256I	210K	2.5/3.3	-4	Lead-Free fpBGA	256
LFX200EB-03FN256I	210K	2.5/3.3	-3	Lead-Free fpBGA	256
LFX200EC-03FN256I	210K	1.8	-3	Lead-Free fpBGA	256
LFX500EB-04FN900I	476K	2.5/3.3	-4	Lead-Free fpBGA	900
LFX500EB-03FN900I	476K	2.5/3.3	-3	Lead-Free fpBGA	900
LFX500EC-03FN900I	476K	1.8	-3	Lead-Free fpBGA	900

For Further Information

In addition to this data sheet, the following Lattice technical notes may be helpful when designing with the ispXPGA Family:

- TN1028, ispXPGA Memory Usage Guidelines
- TN1003, sysCLOCK PLL Usage and Design Guidelines
- TN1000, sysIO Usage Guidelines for Lattice Devices
- TN1026, ispXP Configuration Usage Guidelines
- TN1020, sysHSI Usage Guidelines
- TN1043, Power Estimation in ispXPGA Devices

Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
September 2003	07	Improved typical Icc data for LFX125B/C and LFX500B/C.
		Improved external switching characteristics timing numbers for LFX125B/C.
		Improved PIC timing numbers for LFX125B/C.
		Improved $t_{IOINDLY}$ timing numbers for LFX125B/C.
		Improved external switching characteristics timing numbers for LFX500B/C.
		Improved PIC timing numbers for LFX500B/C.
		Improved $t_{IOINDLY}$ timing numbers for LFX500B/C.
		Enhanced CDR functionality description.
		Logic Signal Connections and Signal Descriptions - removed CDRLOCK, LOSS and EXLOSS descriptions.
January 2004	07.1	Added lead-free package designators.
June 2004	08.0	Updated CDR specifications and reference notes. Removed Source Synchronous (SS:No CAL) mode references for the sysHSI blocks.
		Revised Figures 16 and 24 for clarification.
		Clarification of VCC sysHSI Block for 1.8V devices.
		Updated IIL and IIH max specification.
		Updated LVTTL and PCI 3.3 to support 5V tolerance.