



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	15376
Total RAM Bits	423936
Number of I/O	496
Number of Gates	1250000
Voltage - Supply	2.3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	680-LBGA
Supplier Device Package	680-FPSBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx1200eb-05fe680c

■ Non-volatile, Infinitely Reconfigurable

- Instant-on - Powers up in microseconds via on-chip E²CMOS® based memory
- No external configuration memory
- Excellent design security, no bit stream to intercept
- Reconfigure SRAM based logic in milliseconds

■ High Logic Density for System-level Integration

- 139K to 1.25M functional gates
- 160 to 496 I/O
- 1.8V, 2.5V, and 3.3V V_{CC} operation
- Up to 414Kb sysMEM™ embedded memory

■ High Performance Programmable Function Unit (PFU)

- Four LUT-4 per PFU supports wide and narrow functions
- Dual flip-flops per LUT-4 for extensive pipelining
- Dedicated logic for adders, multipliers, multiplexers, and counters

■ Flexible Memory Resources

- Multiple sysMEM Embedded RAM Blocks
 - Single port, Dual port, and FIFO operation
- 64-bit distributed memory in each PFU
 - Single port, Double port, FIFO, and Shift Register operation

■ Flexible Programming, Reconfiguration, and Testing

- Supports IEEE 1532 and 1149.1

- Microprocessor configuration interface
- Program E²CMOS while operating from SRAM

■ Eight sysCLOCK™ Phase Locked Loops (PLLs) for Clock Management

- True PLL technology
- 10MHz to 320MHz operation
- Clock multiplication and division
- Phase adjustment
- Shift clocks in 250ps steps

■ sysIO™ for High System Performance

- High speed memory support through SSTL and HSTL
- Advanced buses supported through PCI, GTL+, LVDS, BLVDS, and LVPECL
- Standard logic supported through LVTTTL, LVCMOS 3.3, 2.5 and 1.8
- 5V tolerant I/O for LVCMOS 3.3 and LVTTTL interfaces
- Programmable drive strength for series termination
- Programmable bus maintenance

■ Two Options Available

- High-performance sysHSI (standard part number)
- Low-cost, no sysHSI ("E-Series")

■ sysHSI™ Capability for Ultra Fast Serial Communications

- Up to 800Mbps performance
- Up to 20 channels per device
- Built in Clock Data Recovery (CDR) and Serialization and De-serialization (SERDES)

Table 1. ispXPGA Family Selection Guide

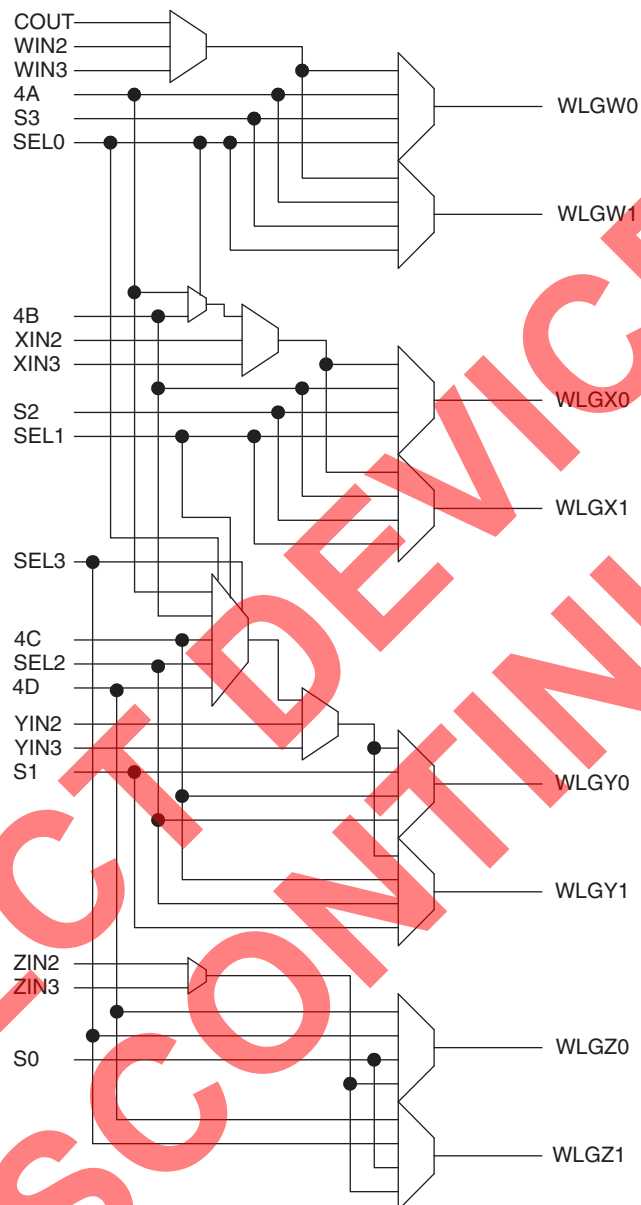
	ispXPGA 125/E	ispXPGA 200/E	ispXPGA 500/E	ispXPGA 1200/E ³
Functional Gates	139K	210K	476K	1.25M
PFUs	484	676	1764	3844
LUT-4s	1936	2704	7056	15376
Logic FFs	3.8K	5.4K	14.1K	30.7K
sysMEM Memory	92K	111K	184K	414K
Distributed Memory	30K	43K	112K	246K
EBR	20	24	40	90
sysHSI Channels ¹	4	8	12	20
User I/O	160/176	160/208	336	496
Packaging	256 fpBGA 516 fpBGA ²	256 fpBGA 516 fpBGA ²	516 fpBGA ² 900 fpBGA	680 fpSBGA 900 fpBGA

1. "E-Series" does not support sysHSI.

2. FH516 package was converted to F516 via [PCN #09A-08](#).

3. Discontinued via [PCN #03A-10](#).

Figure 6. ispXPGA Wide Logic Generator

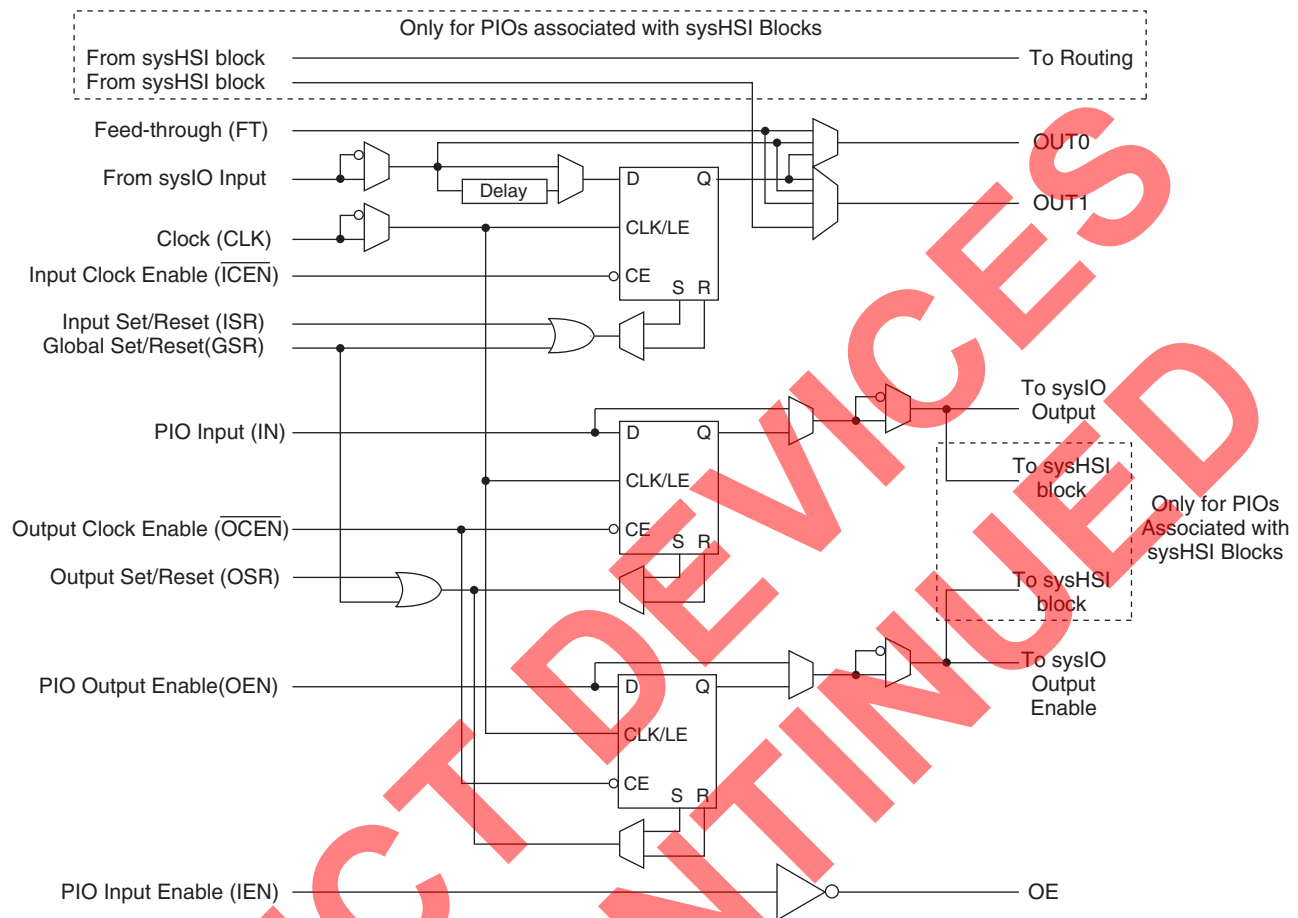


Configurable Sequential Element

There are two registers in each CSE for a total of eight registers in each PFU. This high register count assists in implementing efficient pipelined applications with no utilization penalty. Each register can be configured as a latch or D type flip-flop with either synchronous or asynchronous set or reset. Figure 2 shows the signals that feed the register's D inputs. Feed-through signals in the architecture ensure that registers are efficiently utilized even if the accompanying LUT is occupied.

Control Logic

The control signals available to the registers in a PFU are Clock, Clock Enable, and Set/Reset. Figure 7 shows the various options available to generate the clock signal. As can be seen, the clock signal is the output of a 12:1 MUX with true and complement versions available from the 12:1 MUX. Each CSE can choose whether it uses the true or complement form of the clock. Figure 8 shows the Set/Reset selection for each PFU in the ispXPGA. A common

Figure 11. ispXPGA PIO

VLI Routing Resources

The ispXPGA architecture contains a Variable-Length-Interconnect (VLI) routing technology connecting the PFUs, PICs, and EBRs in the device. There are four types of routing resources, Global Lines, Long Lines, General Interconnect, and Local Lines forming the global routing structure. This allows a signal to be routed to any element in the device with the optimal delay.

The Global Lines consist of global clock lines and a global set/reset line. These lines are routed to all elements in the device. They are specifically designed for high speed, predictable timing regardless of fan-out. The global clock lines can also be used as dedicated inputs.

The Long Lines consist of Horizontal and Vertical Long Lines (HLL and VLL). The VLL and HLL are tri-statable lines spanning the entire device. These lines allow fast routing for high fan-out nets and general-purpose functions.

The General Interconnect consists of Double and Deca Lines. The Double Lines connect up to three elements (two plus the driving element), while the Deca Lines connect up to eleven elements (ten plus the driving element).

The Local Lines are extremely fast routing paths consisting of Feedback and Direct Connect Lines. The Feedback Lines are internal routing paths from the PFU outputs to the PFU inputs. The Direct Connect Lines connect all adjacent elements.

The Common Interface Block (CIB) provides the link between the logic element (PFU, PIC, or EBR) and the VLI Routing resources. The CIB is a switch matrix that can be programmed to connect virtually any routing resource to any input or output of the logic element.

Memory

The ispXPGA architecture provides a large amount of resources for memory intensive applications. Embedded Block RAMs (EBRs) are available to complement the Distributed Memory that is configured in the PFUs (see Look-Up Table -Distributed Memory Mode in the PPU section above). Each memory element can be configured as RAM or ROM. Additionally, the internal logic of the device can be used to configure the memory elements as FIFO and other storage types. These EBRs are referred to as sysMEM blocks. Refer to Table 1 for memory resources per device.

sysMEM Blocks

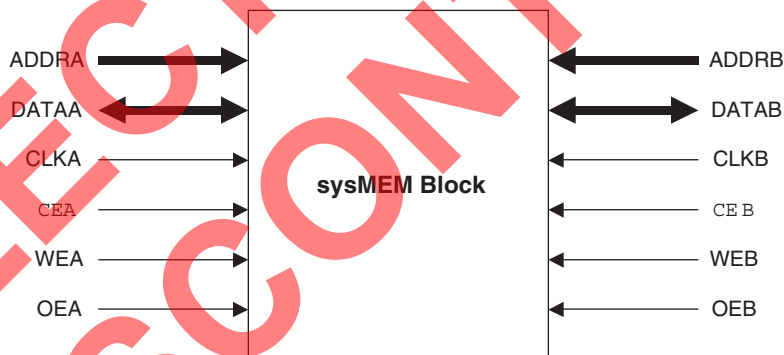
The sysMEM blocks are organized in columns distributed throughout the device. Each EBR contains 4.6K bits of dual-port RAM with dedicated control, address, and data lines for each port. Each column of sysMEM blocks has dedicated address and control lines that can be used by each block separately or cascaded to form larger memory elements. The memory cells are symmetrical and contain two sets of identical control signals. Each port has a read/write clock, clock enable, write enable, and output enable. Figure 12 illustrates the sysMEM block.

The ispXPGA memory block can operate as single-port or dual-port RAM. Supported configurations are:

- 512 x 9 bits single-port (8 bits data / 1 bit parity)
- 256 x 18 bits single-port (16 bits data / 2 bits parity)
- 512 x 9 bits dual-port (8 bits data / 1 bit parity)
- 256 x 18 bits dual-port (16 bits data / 2 bits parity)

The data widths of “9” and “18” are ideal for applications where parity is necessary. This allows 9 data bits, 8 data bits plus a parity bit, 18 data bits, or 16 data bits plus two parity bits. The logic for generating and checking the parity must be customized separately.

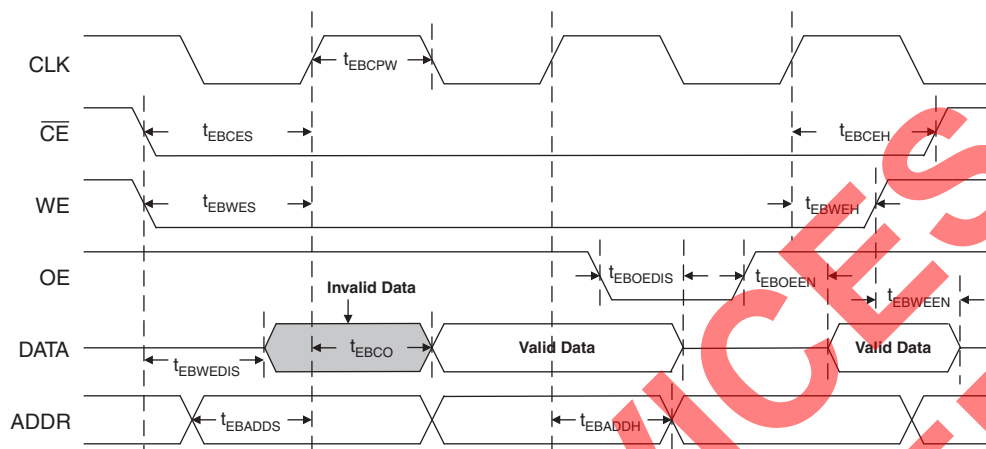
Figure 12. sysMEM Block Diagram



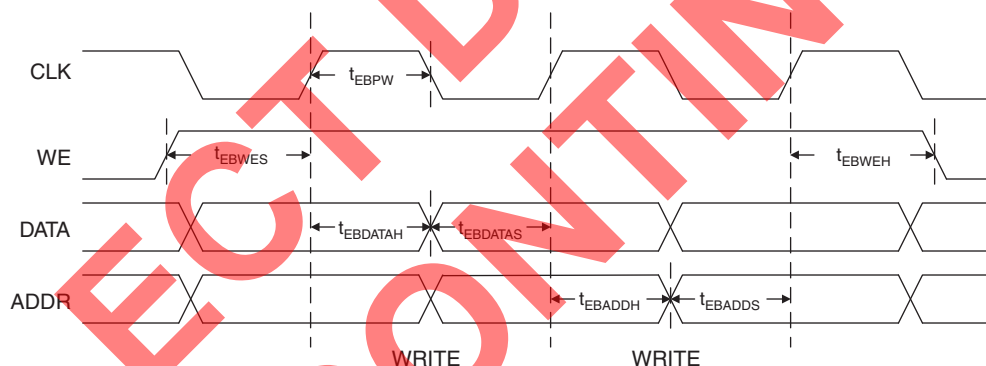
Read and Write Operations

The ispXPGA EBR has fully synchronous read and write operations as well as an asynchronous read operation. These operations allow several different types of memory to be implemented in the device.

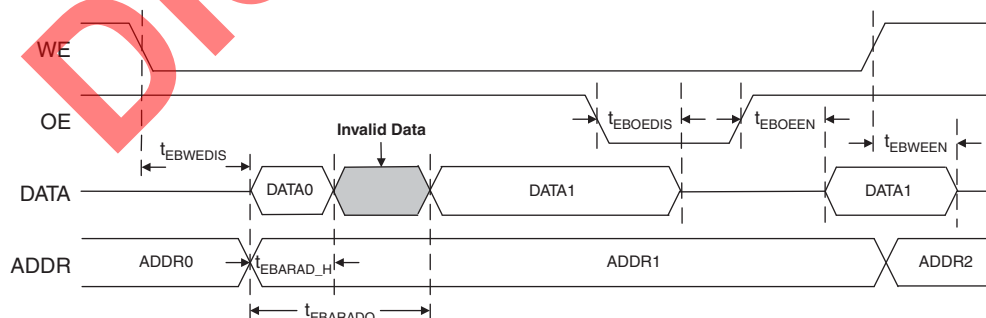
Synchronous Read: The Clock Enable ($\overline{CE}$) and Write Enable (WE) signals control the synchronous read operation. When the $\overline{CE}$ signal is low, the clock is enabled. When the WE signal is low the read operation begins. Once the address (ADDR) is present, a rising clock edge (or falling edge depending on polarity) causes the stored data to be available on the DATA port. Figure 13 illustrates the synchronous read timing.

Figure 13. EBR Synchronous Read Timing Diagram

Synchronous Write: The WE signal controls the synchronous write operation. When the WE signal is high, the write operation begins. Once the address and data are present and the Output Enable (OE) is active, a rising clock edge (or falling edge depending on polarity) causes the data to be stored into the EBR. Figure 14 illustrates the synchronous write timing.

Figure 14. EBR Synchronous Write Timing Diagram

Asynchronous Read: The WE signal controls the asynchronous read operation. When the WE signal is low, the read operation begins. Shortly after the address is present, the stored data is available on the DATA port. Figure 15 illustrates the asynchronous read timing. For more information about the EBR, refer to TN1028 [ispXPGA Memory Usage Guidelines](#).

Figure 15. EBR Asynchronous Read Timing Diagram

sysIO DC Electrical Characteristics

Over Recommended Operating Conditions

Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	5.5	0.4	$V_{CCO} - 0.4$	20, 16, 12, 8, 5.33, 4	-20, -16, -12, -8, -5.33, -4
					0.2	$V_{CCO} - 0.2$	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	$V_{CCO} - 0.4$	16, 12, 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	$V_{CCO} - 0.2$	0.1	-0.1
LVCMOS 1.8 ¹	-0.3	0.68 ³	1.07 ³	3.6	0.4	$V_{CCO} - 0.4$	12, 8 ¹ , 5.33, 4	-12, -8 ¹ , -5.33, -4
		0.35 V_{CC}	0.65 V_{CC}		0.2	$V_{CCO} - 0.2$	0.1	-0.1
LVTTTL	-0.3	0.8	2.0	5.5	0.4	$V_{CCO} - 0.4$	4	-4
					0.2	$V_{CCO} - 0.2$	0.1	-0.1
PCI 3.3	-0.3	1.08 ³	1.5 ³	5.5	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
		0.3 V_{CCO}	0.5 V_{CCO}					
AGP-1X	-0.3	1.08 ³	1.5 ³	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
		0.3 V_{CCO}	0.5 V_{CCO}					
SSTL 3 Class I	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.7	$V_{CCO} - 1.1$	8	-8
SSTL 3 Class II	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.5	$V_{CCO} - 0.9$	16	-16
SSTL 2 Class I	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.54	$V_{CCO} - 0.62$	7.6	-7.6
SSTL 2 Class II	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.35	$V_{CCO} - 0.43$	15.2	-15.2
CTT 3.3	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.4$	$V_{REF} + 0.4$	8	-8
CTT 2.5	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.4$	$V_{REF} + 0.4$	8	-8
HSTL Class I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	8	-8
HSTL Class III	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	24	-8
GTL+	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.6	N/A	36	N/A

1. Design tool default setting.
2. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed $n \cdot 8\text{mA}$. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.
3. Applicable for ispXPGA B devices.

ispXPGA 125B/C & ispXPGA 125EB/EC PFU Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5 ¹		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Functional Delays								
LUTs								
t _{LUT4}	4-Input LUT Delay	—	0.41	—	0.44	—	0.51	ns
t _{LUT5}	5-Input LUT Delay	—	0.73	—	0.79	—	0.91	ns
t _{LUT6}	6-Input LUT Delay	—	0.86	—	0.93	—	1.07	ns
Shift Register (LUT)								
t _{LSR_S}	Shift Register Setup Time	-0.64	—	-0.62	—	-0.53	—	ns
t _{LSR_H}	Shift Register Hold Time	0.61	—	0.63	—	0.72	—	ns
t _{LSR_CO}	Shift Register Clock to Output Delay	—	0.70	—	0.75	—	0.86	ns
Arithmetic Functions								
t _{LCTHRUR}	MC (Macro Cell) Carry In to MC Carry Out Delay (Ripple)	—	0.08	—	0.09	—	0.10	ns
t _{LCTHRUL} ²	MC Carry In to MC Carry Out Delay (Look Ahead)	—	0.05	—	0.05	—	0.06	ns
t _{LSTHRU}	MC Sum In to MC Sum Out Delay	—	0.42	—	0.45	—	0.52	ns
t _{LSINCOUT}	MC Sum In to MC Carry Out Delay	—	0.29	—	0.31	—	0.36	ns
t _{LCINSOUTR}	MC Carry In to MC Sum Out Delay (Ripple)	—	0.36	—	0.39	—	0.45	ns
t _{LCINSOUTL}	MC Carry In to MC Sum Out Delay (Look Ahead)	—	0.26	—	0.28	—	0.32	ns
Feed-thru								
t _{LFT}	PFU Feed-Thru Delay	—	0.15	—	0.16	—	0.18	ns
Distributed RAM								
t _{LRAM_CO}	Clock to RAM Output	—	1.24	—	1.33	—	1.53	ns
t _{LRAMAD_S}	Address Setup Time	-0.41	—	-0.40	—	-0.34	—	ns
t _{LRAMD_S}	Data Setup Time	0.21	—	0.22	—	0.25	—	ns
t _{LRAMWE_S}	Write Enable Setup Time	0.45	—	0.46	—	0.53	—	ns
t _{LRAMAD_H}	Address Hold Time	0.58	—	0.60	—	0.69	—	ns
t _{LRAMD_H}	Data Hold Time	0.11	—	0.11	—	0.13	—	ns
t _{LRAMWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
t _{LRAMCPW}	Clock Pulse Width (High or Low)	2.91	—	3.00	—	3.45	—	ns
t _{LRAMADO}	Address to Output Delay	—	0.86	—	0.93	—	1.07	ns
Register/Latch Delays								
Registers								
t _{L_CO}	Register Clock to Output Delay	—	0.58	—	0.62	—	0.71	ns
t _{L_S}	Register Setup Time (Data before Clock)	0.14	—	0.14	—	0.16	—	ns
t _{L_H}	Register Hold Time (Data after Clock)	-0.12	—	-0.12	—	-0.10	—	ns
t _{LCE_S}	Register Clock Enable Setup Time	-0.11	—	-0.11	—	-0.09	—	ns
t _{LCE_H}	Register Clock Enable Hold Time	0.11	—	0.11	—	0.13	—	ns
Latches								
t _{L_GO}	Latch Gate to Output Delay	—	0.09	—	0.10	—	0.12	ns
t _{LL_S}	Latch Setup Time	0.14	—	0.14	—	0.16	—	ns
t _{LL_H}	Latch Hold Time	-0.12	—	-0.12	—	-0.10	—	ns
t _{LLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns

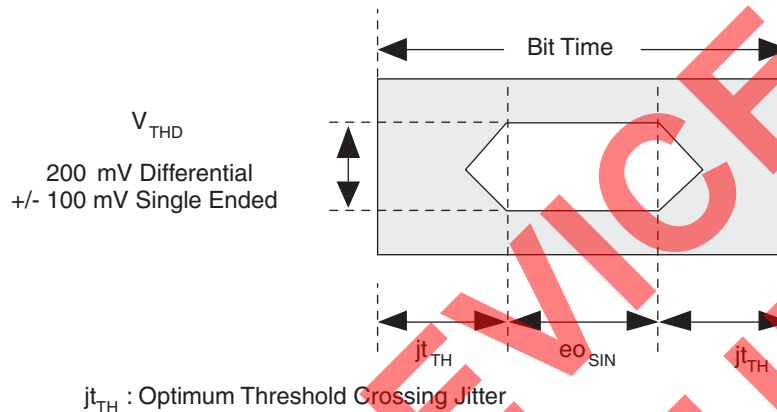
ispXPGA 200B/C & ispXPGA 200EB/EC Timing Adders

Parameter	Description	Base Parameter	-5 ¹		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
t _{IOINDLY}	Input Delay	—	—	4.84	—	5.2	—	5.98	ns
t _{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t _{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVC MOS_18_in	Using 1.8V CMOS	t _{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVC MOS_25_in	Using 2.5V CMOS	t _{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVC MOS_33_in	Using 3.3V CMOS	t _{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t _{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t _{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t _{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t _{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t _{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t _{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t _{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t _{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t _{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t _{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t _{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t _{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t _{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t _{IOIN}	—	0.8	—	0.8	—	0.8	ns
t _{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVC MOS Outputs only)	t _{IOBUF} t _{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVC MOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVC MOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVC MOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVC MOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVC MOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVC MOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVC MOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVC MOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVC MOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.5	—	0.5	—	0.5	ns

sysHSI Block Timing

Figure 24 provides a graphical representation of the SERDES receiver input requirements. It provides guidance on a number of input parameters, including signal amplitude and rise time limits, noise and jitter limits, and P and N input skew tolerance.

Figure 24. Receive Data Eye Diagram Template (Differential)



The data pattern eye opening at the receive end of a link is considered the ultimate measure of received signal quality. Almost all detrimental characteristics of a transmit signal and the interconnection link design result in eye closure. This combined with the eye-opening limitations of the line receiver can provide a good indication of a link's ability to transfer error-free data.

Signal jitter is of special interest to system designers. It is often the primary limiting characteristic of long digital links and of systems with high noise level environments. An interesting characteristic of the clock and data recovery (CDR) portion of the ispXPGA SERDES receiver is its ability to filter incoming signal jitter that is below the clock recovery PLL bandwidth. For signals with high levels of low frequency jitter, the receiver can detect incoming data error free, with eye openings significantly less than that shown in Figure 24.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Units
t_{PWH}	Input clock, high time	80% to 80%	1.2	—	ns
t_{PWL}	Input clock, low time	20% to 20%	1.2	—	ns
t_R, t_F	Input Clock, rise and fall time	20% to 80%	—	3.0	ns
t_{INSTB}	Input clock stability, cycle to cycle (peak)		—	+/- 250	ps
f_{MDIVIN}	M Divider input, frequency range		10	320	MHz
$f_{MDIVOUT}$	M Divider output, frequency range		10	320	MHz
f_{NDIVIN}	N Divider input, frequency range		10	320	MHz
$f_{NDIVOUT}$	N Divider output, frequency range		10	320	MHz
f_{VDIVIN}	V Divider input, frequency range		100	400	MHz
$f_{VDIVOUT}$	V Divider output, frequency range		10	320	MHz
$t_{OUTDUTY}$	output clock, duty cycle		40	60	%
$t_{JIT(CC)}$	Output clock, cycle to cycle jitter (peak)	Clean reference ¹ 10MHz δ $f_{MDIVOUT}$ δ 40MHz or 100MHz δ f_{VDIVIN} δ 160MHz	—	+/- 600	ps
		Clean reference ¹ 40MHz δ $f_{MDIVOUT}$ δ 320MHz and 160MHz δ f_{VDIVIN} δ 400MHz	—	+/- 150	ps
$t_{JIT(PER)}^2$	Output clock, period jitter (peak)	Clean reference ¹ 10MHz δ $f_{MDIVOUT}$ δ 40MHz or 100MHz δ f_{VDIVIN} δ 160MHz	—	+/- 600	ps
		Clean reference ¹ 40MHz δ $f_{MDIVOUT}$ δ 320MHz and 160MHz δ f_{VDIVIN} δ 400MHz	—	+/- 150	ps
$t_{CLK_OUT_DELAY}$	Input clock to CLK_OUT delay	Internal feedback	—	3.0	ns
t_{PHASE}	Input clock to external feedback delta	External feedback	—	1.5	ns
t_{LOCK}	Time to acquire phase lock after input stable		—	25	us
t_{PLL_DELAY}	Delay increment (Lead/Lag)	Typical = +/- 250ps	+/- 120	+/- 550	ps
t_{RANGE}	Total output delay range (lead/lag)		+/- 0.84	+/- 3.85	ns
t_{PLL_RSTW}	Minimum reset pulse width		1.8	—	ns
$t_{CLK_IN}^3$	Global clock input delay		—	1.0	ns
$t_{PLL_SEC_DELAY}$	Secondary PLL output delay		—	1.5	ns

1. This condition assures that the output phase jitter will remain within specifications. Jitter spec is based on optimized M, N and V settings determined by the ispLEVER software.

2. Accumulated jitter measured over 10,000 waveform samples

3. Internal timing for reference only.

ispXPGA Power Supply and NC Connections¹

Signal	256-Ball fpBGA ³	516-Ball fpBGA ³
V _{CC}	C3, C14, D4, D13, E5, E12, F6, F11, L6, L11, M5, M12, N4, N13, P3, P14	A9, A22, D4, D27, J1, J30, L11, L12, L15, L16, L19, L20, M11, M20, R11, R20, T11, T20, W11, W20, Y11, Y12, Y15, Y16, Y19, Y20, AB1, AB30, AG4, AG27, AK9, AK22
V _{CCO0}	F5, G5	F4, J4, M4, N11, P4, P11
V _{CCO1}	K5, L5	U4, U11, V11, W4, AB4, AE4
V _{CCO2}	M6, M7	Y13, Y14, AG6, AG9, AG12, AG14
V _{CCO3}	M10, M11	Y17, Y18, AG17, AG19, AG22, AG25
V _{CCO4}	K12, L12	U20, U27, V20, W27, AB27, AE27
V _{CCO5}	G12, F12	F27, J27, M27, N20, P20, P27
V _{CCO6}	E10, E11	D17, D19, D22, D25, L17, L18
V _{CCO7}	E6, E7	D6, D9, D12, D14, L13, L14
V _{CCP}	H3, J15	R4, T30
V _{CCJ}	A2	C4
GND	A1, A16, B2, B15, F7, F8, F9, F10, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L7, L8, L9, L10, R2, R15, T1, T16	A1, A30, B2, B29, C3, C28, M12, M13, M14, M15, M16, M17, M18, M19, N12, N13, N14, N15, N16, N17, N18, N19, P12, P13, P14, P15, P16, P17, P18, P19, R12, R13, R14, R15, R16, R17, R18, R19, T12, T13, T14, T15, T16, T17, T18, T19, U12, U13, U14, U15, U16, U17, U18, U19, V12, V13, V14, V15, V16, V17, V18, V19, W12, W13, W14, W15, W16, W17, W18, W19, AH3, AH28, AJ2, AJ29, AK1, AK30
GND _P	H15, J4	R29, T4
NC ²	—	LFX125: A10, A13, A16, A17, A24, A25, A26, A4, A5, A6, A7, AA1, AA2, AA28, AA29, AA3, AB28, AC1, AC28, AD1, AD27, AD4, AE28, AE29, AE3, AE30, AF27, AF28, AF29, AF3, AF4, AG1, AG10, AG11, AG15, AG2, AG20, AG23, AG24, AG29, AG3, AG8, AH1, AH15, AH19, AH2, AH20, AH23, AH24, AH30, AH7, AH8, AH9, AJ1, AJ12, AJ14, AJ15, AJ19, AJ20, AJ21, AJ23, AJ24, AJ25, AJ27, AJ30, AJ6, AJ7, AJ8, AK11, AK14, AK15, AK20, AK21, AK23, AK24, AK25, AK27, AK5, AK6, AK7, B10, B13, B16, B17, B18, B23, B24, B25, B5, B6, B7, C11, C13, C14, C16, C17, C22, C23, C24, C25, C6, C7, C8, D11, D16, D23, D24, D28, D29, D3, D7, D8, E30, E4, F1, F29, F30, G1, G2, G27, G28, G29, G30, H1, H2, H27, H28, H29, H30, J2, J28, J29, J3, K1, K2, K27, K28, K3, K4, L1, L2, L27, L3, L4, M1, M2, M29, M3, M30, V27, V28, V3, V4, W1, W30, Y1, Y27, Y28, Y3, Y30 LFX200: A26, A25, A24, A17, A10, A7, A6, A5, A4, B25, B24, B23, B17, B10, B7, B6, B5, C25, C24, C23, C22, C16, C11, C8, C7, C6, D24, D23, D16, D11, D8, D7, E30, F30, F29, F1, G30, G29, G28, G27, G2, G1, H30, H29, H28, H27, H2, H1, J29, J28, J3, J2, K28, K27, K4, K3, K2, K1, L27, L4, L3, L2, L1, M3, V28, V27, V4, V3, W30, W1, Y30, Y28, Y27, Y3, Y1, AA29, AA28, AA3, AA2, AA1, AD27, AD4, AE28, AE3, AF29, AF28, AF27, AF3, AG29, AG24, AG23, AG20, AG11, AG10, AG8, AG2, AG1, AH30, AH24, AH23, AH20, AH9, AH8, AH7, AH2, AH1, AJ30, AJ27, AJ25, AJ24, AJ23, AJ21, AJ15, AJ12, AJ8, AJ7, AJ6, AJ1, AK27, AK25, AK24, AK23, AK21, AK15, AK11, AK7, AK6, AK5

1. All grounds must be electrically connected at the board level.

2. NC pins should not be connected to any active signals, V_{CC} or GND.

3. Balls for GND, V_{CC} and V_{CCOx} are connected within the substrate to their respective common signals. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ²	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ²
C8	BK7_IO1	-	91N	BK7_IO1	-	77N
B8	BK7_IO2	-	92P	BK7_IO2	-	78P
B7	BK7_IO3	-	92N	BK7_IO3	-	78N
A9	BK7_IO6	-	94P	BK7_IO4	-	79P
-	GND (Bank 7)	-	-	-	-	-
A8	BK7_IO7	-	94N	BK7_IO5	-	79N
C7	BK7_IO10	-	96P	BK7_IO6	-	80P
D7	BK7_IO11	-	96N	BK7_IO7	-	80N
D6	BK7_IO12	-	97P	BK7_IO8	-	81P
-	-	-	-	GND (Bank 7)	-	-
C6	BK7_IO13	-	97N	BK7_IO9	-	81N
B6	BK7_IO14	-	98P	BK7_IO10	-	82P
-	GND (Bank 7)	-	-	-	-	-
B5	BK7_IO15	-	98N	BK7_IO11	-	82N
A7	BK7_IO16	VREF7	99P	BK7_IO12	VREF7	83P
A6	BK7_IO17	-	99N	BK7_IO13	-	83N
D5	BK7_IO18	-	100P	BK7_IO14	-	84P
C5	BK7_IO19	-	100N	BK7_IO15	-	84N
A5	BK7_IO20	-	101P	BK7_IO16	-	85P
-	-	-	-	GND (Bank 7)	-	-
A4	BK7_IO21	-	101N	BK7_IO17	-	85N
B4	BK7_IO22	-	102P	BK7_IO18	-	86P
-	GND (Bank 7)	-	-	-	-	-
B3	BK7_IO23	-	102N	BK7_IO19	-	86N
A3	TDO	-	-	TDO	-	-
A2	VCCJ	-	-	VCCJ	-	-
C4	TDI	-	-	TDI	-	-

1. Not available for differential pairs.

2. If a sysHSI Block is used, the indicated sysHSI reserved pins are unavailable for general purpose I/O use.

ispXPGA Logic Signal Connections: 516-Ball fpBGA

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/sysHSI Reserved ¹	Signal Name	Second Function	LVDS Pair/sysHSI Reserved ¹	Signal Name	Second Function	LVDS Pair/sysHSI Reserved ¹
E4	BK0_IO0	-	0P	BK0_IO0	-	0P/HSI0	NC	-	-
D3	BK0_IO1	-	0N	BK0_IO1	-	0N/HSI0	NC	-	-
E3	BK0_IO2	HSI0A_SOUTP	1P/HSI0	BK0_IO2	HSI0A_SOUTP	1P/HSI0	BK0_IO0	HSI0A_SOUTP	0P
-	GND (Bank 0)	-	-	GND (Bank 0)	-	-	-	-	-
F3	BK0_IO3	HSI0A_SOUTN	1N/HSI0	BK0_IO3	HSI0A_SOUTN	1N/HSI0	BK0_IO1	HSI0A_SOUTN	0N
C2	BK0_IO4	-	2P/HSI0	BK0_IO4	-	2P/HSI0	BK0_IO2	-	1P/HSI0
B1	BK0_IO5	-	2N/HSI0	BK0_IO5	-	2N/HSI0	BK0_IO3	-	1N/HSI0
G4	BK0_IO6	HSI0A_SINP	3P/HSI0	BK0_IO6	HSI0A_SINP	3P/HSI0	BK0_IO4	HSI0A_SINP	2P/HSI0
-	-	-	-	-	-	-	GND (Bank 0)	-	-
G3	BK0_IO7	HSI0A_SINN	3N/HSI0	BK0_IO7	HSI0A_SINN	3N/HSI0	BK0_IO5	HSI0A_SINN	2N/HSI0
C1	BK0_IO8	-	4P/HSI0	BK0_IO8	-	4P/HSI0	BK0_IO6	-	3P/HSI0
D2	BK0_IO9	VREF0	4N/HSI0	BK0_IO9	VREF0	4N/HSI0	BK0_IO7	VREF0	3N/HSI0
H4	BK0_IO10	HSI0B_SOUTP	5P/HSI0	BK0_IO10	HSI0B_SOUTP	5P/HSI0	BK0_IO8	HSI0B_SOUTP	4P/HSI0
-	GND (Bank 0)	-	-	GND (Bank 0)	-	-	-	-	-
H3	BK0_IO11	HSI0B_SOUTN	5N/HSI0	BK0_IO11	HSI0B_SOUTN	5N/HSI0	BK0_IO9	HSI0B_SOUTN	4N/HSI0
D1	BK0_IO12	-	6P/HSI0	BK0_IO12	-	6P/HSI0	BK0_IO10	-	5P/HSI0
E1	BK0_IO13	-	6N/HSI0	BK0_IO13	-	6N/HSI0	BK0_IO11	-	5N/HSI0
E2	BK0_IO14	HSI0B_SINP	7P/HSI0	BK0_IO14	HSI0B_SINP	7P/HSI0	BK0_IO12	HSI0B_SINP	6P/HSI0
-	-	-	-	-	-	-	GND (Bank 0)	-	-
F2	BK0_IO15	HSI0B_SINN	7N/HSI0	BK0_IO15	HSI0B_SINN	7N/HSI0	BK0_IO13	HSI0B_SINN	6N/HSI0
G2	BK0_IO16	-	8P/HSI0	NC	-	-	NC	-	-
F1	BK0_IO17	-	8N/HSI0	NC	-	-	NC	-	-
J3	BK0_IO18	HSI1A_SOUTP	9P	NC	-	-	NC	-	-
-	GND (Bank 0)	-	-	-	-	-	-	-	-
K3	BK0_IO19	HSI1A_SOUTN	9N	NC	-	-	NC	-	-
K4	BK0_IO20	-	10P	NC	-	-	NC	-	-
L4	BK0_IO21	-	10N	NC	-	-	NC	-	-
H2	BK0_IO22	HSI1A_SINP	11P	NC	-	-	NC	-	-
J2	BK0_IO23	HSI1A_SINN	11N	NC	-	-	NC	-	-
G1	BK0_IO24	-	12P	NC	-	-	NC	-	-
H1	BK0_IO25	-	12N	NC	-	-	NC	-	-
L3	BK0_IO26	HSI1B_SOUTP	13P	NC	-	-	NC	-	-
-	GND (Bank 0)	-	-	-	-	-	-	-	-
M3	BK0_IO27	HSI1B_SOUTN	13N	NC	-	-	NC	-	-
K2	BK0_IO28	-	14P	NC	-	-	NC	-	-
L2	BK0_IO29	-	14N	NC	-	-	NC	-	-
K1	BK0_IO30	HSI1B_SINP	15P	NC	-	-	NC	-	-
L1	BK0_IO31	HSI1B_SINN	15N	NC	-	-	NC	-	-
M2	BK0_IO32	-	16P	BK0_IO16	-	8P	NC	-	-
M1	BK0_IO33	-	16N	BK0_IO17	-	8N	NC	-	-
N3	BK0_IO34	PLL_FBK0	17P	BK0_IO18	PLL_FBK0	9P	BK0_IO14	PLL_FBK0	7P/HSI0
-	GND (Bank 0)	-	-	GND (Bank 0)	-	-	-	-	-
N4	BK0_IO35	PLL_RST1	17N	BK0_IO19	PLL_RST1	9N	BK0_IO15	PLL_RST1	7N/HSI0
N2	BK0_IO36	-	18P	BK0_IO20	-	10P	BK0_IO16	-	8P/HSI0
N1	BK0_IO37	PLL_FBK1	18N	BK0_IO21	PLL_FBK1	10N	BK0_IO17	PLL_FBK1	8N/HSI0
P1	BK0_IO38	PLL_RST0	19P	BK0_IO22	PLL_RST0	11P	BK0_IO18	PLL_RST0	9P
-	-	-	-	-	-	-	GND (Bank 0)	-	-
R1	BK0_IO39	-	19N	BK0_IO23	-	11N	BK0_IO19	-	9N
P3	BK0_IO40	CLK_OUT0	20P	BK0_IO24	CLK_OUT0	12P	BK0_IO20	CLK_OUT0	10P
-	GND (Bank 0)	-	-	-	-	-	-	-	-
P2	BK0_IO41	CLK_OUT1	20N	BK0_IO25	CLK_OUT1	12N	BK0_IO21	CLK_OUT1	10N

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved ¹
-	GND (Bank 2)	-	-
K36	BK2_IO19	-	71N
H38	BK2_IO20	-	72P
J38	BK2_IO21	-	72N
J39	BK2_IO22	-	73P
L36	BK2_IO23	-	73N
K38	BK2_IO24	-	74P
M36	BK2_IO25	-	74N
L37	BK2_IO26	-	75P
-	GND (Bank 2)	-	-
K39	BK2_IO27	-	75N
L38	BK2_IO28	-	76P
P35	BK2_IO29	-	76N
N36	BK2_IO30	-	77P
M37	BK2_IO31	-	77N
L39	BK2_IO32	-	78P
M38	BK2_IO33	-	78N
M39	BK2_IO34	-	79P
-	GND (Bank 2)	-	-
P36	BK2_IO35	-	79N
R36	BK2_IO36	-	80P
N37	BK2_IO37	-	80N
P38	BK2_IO38	-	81P
T35	BK2_IO39	-	81N
R37	BK2_IO40	-	82P
R38	BK2_IO41	-	82N
P39	BK2_IO42	-	83P
-	GND (Bank 2)	-	-
R39	BK2_IO43	-	83N
T38	BK2_IO44	-	84P
T36	BK2_IO45	-	84N
T37	BK2_IO46	-	85P
U36	BK2_IO47	-	85N
U37	BK2_IO48	-	86P
T39	BK2_IO49	-	86N
V36	BK2_IO50	-	87P
-	GND (Bank 2)	-	-
U38	BK2_IO51	-	87N
U39	BK2_IO52	-	88P
V38	BK2_IO53	-	88N
V37	BK2_IO54	-	89P
W36	BK2_IO55	-	89N
W35	BK2_IO56	-	90P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved ¹
AK2	BK6_IO23	-	197N
AK1	BK6_IO24	-	198P
AJ4	BK6_IO25	-	198N
AJ3	BK6_IO26	-	199P
-	GND (Bank 6)	-	-
AH4	BK6_IO27	-	199N
AH3	BK6_IO28	-	200P
AH2	BK6_IO29	-	200N
AH1	BK6_IO30	-	201P
AG4	BK6_IO31	-	201N
AF5	BK6_IO32	DATA7	202P
AG3	BK6_IO33	DATA6	202N
AG2	BK6_IO34	-	203P
-	GND (Bank 6)	-	-
AF4	BK6_IO35	-	203N
AF3	BK6_IO36	DATA5	204P
AG1	BK6_IO37	DATA4	204N
AE2	BK6_IO38	-	205P
AF1	BK6_IO39	-	205N
AF2	BK6_IO40	-	206P
AE1	BK6_IO41	-	206N
AE4	BK6_IO42	-	207P
-	GND (Bank 6)	-	-
AD4	BK6_IO43	-	207N
AD5	BK6_IO44	-	208P
AD3	BK6_IO45	-	208N
AD2	BK6_IO46	-	209P
AD1	BK6_IO47	-	209N
AC4	BK6_IO48	-	210P
AC3	BK6_IO49	-	210N
AC2	BK6_IO50	DATA3	211P
-	GND (Bank 6)	-	-
AC1	BK6_IO51	DATA2	211N
AB3	BK6_IO52	-	212P
AB4	BK6_IO53	-	212N
AB2	BK6_IO54	DATA1	213P
AB1	BK6_IO55	DATA0	213N
AA3	BK6_IO56	-	214P
AA4	BK6_IO57	-	214N
AA5	BK6_IO58	-	215P
-	GND (Bank 6)	-	-
AA2	BK6_IO59	-	215N
AA1	BK6_IO60	-	216P

ispXPGA Logic Signal Connections: 900-Ball fpBGA

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹
D3	BK0_IO0	-	0P	NC	-	-
E3	BK0_IO1	-	0N	NC	-	-
C2	BK0_IO2	-	1P	NC	-	-
-	GND (Bank 0)	-	-	-	-	-
C1	BK0_IO3	-	1N	NC	-	-
E4	BK0_IO4	-	2P	BK0_IO0	-	0P
F5	BK0_IO5	-	2N	BK0_IO1	-	0N
D2	BK0_IO6	HSI0A_SOUTP	3P	BK0_IO2	HSI0A_SOUTP	1P/HSI0
-	-	-	-	GND (Bank 0)	-	-
D1	BK0_IO7	HSI0A_SOUTN	3N	BK0_IO3	HSI0A_SOUTN	1N/HSI0
F4	BK0_IO8	-	4P	BK0_IO4	-	2P/HSI0
F3	BK0_IO9	-	4N	BK0_IO5	-	2N/HSI0
E2	BK0_IO10	HSI0A_SINP	5P/HSI0	BK0_IO6	HSI0A_SINP	3P/HSI0
-	GND (Bank 0)	-	-	-	-	-
E1	BK0_IO11	HSI0A_SINN	5N/HSI0	BK0_IO7	HSI0A_SINN	3N/HSI0
G6	BK0_IO12	VREF0	6P/HSI0	BK0_IO9	VREF0	4N/HSI0
G5	BK0_IO13	-	6N/HSI0	BK0_IO8	-	4P/HSI0
F1	BK0_IO14	HSI0B_SOUTP	7P/HSI0	NC	-	-
F2	BK0_IO15	HSI0B_SOUTN	7N/HSI0	NC	-	-
G4	BK0_IO16	-	8P/HSI0	NC	-	-
G3	BK0_IO17	-	8N/HSI0	NC	-	-
G2	BK0_IO18	HSI0B_SINP	9P/HSI0	NC	-	-
-	GND (Bank 0)	-	-	-	-	-
G1	BK0_IO19	HSI0B_SINN	9N/HSI0	NC	-	-
H3	BK0_IO20	-	10P/HSI0	NC	-	-
H4	BK0_IO21	-	10N/HSI0	NC	-	-
H1	BK0_IO22	HSI1A_SOUTP	11P/HSI0	NC	-	-
H2	BK0_IO23	HSI1A_SOUTN	11N/HSI0	NC	-	-
J7	BK0_IO24	-	12P/HSI0	NC	-	-
J6	BK0_IO25	-	12N/HSI0	NC	-	-
J1	BK0_IO26	HSI1A_SINP	13P/HSI1	NC	-	-
-	GND (Bank 0)	-	-	-	-	-
J2	BK0_IO27	HSI1A_SINN	13N/HSI1	NC	-	-
J4	BK0_IO28	-	14P/HSI1	NC	-	-
J5	BK0_IO29	-	14N/HSI1	NC	-	-
K1	BK0_IO30	HSI1B_SOUTP	15P/HSI1	BK0_IO10	HSI0B_SOUTP	5P/HSI0
-	-	-	-	GND (Bank 0)	-	-
K2	BK0_IO31	HSI1B_SOUTN	15N/HSI1	BK0_IO11	HSI0B_SOUTN	5N/HSI0
K5	BK0_IO32	-	16P/HSI1	BK0_IO12	-	6P/HSI0
K4	BK0_IO33	-	16N/HSI1	BK0_IO13	-	6N/HSI0
L1	BK0_IO34	HSI1B_SINP	17P/HSI1	BK0_IO14	HSI0B_SINP	7P/HSI0
-	GND (Bank 0)	-	-	-	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹
L2	BK0_IO35	HSI1B_SINN	17N/HSI1	BK0_IO15	HSI0B_SINN	7N/HSI0
L6	BK0_IO36	-	18P/HSI1	BK0_IO16	-	8P/HSI0
L5	BK0_IO37	-	18N/HSI1	BK0_IO17	-	8N/HSI0
M1	BK0_IO38	HSI2A_SOUTP	19P/HSI1	BK0_IO18	HSI1A_SOUTP	9P/HSI1
-	-	-	-	GND (Bank 0)	-	-
M2	BK0_IO39	HSI2A_SOUTN	19N/HSI1	BK0_IO19	HSI1A_SOUTN	9N/HSI1
L3	BK0_IO40	-	20P/HSI1	BK0_IO20	-	10P/HSI1
L4	BK0_IO41	-	20N/HSI1	BK0_IO21	-	10N/HSI1
M6	BK0_IO42	HSI2A_SINP	21P/HSI2	BK0_IO22	HSI1A_SINP	11P/HSI1
-	GND (Bank 0)	-	-	-	-	-
M5	BK0_IO43	HSI2A_SINN	21N/HSI2	BK0_IO23	HSI1A_SINN	11N/HSI1
M4	BK0_IO44	-	22P/HSI2	BK0_IO24	-	12P/HSI1
M3	BK0_IO45	-	22N/HSI2	BK0_IO25	-	12N/HSI1
N1	BK0_IO46	HSI2B_SOUTP	23P/HSI2	BK0_IO26	HSI1B_SOUTP	13P/HSI1
-	-	-	-	GND (Bank 0)	-	-
N2	BK0_IO47	HSI2B_SOUTN	23N/HSI2	BK0_IO27	HSI1B_SOUTN	13N/HSI1
N7	BK0_IO48	-	24P/HSI2	BK0_IO28	-	14P/HSI1
N6	BK0_IO49	-	24N/HSI2	BK0_IO29	-	14N/HSI1
P1	BK0_IO50	HSI2B_SINP	25P/HSI2	BK0_IO30	HSI1B_SINP	15P/HSI1
-	GND (Bank 0)	-	-	-	-	-
P2	BK0_IO51	HSI2B_SINN	25N/HSI2	BK0_IO31	HSI1B_SINN	15N/HSI1
N3	BK0_IO52	-	26P/HSI2	BK0_IO32	-	16P/HSI1
N4	BK0_IO53	-	26N/HSI2	BK0_IO33	-	16N/HSI1
P6	BK0_IO54	PLL_RST0	27P/HSI2	BK0_IO38	PLL_RST0	19P
P5	BK0_IO55	PLL_RST1	27N/HSI2	BK0_IO35	PLL_RST1	17N
P3	BK0_IO56	-	28P/HSI2	BK0_IO36	-	18P
P4	BK0_IO57	-	28N/HSI2	BK0_IO39	-	19N
R7	BK0_IO58	PLL_FBK0	29P	BK0_IO34	PLL_FBK0	17P
-	GND (Bank 0)	-	-	GND (Bank 0)	-	-
R6	BK0_IO59	PLL_FBK1	29N	BK0_IO37	PLL_FBK1	18N
R1	BK0_IO60	CLK_OUT0	30P	BK0_IO40	CLK_OUT0	20P
-	-	-	-	GND (Bank 0)	-	-
R2	BK0_IO61	CLK_OUT1	30N	BK0_IO41	CLK_OUT1	20N
-	GND (Bank 0)	-	-	-	-	-
R3	GCLK0	-	LVDS Pair0P	GCLK0	-	LVDS Pair0P
R4	GCLK1	-	LVDS Pair0N	GCLK1	-	LVDS Pair0N
R5	VCCP0	-	-	VCCP0	-	-
T3	GNDP0	-	-	GNDP0	-	-
T4	GCLK2	-	LVDS Pair1P	GCLK2	-	LVDS Pair1P
T5	GCLK3	-	LVDS Pair1N	GCLK3	-	LVDS Pair1N
-	GND (Bank 1)	-	-	-	-	-
T2	BK1_IO0	CLK_OUT2	31P	BK1_IO0	CLK_OUT2	21P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹
AB1	BK1_IO35	HSI3B_SOUTN	48N/HSI3	NC	-	-
AC6	BK1_IO36	-	49P/HSI4	NC	-	-
AC5	BK1_IO37	-	49N/HSI4	NC	-	-
AC2	BK1_IO38	HSI3B_SINP	50P/HSI4	NC	-	-
AC1	BK1_IO39	HSI3B_SINN	50N/HSI4	NC	-	-
AC4	BK1_IO40	-	51P/HSI4	NC	-	-
AC3	BK1_IO41	-	51N/HSI4	NC	-	-
AD2	BK1_IO42	HSI4A_SOUTP	52P/HSI4	NC	-	-
-	GND (Bank 1)	-	-	-	-	-
AD1	BK1_IO43	HSI4A_SOUTN	52N/HSI4	NC	-	-
AD3	BK1_IO44	-	53P/HSI4	BK1_IO32	-	37P/HSI3
AD4	BK1_IO45	-	53N/HSI4	BK1_IO33	-	37N
AE2	BK1_IO46	HSI4A_SINP	54P/HSI4	BK1_IO34	-	38P
AE1	BK1_IO47	HSI4A_SINN	54N/HSI4	BK1_IO35	-	38N
AD5	BK1_IO48	-	55P/HSI4	BK1_IO25	-	33N
AD6	BK1_IO49	VREF1	55N/HSI4	BK1_IO24	VREF1	33P
AF2	BK1_IO50	HSI4B_SOUTP	56P/HSI4	BK1_IO26	HSI2B_SOUTP	34P
-	GND (Bank 1)	-	-	-	-	-
AF1	BK1_IO51	HSI4B_SOUTN	56N/HSI4	BK1_IO27	HSI2B_SOUTN	34N
AE3	BK1_IO52	-	57P	BK1_IO28	-	35P
AE4	BK1_IO53	-	57N	BK1_IO29	-	35N
AG1	BK1_IO54	HSI4B_SINP	58P	BK1_IO30	HSI2B_SINP	36P
-	-	-	-	GND (Bank 1)	-	-
AG2	BK1_IO55	HSI4B_SINN	58N	BK1_IO31	HSI2B_SINN	36N
AE5	BK1_IO56	-	59P	BK1_IO36	-	39P
AF4	BK1_IO57	-	59N	BK1_IO37	-	39N
AH1	BK1_IO58	-	60P	BK1_IO38	-	40P
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-
AH2	BK1_IO59	-	60N	BK1_IO39	-	40N
AF3	BK1_IO60	-	61P	BK1_IO40	-	41P
AG3	BK1_IO61	-	61N	BK1_IO41	-	41N
AH4	TCK	-	-	TCK	-	-
AJ3	TMS	-	-	TMS	-	-
AK3	TOE	-	-	TOE	-	-
AG5	BK2_IO0	-	62P	BK2_IO0	-	42P
AH5	BK2_IO1	-	62N	BK2_IO1	-	42N
AJ4	BK2_IO2	-	63P	BK2_IO2	-	43P
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
AK4	BK2_IO3	-	63N	BK2_IO3	-	43N
AG6	BK2_IO4	-	64P	BK2_IO4	-	44P
AH6	BK2_IO5	-	64N	BK2_IO5	-	44N
AJ5	BK2_IO6	-	65P	BK2_IO6	-	45P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹
AJ25	BK3_IO50	-	118P	BK3_IO30	-	78P
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-
AK25	BK3_IO51	-	118N	BK3_IO31	-	78N
AF24	BK3_IO52	-	119P	BK3_IO32	-	79P
AE24	BK3_IO53	-	119N	BK3_IO33	-	79N
AK26	BK3_IO54	-	120P	BK3_IO34	-	80P
AJ26	BK3_IO55	-	120N	BK3_IO35	-	80N
AH25	BK3_IO56	-	121P	BK3_IO36	-	81P
AG25	BK3_IO57	-	121N	BK3_IO37	-	81N
AK27	BK3_IO58	-	122P	BK3_IO38	-	82P
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-
AJ27	BK3_IO59	-	122N	BK3_IO39	-	82N
AG26	BK3_IO60	-	123P	BK3_IO40	-	83P
AH26	BK3_IO61	-	123N	BK3_IO41	-	83N
AK28	GSR	-	-	GSR	-	-
AJ28	DXP	-	-	DXP	-	-
AH27	DXN	-	-	DXN	-	-
AG28	BK4_IO0	-	124P	BK4_IO0	-	84P
AF27	BK4_IO1	-	124N	BK4_IO1	-	84N
AF28	BK4_IO2	-	125P	BK4_IO2	-	85P/HSI3
-	GND (Bank 4)	-	-	GND (Bank 4)	-	-
AE26	BK4_IO3	-	125N	BK4_IO3	-	85N/HSI3
AE27	BK4_IO4	-	126P	BK4_IO4	-	86P/HSI3
AE28	BK4_IO5	-	126N	BK4_IO5	-	86N/HSI3
AH30	BK4_IO6	HSI5A_SINP	127P	BK4_IO10	HSI3A_SINP	89P/HSI3
-	-	-	-	GND (Bank 4)	-	-
AH29	BK4_IO7	HSI5A_SINN	127N	BK4_IO11	HSI3A_SINN	89N/HSI3
AD25	BK4_IO8	-	128P	BK4_IO12	-	90P/HSI3
AD26	BK4_IO9	-	128N	BK4_IO13	-	90N/HSI3
AG29	BK4_IO10	HSI5A_SOUTP	129P/HSI5	BK4_IO14	HSI3A_SOUTP	91P/HSI3
-	GND (Bank 4)	-	-	-	-	-
AG30	BK4_IO11	HSI5A_SOUTN	129N/HSI5	BK4_IO15	HSI3A_SOUTN	91N/HSI3
AD27	BK4_IO12	VREF4	130P/HSI5	BK4_IO17	VREF4	92N/HSI3
AD28	BK4_IO13	-	130N/HSI5	BK4_IO16	-	92P/HSI3
AF29	BK4_IO14	HSI5B_SINP	131P/HSI5	BK4_IO6	-	87P/HSI3
AF30	BK4_IO15	HSI5B_SINN	131N/HSI5	BK4_IO7	-	87N/HSI3
AC25	BK4_IO16	-	132P/HSI5	BK4_IO8	-	88P/HSI3
AC26	BK4_IO17	-	132N/HSI5	BK4_IO9	-	88N/HSI3
AE29	BK4_IO18	HSI5B_SOUTP	133P/HSI5	NC	-	-
-	GND (Bank 4)	-	-	-	-	-
AE30	BK4_IO19	HSI5B_SOUTN	133N/HSI5	NC	-	-
AC28	BK4_IO20	-	134P/HSI5	NC	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹
K30	BK5_IO22	HSI7B_SOUTP	166P/HSI8	BK5_IO22	HSI4B_SOUTP	116P/HSI4
-	-	-	-	GND (Bank 5)	-	-
K29	BK5_IO23	HSI7B_SOUTN	166N/HSI8	BK5_IO23	HSI4B_SOUTN	116N/HSI4
L28	BK5_IO24	-	167P/HSI8	BK5_IO24	-	117P/HSI5
L27	BK5_IO25	-	167N/HSI8	BK5_IO25	-	117N/HSI5
L26	BK5_IO26	HSI8A_SINP	168P/HSI8	BK5_IO26	HSI5A_SINP	118P/HSI5
-	GND (Bank 5)	-	-	-	-	-
L25	BK5_IO27	HSI8A_SINN	168N/HSI8	BK5_IO27	HSI5A_SINN	118N/HSI5
K27	BK5_IO28	-	169P/HSI8	BK5_IO28	-	119P/HSI5
K26	BK5_IO29	-	169N/HSI8	BK5_IO29	-	119N/HSI5
J30	BK5_IO30	HSI8A_SOUTP	170P/HSI8	BK5_IO30	HSI5A_SOUTP	120P/HSI5
-	-	-	-	GND (Bank 5)	-	-
J29	BK5_IO31	HSI8A_SOUTN	170N/HSI8	BK5_IO31	HSI5A_SOUTN	120N/HSI5
J26	BK5_IO32	-	171P/HSI8	NC	-	-
J27	BK5_IO33	-	171N/HSI8	NC	-	-
H30	BK5_IO34	HSI8B_SINP	172P/HSI8	NC	-	-
-	GND (Bank 5)	-	-	-	-	-
H29	BK5_IO35	HSI8B_SINN	172N/HSI8	NC	-	-
J25	BK5_IO36	-	173P/HSI9	NC	-	-
J24	BK5_IO37	-	173N/HSI9	NC	-	-
G30	BK5_IO38	HSI8B_SOUTP	174P/HSI9	NC	-	-
G29	BK5_IO39	HSI8B_SOUTN	174N/HSI9	NC	-	-
H27	BK5_IO40	-	175P/HSI9	NC	-	-
H28	BK5_IO41	-	175N/HSI9	NC	-	-
F30	BK5_IO42	HSI9A_SINP	176P/HSI9	NC	-	-
-	GND (Bank 5)	-	-	-	-	-
F29	BK5_IO43	HSI9A_SINN	176N/HSI9	NC	-	-
G27	BK5_IO44	-	177P/HSI9	NC	-	-
G28	BK5_IO45	-	177N/HSI9	NC	-	-
E30	BK5_IO46	HSI9A_SOUTP	178P/HSI9	NC	-	-
E29	BK5_IO47	HSI9A_SOUTN	178N/HSI9	NC	-	-
H26	BK5_IO48	-	179P/HSI9	BK5_IO33	-	121N/HSI5
H25	BK5_IO49	VREF5	179N/HSI9	BK5_IO32	VREF5	121P/HSI5
D30	BK5_IO50	HSI9B_SINP	180P/HSI9	BK5_IO34	HSI5B_SINP	122P/HSI5
-	GND (Bank 5)	-	-	-	-	-
D29	BK5_IO51	HSI9B_SINN	180N/HSI9	BK5_IO35	HSI5B_SINN	122N/HSI5
F28	BK5_IO52	-	181P	BK5_IO36	-	123P/HSI5
F27	BK5_IO53	-	181N	BK5_IO37	-	123N/HSI5
C30	BK5_IO54	HSI9B_SOUTP	182P	BK5_IO38	HSI5B_SOUTP	124P/HSI5
-	-	-	-	GND (Bank 5)	-	-
C29	BK5_IO55	HSI9B_SOUTN	182N	BK5_IO39	HSI5B_SOUTN	124N/HSI5
G26	BK5_IO56	-	183P	NC	-	-