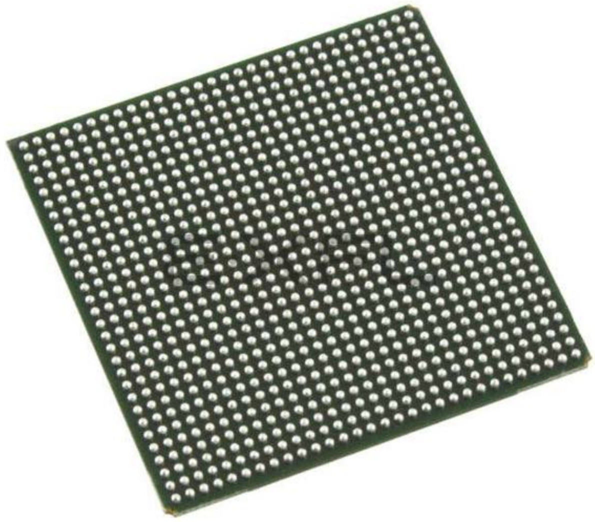


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	15376
Total RAM Bits	423936
Number of I/O	496
Number of Gates	1250000
Voltage - Supply	1.65V ~ 1.95V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx1200ec-03f900c

Product Line	Ordering Part Number	Product Status	Reference PCN
LFX125EC (Cont'd)	LFX125EC-03F516C	**Discontinued**	PCN#09-10
	LFX125EC-04F516C		
	LFX125EC-03F516I		
LFX200EB	LFX200EB-03F256C	Active / Orderable	
	LFX200EB-03FN256C		
	LFX200EB-04F256C		
	LFX200EB-04FN256C		
	LFX200EB-05F256C		
	LFX200EB-05FN256C		
	LFX200EB-03F256I		
	LFX200EB-03FN256I		
	LFX200EB-04F256I		
	LFX200EB-04FN256I		
	LFX200EB-03F516C	**Discontinued**	PCN#09-10
	LFX200EB-04F516C		
	LFX200EB-05F516C		
	LFX200EB-03F516I		
	LFX200EB-04F516I		
LFX200EC	LFX200EC-03F256C	**Discontinued**	PCN#09-10
	LFX200EC-03FN256C		
	LFX200EC-04F256C		
	LFX200EC-04FN256C		
	LFX200EC-03F256I		
	LFX200EC-03FN256I		
	LFX200EC-03F516C		
	LFX200EC-04F516C		
	LFX200EC-03F516I		
LFX500EB	LFX500EB-03F516C	**Discontinued**	PCN#09-10
	LFX500EB-04F516C		
	LFX500EB-05F516C		
	LFX500EB-03F516I		
	LFX500EB-04F516I		
	LFX500EB-03F900C		
	LFX500EB-03FN900C		
	LFX500EB-04F900C		
	LFX500EB-04FN900C		
	LFX500EB-05F900C		
	LFX500EB-05FN900C		
	LFX500EB-03F900I		
	LFX500EB-03FN900I		
	LFX500EB-04F900I		
	LFX500EB-04FN900I		
LFX500EC	LFX500EC-03F516C	**Discontinued**	PCN#09-10
	LFX500EC-04F516C		
	LFX500EC-03F516I		

ispXPGA® Family

Includes High-Performance, Low-Cost “E-Series”

February 2010 Data Sheet DS1026

Non-volatile, Infinitely Reconfigurable

- Instant-on - Powers up in microseconds via on-chip E^2CMOS® based memory
- No external configuration memory
- Excellent design security, no bit stream to intercept
- Reconfigure SRAM based logic in milliseconds

High Logic Density for System-level Integration

- 139K to 1.25M functional gates
- 160 to 496 I/O
- 1.8V, 2.5V, and 3.3V V_{CC} operation
- Up to 414Kb sysMEM™ embedded memory

High Performance Programmable Function Unit (PFU)

- Four LUT-4 per PFU supports wide and narrow functions
- Dual flip-flops per LUT-4 for extensive pipelining
- Dedicated logic for adders, multipliers, multiplexers, and counters

Flexible Memory Resources

- Multiple sysMEM Embedded RAM Blocks
  - Single port, Dual port, and FIFO operation
- 64-bit distributed memory in each PFU
  - Single port, Double port, FIFO, and Shift Register operation

Flexible Programming, Reconfiguration, and Testing

- Supports IEEE 1532 and 1149.1
- Microprocessor configuration interface
- Program E^2CMOS while operating from SRAM

Eight sysCLOCK™ Phase Locked Loops (PLLs) for Clock Management

- True PLL technology
- 10MHz to 320MHz operation
- Clock multiplication and division
- Phase adjustment
- Shift clocks in 250ps steps

sysIO™ for High System Performance

- High speed memory support through SSTL and HSTL
- Advanced buses supported through PCI, GTL+, LVDS, BLVDS, and LVPECL
- Standard logic supported through LVTTL, LVCMOS 3.3, 2.5 and 1.8
- 5V tolerant I/O for LVCMOS 3.3 and LVTTL interfaces
- Programmable drive strength for series termination
- Programmable bus maintenance

Two Options Available

- High-performance sysHSI (standard part number)
- Low-cost, no sysHSI (“E-Series”)

sysHSI™ Capability for Ultra Fast Serial Communications

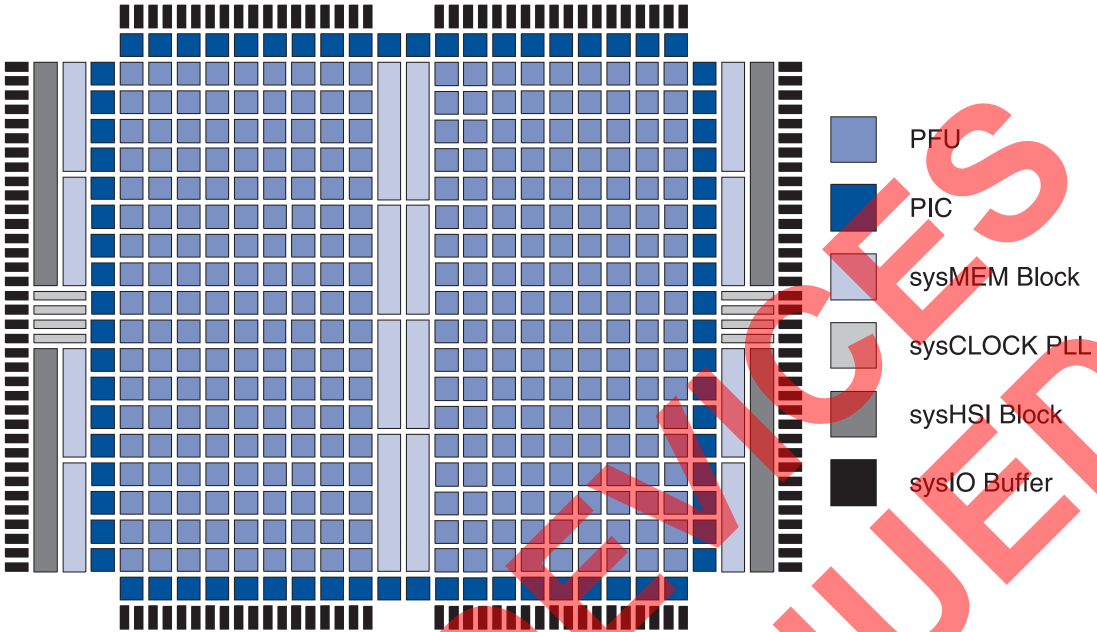
- Up to 800Mbps performance
- Up to 20 channels per device
- Built in Clock Data Recovery (CDR) and Serialization and De-serialization (SERDES)

Table 1. ispXPGA Family Selection Guide

	ispXPGA 125/E	ispXPGA 200/E	ispXPGA 500/E	ispXPGA 1200/E[3]
Functional Gates	139K	210K	476K	1.25M
PFUs	484	676	1764	3844
LUT-4s	1936	2704	7056	15376
Logic FFs	3.8K	5.4K	14.1K	30.7K
sysMEM Memory	92K	111K	184K	414K
Distributed Memory	30K	43K	112K	246K
EBR	20	24	40	90
sysHSI Channels[1]	4	8	12	20
User I/O	160/176	160/208	336	496
Packaging	256 fpBGA 516 fpBGA[2]	256 fpBGA 516 fpBGA[2]	516 fpBGA[2] 900 fpBGA	680 fpSBGA 900 fpBGA

1. “E-Series” does not support sysHSI.
2. FH516 package was converted to F516 via PCN #09A-08.
3. Discontinued via PCN #03A-10.

Figure 1. ispXPGA Block Diagram



Programmable Function Unit

The Programmable Function Unit (PFU) is the basic building block of the ispXPGA architecture. The PFUs are arranged in rows and columns in the device with PFU (1,1) referring to (row 1, column 1). Each PFU consists of four Configurable Logic Elements (CLEs), four Configurable Sequential Elements (CSEs), and a Wide Logic Generator (WLG). By utilizing these components, the PFU can implement a variety of functions. Table 3 lists some of the function capabilities of the PFU.

There are 57 inputs to each PFU and nine outputs. The PFU uses 20 inputs for logic, and 37 inputs drive the control logic from which six control signals are derived for the PFU.

Table 3. Function Capability of ispXPGA PFU

Function	Capability
Look-up table	LUT-4, LUT-5, LUT-6
Wide logic functions	Up to 20 input logic functions
Multiplexing	2:1, 4:1, 8:1
Arithmetic logic	Dedicated carry chain and booth multiplication logic
Single-port RAM	16X1, 16X2, 16X4, 32X1, 32X2, 64X1
Double-port RAM	16X1, 16X2, 32X1
Shift register	8-bit shift registers (up to 32-bit shift capability)

Configurable Logic Element

The CLE is made up of a four-input Look-up Table (LUT-4), a Carry Chain Generator (CCG), and a two-input AND gate. The LUT-4 creates various combinatorial and memory elements, the CCG creates a single one-bit full adder, and the two-input AND gate can expand the CCG to incorporate Booth Multiplier capability by feeding the output of the AND gate to one of the inputs of the CCG.

Of the five inputs that feed each CLE, two are dedicated inputs into each LUT-4 and the remaining three take on varying functionality. The third and fourth inputs can be used as either inputs to the LUT-4 or as a Feed-Thru to the CSE via the WLG. The fifth input can be a data port when the LUT is configured as Distributed Memory, a select line for multiplexer operation, or a Feed-Thru directly to the CSE via the WLG (Figure 2).

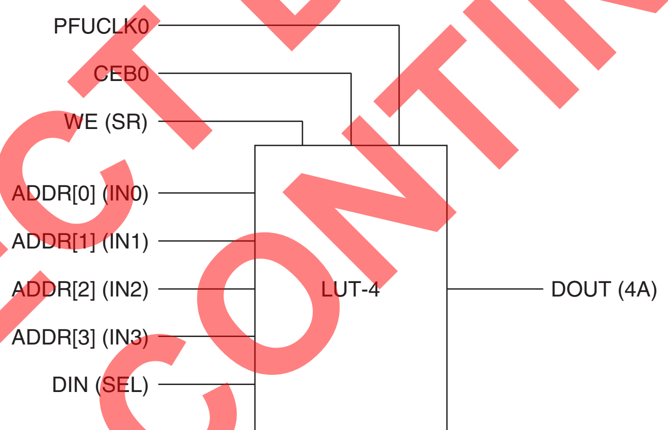
Look-Up Table – Combinatorial Mode

In combinatorial mode, the LUT-4 can implement any logic function up to four inputs. By using the carry chain and the WLG, each LUT-4 can be combined to form the enhanced functions listed in Table 3.

Look-Up Table – Distributed Memory Mode

In the distributed memory mode, the LUT functions as a memory element. The inputs to the LUT function as Address and Data. Each PFU is capable of implementing up to 64 SRAM bits. Both single and double port RAM can be performed in the PFU (Table 3). Furthermore, the distributed memory can be configured as either synchronous or asynchronous memory. Figure 3 illustrates the LUT while in distributed memory mode. When using any LUT in the PFU in memory mode, the Set/Reset signal will be used for Write Enable (WE(SR)) and the CLK0 signal will be used as the clock for synchronous read and write.

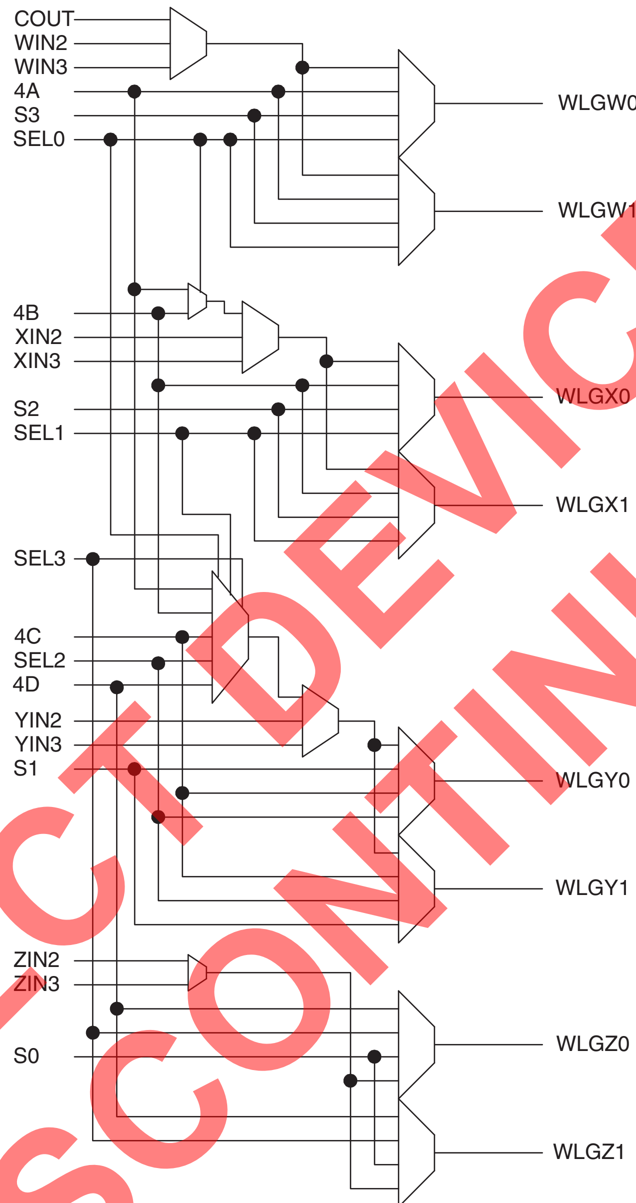
Figure 3. LUT in Distributed Memory Mode



Look-Up Table – Shift Register Mode

In the shift register mode, the LUT functions as a 1-bit to 8-bit shift register. This means that each PFU can implement up to four 8-bit shift registers or any cascaded combination. Figure 4 illustrates the LUT when configured in shift register mode.

Figure 6. ispXPGA Wide Logic Generator



Configurable Sequential Element

There are two registers in each CSE for a total of eight registers in each PFU. This high register count assists in implementing efficient pipelined applications with no utilization penalty. Each register can be configured as a latch or D type flip-flop with either synchronous or asynchronous set or reset. Figure 2 shows the signals that feed the register's D inputs. Feed-through signals in the architecture ensure that registers are efficiently utilized even if the accompanying LUT is occupied.

Control Logic

The control signals available to the registers in a PFU are Clock, Clock Enable, and Set/Reset. Figure 7 shows the various options available to generate the clock signal. As can be seen, the clock signal is the output of a 12:1 MUX with true and compliment versions available from the 12:1 MUX. Each CSE can chose whether it uses the true or complement form of the clock. Figure 8 shows the Set/Reset selection for each PFU in the ispXPGA. A common

Memory

The ispXPGA architecture provides a large amount of resources for memory intensive applications. Embedded Block RAMs (EBRs) are available to complement the Distributed Memory that is configured in the PFUs (see Look-Up Table -Distributed Memory Mode in the PFU section above). Each memory element can be configured as RAM or ROM. Additionally, the internal logic of the device can be used to configure the memory elements as FIFO and other storage types. These EBRs are referred to as sysMEM blocks. Refer to Table 1 for memory resources per device.

sysMEM Blocks

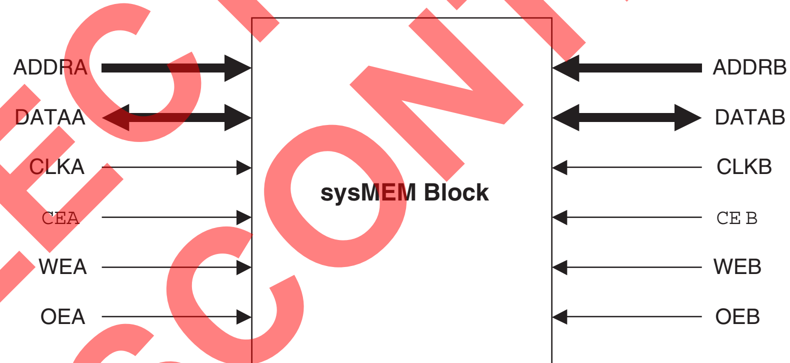
The sysMEM blocks are organized in columns distributed throughout the device. Each EBR contains 4.6K bits of dual-port RAM with dedicated control, address, and data lines for each port. Each column of sysMEM blocks has dedicated address and control lines that can be used by each block separately or cascaded to form larger memory elements. The memory cells are symmetrical and contain two sets of identical control signals. Each port has a read/write clock, clock enable, write enable, and output enable. Figure 12 illustrates the sysMEM block.

The ispXPGA memory block can operate as single-port or dual-port RAM. Supported configurations are:

- 512 x 9 bits single-port (8 bits data / 1 bit parity)
- 256 x 18 bits single-port (16 bits data / 2 bits parity)
- 512 x 9 bits dual-port (8 bits data / 1 bit parity)
- 256 x18 bits dual-port (16 bits data / 2 bits parity)

The data widths of “9” and “18” are ideal for applications where parity is necessary. This allows 9 data bits, 8 data bits plus a parity bit, 18 data bits, or 16 data bits plus two parity bits. The logic for generating and checking the parity must be customized separately.

Figure 12. sysMEM Block Diagram



Read and Write Operations

The ispXPGA EBR has fully synchronous read and write operations as well as an asynchronous read operation. These operations allow several different types of memory to be implemented in the device.

Synchronous Read: The Clock Enable ($\overline{CE}$) and Write Enable (WE) signals control the synchronous read operation. When the $\overline{CE}$ signal is low, the clock is enabled. When the WE signal is low the read operation begins. Once the address (ADDR) is present, a rising clock edge (or falling edge depending on polarity) causes the stored data to be available on the DATA port. Figure 13 illustrates the synchronous read timing.

ispXPGA 125B/C & ispXPGA 125EB/EC Timing Adders

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	4.28	—	4.6	—	5.29	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

ispXPGA 200B/C & ispXPGA 200EB/EC PFU Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Set								
t_{LASSRO}	Asynchronous Set/Reset to Output	—	1.09	—	1.17	—	1.35	ns
$t_{LASSRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{LASSRR}	Asynchronous Set/Reset Recovery	—	0.51	—	0.55	—	0.63	ns
t_{LSSR_S}	Synchronous Set/Reset Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{LSSR_H}	Synchronous Set/Reset Hold Time	0.03	—	0.03	—	0.03	—	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.
2. $t_{LCTHRUL}$ quoted bit by bit.

Timing v.0.3

ispXPGA 200B/C & ispXPGA 200EB/EC PIC Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Register/Latch Delays								
t_{IO_CO}	Register Clock to Output Delay	—	0.93	—	1.00	—	1.15	ns
t_{IO_S}	Register Setup Time (Data before Clock)	0.05	—	0.05	—	0.06	—	ns
t_{IO_H}	Register Hold Time (Data after Clock)	0.06	—	0.06	—	0.07	—	ns
t_{IOCE_S}	Register Clock Enable Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{IOCE_H}	Register Clock Enable Hold Time	0.13	—	0.13	—	0.15	—	ns
t_{IO_GO}	Latch Gate to Output Delay	—	0.72	—	0.77	—	0.89	ns
t_{IOL_S}	Latch Setup Time	0.05	—	0.05	—	0.06	—	ns
t_{IOL_H}	Latch Hold Time	0.06	—	0.06	—	0.07	—	ns
t_{IOLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns
t_{IOASRO}	Asynchronous Set/Reset to Output	—	1.04	—	1.12	—	1.29	ns
$t_{IOASRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{IOASRR}	Asynchronous Set/Reset Recovery Time	—	0.23	—	0.25	—	0.29	ns
Input/Output Delays								
t_{IOBUF}	Output Buffer Delay	—	0.97	—	1.04	—	1.20	ns
t_{IOIN}	Input Buffer Delay	—	0.60	—	0.64	—	0.74	ns
t_{IOEN}	Output Enable Delay	—	0.53	—	0.57	—	0.66	ns
t_{IODIS}	Output Disable Delay	—	-0.13	—	-0.12	—	-0.10	ns
t_{IOFT}	Feed-thru Delay	—	0.19	—	0.20	—	0.23	ns

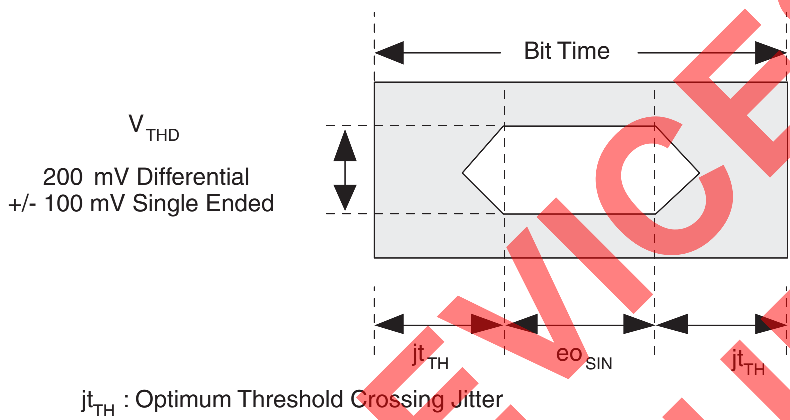
1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.

Timing v.0.3

sysHSI Block Timing

Figure 24 provides a graphical representation of the SERDES receiver input requirements. It provides guidance on a number of input parameters, including signal amplitude and rise time limits, noise and jitter limits, and P and N input skew tolerance.

Figure 24. Receive Data Eye Diagram Template (Differential)



The data pattern eye opening at the receive end of a link is considered the ultimate measure of received signal quality. Almost all detrimental characteristics of a transmit signal and the interconnection link design result in eye closure. This combined with the eye-opening limitations of the line receiver can provide a good indication of a link's ability to transfer error-free data.

Signal jitter is of special interest to system designers. It is often the primary limiting characteristic of long digital links and of systems with high noise level environments. An interesting characteristic of the clock and data recovery (CDR) portion of the ispXPGA SERDES receiver is its ability to filter incoming signal jitter that is below the clock recovery PLL bandwidth. For signals with high levels of low frequency jitter, the receiver can detect incoming data error free, with eye openings significantly less than that shown in Figure 24.

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
R8	BK2_IO19	-	35N	BK2_IO19	-	31N
N8	BK2_IO20	-	36P	BK2_IO20	-	32P
P8	BK2_IO21	-	36N	BK2_IO21	-	32N
-	GND (Bank 2)	-	-	-	-	-
-	GND (Bank 3)	-	-	-	-	-
T8	BK3_IO0	-	39P	BK3_IO0	-	33P
T9	BK3_IO1	-	39N	BK3_IO1	-	33N
R9	BK3_IO2	-	40P	BK3_IO2	-	34P
-	-	-	-	GND (Bank 3)	-	-
R10	BK3_IO3	-	40N	BK3_IO3	-	34N
P9	BK3_IO4	-	41P	BK3_IO4	-	35P
N9	BK3_IO5	-	41N	BK3_IO5	-	35N
T10	BK3_IO6	-	42P	BK3_IO6	-	36P
-	GND (Bank 3)	-	-	-	-	-
T11	BK3_IO7	-	42N	BK3_IO7	-	36N
P10	BK3_IO8	-	43P	BK3_IO8	-	37P
-	-	-	-	GND (Bank 3)	-	-
N10	BK3_IO9	-	43N	BK3_IO9	-	37N
R11	BK3_IO14	-	46P	BK3_IO10	-	38P
-	GND (Bank 3)	-	-	-	-	-
R12	BK3_IO15	-	46N	BK3_IO11	-	38N
P11	BK3_IO16	VREF3	47P	BK3_IO12	VREF3	39P
N11	BK3_IO17	-	47N	BK3_IO13	-	39N
T12	BK3_IO18	-	48P	BK3_IO14	-	40P
T13	BK3_IO19	-	48N	BK3_IO15	-	40N
R13	BK3_IO20	-	49P	BK3_IO16	-	41P
-	-	-	-	GND (Bank 3)	-	-
R14	BK3_IO21	-	49N	BK3_IO17	-	41N
P12	BK3_IO22	-	50P	BK3_IO18	-	42P
-	GND (Bank 3)	-	-	-	-	-
N12	BK3_IO23	-	50N	BK3_IO19	-	42N
T14	GSR	-	-	GSR	-	-
T15	DXP	-	-	DXP	-	-
P13	DXN	-	-	DXN	-	-
P15	BK4_IO0	-	52P/HSI2	BK4_IO0	-	44P
N14	BK4_IO1	-	52N/HSI2	BK4_IO1	-	44N
R16	BK4_IO2	HSI2A_SINP	53P/HSI2	BK4_IO2	-	45P
-	GND (Bank 4)	-	-	-	-	-
P16	BK4_IO3	HSI2A_SINN	53N/HSI2	BK4_IO3	-	45N
N15	BK4_IO4	-	54P/HSI2	BK4_IO4	-	46P
-	-	-	-	GND (Bank 4)	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
D21	BK6_IO20	-	136P	BK6_IO8	-	82P	BK6_IO8	-	70P
C21	BK6_IO21	VREF6	136N	BK6_IO9	VREF6	82N	BK6_IO9	VREF6	70N
B21	BK6_IO22	DATA5	137P	BK6_IO10	DATA5	83P	BK6_IO10	DATA5	71P
-	-	-	-	GND (Bank 6)	-	-	-	-	-
A21	BK6_IO23	DATA4	137N	BK6_IO11	DATA4	83N	BK6_IO11	DATA4	71N
D20	BK6_IO24	-	138P	BK6_IO12	-	84P	BK6_IO12	-	72P
-	-	-	-	-	-	-	GND (Bank 6)	-	-
C20	BK6_IO25	-	138N	BK6_IO13	-	84N	BK6_IO13	-	72N
B20	BK6_IO26	DATA3	139P	BK6_IO14	DATA3	85P	BK6_IO14	DATA3	73P
-	GND (Bank 6)	-	-	-	-	-	-	-	-
A20	BK6_IO27	DATA2	139N	BK6_IO15	DATA2	85N	BK6_IO15	DATA2	73N
C19	BK6_IO28	-	140P	BK6_IO16		86P	BK6_IO16	-	74P
B19	BK6_IO29	-	140N	BK6_IO17		86N	BK6_IO17	-	74N
A19	BK6_IO30	DATA1	141P	BK6_IO18	DATA1	87P	BK6_IO18	DATA1	75P
-	-	-	-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
A18	BK6_IO31	DATA0	141N	BK6_IO19	DATA0	87N	BK6_IO19	DATA0	75N
D18	BK6_IO32	-	142P	BK6_IO20		88P	BK6_IO20	-	76P
C18	BK6_IO33	-	142N	BK6_IO21		88N	BK6_IO21	-	76N
B18	BK6_IO34	-	143P	BK6_IO22		89P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-	-	-	-
C17	BK6_IO35	-	143N	BK6_IO23		89N	NC	-	-
B17	BK6_IO36	-	144P	NC	-	-	NC	-	-
A17	BK6_IO37	-	144N	NC	-	-	NC	-	-
D16	BK6_IO38	-	145P	NC	-	-	NC	-	-
C16	BK6_IO39	-	145N	NC	-	-	NC	-	-
B16	BK6_IO40	-	146P	BK6_IO24	-	90P	NC	-	-
A16	BK6_IO41	-	146N	BK6_IO25	-	90N	NC	-	-
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-	-	-	-
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-	-	-	-
A15	BK7_IO0	-	147P	BK7_IO0	-	91P	BK7_IO0	-	77P
B15	BK7_IO1	-	147N	BK7_IO1	-	91N	BK7_IO1	-	77N
C15	BK7_IO2	-	148P	BK7_IO2	-	92P	BK7_IO2	-	78P
-	-	-	-	-	-	-	GND (Bank 7)	-	-
D15	BK7_IO3	-	148N	BK7_IO3	-	92N	BK7_IO3	-	78N
A14	BK7_IO4	-	149P	BK7_IO4	-	93P	BK7_IO4	-	79P
B14	BK7_IO5	-	149N	BK7_IO5	-	93N	BK7_IO5	-	79N
C14	BK7_IO6	-	150P	BK7_IO6	-	94P	NC	-	-
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-	-	-	-
A13	BK7_IO7	-	150N	BK7_IO7	-	94N	NC	-	-
B13	BK7_IO8	-	151P	BK7_IO8	-	95P	NC	-	-
C13	BK7_IO9	-	151N	BK7_IO9	-	95N	NC	-	-
D13	BK7_IO10	-	152P	BK7_IO10	-	96P	BK7_IO6	-	80P
B12	BK7_IO11	-	152N	BK7_IO11	-	96N	BK7_IO7	-	80N
C12	BK7_IO12	-	153P	BK7_IO12	-	97P	BK7_IO8	-	81P
-	-	-	-	-	-	-	GND (Bank 7)	-	-
A12	BK7_IO13	-	153N	BK7_IO13		97N	BK7_IO9	-	81N
A11	BK7_IO14	-	154P	BK7_IO14	-	98P	BK7_IO10	-	82P
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-	-	-	-
B11	BK7_IO15	-	154N	BK7_IO15	-	98N	BK7_IO11	-	82N
C11	BK7_IO16	-	155P	NC	-	-	NC	-	-
D11	BK7_IO17	-	155N	NC	-	-	NC	-	-

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
A33	BK1_IO45	-	53N/HSI4
C33	BK1_IO46	HSI4A_SINP	54P/HSI4
B33	BK1_IO47	HSI4A_SINN	54N/HSI4
A34	BK1_IO48	-	55P/HSI4
A35	BK1_IO49	VREF1	55N/HSI4
D32	BK1_IO50	HSI4B_SOUTP	56P/HSI4
-	GND (Bank 1)	-	-
D33	BK1_IO51	HSI4B_SOUTN	56N/HSI4
E32	BK1_IO52	-	57P
C34	BK1_IO53	-	57N
B34	BK1_IO54	HSI4B_SINP	58P
B35	BK1_IO55	HSI4B_SINN	58N
A36	BK1_IO56	-	59P
D34	BK1_IO57	-	59N
C35	BK1_IO58	-	60P
-	GND (Bank 1)	-	-
E34	BK1_IO59	-	60N
B36	BK1_IO60	-	61P
C36	BK1_IO61	-	61N
D39	TCK	-	-
D37	TMS	-	-
D38	TOE	-	-
E37	BK2_IO0	-	62P
F35	BK2_IO1	-	62N
E39	BK2_IO2	-	63P
-	GND (Bank 2)	-	-
F39	BK2_IO3	-	63N
F36	BK2_IO4	-	64P
E38	BK2_IO5	-	64N
G38	BK2_IO6	-	65P
F37	BK2_IO7	-	65N
G36	BK2_IO8	-	66P
G39	BK2_IO9	-	66N
H35	BK2_IO10	-	67P
-	GND (Bank 2)	-	-
F38	BK2_IO11	-	67N
J37	BK2_IO12	VREF2	68P
H36	BK2_IO13	-	68N
G37	BK2_IO14	-	69P
H37	BK2_IO15	-	69N
H39	BK2_IO16	-	70P
K35	BK2_IO17	-	70N
J36	BK2_IO18	-	71P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
-	GND (Bank 2)	-	-
K36	BK2_IO19	-	71N
H38	BK2_IO20	-	72P
J38	BK2_IO21	-	72N
J39	BK2_IO22	-	73P
L36	BK2_IO23	-	73N
K38	BK2_IO24	-	74P
M36	BK2_IO25	-	74N
L37	BK2_IO26	-	75P
-	GND (Bank 2)	-	-
K39	BK2_IO27	-	75N
L38	BK2_IO28	-	76P
P35	BK2_IO29	-	76N
N36	BK2_IO30	-	77P
M37	BK2_IO31	-	77N
L39	BK2_IO32	-	78P
M38	BK2_IO33	-	78N
M39	BK2_IO34	-	79P
-	GND (Bank 2)	-	-
P36	BK2_IO35	-	79N
R36	BK2_IO36	-	80P
N37	BK2_IO37	-	80N
P38	BK2_IO38	-	81P
T35	BK2_IO39	-	81N
R37	BK2_IO40	-	82P
R38	BK2_IO41	-	82N
P39	BK2_IO42	-	83P
-	GND (Bank 2)	-	-
R39	BK2_IO43	-	83N
T38	BK2_IO44	-	84P
T36	BK2_IO45	-	84N
T37	BK2_IO46	-	85P
U36	BK2_IO47	-	85N
U37	BK2_IO48	-	86P
T39	BK2_IO49	-	86N
V36	BK2_IO50	-	87P
-	GND (Bank 2)	-	-
U38	BK2_IO51	-	87N
U39	BK2_IO52	-	88P
V38	BK2_IO53	-	88N
V37	BK2_IO54	-	89P
W36	BK2_IO55	-	89N
W35	BK2_IO56	-	90P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
AH39	BK3_IO31	-	108N
AK39	BK3_IO32	-	109P
AK38	BK3_IO33	-	109N
AF35	BK3_IO34	-	110P
-	GND (Bank 3)	-	-
AJ37	BK3_IO35	-	110N
AH36	BK3_IO36	-	111P
AM39	BK3_IO37	-	111N
AL38	BK3_IO38	-	112P
AL39	BK3_IO39	-	112N
AJ36	BK3_IO40	-	113P
AH35	BK3_IO41	-	113N
AL37	BK3_IO42	-	114P
-	GND (Bank 3)	-	-
AN38	BK3_IO43	-	114N
AM38	BK3_IO44	-	115P
AK36	BK3_IO45	-	115N
AM37	BK3_IO46	-	116P
AN37	BK3_IO47	-	116N
AN39	BK3_IO48	-	117P
AL36	BK3_IO49	VREF3	117N
AK35	BK3_IO50	-	118P
-	GND (Bank 3)	-	-
AP39	BK3_IO51	-	118N
AM36	BK3_IO52	-	119P
AP38	BK3_IO53	-	119N
AR39	BK3_IO54	-	120P
AN36	BK3_IO55	-	120N
AM35	BK3_IO56	-	121P
AR38	BK3_IO57	-	121N
AP37	BK3_IO58	-	122P
-	GND (Bank 3)	-	-
AT39	BK3_IO59	-	122N
AR37	BK3_IO60	-	123P
AP36	BK3_IO61	-	123N
AT38	GSR	-	-
AP35	DXP	-	-
AT37	DXN	-	-
AU36	BK4_IO0	-	124P
AV36	BK4_IO1	-	124N
AR34	BK4_IO2	-	125P
-	GND (Bank 4)	-	-
AW36	BK4_IO3	-	125N

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
-	GND (Bank 4)	-	-
AW26	BK4_IO43	-	145N
AV25	BK4_IO44	-	146P
AT24	BK4_IO45	-	146N
AU24	BK4_IO46	-	147P
AU25	BK4_IO47	-	147N
AW25	BK4_IO48	PLL_RST4	148P
AW24	BK4_IO49	PLL_RST5	148N
AU23	BK4_IO50	-	149P
-	GND (Bank 4)	-	-
AT23	BK4_IO51	-	149N
AV24	BK4_IO52	-	150P
AW23	BK4_IO53	-	150N
AV23	BK4_IO54	SS_CLKIN1P	151P
AU22	BK4_IO55	SS_CLKIN1N	151N
AR21	BK4_IO56	PLL_FBK4	152P
AT22	BK4_IO57	PLL_FBK5	152N
AV22	BK4_IO58	SS_CLKOUT1P	153P
-	GND (Bank 4)	-	-
AV21	BK4_IO59	SS_CLKOUT1N	153N
AT21	BK4_IO60	CLK_OUT4	154P
AU21	BK4_IO61	CLK_OUT5	154N
-	GND (Bank 4)	-	-
AT19	GCLK4	-	LVDS Pair2P
AU19	GCLK5	-	LVDS Pair2N
AW22	VCCP1	-	-
AR20	GNDP1	-	-
AU18	GCLK6	-	LVDS Pair3P
AT18	GCLK7	-	LVDS Pair3N
-	GND (Bank 5)	-	-
AV17	BK5_IO0	CLK_OUT6	155P
AV18	BK5_IO1	CLK_OUT7	155N
AW21	BK5_IO2	PLL_FBK6	156P
-	GND (Bank 5)	-	-
AV19	BK5_IO3	PLL_FBK7	156N
AR19	BK5_IO4	-	157P/HSI7
AW19	BK5_IO5	-	157N/HSI7
AW18	BK5_IO6	PLL_RST6	158P/HSI7
AW17	BK5_IO7	PLL_RST7	158N/HSI7
AT17	BK5_IO8	-	159P/HSI7
AV16	BK5_IO9	-	159N/HSI7
AU17	BK5_IO10	HSI7A_SINP	160P/HSI7
-	GND (Bank 5)	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
-	-	-	-	GND (Bank 1)	-	-
T1	BK1_IO1	CLK_OUT3	31N	BK1_IO1	CLK_OUT3	21N
U2	BK1_IO2	SS_CLKOUT0P	32P	BK1_IO2	SS_CLKOUT0P	22P
-	GND (Bank 1)	-	-	-	-	-
U1	BK1_IO3	SS_CLKOUT0N	32N	BK1_IO3	SS_CLKOUT0N	22N
U3	BK1_IO4	PLL_FBK2	33P	BK1_IO4	PLL_FBK2	23P
U4	BK1_IO5	PLL_FBK3	33N	BK1_IO5	PLL_FBK3	23N
V1	BK1_IO6	SS_CLKIN0P	34P	BK1_IO10	SS_CLKIN0P	26P
V2	BK1_IO7	SS_CLKIN0N	34N	BK1_IO11	SS_CLKIN0N	26N
U5	BK1_IO8	-	35P	BK1_IO12	-	27P
U6	BK1_IO9	-	35N	BK1_IO13	-	27N
V4	BK1_IO10	-	36P	BK1_IO6	-	24P
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-
V3	BK1_IO11	-	36N	BK1_IO7	-	24N
V6	BK1_IO12	PLL_RST2	37P	BK1_IO20	PLL_RST2	31P
V7	BK1_IO13	PLL_RST3	37N	BK1_IO21	PLL_RST3	31N
W1	BK1_IO14	-	38P	BK1_IO8	-	25P
W2	BK1_IO15	-	38N	BK1_IO9	-	25N
W3	BK1_IO16	-	39P	BK1_IO14	-	28P
-	-	-	-	GND (Bank 1)	-	-
W4	BK1_IO17	-	39N	BK1_IO15	-	28N
W5	BK1_IO18	-	40P	BK1_IO16	-	29P
-	GND (Bank 1)	-	-	-	-	-
W6	BK1_IO19	-	40N	BK1_IO17	-	29N
Y6	BK1_IO20	-	41P/HSI3	NC	-	-
Y5	BK1_IO21	-	41N/HSI3	NC	-	-
Y4	BK1_IO22	-	42P/HSI3	NC	-	-
Y3	BK1_IO23	-	42N/HSI3	NC	-	-
AA5	BK1_IO24	-	43P/HSI3	NC	-	-
AA4	BK1_IO25	-	43N/HSI3	NC	-	-
Y2	BK1_IO26	HSI3A_SOUTP	44P/HSI3	BK1_IO18	HSI2A_SOUTP	30P
-	GND (Bank 1)	-	-	-	-	-
Y1	BK1_IO27	HSI3A_SOUTN	44N/HSI3	BK1_IO19	HSI2A_SOUTN	30N
AB7	BK1_IO28	-	45P/HSI3	NC	-	-
AB6	BK1_IO29	-	45N/HSI3	NC	-	-
AA2	BK1_IO30	HSI3A_SINP	46P/HSI3	BK1_IO22	HSI2A_SINP	32P
-	-	-	-	GND (Bank 1)	-	-
AA1	BK1_IO31	HSI3A_SINN	46N/HSI3	BK1_IO23	HSI2A_SINN	32N
AB5	BK1_IO32	-	47P/HSI3	NC	-	-
AB4	BK1_IO33	-	47N/HSI3	NC	-	-
AB2	BK1_IO34	HSI3B_SOUTP	48P/HSI3	NC	-	-
-	GND (Bank 1)	-	-	-	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AB1	BK1_IO35	HSI3B_SOUTN	48N/HSI3	NC	-	-
AC6	BK1_IO36	-	49P/HSI4	NC	-	-
AC5	BK1_IO37	-	49N/HSI4	NC	-	-
AC2	BK1_IO38	HSI3B_SINP	50P/HSI4	NC	-	-
AC1	BK1_IO39	HSI3B_SINN	50N/HSI4	NC	-	-
AC4	BK1_IO40	-	51P/HSI4	NC	-	-
AC3	BK1_IO41	-	51N/HSI4	NC	-	-
AD2	BK1_IO42	HSI4A_SOUTP	52P/HSI4	NC	-	-
-	GND (Bank 1)	-	-	-	-	-
AD1	BK1_IO43	HSI4A_SOUTN	52N/HSI4	NC	-	-
AD3	BK1_IO44	-	53P/HSI4	BK1_IO32	-	37P/HSI3
AD4	BK1_IO45	-	53N/HSI4	BK1_IO33	-	37N
AE2	BK1_IO46	HSI4A_SINP	54P/HSI4	BK1_IO34	-	38P
AE1	BK1_IO47	HSI4A_SINN	54N/HSI4	BK1_IO35	-	38N
AD5	BK1_IO48	-	55P/HSI4	BK1_IO25	-	33N
AD6	BK1_IO49	VREF1	55N/HSI4	BK1_IO24	VREF1	33P
AF2	BK1_IO50	HSI4B_SOUTP	56P/HSI4	BK1_IO26	HSI2B_SOUTP	34P
-	GND (Bank 1)	-	-	-	-	-
AF1	BK1_IO51	HSI4B_SOUTN	56N/HSI4	BK1_IO27	HSI2B_SOUTN	34N
AE3	BK1_IO52	-	57P	BK1_IO28	-	35P
AE4	BK1_IO53	-	57N	BK1_IO29	-	35N
AG1	BK1_IO54	HSI4B_SINP	58P	BK1_IO30	HSI2B_SINP	36P
-	-	-	-	GND (Bank 1)	-	-
AG2	BK1_IO55	HSI4B_SINN	58N	BK1_IO31	HSI2B_SINN	36N
AE5	BK1_IO56	-	59P	BK1_IO36	-	39P
AF4	BK1_IO57	-	59N	BK1_IO37	-	39N
AH1	BK1_IO58	-	60P	BK1_IO38	-	40P
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-
AH2	BK1_IO59	-	60N	BK1_IO39	-	40N
AF3	BK1_IO60	-	61P	BK1_IO40	-	41P
AG3	BK1_IO61	-	61N	BK1_IO41	-	41N
AH4	TCK	-	-	TCK	-	-
AJ3	TMS	-	-	TMS	-	-
AK3	TOE	-	-	TOE	-	-
AG5	BK2_IO0	-	62P	BK2_IO0	-	42P
AH5	BK2_IO1	-	62N	BK2_IO1	-	42N
AJ4	BK2_IO2	-	63P	BK2_IO2	-	43P
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
AK4	BK2_IO3	-	63N	BK2_IO3	-	43N
AG6	BK2_IO4	-	64P	BK2_IO4	-	44P
AH6	BK2_IO5	-	64N	BK2_IO5	-	44N
AJ5	BK2_IO6	-	65P	BK2_IO6	-	45P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AK5	BK2_IO7	-	65N	BK2_IO7	-	45N
AE7	BK2_IO8	-	66P	BK2_IO8	-	46P
AF7	BK2_IO9	-	66N	BK2_IO9	-	46N
AG7	BK2_IO10	-	67P	BK2_IO10	-	47P
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
AH7	BK2_IO11	-	67N	BK2_IO11	-	47N
AE8	BK2_IO12	VREF2	68P	BK2_IO21	VREF2	52N
AF8	BK2_IO13	-	68N	BK2_IO20	-	52P
AJ6	BK2_IO14	-	69P	BK2_IO12	-	48P
AK6	BK2_IO15	-	69N	BK2_IO13	-	48N
AG8	BK2_IO16	-	70P	BK2_IO14	-	49P
AH8	BK2_IO17	-	70N	BK2_IO15	-	49N
AJ7	BK2_IO18	-	71P	BK2_IO16	-	50P
-	GND (Bank 2)	-	-	-	-	-
AK7	BK2_IO19	-	71N	BK2_IO17	-	50N
AF9	BK2_IO20	-	72P	BK2_IO18	-	51P
-	-	-	-	GND (Bank 2)	-	-
AG9	BK2_IO21	-	72N	BK2_IO19	-	51N
AJ8	BK2_IO22	-	73P	NC	-	-
AK8	BK2_IO23	-	73N	NC	-	-
AD10	BK2_IO24	-	74P	NC	-	-
AE10	BK2_IO25	-	74N	NC	-	-
AJ9	BK2_IO26	-	75P	NC	-	-
-	GND (Bank 2)	-	-	-	-	-
AK9	BK2_IO27	-	75N	NC	-	-
AF10	BK2_IO28	-	76P	NC	-	-
AG10	BK2_IO29	-	76N	NC	-	-
AK10	BK2_IO30	-	77P	NC	-	-
AJ10	BK2_IO31	-	77N	NC	-	-
AE11	BK2_IO32	-	78P	NC	-	-
AF11	BK2_IO33	-	78N	NC	-	-
AG11	BK2_IO34	-	79P	NC	-	-
-	GND (Bank 2)	-	-	-	-	-
AH11	BK2_IO35	-	79N	NC	-	-
AE12	BK2_IO36	-	80P	NC	-	-
AF12	BK2_IO37	-	80N	NC	-	-
AJ11	BK2_IO38	-	81P	NC	-	-
AK11	BK2_IO39	-	81N	NC	-	-
AG12	BK2_IO40	-	82P	NC	-	-
AH12	BK2_IO41	-	82N	NC	-	-
AK12	BK2_IO42	-	83P	BK2_IO22	-	53P
-	GND (Bank 2)	-	-	-	-	-

Part Number Description

LFX XXXX X X – XX XXXXX X

Device Family
LFX

Gates
125 = 139K Gates
200 = 210K Gates
500 = 476K Gates
1200 = 1.25M Gates[1]

sysHSI Support
Blank = Supports sysHSI
E = No sysHSI Support

Power Supply Voltage
B = 2.5/3.3V
C = 1.8V

Grade
C = Commercial
I = Industrial

Package
F256 = 256-Ball fpBGA
FH516 = 516-Ball fpBGA (with Heat Spreader)
F516 = 516-Ball fpBGA (without Heat Spreader)
FE680 = 680-Ball fpSBGA
F900 = 900-Ball fpBGA
FN256 = Lead-Free 256-Ball fpBGA
FN900 = Lead-Free 900-Ball fpBGA[2]

Speed
5 = Fastest
4
3 = Slowest

1. Discontinued via PCN #03A-10.
2. Select products only. See Ordering Information tables below for specific support.

Ordering Information

Conventional Packaging

Commercial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125B-05F256C	139K	2.5/3.3	-5	fpBGA	256
LFX125B-04F256C	139K	2.5/3.3	-4	fpBGA	256
LFX125B-03F256C	139K	2.5/3.3	-3	fpBGA	256
LFX125C-04F256C	139K	1.8	-4	fpBGA	256
LFX125C-03F256C	139K	1.8	-3	fpBGA	256
LFX125B-05F516C	139K	2.5/3.3	-5	fpBGA	516
LFX125B-04F516C	139K	2.5/3.3	-4	fpBGA	516
LFX125B-03F516C	139K	2.5/3.3	-3	fpBGA	516
LFX125C-04F516C	139K	1.8	-4	fpBGA	516
LFX125C-03F516C	139K	1.8	-3	fpBGA	516
LFX125B-05FH516C[1]	139K	2.5/3.3	-5	fpBGA	516
LFX125B-04FH516C[1]	139K	2.5/3.3	-4	fpBGA	516
LFX125B-03FH516C[1]	139K	2.5/3.3	-3	fpBGA	516
LFX125C-04FH516C[1]	139K	1.8	-4	fpBGA	516
LFX125C-03FH516C[1]	139K	1.8	-3	fpBGA	516
LFX200B-05F256C	210K	2.5/3.3	-5	fpBGA	256
LFX200B-04F256C	210K	2.5/3.3	-4	fpBGA	256
LFX200B-03F256C	210K	2.5/3.3	-3	fpBGA	256
LFX200C-04F256C	210K	1.8	-4	fpBGA	256
LFX200C-03F256C	210K	1.8	-3	fpBGA	256

Revision History (Cont.)

Date	Version	Change Summary
June 2004 (cont.)	08.0 (cont.)	Updated Global Clock Input Setup time specifications.
		Clarification of Serial Out LVDS test condition.
		Clarification of REFCLK, SS_CLKIN peak-to-peak period jitter condition.
		Added sysHSI Reserved pins and footnote.
		Removed industrial ordering part numbers.
July 2004	09.0	Added “E” Series product family.
August 2004	10.0	Final release.
December 2004	10.1	Updated NC Connections table.
April 2005	10.2	Clarification of IDK specification.
April 2005	11.0	Select lead-free packages release.
July 2005	12.0	Added lead-free 516 fpBGA ordering part numbers.
April 2007	13.0	Removed lead-free 680 fpSBGA information from Part Number Description and Ordering Part Number tables. Removed lead-free 516 fpBGA for LFX125 from Ordering Part Number tables.
November 2007	14.0	Removed lead-free 516 fpBGA information from Part Number Description and Ordering Part Number tables.
July 2008	14.1	Added 516 fpBGA package without heat spreader to Part Number Description and Ordering Part Number tables.
February 2010	15.0	Ordering part numbers and ispXPGA Family Selection Guide table have been updated per PCN #03A-10 (discontinuation of the ispXPGA 1200 devices).
		References to "system gates" changed to "functional gates."