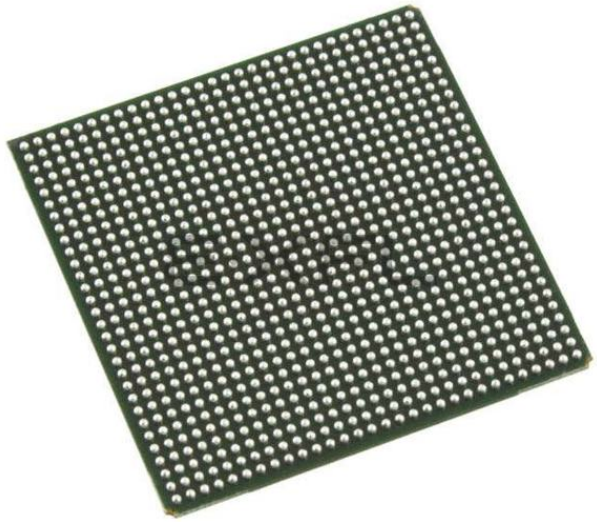
Lattice Semiconductor Corporation - LFX1200EC-03F900I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

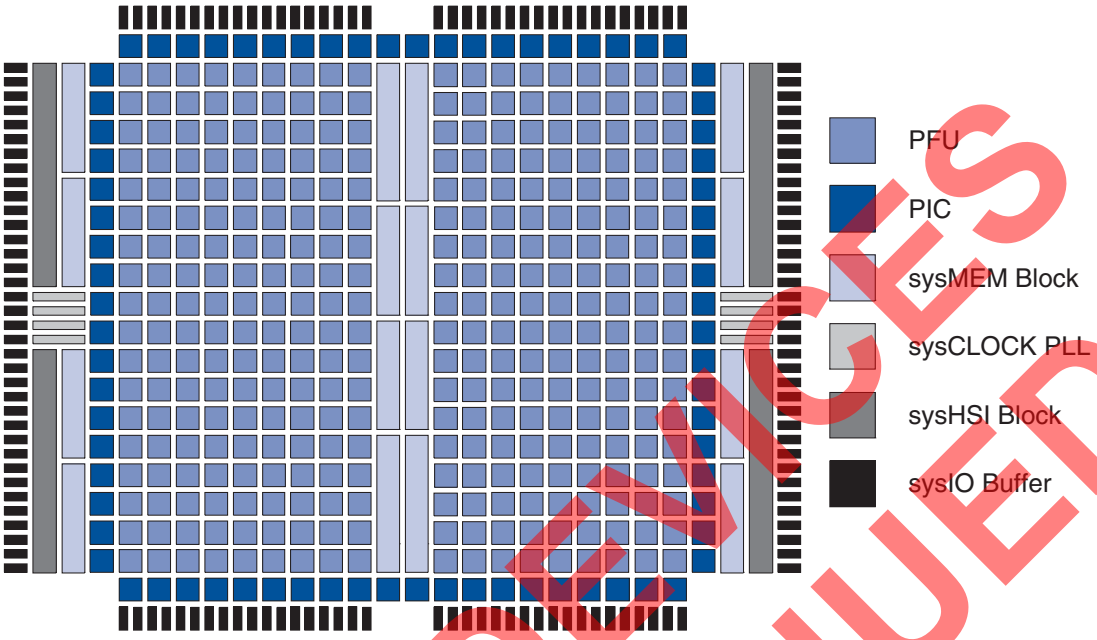
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	15376
Total RAM Bits	423936
Number of I/O	496
Number of Gates	1250000
Voltage - Supply	1.65V ~ 1.95V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx1200ec-03f900i

Figure 1. ispXPGA Block Diagram



Programmable Function Unit

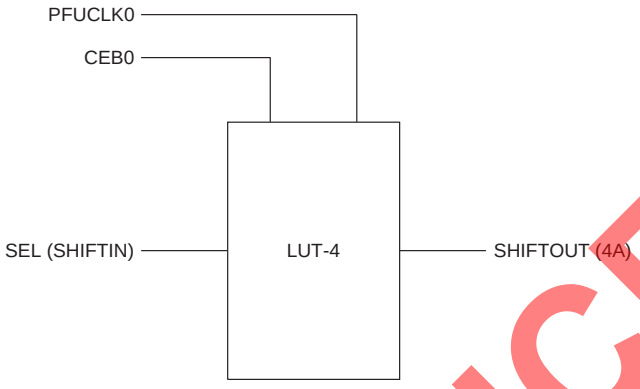
The Programmable Function Unit (PFU) is the basic building block of the ispXPGA architecture. The PFUs are arranged in rows and columns in the device with PFU (1,1) referring to (row 1, column 1). Each PFU consists of four Configurable Logic Elements (CLEs), four Configurable Sequential Elements (CSEs), and a Wide Logic Generator (WLG). By utilizing these components, the PFU can implement a variety of functions. Table 3 lists some of the function capabilities of the PFU.

There are 57 inputs to each PFU and nine outputs. The PFU uses 20 inputs for logic, and 37 inputs drive the control logic from which six control signals are derived for the PFU.

Table 3. Function Capability of ispXPGA PFU

Function	Capability
Look-up table	LUT-4, LUT-5, LUT-6
Wide logic functions	Up to 20 input logic functions
Multiplexing	2:1, 4:1, 8:1
Arithmetic logic	Dedicated carry chain and booth multiplication logic
Single-port RAM	16X1, 16X2, 16X4, 32X1, 32X2, 64X1
Double-port RAM	16X1, 16X2, 32X1
Shift register	8-bit shift registers (up to 32-bit shift capability)

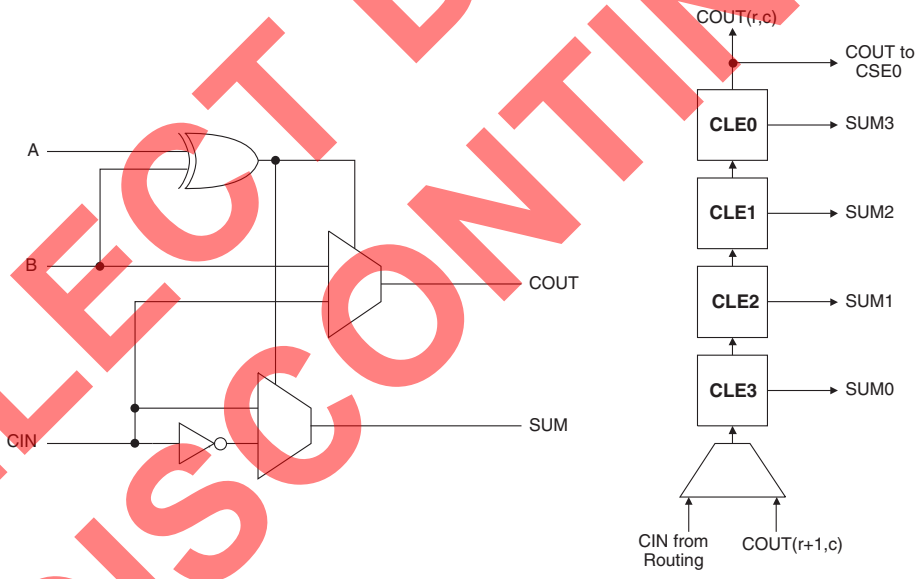
Figure 4. LUT in Shift Register Mode



Carry Chain Generator

The Carry Chain Generator is useful for implementing high-speed arithmetic functions. The CCG consists of a two-input XOR gate whose carryout can be cascaded with the input of the adjacent CCG. As shown in Figure 5, the carryin signal feeds CLE3 of the PFU and is propagated through CLE2 and CLE1 before reaching CLE0. The sum output of the CCG can be fed to the CSE through the WLG. The carryout must propagate to CLE0 for use outside the PFU. The carryout from the PFU can feed the W0 input of CSE0. The CCG also helps to effectively implement wider functions by using its logic elements to expand the capabilities of the LUT-4.

Figure 5. Carry Chain Generator



Wide Logic Generator

The WLG contains the logic necessary to implement wide gate functions. This is made up of a set of multiplexers that are located between the CLE and the CSE. The WLG helps in enhancing the wide gating capability of the PFU. The outputs of each CLE can be cascaded in the WLG to build wide gating functions. Wide multiplexing functions are also possible with a similar use of the WLG. Figure 6 illustrates the WLG.

High Speed Serial Interface Block (sysHSI Block)[1]

The High Speed Serial Interface (sysHSI) allows high speed serial data transfer over a pair of LVDS I/O. The ispXPGA devices have multiple sysHSI blocks.

Each sysHSI block has two SERDES blocks which contain two main sub-blocks, Transmitter (with a serializer) and Receiver (with a deserializer) including Clock/Data Recovery Circuit (CDR). Each SERDES can be used as a full duplex channel. The two SERDES in sysHSI blocks share a common clock and must operate at the same nominal frequency. Figure 20 shows the sysHSI block.

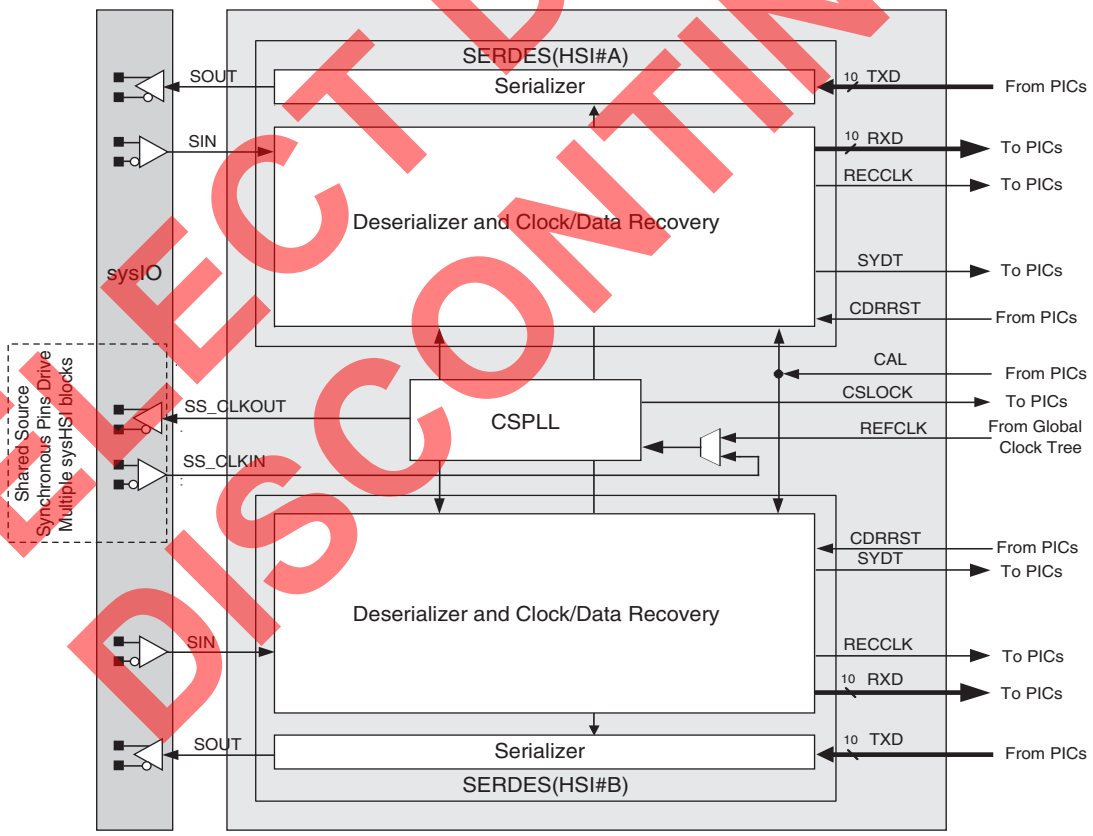
Device features support two data coding modes: 10B/12B and 8B/10B (for use with other encoding schemes, see Lattice's sysHSI technical notes). The encoding and decoding of the 10B/12B standard are performed within the sysHSI block. For the 8B/10B standard, the symbol boundaries are aligned internally but the encoding and decoding are performed outside the sysHSI block.

Each SERDES block receives a single high speed serial data input stream (with embedded clock) from an input, and provide a low speed 10-bit wide data stream and a recovered clock to the device. For transmitting, SERDES converts a 10-bit wide low-speed data stream to a single high-speed data stream with embedded clock for output.

Additionally, multiple sysHSI blocks can be grouped together to form a source synchronous interface of 1-10 channels.

For more information on the SERDES/CDR, refer to TN1020, sysHSI Usage Guidelines.

Figure 20. sysHSI Block Diagram



1. "E-Series" does not support sysHSI.

sysIO Recommended Operating Conditions

Standard	V_{CCO} (V)[1]			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.0	3.3	3.6	-	-	-
LVCMOS 2.5	2.3	2.5	2.7	-	-	-
LVCMOS 1.8[2]	1.65	1.8	1.95	-	-	-
LVTTL	3.0	3.3	3.6	-	-	-
PCI 3.3	3.0	3.3	3.6	-	-	-
AGP-1X	3.15	3.3	3.45	-	-	-
SSTL 2	2.3	2.5	2.7	1.15	1.25	1.35
SSTL 3	3.0	3.3	3.6	1.3	1.5	1.7
CTT 3.3	3.0	3.3	3.6	1.35	1.5	1.65
CTT 2.5	2.3	2.5	2.7	1.35	1.5	1.65
HSTL Class I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL Class III	1.4	1.5	1.6	-	0.9	-
GTL+	-	-	-	0.882	1.0	1.122
LVDS	2.3	2.5	2.7	-	-	-
LVPECL	3.0	3.3	3.6	-	-	-
BLVDS	2.3	2.5	2.7	-	-	-

1. Inputs independent of V_{CCO}.
2. Design tool default setting.

ispXPGA 125B/C & ispXPGA 125EB/EC Timing Adders

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	4.28	—	4.6	—	5.29	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

ispXPGA 200B/C & ispXPGA 200EB/EC PFU Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Set								
t_{LASSRO}	Asynchronous Set/Reset to Output	—	1.09	—	1.17	—	1.35	ns
$t_{LASSRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{LASSRR}	Asynchronous Set/Reset Recovery	—	0.51	—	0.55	—	0.63	ns
t_{LSSR_S}	Synchronous Set/Reset Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{LSSR_H}	Synchronous Set/Reset Hold Time	0.03	—	0.03	—	0.03	—	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.
2. $t_{LCTHRUL}$ quoted bit by bit.

Timing v.0.3

ispXPGA 200B/C & ispXPGA 200EB/EC PIC Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Register/Latch Delays								
t_{IO_CO}	Register Clock to Output Delay	—	0.93	—	1.00	—	1.15	ns
t_{IO_S}	Register Setup Time (Data before Clock)	0.05	—	0.05	—	0.06	—	ns
t_{IO_H}	Register Hold Time (Data after Clock)	0.06	—	0.06	—	0.07	—	ns
t_{IOCE_S}	Register Clock Enable Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{IOCE_H}	Register Clock Enable Hold Time	0.13	—	0.13	—	0.15	—	ns
t_{IO_GO}	Latch Gate to Output Delay	—	0.72	—	0.77	—	0.89	ns
t_{IOL_S}	Latch Setup Time	0.05	—	0.05	—	0.06	—	ns
t_{IOL_H}	Latch Hold Time	0.06	—	0.06	—	0.07	—	ns
t_{IOLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns
t_{IOASRO}	Asynchronous Set/Reset to Output	—	1.04	—	1.12	—	1.29	ns
$t_{IOASRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{IOASRR}	Asynchronous Set/Reset Recovery Time	—	0.23	—	0.25	—	0.29	ns
Input/Output Delays								
t_{IOBUF}	Output Buffer Delay	—	0.97	—	1.04	—	1.20	ns
t_{IOIN}	Input Buffer Delay	—	0.60	—	0.64	—	0.74	ns
t_{IOEN}	Output Enable Delay	—	0.53	—	0.57	—	0.66	ns
t_{IODIS}	Output Disable Delay	—	-0.13	—	-0.12	—	-0.10	ns
t_{IOFT}	Feed-thru Delay	—	0.19	—	0.20	—	0.23	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 200B/C & ispXPGA 200EB/EC Timing Adders

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	4.84	—	5.2	—	5.98	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

ispXPGA 500B/C & ispXPGA 500EB/EC Timing Adders (Cont.)

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LVCMOS_33_4mA_out	Using 3.3V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_33_5.33mA_out	Using 3.3V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_33_8mA_out	Using 3.3V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_33_12mA_out	Using 3.3V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_33_16mA_out	Using 3.3V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_33_24mA_out	Using 3.3V CMOS Standard, 24mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_out	Using AGP 1x Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
CTT25_out	Using CTT 2.5V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
CTT33_out	Using CTT 3.3V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
GTL+_out	Using GTL+	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_out	Using HSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_out	Using HSTL 2.5V, Class III	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVDS_out	Using Low Voltage Differential Signaling (LVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
BLVDS_out	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVPECL_out	Using Low Voltage PECL	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
PCI_out	Using PCI Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL2_I_out	Using SSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL2_II_out	Using SSTL 2.5V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_out	Using SSTL 3.3V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL3_II_out	Using SSTL 3.3V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

1. Only available for ispXPGA 500B and ispXPGA 500EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 1200B/C & ispXPGA 1200EB/EC PFU Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Functional Delays								
LUTs								
t_{LUT4}	4-Input LUT Delay	—	0.41	—	0.44	—	0.51	ns
t_{LUT5}	5-Input LUT Delay	—	0.73	—	0.79	—	0.91	ns
t_{LUT6}	6-Input LUT Delay	—	0.86	—	0.93	—	1.07	ns
Shift Register (LUT)								
t_{LSR_S}	Shift Register Setup Time	-0.64	—	-0.62	—	-0.53	—	ns
t_{LSR_H}	Shift Register Hold Time	0.61	—	0.63	—	0.72	—	ns
t_{LSR_CO}	Shift Register Clock to Output Delay	—	0.70	—	0.75	—	0.86	ns
Arithmetic Functions								
$t_{LCTHRUR}$	MC (Macro Cell) Carry In to MC Carry Out Delay (Ripple)	—	0.08	—	0.09	—	0.10	ns
$t_{LCTHRUL}$[2]	MC Carry In to MC Carry Out Delay (Look Ahead)	—	0.05	—	0.05	—	0.06	ns
t_{LSTHRU}	MC Sum In to MC Sum Out Delay	—	0.42	—	0.45	—	0.52	ns
$t_{LSINCOUT}$	MC Sum In to MC Carry Out Delay	—	0.29	—	0.31	—	0.36	ns
$t_{LCINSOUTR}$	MC Carry In to MC Sum Out Delay (Ripple)	—	0.36	—	0.39	—	0.45	ns
$t_{LCINSOUTL}$	MC Carry In to MC Sum Out Delay (Look Ahead)	—	0.26	—	0.28	—	0.32	ns
Feed-thru								
t_{LFT}	PFU Feed-Thru Delay	—	0.15	—	0.16	—	0.18	ns
Distributed RAM								
t_{LRAM_CO}	Clock to RAM Output	—	1.24	—	1.33	—	1.53	ns
t_{LRAMAD_S}	Address Setup Time	-0.41	—	-0.40	—	-0.34	—	ns
t_{LRAMD_S}	Data Setup Time	0.21	—	0.22	—	0.25	—	ns
t_{LRAMWE_S}	Write Enable Setup Time	0.45	—	0.46	—	0.53	—	ns
t_{LRAMAD_H}	Address Hold Time	0.58	—	0.60	—	0.69	—	ns
t_{LRAMD_H}	Data Hold Time	0.11	—	0.11	—	0.13	—	ns
t_{LRAMWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{LRAMCPW}$	Clock Pulse Width (High or Low)	2.91	—	3.00	—	3.45	—	ns
$t_{LRAMADO}$	Address to Output Delay	—	0.86	—	0.93	—	1.07	ns
Register/Latch Delays								
Registers								
t_{L_CO}	Register Clock to Output Delay	—	0.58	—	0.62	—	0.71	ns
t_{L_S}	Register Setup Time (Data before Clock)	0.14	—	0.14	—	0.16	—	ns
t_{L_H}	Register Hold Time (Data after Clock)	-0.12	—	-0.12	—	-0.10	—	ns
t_{LCE_S}	Register Clock Enable Setup Time	-0.11	—	-0.11	—	-0.09	—	ns
t_{LCE_H}	Register Clock Enable Hold Time	0.11	—	0.11	—	0.13	—	ns
Latches								
t_{L_GO}	Latch Gate to Output Delay	—	0.09	—	0.10	—	0.12	ns
t_{LL_S}	Latch Setup Time	0.14	—	0.14	—	0.16	—	ns
t_{LL_H}	Latch Hold Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{LLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns

ispXPGA 1200B/C & ispXPGA 1200EB/EC Timing Adders (Cont.)

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LVCMOS_33_4mA_out	Using 3.3V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_33_5.33mA_out	Using 3.3V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_33_8mA_out	Using 3.3V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_33_12mA_out	Using 3.3V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_33_16mA_out	Using 3.3V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_33_24mA_out	Using 3.3V CMOS Standard, 24mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_out	Using AGP 1x Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
CTT25_out	Using CTT 2.5V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
CTT33_out	Using CTT 3.3V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
GTL+_out	Using GTL+	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_out	Using HSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_out	Using HSTL 2.5V, Class III	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVDS_out	Using Low Voltage Differential Signaling (LVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
BLVDS_out	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVPECL_out	Using Low Voltage PECL	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
PCI_out	Using PCI Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL2_I_out	Using SSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL2_II_out	Using SSTL 2.5V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_out	Using SSTL 3.3V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL3_II_out	Using SSTL 3.3V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

1. Only available for ispXPGA 1200B and ispXPGA 1200EB (2.5V/3.3V) devices.

Timing v.2.1

ispXP sysCONFIG Port Timing Specifications

Symbol	Timing Parameter	Min.	Typ.	Max.	Units
sysCONFIG Write Cycle Timing					
t_{SUCS}	Input setup time of CS to CCLK rise	10	—	—	ns
t_{HCS}	Hold time of CS to CCLK Rise	0	—	—	ns
t_{SUWD}	Input setup time of write data to CCLK rise	12	—	—	ns
t_{HWD}	Hold time of write data to CCLK rise	0	—	—	ns
t_{PRGM}	Low time to reset device SRAM	5	—	50	ns
t_{WINIT}	INIT pulse width	—	—	5	ms
t_{IODISS}	User I/O disable	—	—	30	ns
t_{IOENSS}	User I/O enable	—	—	30	ns
t_{WH}	Write clock High pulse width	12	—	—	ns
t_{WL}	Write clock Low pulse width	12	—	—	ns
f_{MAXW}	Write f_{MAX}	—	—	33	MHz
sysCONFIG Read Cycle Timing					
t_{HREAD}	Hold time of READ to CCLK rise	0	—	—	ns
t_{SUREAD}	Input setup time of READ High to CCLK rise	30	—	—	ns
t_{RH}	READ clock high pulse width	12	—	—	ns
t_{RL}	READ clock low pulse width	15	—	—	ns
f_{MAXR}	Read f_{MAX}	—	—	33	MHz
t_{CORD}	Clock to out for read data	—	—	25	ns

Boundary Scan Timing

Parameter	Description	Min.	Max.	Units
t_{BTCP}	TCK [BSCAN] Clock Pulse Width	40	—	ns
t_{BTCPH}	TCK [BSCAN] Clock Pulse Width High	20	—	ns
t_{BTCPL}	TCK [BSCAN] Clock Pulse Width Low	20	—	ns
t_{BTS}	TCK [BSCAN] Setup Time	8	—	ns
t_{BTH}	TCK [BSCAN] Hold Time	10	—	ns
t_{BTRF}	TCK [BSCAN] Rise/Fall Time	50	—	mV/ns
t_{BTCO}	TAP Controller Falling Edge of Clock to Valid Output	—	18	ns
$t_{BTCODIS}$	TAP Controller Falling Edge of Clock to Valid Disable	—	18	ns
t_{BTCOEN}	TAP Controller Falling Edge of Clock to Valid Enable	—	18	ns
t_{BTCRS}	BSCAN Test Capture Register Setup Time	8	—	ns
t_{BTCRH}	BSCAN Test Capture Register Hold Time	25	—	ns
t_{BUTCO}	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	45	ns
$t_{BTUODIS}$	BSCAN Test Update Register, Falling Edge of Clock to Valid Disable	—	20	ns
$t_{BTUPOEN}$	BSCAN Test Update Register, Falling Edge of Clock to Valid Enable	—	20	ns

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
M15	BK4_IO5	-	54N/HSI2	BK4_IO5	-	46N
M14	BK4_IO8	-	56P/HSI2	BK4_IO6	-	47P
M13	BK4_IO9	VREF4	56N/HSI2	BK4_IO7	VREF4	47N
-	GND (Bank 4)	-	-	-	-	-
L13	BK4_IO12	PLL_RST4	58P/HSI2	BK4_IO8	PLL_RST4	48P
L14	BK4_IO13	PLL_RST5	58N/HSI2	BK4_IO9	PLL_RST5	48N
N16	BK4_IO14	HSI2B_SOUTP	59P/HSI2	BK4_IO10	-	49P
M16	BK4_IO15	HSI2B_SOUTN	59N/HSI2	BK4_IO11	-	49N
-	-	-	-	GND (Bank 4)	-	-
L15	BK4_IO18	SS_CLKIN1P	61P	BK4_IO14	SS_CLKIN1P	51P
-	GND (Bank 4)	-	-	-	-	-
K15	BK4_IO19	SS_CLKIN1N	61N	BK4_IO15	SS_CLKIN1N	51N
K14	BK4_IO20	PLL_FBK4	62P	BK4_IO16	PLL_FBK4	52P
K13	BK4_IO21	PLL_FBK5	62N	BK4_IO17	PLL_FBK5	52N
L16	BK4_IO22	SS_CLKOUT1P	63P	BK4_IO18	SS_CLKOUT1P	53P
-	-	-	-	GND (Bank 4)	-	-
K16	BK4_IO23	SS_CLKOUT1N	63N	BK4_IO19	SS_CLKOUT1N	53N
J13	BK4_IO24	CLK_OUT4	64P	BK4_IO20	CLK_OUT4	54P
J12	BK4_IO25	CLK_OUT5	64N	BK4_IO21	CLK_OUT5	54N
-	GND (Bank 4)	-	-	-	-	-
J14	GCLK4	-	LVDS Pair2P	GCLK4	-	LVDS Pair2P
H14	GCLK5	-	LVDS Pair2N	GCLK5	-	LVDS Pair2N
J15	VCCP1	-	-	VCCP1	-	-
H15	GNDP1	-	-	GNDP1	-	-
J16	GCLK6	-	LVDS Pair3P	GCLK6	-	LVDS Pair3P
H16	GCLK7	-	LVDS Pair3N	GCLK7	-	LVDS Pair3N
-	GND (Bank 5)	-	-	-	-	-
H12	BK5_IO0	CLK_OUT6	65P	BK5_IO0	CLK_OUT6	55P
H13	BK5_IO1	CLK_OUT7	65N	BK5_IO1	CLK_OUT7	55N
G14	BK5_IO2	-	66P	BK5_IO2	-	56P
-	-	-	-	GND (Bank 5)	-	-
G15	BK5_IO3	PLL_RST7	66N	BK5_IO3	PLL_RST7	56N
G13	BK5_IO6	PLL_RST6	68P	BK5_IO6	PLL_RST6	58P/HSI1
-	GND (Bank 5)	-	-	-	-	-
F13	BK5_IO7	PLL_FBK7	68N	BK5_IO7	PLL_FBK7	58N/HSI1
G16	BK5_IO10	HSI3A_SINP	70P	BK5_IO8	HSI1A_SINP	59P/HSI1
-	-	-	-	GND (Bank 5)	-	-
F16	BK5_IO11	HSI3A_SINN	70N/HSI3	BK5_IO9	HSI1A-SINN	59N/HSI1
F14	BK5_IO12	-	71P/HSI3	BK5_IO10	-	60P/HSI1
F15	BK5_IO13	-	71N/HSI3	BK5_IO11	-	60N/HSI1
E16	BK5_IO14	HSI3A_SOUTP	72P/HSI3	BK5_IO12	HSI1A_SOUTP	61P/HSI1
-	GND (Bank 5)	-	-	-	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AJ25	BK3_IO32	-	79P	NC	-	-	NC	-	-
AG24	BK3_IO33	-	79N	NC	-	-	NC	-	-
AK26	BK3_IO34	-	80P	BK3_IO20	-	49P	BK3_IO16	-	41P
-	-	-	-	-	-	-	GND (Bank 3)	-	-
AH25	BK3_IO35	-	80N	BK3_IO21	-	49N	BK3_IO17	-	41N
AJ26	BK3_IO36	-	81P	BK3_IO22	-	50P	BK3_IO18	-	42P
-	-	-	-	GND (Bank 3)	-	-	-	-	-
AH26	BK3_IO37	-	81N	BK3_IO23	-	50N	BK3_IO19	-	42N
AK27	BK3_IO38	-	82P	NC	-	-	NC	-	-
-	GND (Bank 3)	-	-	-	-	-	-	-	-
AJ27	BK3_IO39	-	82N	NC	-	-	NC	-	-
AG26	BK3_IO40	-	83P	BK3_IO24	-	51P	BK3_IO20	-	43P
AH27	BK3_IO41	-	83N	BK3_IO25	-	51N	BK3_IO21	-	43N
AK28	GSR	-	-	GSR	-	-	GSR	-	-
AJ28	DXP	-	-	DXP	-	-	DXP	-	-
AK29	DXN	-	-	DXN	-	-	DXN	-	-
AH29	BK4_IO0	-	84P	BK4_IO0	-	52P/HSI2	BK4_IO0	-	44P
AG28	BK4_IO1	-	84N	BK4_IO1	-	52N/HSI2	BK4_IO1	-	44N
AF27	BK4_IO2	-	85P/HSI3	NC	-	-	NC	-	-
-	GND (Bank 4)	-	-	-	-	-	-	-	-
AF28	BK4_IO3	-	85N/HSI3	NC	-	-	NC	-	-
AJ30	BK4_IO4	-	86P/HSI3	NC	-	-	NC	-	-
AH30	BK4_IO5	-	86N/HSI3	NC	-	-	NC	-	-
AG29	BK4_IO6	-	87P/HSI3	NC	-	-	NC	-	-
AF29	BK4_IO7	-	87N/HSI3	NC	-	-	NC	-	-
AE28	BK4_IO8	-	88P/HSI3	NC	-	-	NC	-	-
AD27	BK4_IO9	-	88N/HSI3	NC	-	-	NC	-	-
AG30	BK4_IO10	HSI3A_SINP	89P/HSI3	BK4_IO2	HSI2A_SINP	53P/HSI2	BK4_IO2	-	45P
-	GND (Bank 4)	-	-	GND (Bank 4)	-	-	-	-	-
AF30	BK4_IO11	HSI3A_SINN	89N/HSI3	BK4_IO3	HSI2A_SINN	53N/HSI2	BK4_IO3	-	45N
AD28	BK4_IO12	-	90P/HSI3	BK4_IO4	-	54P/HSI2	BK4_IO4	-	46P
-	-	-	-	-	-	-	GND (Bank 4)	-	-
AC27	BK4_IO13	-	90N/HSI3	BK4_IO5	-	54N/HSI2	BK4_IO5	-	46N
AE29	BK4_IO14	HSI3A_SOUTP	91P/HSI3	BK4_IO6	HSI2A_SOUTP	55P/HSI2	NC	-	-
AE30	BK4_IO15	HSI3A_SOUTN	91N/HSI3	BK4_IO7	HSI2A_SOUTN	55N/HSI2	NC	-	-
AD29	BK4_IO16	-	92P/HSI3	BK4_IO8	-	56P/HSI2	BK4_IO6	-	47P
AD30	BK4_IO17	VREF4	92N/HSI3	BK4_IO9	VREF4	56N/HSI2	BK4_IO7	VREF4	47N
AC28	BK4_IO18	HSI3B_SINP	93P	BK4_IO10	HSI2B_SINP	57P/HSI2	NC	-	-
-	GND (Bank 4)	-	-	GND (Bank 4)	-	-	-	-	-
AB28	BK4_IO19	HSI3B_SINN	93N	BK4_IO11	HSI2B_SINN	57N/HSI2	NC	-	-
AA27	BK4_IO20	PLL_RST4	94P	BK4_IO12	PLL_RST4	58P/HSI2	BK4_IO8	PLL_RST4	48P
AB29	BK4_IO21	PLL_RST5	94N	BK4_IO13	PLL_RST5	58N/HSI2	BK4_IO9	PLL_RST5	48N
AC29	BK4_IO22	HSI3B_SOUTP	95P	BK4_IO14	HSI2B_SOUTP	59P/HSI2	BK4_IO10	-	49P
AC30	BK4_IO23	HSI3B_SOUTN	95N	BK4_IO15	HSI2B_SOUTN	59N/HSI2	BK4_IO11	-	49N
AA28	BK4_IO24	-	96P	NC	-	-	NC	-	-
Y27	BK4_IO25	-	96N	NC	-	-	NC	-	-
Y28	BK4_IO26	-	97P	NC	-	-	NC	-	-
-	GND (Bank 4)	-	-	-	-	-	-	-	-
AA29	BK4_IO27	-	97N	NC	-	-	NC	-	-
Y29	BK4_IO28	-	98P	BK4_IO16	-	60P	BK4_IO12	-	50P
-	-	-	-	-	-	-	GND (Bank 4)	-	-

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
C24	BK1_IO7	SS_CLKIN0N	34N
A22	BK1_IO8	-	35P
D22	BK1_IO9	-	35N
A23	BK1_IO10	-	36P
-	GND (Bank 1)	-	-
B25	BK1_IO11	-	36N
D23	BK1_IO12	PLL_RST2	37P
A24	BK1_IO13	PLL_RST3	37N
A25	BK1_IO14	-	38P
E24	BK1_IO15	-	38N
D24	BK1_IO16	-	39P
A26	BK1_IO17	-	39N
D25	BK1_IO18	-	40P
-	GND (Bank 1)	-	-
C25	BK1_IO19	-	40N
B26	BK1_IO20	-	41P/HSI3
B27	BK1_IO21	-	41N/HSI3
D26	BK1_IO22	-	42P/HSI3
A27	BK1_IO23	-	42N/HSI3
A28	BK1_IO24	-	43P/HSI3
E26	BK1_IO25	-	43N/HSI3
C27	BK1_IO26	HSI3A_SOUTP	44P/HSI3
-	GND (Bank 1)	-	-
D27	BK1_IO27	HSI3A_SOUTN	44N/HSI3
B28	BK1_IO28	-	45P/HSI3
A30	BK1_IO29	-	45N/HSI3
C28	BK1_IO30	HSI3A_SINP	46P/HSI3
D28	BK1_IO31	HSI3A_SINN	46N/HSI3
A31	BK1_IO32	-	47P/HSI3
B30	BK1_IO33	-	47N/HSI3
E28	BK1_IO34	HSI3B_SOUTP	48P/HSI3
-	GND (Bank 1)	-	-
D29	BK1_IO35	HSI3B_SOUTN	48N/HSI3
C29	BK1_IO36	-	49P/HSI4
B31	BK1_IO37	-	49N/HSI4
D30	BK1_IO38	HSI3B_SINP	50P/HSI4
E30	BK1_IO39	HSI3B_SINN	50N/HSI4
A32	BK1_IO40	-	51P/HSI4
C31	BK1_IO41	-	51N/HSI4
D31	BK1_IO42	HSI4A_SOUTP	52P/HSI4
-	GND (Bank 1)	-	-
C32	BK1_IO43	HSI4A_SOUTN	52N/HSI4
B32	BK1_IO44	-	53P/HSI4

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
V39	BK2_IO57	-	90N
W37	BK2_IO58	-	91P
-	GND (Bank 2)	-	-
W38	BK2_IO59	-	91N
W39	BK2_IO60	-	92P
AA39	BK2_IO61	-	92N
-	GND (Bank 2)	-	-
-	GND (Bank 3)	-	-
AA38	BK3_IO0	-	93P
Y35	BK3_IO1	-	93N
AA37	BK3_IO2	-	94P
-	GND (Bank 3)	-	-
AA35	BK3_IO3	-	94N
AB39	BK3_IO4	-	95P
AB38	BK3_IO5	-	95N
AA36	BK3_IO6	-	96P
AB37	BK3_IO7	-	96N
AC39	BK3_IO8	-	97P
AC38	BK3_IO9	-	97N
AB36	BK3_IO10	-	98P
-	GND (Bank 3)	-	-
AC37	BK3_IO11	-	98N
AC36	BK3_IO12	-	99P
AD39	BK3_IO13	-	99N
AD37	BK3_IO14	-	100P
AD36	BK3_IO15	-	100N
AD35	BK3_IO16	-	101P
AE38	BK3_IO17	-	101N
AD38	BK3_IO18	-	102P
-	GND (Bank 3)	-	-
AE39	BK3_IO19	-	102N
AF38	BK3_IO20	-	103P
AF37	BK3_IO21	-	103N
AF39	BK3_IO22	-	104P
AE36	BK3_IO23	-	104N
AF36	BK3_IO24	-	105P
AG38	BK3_IO25	-	105N
AG39	BK3_IO26	-	106P
-	GND (Bank 3)	-	-
AG37	BK3_IO27	-	106N
AH37	BK3_IO28	-	107P
AH38	BK3_IO29	-	107N
AG36	BK3_IO30	-	108P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
-	GND (Bank 4)	-	-
AW26	BK4_IO43	-	145N
AV25	BK4_IO44	-	146P
AT24	BK4_IO45	-	146N
AU24	BK4_IO46	-	147P
AU25	BK4_IO47	-	147N
AW25	BK4_IO48	PLL_RST4	148P
AW24	BK4_IO49	PLL_RST5	148N
AU23	BK4_IO50	-	149P
-	GND (Bank 4)	-	-
AT23	BK4_IO51	-	149N
AV24	BK4_IO52	-	150P
AW23	BK4_IO53	-	150N
AV23	BK4_IO54	SS_CLKIN1P	151P
AU22	BK4_IO55	SS_CLKIN1N	151N
AR21	BK4_IO56	PLL_FBK4	152P
AT22	BK4_IO57	PLL_FBK5	152N
AV22	BK4_IO58	SS_CLKOUT1P	153P
-	GND (Bank 4)	-	-
AV21	BK4_IO59	SS_CLKOUT1N	153N
AT21	BK4_IO60	CLK_OUT4	154P
AU21	BK4_IO61	CLK_OUT5	154N
-	GND (Bank 4)	-	-
AT19	GCLK4	-	LVDS Pair2P
AU19	GCLK5	-	LVDS Pair2N
AW22	VCCP1	-	-
AR20	GNDP1	-	-
AU18	GCLK6	-	LVDS Pair3P
AT18	GCLK7	-	LVDS Pair3N
-	GND (Bank 5)	-	-
AV17	BK5_IO0	CLK_OUT6	155P
AV18	BK5_IO1	CLK_OUT7	155N
AW21	BK5_IO2	PLL_FBK6	156P
-	GND (Bank 5)	-	-
AV19	BK5_IO3	PLL_FBK7	156N
AR19	BK5_IO4	-	157P/HSI7
AW19	BK5_IO5	-	157N/HSI7
AW18	BK5_IO6	PLL_RST6	158P/HSI7
AW17	BK5_IO7	PLL_RST7	158N/HSI7
AT17	BK5_IO8	-	159P/HSI7
AV16	BK5_IO9	-	159N/HSI7
AU17	BK5_IO10	HSI7A_SINP	160P/HSI7
-	GND (Bank 5)	-	-

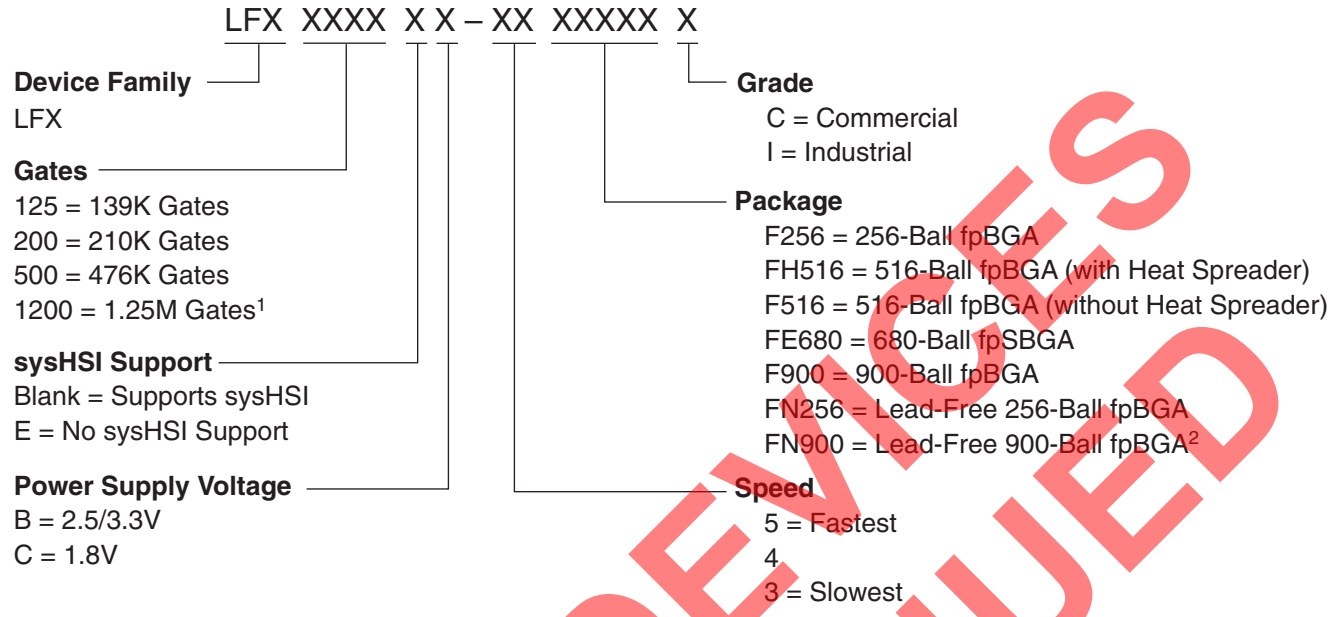
ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
Y5	BK6_IO61	-	216N
-	GND (Bank 6)	-	-
-	GND (Bank 7)	-	-
W3	BK7_IO0	-	217P
W1	BK7_IO1	-	217N
W2	BK7_IO2	-	218P
-	GND (Bank 7)	-	-
W4	BK7_IO3	-	218N
V1	BK7_IO4	-	219P
V2	BK7_IO5	-	219N
V3	BK7_IO6	-	220P
V4	BK7_IO7	-	220N
W5	BK7_IO8	-	221P
U1	BK7_IO9	-	221N
U2	BK7_IO10	-	222P
-	GND (Bank 7)	-	-
U3	BK7_IO11	-	222N
U4	BK7_IO12	-	223P
T1	BK7_IO13	-	223N
T2	BK7_IO14	-	224P
T3	BK7_IO15	-	224N
R1	BK7_IO16	-	225P
R2	BK7_IO17	-	225N
T4	BK7_IO18	-	226P
-	GND (Bank 7)	-	-
P1	BK7_IO19	-	226N
P2	BK7_IO20	-	227P
P3	BK7_IO21	-	227N
R4	BK7_IO22	-	228P
T5	BK7_IO23	-	228N
M1	BK7_IO24	-	229P
M2	BK7_IO25	-	229N
N3	BK7_IO26	-	230P
-	GND (Bank 7)	-	-
P4	BK7_IO27	-	230N
L1	BK7_IO28	-	231P
M3	BK7_IO29	-	231N
L2	BK7_IO30	-	232P
N4	BK7_IO31	-	232N
K1	BK7_IO32	-	233P
K2	BK7_IO33	-	233N
P5	BK7_IO34	-	234P
-	GND (Bank 7)	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
B15	BK7_IO1	-	217N	BK7_IO1	-	147N
C15	BK7_IO2	-	218P	BK7_IO2	-	148P
-	GND (Bank 7)	-	-		-	-
D15	BK7_IO3	-	218N	BK7_IO3	-	148N
E15	BK7_IO4	-	219P	BK7_IO4	-	149P
F15	BK7_IO5	-	219N	BK7_IO5	-	149N
A14	BK7_IO6	-	220P	BK7_IO6	-	150P
-	-	-	-	GND (Bank 7)	-	-
B14	BK7_IO7	-	220N	BK7_IO7	-	150N
C14	BK7_IO8	-	221P	BK7_IO8	-	151P
D14	BK7_IO9	-	221N	BK7_IO9	-	151N
E14	BK7_IO10	-	222P	BK7_IO10	-	152P
-	GND (Bank 7)	-	-	-	-	-
F14	BK7_IO11	-	222N	BK7_IO11	-	152N
C13	BK7_IO12	-	223P	BK7_IO12	-	153P
D13	BK7_IO13	-	223N	BK7_IO13	-	153N
B13	BK7_IO14	-	224P	BK7_IO14	-	154P
-	-	-	-	GND (Bank 7)	-	-
A13	BK7_IO15	-	224N	BK7_IO15	-	154N
F13	BK7_IO16	-	225P	BK7_IO16	-	155P
G13	BK7_IO17	-	225N	BK7_IO17	-	155N
A12	BK7_IO18	-	226P	BK7_IO18	-	156P
-	GND (Bank 7)	-	-	-	-	-
B12	BK7_IO19	-	226N	BK7_IO19	-	156N
C12	BK7_IO20	-	227P	NC	-	-
D12	BK7_IO21	-	227N	NC	-	-
A11	BK7_IO22	-	228P	NC	-	-
B11	BK7_IO23	-	228N	NC	-	-
E12	BK7_IO24	-	229P	NC	-	-
F12	BK7_IO25	-	229N	NC	-	-
C11	BK7_IO26	-	230P	NC	-	-
-	GND (Bank 7)	-	-	-	-	-
D11	BK7_IO27	-	230N	NC	-	-
E11	BK7_IO28	-	231P	NC	-	-
F11	BK7_IO29	-	231N	NC	-	-
B10	BK7_IO30	-	232P	NC	-	-
A10	BK7_IO31	-	232N	NC	-	-
D10	BK7_IO32	-	233P	NC	-	-
E10	BK7_IO33	-	233N	NC	-	-
A9	BK7_IO34	-	234P	NC	-	-
-	GND (Bank 7)	-	-	-	-	-
B9	BK7_IO35	-	234N	NC	-	-

Part Number Description



1. Discontinued via PCN #03A-10.
2. Select products only. See Ordering Information tables below for specific support.

Ordering Information

Conventional Packaging

Commercial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125B-05F256C	139K	2.5/3.3	-5	fpBGA	256
LFX125B-04F256C	139K	2.5/3.3	-4	fpBGA	256
LFX125B-03F256C	139K	2.5/3.3	-3	fpBGA	256
LFX125C-04F256C	139K	1.8	-4	fpBGA	256
LFX125C-03F256C	139K	1.8	-3	fpBGA	256
LFX125B-05F516C	139K	2.5/3.3	-5	fpBGA	516
LFX125B-04F516C	139K	2.5/3.3	-4	fpBGA	516
LFX125B-03F516C	139K	2.5/3.3	-3	fpBGA	516
LFX125C-04F516C	139K	1.8	-4	fpBGA	516
LFX125C-03F516C	139K	1.8	-3	fpBGA	516
LFX125B-05FH516C[1]	139K	2.5/3.3	-5	fpBGA	516
LFX125B-04FH516C[1]	139K	2.5/3.3	-4	fpBGA	516
LFX125B-03FH516C[1]	139K	2.5/3.3	-3	fpBGA	516
LFX125C-04FH516C[1]	139K	1.8	-4	fpBGA	516
LFX125C-03FH516C[1]	139K	1.8	-3	fpBGA	516
LFX200B-05F256C	210K	2.5/3.3	-5	fpBGA	256
LFX200B-04F256C	210K	2.5/3.3	-4	fpBGA	256
LFX200B-03F256C	210K	2.5/3.3	-3	fpBGA	256
LFX200C-04F256C	210K	1.8	-4	fpBGA	256
LFX200C-03F256C	210K	1.8	-3	fpBGA	256

Revision History (Cont.)

Date	Version	Change Summary
June 2004 (cont.)	08.0 (cont.)	Updated Global Clock Input Setup time specifications.
		Clarification of Serial Out LVDS test condition.
		Clarification of REFCLK, SS_CLKIN peak-to-peak period jitter condition.
		Added sysHSI Reserved pins and footnote.
		Removed industrial ordering part numbers.
July 2004	09.0	Added “E” Series product family.
August 2004	10.0	Final release.
December 2004	10.1	Updated NC Connections table.
April 2005	10.2	Clarification of IDK specification.
April 2005	11.0	Select lead-free packages release.
July 2005	12.0	Added lead-free 516 fpBGA ordering part numbers.
April 2007	13.0	Removed lead-free 680 fpSBGA information from Part Number Description and Ordering Part Number tables. Removed lead-free 516 fpBGA for LFX125 from Ordering Part Number tables.
November 2007	14.0	Removed lead-free 516 fpBGA information from Part Number Description and Ordering Part Number tables.
July 2008	14.1	Added 516 fpBGA package without heat spreader to Part Number Description and Ordering Part Number tables.
February 2010	15.0	Ordering part numbers and ispXPGA Family Selection Guide table have been updated per PCN #03A-10 (discontinuation of the ispXPGA 1200 devices).
		References to "system gates" changed to "functional gates."