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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	15376
Total RAM Bits	423936
Number of I/O	496
Number of Gates	1250000
Voltage - Supply	1.65V ~ 1.95V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	680-LBGA
Supplier Device Package	680-FPSBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx1200ec-03fe680i



Product Line	Ordering Part Number	Product Status	Reference PCN
LFX125EC (Cont'd)	LFX125EC-03F516C	Discontinued	<u>PCN#09-10</u>
	LFX125EC-04F516C		
	LFX125EC-03F516I		
LFX200EB	LFX200EB-03F256C	Active / Orderable	
	LFX200EB-03FN256C		
	LFX200EB-04F256C		
	LFX200EB-04FN256C		
	LFX200EB-05F256C		
	LFX200EB-05FN256C		
	LFX200EB-03F256I		
	LFX200EB-03FN256I		
	LFX200EB-04F256I	Discontinued	<u>PCN#09-10</u>
	LFX200EB-04FN256I		
	LFX200EB-03F516C		
	LFX200EB-04F516C		
	LFX200EB-05F516C		
	LFX200EB-03F516I		
	LFX200EB-04F516I		
LFX200EC	LFX200EC-03F256C	Discontinued	<u>PCN#09-10</u>
	LFX200EC-03FN256C		
	LFX200EC-04F256C		
	LFX200EC-04FN256C		
	LFX200EC-03F256I		
	LFX200EC-03FN256I		
	LFX200EC-03F516C		
	LFX200EC-04F516C		
	LFX200EC-03F516I		
LFX500EB	LFX500EB-03F516C	Discontinued	<u>PCN#09-10</u>
	LFX500EB-04F516C		
	LFX500EB-05F516C		
	LFX500EB-03F516I		
	LFX500EB-04F516I		
	LFX500EB-03F900C		
	LFX500EB-03FN900C		
	LFX500EB-04F900C		
	LFX500EB-04FN900C		
	LFX500EB-05F900C		
	LFX500EB-05FN900C		
	LFX500EB-03F900I		
	LFX500EB-03FN900I		
	LFX500EB-04F900I		
	LFX500EB-04FN900I		
LFX500EC	LFX500EC-03F516C	Discontinued	<u>PCN#09-10</u>
	LFX500EC-04F516C		
	LFX500EC-03F516I		

■ Non-volatile, Infinitely Reconfigurable

- Instant-on - Powers up in microseconds via on-chip E²CMOS® based memory
- No external configuration memory
- Excellent design security, no bit stream to intercept
- Reconfigure SRAM based logic in milliseconds

■ High Logic Density for System-level Integration

- 139K to 1.25M functional gates
- 160 to 496 I/O
- 1.8V, 2.5V, and 3.3V V_{CC} operation
- Up to 414Kb sysMEM™ embedded memory

■ High Performance Programmable Function Unit (PFU)

- Four LUT-4 per PFU supports wide and narrow functions
- Dual flip-flops per LUT-4 for extensive pipelining
- Dedicated logic for adders, multipliers, multiplexers, and counters

■ Flexible Memory Resources

- Multiple sysMEM Embedded RAM Blocks
 - Single port, Dual port, and FIFO operation
- 64-bit distributed memory in each PFU
 - Single port, Double port, FIFO, and Shift Register operation

■ Flexible Programming, Reconfiguration, and Testing

- Supports IEEE 1532 and 1149.1

- Microprocessor configuration interface
- Program E²CMOS while operating from SRAM

■ Eight sysCLOCK™ Phase Locked Loops (PLLs) for Clock Management

- True PLL technology
- 10MHz to 320MHz operation
- Clock multiplication and division
- Phase adjustment
- Shift clocks in 250ps steps

■ sysIO™ for High System Performance

- High speed memory support through SSTL and HSTL
- Advanced buses supported through PCI, GTL+, LVDS, BLVDS, and LVPECL
- Standard logic supported through LVTTTL, LVCMOS 3.3, 2.5 and 1.8
- 5V tolerant I/O for LVCMOS 3.3 and LVTTTL interfaces
- Programmable drive strength for series termination
- Programmable bus maintenance

■ Two Options Available

- High-performance sysHSI (standard part number)
- Low-cost, no sysHSI ("E-Series")

■ sysHSI™ Capability for Ultra Fast Serial Communications

- Up to 800Mbps performance
- Up to 20 channels per device
- Built in Clock Data Recovery (CDR) and Serialization and De-serialization (SERDES)

Table 1. ispXPGA Family Selection Guide

	ispXPGA 125/E	ispXPGA 200/E	ispXPGA 500/E	ispXPGA 1200/E ³
Functional Gates	139K	210K	476K	1.25M
PFUs	484	676	1764	3844
LUT-4s	1936	2704	7056	15376
Logic FFs	3.8K	5.4K	14.1K	30.7K
sysMEM Memory	92K	111K	184K	414K
Distributed Memory	30K	43K	112K	246K
EBR	20	24	40	90
sysHSI Channels ¹	4	8	12	20
User I/O	160/176	160/208	336	496
Packaging	256 fpBGA 516 fpBGA ²	256 fpBGA 516 fpBGA ²	516 fpBGA ² 900 fpBGA	680 fpSBGA 900 fpBGA

1. "E-Series" does not support sysHSI.

2. FH516 package was converted to F516 via [PCN #09A-08](#).

3. Discontinued via [PCN #03A-10](#).

Architecture Overview

The ispXPGA architecture is a symmetrical architecture consisting of an array of Programmable Function Units (PFUs) enclosed by Input Output Groups (PICs) with columns of sysMEM Embedded Block RAMs (EBRs) distributed throughout the array. Figure 1 illustrates the ispXPGA architecture. Each PIC has two corresponding sysIO blocks, each of which includes one input and output buffer. On two sides of the device, between the PICs and the sysIO blocks, there are sysHSI High-Speed Interface blocks. The symmetrical architecture allows designers to easily implement their designs, since any logic function can be placed in any section of the device.

The PFUs contain the basic building blocks to create logic, memory, arithmetic, and register functions. They are optimized for speed and flexibility allowing complex designs to be implemented quickly and efficiently.

The PICs interface the PFUs and EBRs to the external pins of the device. They allow the signals to be registered quickly to minimize setup times for high-speed designs. They also allow connections directly to the different logic elements for fast access to combinatorial functions.

The sysMEM EBRs are large, fast memory elements that can be configured as RAM, ROM, FIFO, and other storage types. They are designed to facilitate both single and dual-port memory for high-speed applications.

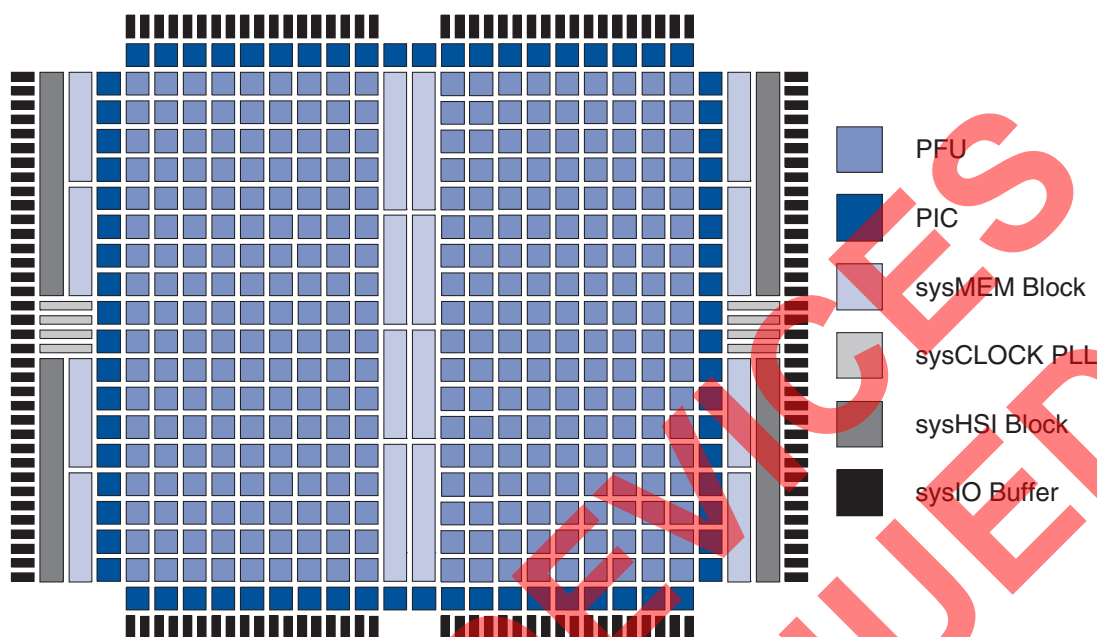
These three components of the architecture are interconnected via a high-speed, flexible routing array. The routing array consists of Variable Length Interconnect (VLI) lines between the PICs, PFUs, and EBRs. There is additional routing available to the PFU for feedback and direct routing of signals to adjacent PFUs or PICs.

The sysIO blocks consist of configurable input and output buffers connected directly to the PICs. These buffers can be configured to interface with 16 different I/O standards. This allows the ispXPGA to interface with other devices without the need for external transceivers.

The sysHSI blocks provide the necessary components to allow the ispXPGA device to transfer data at up to 800Mbps using the LVDS standard. These components include serializing, de-serializing, and clock data recovery (CDR) logic.

The sysCLOCK blocks provide clock multiplication/division, clock distribution, delay compensation, and increased performance through the use of PLL circuitry that manipulates the global clocks. There is one sysCLOCK block for each global clock tree in the device.

Figure 1. ispXPGA Block Diagram



Programmable Function Unit

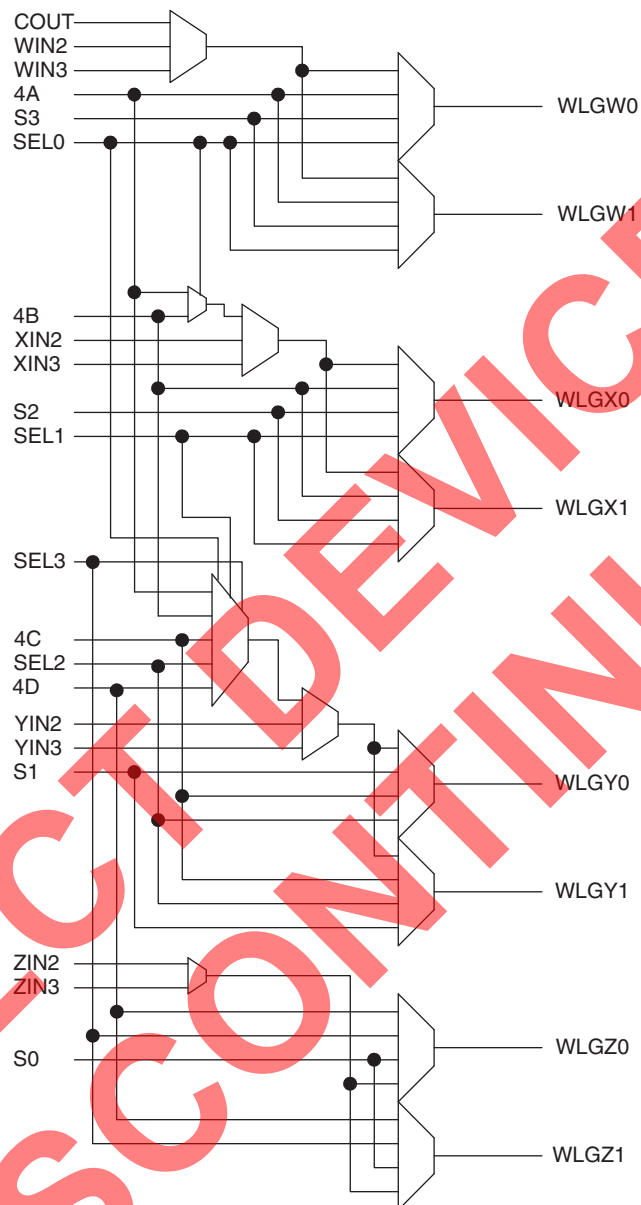
The Programmable Function Unit (PFU) is the basic building block of the ispXPGA architecture. The PFUs are arranged in rows and columns in the device with PFU (1,1) referring to (row 1, column 1). Each PFU consists of four Configurable Logic Elements (CLEs), four Configurable Sequential Elements (CSEs), and a Wide Logic Generator (WLG). By utilizing these components, the PFU can implement a variety of functions. Table 3 lists some of the function capabilities of the PFU.

There are 57 inputs to each PFU and nine outputs. The PFU uses 20 inputs for logic, and 37 inputs drive the control logic from which six control signals are derived for the PFU.

Table 3. Function Capability of ispXPGA PFU

Function	Capability
Look-up table	LUT-4, LUT-5, LUT-6
Wide logic functions	Up to 20 input logic functions
Multiplexing	2:1, 4:1, 8:1
Arithmetic logic	Dedicated carry chain and booth multiplication logic
Single-port RAM	16X1, 16X2, 16X4, 32X1, 32X2, 64X1
Double-port RAM	16X1, 16X2, 32X1
Shift register	8-bit shift registers (up to 32-bit shift capability)

Figure 6. ispXPGA Wide Logic Generator

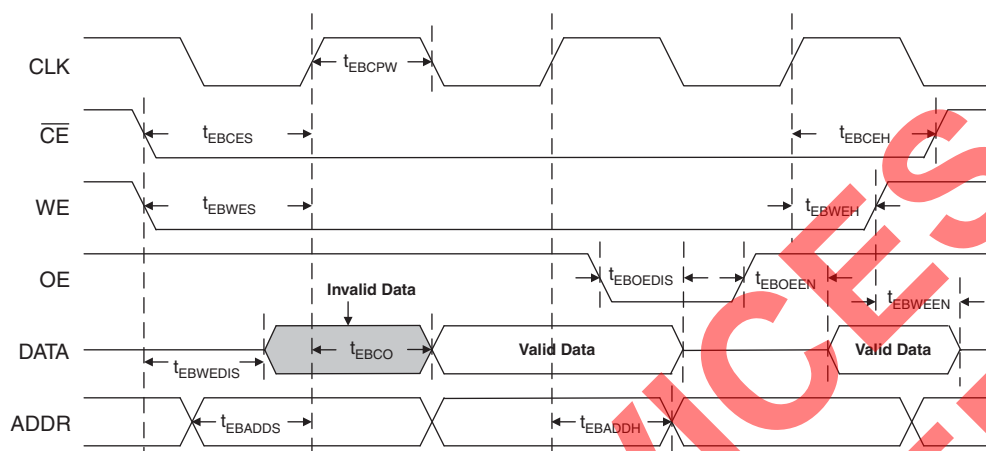


Configurable Sequential Element

There are two registers in each CSE for a total of eight registers in each PFU. This high register count assists in implementing efficient pipelined applications with no utilization penalty. Each register can be configured as a latch or D type flip-flop with either synchronous or asynchronous set or reset. Figure 2 shows the signals that feed the register's D inputs. Feed-through signals in the architecture ensure that registers are efficiently utilized even if the accompanying LUT is occupied.

Control Logic

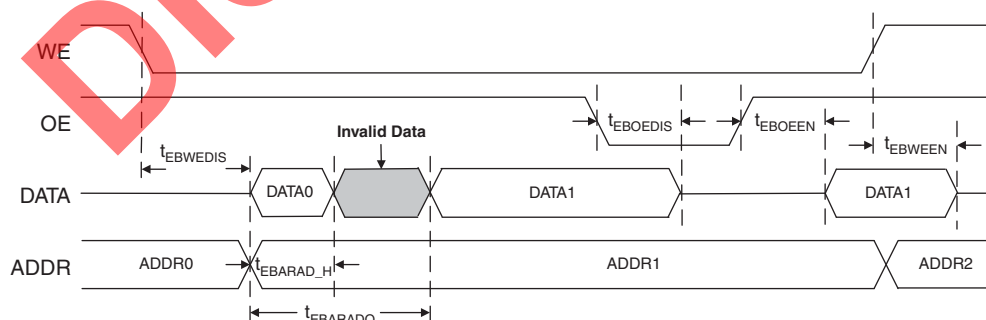
The control signals available to the registers in a PFU are Clock, Clock Enable, and Set/Reset. Figure 7 shows the various options available to generate the clock signal. As can be seen, the clock signal is the output of a 12:1 MUX with true and complement versions available from the 12:1 MUX. Each CSE can choose whether it uses the true or complement form of the clock. Figure 8 shows the Set/Reset selection for each PFU in the ispXPGA. A common

Figure 13. EBR Synchronous Read Timing Diagram

Synchronous Write: The WE signal controls the synchronous write operation. When the WE signal is high, the write operation begins. Once the address and data are present and the Output Enable (OE) is active, a rising clock edge (or falling edge depending on polarity) causes the data to be stored into the EBR. Figure 14 illustrates the synchronous write timing.

Figure 14. EBR Synchronous Write Timing Diagram

Asynchronous Read: The WE signal controls the asynchronous read operation. When the WE signal is low, the read operation begins. Shortly after the address is present, the stored data is available on the DATA port. Figure 15 illustrates the asynchronous read timing. For more information about the EBR, refer to TN1028 [ispXPGA Memory Usage Guidelines](#).

Figure 15. EBR Asynchronous Read Timing Diagram

High Speed Serial Interface Block (sysHSI Block)¹

The High Speed Serial Interface (sysHSI) allows high speed serial data transfer over a pair of LVDS I/O. The ispXPGA devices have multiple sysHSI blocks.

Each sysHSI block has two SERDES blocks which contain two main sub-blocks, Transmitter (with a serializer) and Receiver (with a deserializer) including Clock/Data Recovery Circuit (CDR). Each SERDES can be used as a full duplex channel. The two SERDES in sysHSI blocks share a common clock and must operate at the same nominal frequency. Figure 20 shows the sysHSI block.

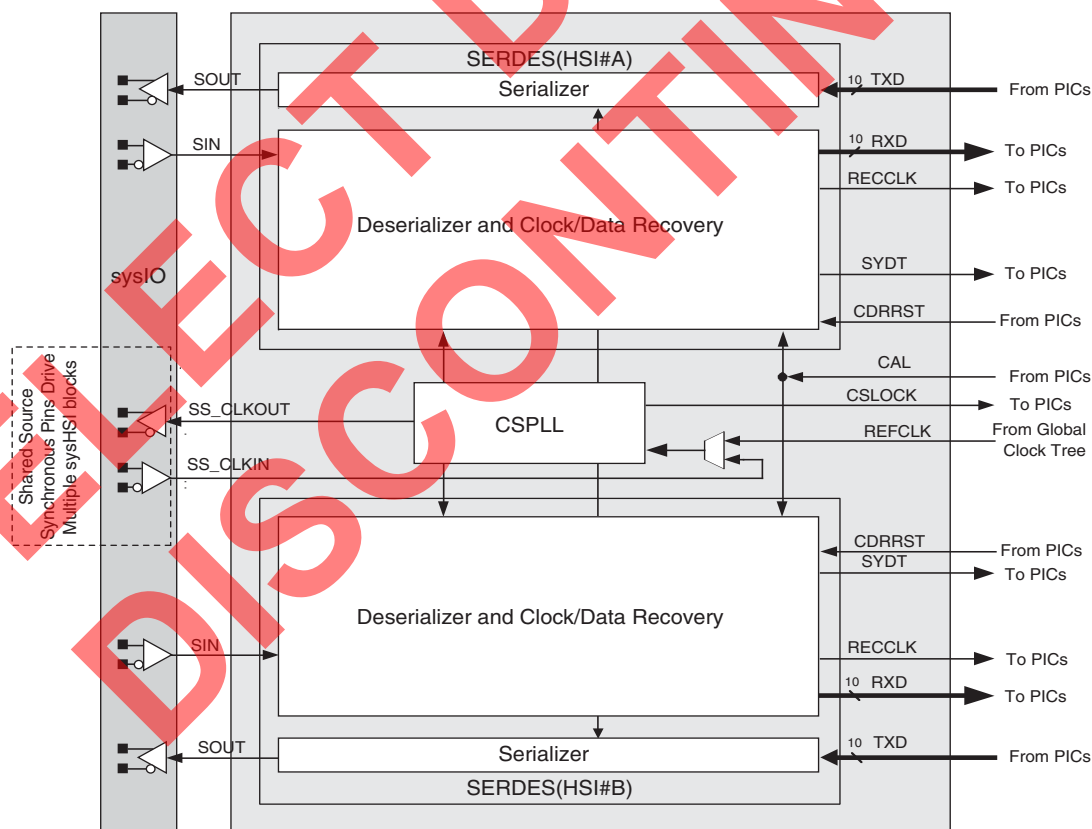
Device features support two data coding modes: 10B/12B and 8B/10B (for use with other encoding schemes, see Lattice's sysHSI technical notes). The encoding and decoding of the 10B/12B standard are performed within the sysHSI block. For the 8B/10B standard, the symbol boundaries are aligned internally but the encoding and decoding are performed outside the sysHSI block.

Each SERDES block receives a single high speed serial data input stream (with embedded clock) from an input, and provide a low speed 10-bit wide data stream and a recovered clock to the device. For transmitting, SERDES converts a 10-bit wide low-speed data stream to a single high-speed data stream with embedded clock for output.

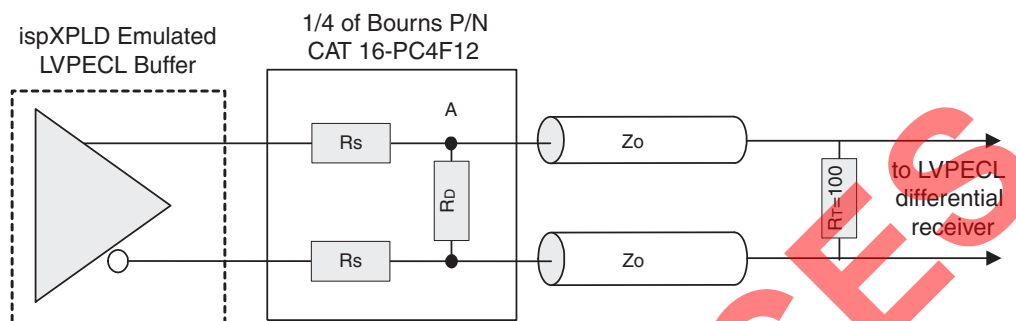
Additionally, multiple sysHSI blocks can be grouped together to form a source synchronous interface of 1-10 channels.

For more information on the SERDES/CDR, refer to TN1020, [sysHSI Usage Guidelines](#).

Figure 20. sysHSI Block Diagram



1. "E-Series" does not support sysHSI.

Figure 23. LVPECL Driver with Three Resistor Pack

ispXPGA 125B/C & ispXPGA 125EB/EC External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Conditions	-5 ¹		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{CO}	Global Clock Input to Output	PIO Output Register	—	5.3	—	5.7	—	6.6	ns
t_S	Global Clock Input Setup	PIO Input Register without input delay	-1.9	—	-1.8	—	-1.5	—	ns
t_H	Global Clock Input Hold	PIO Input Register without input delay	2.7	—	2.9	—	3.3	—	ns
t_{SINDLY}	Global Clock Input Setup	PIO Input Register with input delay	3.1	—	3.3	—	3.8	—	ns
t_{HINDLY}	Global Clock Input Hold	PIO Input Register with input delay	0.0	—	0.0	—	0.0	—	ns
t_{COPLL}	Global Clock Input to Output	PIO Output Register using PLL without delay	—	3.6	—	3.9	—	4.5	ns
t_{SPLL}	Global Clock Input Setup	PIO Input Register without input delay using PLL without delay	0	—	0.1	—	0.3	—	ns
t_{HPLL}	Global Clock Input Hold	PIO Input Register without input delay using PLL without delay	0.9	—	1.0	—	1.2	—	ns
$t_{SINDLYPLL}$	Global Clock Input Setup	PIO Input Register with input delay using PLL without delay	5.1	—	5.5	—	6.3	—	ns
$t_{HINDLYPLL}$	Global Clock Input Hold	PIO Input Register with input delay using PLL without delay	-3.0	—	-2.8	—	-2.4	—	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 125B/C & ispXPGA 125EB/EC Timing Adders (Cont.)

Parameter	Description	Base Parameter	-5 ¹		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LVC MOS_33_4mA_out	Using 3.3V CMOS Standard, 4mA Drive	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVC MOS_33_5.33mA_out	Using 3.3V CMOS Standard, 5.33mA Drive	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVC MOS_33_8mA_out	Using 3.3V CMOS Standard, 8mA Drive	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVC MOS_33_12mA_out	Using 3.3V CMOS Standard, 12mA Drive	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVC MOS_33_16mA_out	Using 3.3V CMOS Standard, 16mA Drive	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVC MOS_33_24mA_out	Using 3.3V CMOS Standard, 24mA Drive	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_out	Using AGP 1x Standard	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.5	—	0.5	—	0.5	ns
CTT25_out	Using CTT 2.5V	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.5	—	0.5	—	0.5	ns
CTT33_out	Using CTT 3.3V	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.5	—	0.5	—	0.5	ns
GTL+_out	Using GTL+	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_out	Using HSTL 2.5V, Class I	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_out	Using HSTL 2.5V, Class III	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVDS_out	Using Low Voltage Differential Signaling (LVDS)	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	1.0	—	1.0	—	1.0	ns
BLVDS_out	Using Bus Low Voltage Differential Signaling (BLVDS)	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVPECL_out	Using Low Voltage PECL	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	1.0	—	1.0	—	1.0	ns
PCI_out	Using PCI Standard	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL2_I_out	Using SSTL 2.5V, Class I	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL2_II_out	Using SSTL 2.5V, Class II	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_out	Using SSTL 3.3V, Class I	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL3_II_out	Using SSTL 3.3V, Class II	t _{IOBUF} , t _{IOEN} , t _{IODIS}	—	0.5	—	0.5	—	0.5	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 500B/C & ispXPGA 500EB/EC External Switching Characteristics**Over Recommended Operating Conditions**

Parameter	Description	Conditions	-5 ¹		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{CO}	Global Clock Input to Output	PIO Output Register	—	6.4	—	6.9	—	7.9	ns
t_S	Global Clock Input Setup	PIO Input Register without input delay	-2.9	—	-2.7	—	-2.3	—	ns
t_H	Global Clock Input Hold	PIO Input Register without input delay	3.6	—	3.9	—	4.5	—	ns
t_{SINDLY}	Global Clock Input Setup	PIO Input Register with input delay	3.3	—	3.6	—	4.1	—	ns
t_{HINDLY}	Global Clock Input Hold	PIO Input Register with input delay	0.0	—	0.0	—	0.0	—	ns
t_{COPLL}	Global Clock Input to Output	PIO Output Register using PLL without delay	—	3.2	—	3.4	—	3.9	ns
t_{SPLL}	Global Clock Input Setup	PIO Input Register without input delay using PLL without delay	0.1	—	0.2	—	0.3	—	ns
t_{HPLL}	Global Clock Input Hold	PIO Input Register without input delay using PLL without delay	0.8	—	0.9	—	1.0	—	ns
$t_{SINDLYPLL}$	Global Clock Input Setup	PIO Input Register with input delay using PLL without delay	6.7	—	7.2	—	8.3	—	ns
$t_{HINDLYPLL}$	Global Clock Input Hold	PIO Input Register with input delay using PLL without delay	-4.3	—	-4.0	—	-3.4	—	ns

1. Only available for ispXPGA 500B and ispXPGA 500EB (2.5V/3.3V) devices.

Timing v0.3

ispXPGA 1200B/C & ispXPGA 1200EB/EC PFU Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-5 ¹		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Set								
t _{LASSRO}	Asynchronous Set/Reset to Output	—	1.09	—	1.17	—	1.35	ns
t _{LASSRPW}	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t _{LASSRR}	Asynchronous Set/Reset Recovery	—	0.51	—	0.55	—	0.63	ns
t _{LSSR_S}	Synchronous Set/Reset Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t _{LSSR_H}	Synchronous Set/Reset Hold Time	0.03	—	0.03	—	0.03	—	ns

1. Only available for ispXPGA 1200B and ispXPGA 1200EB (2.5V/3.3V) devices.

Timing v.2.1

2. t_{LCTHRUL} quoted bit by bit.**ispXPGA 1200B/C & ispXPGA 1200EB/EC PIC Timing Parameters**

Parameter	Description	-5 ¹		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Register/Latch Delays								
t _{IO_CO}	Register Clock to Output Delay	—	1.01	—	1.09	—	1.25	ns
t _{IO_S}	Register Setup Time (Data before Clock)	0.05	—	0.05	—	0.06	—	ns
t _{IO_H}	Register Hold Time (Data after Clock)	0.06	—	0.06	—	0.07	—	ns
t _{IOCE_S}	Register Clock Enable Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t _{IOCE_H}	Register Clock Enable Hold Time	0.13	—	0.13	—	0.15	—	ns
t _{IO_GO}	Latch Gate to Output Delay	—	0.85	—	0.91	—	1.05	ns
t _{IOL_S}	Latch Setup Time	0.05	—	0.05	—	0.06	—	ns
t _{IOL_H}	Latch Hold Time	0.06	—	0.06	—	0.07	—	ns
t _{IOLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns
t _{IOASRO}	Asynchronous Set/Reset to Output	—	1.17	—	1.26	—	1.45	ns
t _{IOASRPW}	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t _{IOASRR}	Asynchronous Set/Reset Recovery Time	—	0.23	—	0.25	—	0.29	ns
Input/Output Delays								
t _{IOBUF}	Output Buffer Delay	—	0.99	—	1.06	—	1.22	ns
t _{IOIN}	Input Buffer Delay	—	0.71	—	0.76	—	0.87	ns
t _{IOEN}	Output Enable Delay	—	0.52	—	0.56	—	0.64	ns
t _{IODIS}	Output Disable Delay	—	-0.11	—	-0.10	—	-0.09	ns
t _{IOFT}	Feed-thru Delay	—	0.19	—	0.20	—	0.23	ns

1. Only available for ispXPGA 1200B and ispXPGA 1200EB (2.5V/3.3V) devices.

Timing v.2.1

ispXPGA Logic Signal Connections: 256-Ball fpBGA

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ²	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ²
C2	BK0_IO2	HSI0A_SOUTP	1P/HSI0	BK0_IO0	HSI0A_SOUTP	0P
-	GND (Bank 0)	-	-	-	-	-
D2	BK0_IO3	HSI0A_SOUTN	1N/HSI0	BK0_IO1	HSI0A_SOUTN	0N
B1	BK0_IO6	HSI0A_SINP	3P/HSI0	BK0_IO4	HSI0A_SINP	2P/HSI0
-	-	-	-	GND (Bank 0)	-	-
C1	BK0_IO7	HSI0A_SINN	3N/HSI0	BK0_IO5	HSI0A_SINN	2N/HSI0
D3	BK0_IO8	-	4P/HSI0	BK0_IO6	-	3P/HSI0
E3	BK0_IO9	VREF0	4N/HSI0	BK0_IO7	VREF0	3N/HSI0
D1	BK0_IO10	HSI0B_SOUTP	5P/HSI0	BK0_IO8	HSI0B_SOUTP	4P/HSI0
-	GND (Bank 0)	-	-	-	-	-
E1	BK0_IO11	HSI0B_SOUTN	5N/HSI0	BK0_IO9	HSI0B_SOUTN	4N/HSI0
E2	BK0_IO12	-	6P/HSI0	BK0_IO10	-	5P/HSI0
F2	BK0_IO13	-	6N/HSI0	BK0_IO11	-	5N/HSI0
F1	BK0_IO14	HSI0B_SINP	7P/HSI0	BK0_IO12	HSI0B_SINP	6P/HSI0
-	-	-	-	GND (Bank 0)	-	-
G1	BK0_IO15	HSI0B_SINN	7N/HSI0	BK0_IO13	HSI0B_SINN	6N/HSI0
F3	BK0_IO18	PLL_FBK0	9P	BK0_IO14	PLL_FBK0	7P/HSI0
-	GND (Bank 0)	-	-	-	-	-
G2	BK0_IO19	PLL_RST1	9N	BK0_IO15	PLL_RST1	7N/HSI0
E4	BK0_IO20	-	10P	BK0_IO16	-	8P/HSI0
F4	BK0_IO21	PLL_FBK1	10N	BK0_IO17	PLL_FBK1	8N/HSI0
H1	BK0_IO22	PLL_RST0	11P	BK0_IO18	PLL_RST0	9P
-	-	-	-	GND (Bank 0)	-	-
J1	BK0_IO23	-	11N	BK0_IO19	-	9N
H2	BK0_IO24	CLK_OUT0	12P	BK0_IO20	CLK_OUT0	10P
G3	BK0_IO25	CLK_OUT1	12N	BK0_IO21	CLK_OUT1	10N
-	GND (Bank 0)	-	-	-	-	-
G4	GCLK0	-	LVDS Pair0P	GCLK0	-	LVDS Pair0P
H4	GCLK1	-	LVDS Pair0N	GCLK1	-	LVDS Pair0N
H3	VCCP0	-	-	VCCP0	-	-
J4	GNDP0	-	-	GNDP0	-	-
J2	GCLK2	-	LVDS Pair1P	GCLK2	-	LVDS Pair1P
J3	GCLK3	-	LVDS Pair1N	GCLK3	-	LVDS Pair1N
-	GND (Bank 1)	-	-	-	-	-
H5	BK1_IO0	CLK_OUT2	13P	BK1_IO0	CLK_OUT2	11P
J5	BK1_IO1	CLK_OUT3	13N	BK1_IO1	CLK_OUT3	11N
K1	BK1_IO2	SS_CLKOUT0P	14P	BK1_IO2	SS_CLKOUT0P	12P
-	-	-	-	GND (Bank 1)	-	-
L1	BK1_IO3	SS_CLKOUT0N	14N	BK1_IO3	SS_CLKOUT0N	12N
K4	BK1_IO4	PLL_FBK2	15P	BK1_IO4	PLL_FBK2	13P
L4	BK1_IO5	PLL_FBK3	15N	BK1_IO5	PLL_FBK3	13N
K3	BK1_IO6	SS_CLKIN0P	16P	BK1_IO6	SS_CLKIN0P	14P

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ²	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ²
-	GND (Bank 1)	-	-	-	-	-
L3	BK1_IO7	SS_CLKIN0N	16N	BK1_IO7	SS_CLKIN0N	14N
K2	BK1_IO8	-	17P	BK1_IO8	-	15P
-	-	-	-	GND (Bank 1)	-	-
L2	BK1_IO9	-	17N	BK1_IO9	-	15N
M1	BK1_IO10	HSI1A_SOUTP	18P/HSI1	BK1_IO10	-	16P
N1	BK1_IO11	HSI1A_SOUTN	18N/HSI1	BK1_IO11	-	16N
M3	BK1_IO12	PLL_RST2	19P/HSI1	BK1_IO12	PLL_RST2	17P
M4	BK1_IO13	PLL_RST3	19N/HSI1	BK1_IO13	PLL_RST3	17N
-	GND (Bank 1)	-	-	-	-	-
M2	BK1_IO16 ¹	VREF1	-	BK1_IO14 ¹	VREF1	-
P1	BK1_IO18	HSI1B_SOUTP	22P/HSI1	BK1_IO16	-	19P
-	-	-	-	GND (Bank 1)	-	-
R1	BK1_IO19	HSI1B_SOUTN	22N/HSI1	BK1_IO17	-	19N
N3	BK1_IO20 ¹	-	-	BK1_IO18 ¹	-	-
N2	BK1_IO22	HSI1B_SINP	24P/HSI1	BK1_IO20	-	21P
-	GND (Bank 1)	-	-	-	-	-
P2	BK1_IO23	HSI1B_SINN	24N/HSI1	BK1_IO21	-	21N
P4	TCK	-	-	TCK	-	-
T2	TMS	-	-	TMS	-	-
T3	TOE	-	-	TOE	-	-
R3	BK2_IO0	-	26P	BK2_IO0	-	22P
R4	BK2_IO1	-	26N	BK2_IO1	-	22N
N5	BK2_IO2	-	27P	BK2_IO2	-	23P
-	GND (Bank 2)	-	-	-	-	-
P5	BK2_IO3	-	27N	BK2_IO3	-	23N
-	-	-	-	GND (Bank 2)	-	-
T4	BK2_IO6	-	29P	BK2_IO6	-	25P
T5	BK2_IO7	-	29N	BK2_IO7	-	25N
N6	BK2_IO8	-	30P	BK2_IO8	-	26P
P6	BK2_IO9	VREF2	30N	BK2_IO9	VREF2	26N
R5	BK2_IO10	-	31P	BK2_IO10	-	27P
-	GND (Bank 2)	-	-	-	-	-
R6	BK2_IO11	-	31N	BK2_IO11	-	27N
N7	BK2_IO12	-	32P	BK2_IO12	-	28P
-	-	-	-	GND (Bank 2)	-	-
P7	BK2_IO13	-	32N	BK2_IO13	-	28N
T6	BK2_IO14	-	33P	BK2_IO14	-	29P
T7	BK2_IO15	-	33N	BK2_IO15	-	29N
M8	BK2_IO16	-	34P	BK2_IO16	-	30P
M9	BK2_IO17	-	34N	BK2_IO17	-	30N
R7	BK2_IO18	-	35P	BK2_IO18	-	31P

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ²	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ²
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
R8	BK2_IO19	-	35N	BK2_IO19	-	31N
N8	BK2_IO20	-	36P	BK2_IO20	-	32P
P8	BK2_IO21	-	36N	BK2_IO21	-	32N
-	GND (Bank 2)	-	-	-	-	-
-	GND (Bank 3)	-	-	-	-	-
T8	BK3_IO0	-	39P	BK3_IO0	-	33P
T9	BK3_IO1	-	39N	BK3_IO1	-	33N
R9	BK3_IO2	-	40P	BK3_IO2	-	34P
-	-	-	-	GND (Bank 3)	-	-
R10	BK3_IO3	-	40N	BK3_IO3	-	34N
P9	BK3_IO4	-	41P	BK3_IO4	-	35P
N9	BK3_IO5	-	41N	BK3_IO5	-	35N
T10	BK3_IO6	-	42P	BK3_IO6	-	36P
-	GND (Bank 3)	-	-	-	-	-
T11	BK3_IO7	-	42N	BK3_IO7	-	36N
P10	BK3_IO8	-	43P	BK3_IO8	-	37P
-	-	-	-	GND (Bank 3)	-	-
N10	BK3_IO9	-	43N	BK3_IO9	-	37N
R11	BK3_IO14	-	46P	BK3_IO10	-	38P
-	GND (Bank 3)	-	-	-	-	-
R12	BK3_IO15	-	46N	BK3_IO11	-	38N
P11	BK3_IO16	VREF3	47P	BK3_IO12	VREF3	39P
N11	BK3_IO17	-	47N	BK3_IO13	-	39N
T12	BK3_IO18	-	48P	BK3_IO14	-	40P
T13	BK3_IO19	-	48N	BK3_IO15	-	40N
R13	BK3_IO20	-	49P	BK3_IO16	-	41P
-	-	-	-	GND (Bank 3)	-	-
R14	BK3_IO21	-	49N	BK3_IO17	-	41N
P12	BK3_IO22	-	50P	BK3_IO18	-	42P
-	GND (Bank 3)	-	-	-	-	-
N12	BK3_IO23	-	50N	BK3_IO19	-	42N
T14	GSR	-	-	GSR	-	-
T15	DXP	-	-	DXP	-	-
P13	DXN	-	-	DXN	-	-
P15	BK4_IO0	-	52P/HSI2	BK4_IO0	-	44P
N14	BK4_IO1	-	52N/HSI2	BK4_IO1	-	44N
R16	BK4_IO2	HSI2A_SINP	53P/HSI2	BK4_IO2	-	45P
-	GND (Bank 4)	-	-	-	-	-
P16	BK4_IO3	HSI2A_SINN	53N/HSI2	BK4_IO3	-	45N
N15	BK4_IO4	-	54P/HSI2	BK4_IO4	-	46P
-	-	-	-	GND (Bank 4)	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹
-	-	-	-	GND (Bank 0)	-	-	-	-	-
R2	GCLK0	-	LVDS Pair0P	GCLK0	-	LVDS Pair0P	GCLK0	-	LVDS Pair0P
R3	GCLK1	-	LVDS Pair0N	GCLK1	-	LVDS Pair0N	GCLK1	-	LVDS Pair0N
R4	VCCP0	-	-	VCCP0	-	-	VCCP0	-	-
T4	GNDP0	-	-	GNDP0	-	-	GNDP0	-	-
T3	GCLK2	-	LVDS Pair1P	GCLK2	-	LVDS Pair1P	GCLK2	-	LVDS Pair1P
T2	GCLK3	-	LVDS Pair1N	GCLK3	-	LVDS Pair1N	GCLK3	-	LVDS Pair1N
-	-	-	-	GND (Bank 1)	-	-	-	-	-
T1	BK1_IO0	CLK_OUT2	21P	BK1_IO0	CLK_OUT2	13P	BK1_IO0	CLK_OUT2	11P
-	GND (Bank 1)	-	-	-	-	-	-	-	-
U1	BK1_IO1	CLK_OUT3	21N	BK1_IO1	CLK_OUT3	13N	BK1_IO1	CLK_OUT3	11N
U2	BK1_IO2	SS_CLKOUT0P	22P	BK1_IO2	SS_CLKOUT0P	14P	BK1_IO2	SS_CLKOUT0P	12P
-	-	-	-	-	-	-	GND (Bank 1)	-	-
U3	BK1_IO3	SS_CLKOUT0N	22N	BK1_IO3	SS_CLKOUT0N	14N	BK1_IO3	SS_CLKOUT0N	12N
V1	BK1_IO4	PLL_FBK2	23P	BK1_IO4	PLL_FBK2	15P	BK1_IO4	PLL_FBK2	13P
V2	BK1_IO5	PLL_FBK3	23N	BK1_IO5	PLL_FBK3	15N	BK1_IO5	PLL_FBK3	13N
V3	BK1_IO6	-	24P	NC	-	-	NC	-	-
-	GND (Bank 1)	-	-	-	-	-	-	-	-
V4	BK1_IO7	-	24N	NC	-	-	NC	-	-
W1	BK1_IO8	-	25P	NC	-	-	NC	-	-
Y1	BK1_IO9	-	25N	NC	-	-	NC	-	-
W2	BK1_IO10	SS_CLKIN0P	26P	BK1_IO6	SS_CLKIN0P	16P	BK1_IO6	SS_CLKIN0P	14P
-	-	-	-	GND (Bank 1)	-	-	-	-	-
W3	BK1_IO11	SS_CLKIN0N	26N	BK1_IO7	SS_CLKIN0N	16N	BK1_IO7	SS_CLKIN0N	14N
Y2	BK1_IO12	-	27P	BK1_IO8	-	17P	BK1_IO8	-	15P
-	-	-	-	-	-	-	GND (Bank 1)	-	-
Y4	BK1_IO13	-	27N	BK1_IO9	-	17N	BK1_IO9	-	15N
Y3	BK1_IO14	-	28P	NC	-	-	NC	-	-
-	GND (Bank 1)	-	-	-	-	-	-	-	-
AA1	BK1_IO15	-	28N	NC	-	-	NC	-	-
AA2	BK1_IO16	-	29P	NC	-	-	NC	-	-
AA3	BK1_IO17	-	29N	NC	-	-	NC	-	-
AB2	BK1_IO18	HSI2A_SOUTP	30P	BK1_IO10	HSI1A_SOUTP	18P/HSI1	BK1_IO10	-	16P
AC2	BK1_IO19	HSI2A_SOUTN	30N	BK1_IO11	HSI1A_SOUTN	18N/HSI1	BK1_IO11	-	16N
AB3	BK1_IO20	PLL_RST2	31P	BK1_IO12	PLL_RST2	19P/HSI1	BK1_IO12	PLL_RST2	17P
AA4	BK1_IO21	PLL_RST3	31N	BK1_IO13	PLL_RST3	19N/HSI1	BK1_IO13	PLL_RST3	17N
AC1	BK1_IO22	HSI2A_SINP	32P	BK1_IO14	HSI1A_SINP	20P/HSI1	NC	-	-
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-	-	-	-
AD1	BK1_IO23	HSI2A_SINN	32N	BK1_IO15	HSI1A_SINN	20N/HSI1	NC	-	-
AE1	BK1_IO24	VREF1	33P/HSI2	BK1_IO16	VREF1	21P/HSI1	BK1_IO14	VREF1	18P
AF1	BK1_IO25	-	33N/HSI2	BK1_IO17	-	21N/HSI1	BK1_IO15	-	18N
AC3	BK1_IO26	HSI2B_SOUTP	34P/HSI2	BK1_IO18	HSI1B_SOUTP	22P/HSI1	BK1_IO16	-	19P
-	-	-	-	-	-	-	GND (Bank 1)	-	-
AC4	BK1_IO27	HSI2B_SOUTN	34N/HSI2	BK1_IO19	HSI1B_SOUTN	22N/HSI1	BK1_IO17	-	19N
AD2	BK1_IO28	-	35P/HSI2	BK1_IO20	-	23P/HSI1	BK1_IO18	-	20P
AD3	BK1_IO29	-	35N/HSI2	BK1_IO21	-	23N/HSI1	BK1_IO19	-	20N
AE2	BK1_IO30	HSI2B_SINP	36P/HSI2	BK1_IO22	HSI1B_SINP	24P/HSI1	BK1_IO20	-	21P
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-	-	-	-
AF2	BK1_IO31	HSI2B_SINN	36N/HSI2	BK1_IO23	HSI1B_SINN	24N/HSI1	BK1_IO21	-	21N
AD4	BK1_IO32	-	37P/HSI2	NC	-	-	NC	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹
AJ13	BK2_IO32	-	58P	BK2_IO18	-	35P	BK2_IO18	-	31P
-	-	-	-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
AK12	BK2_IO33	-	58N	BK2_IO19	-	35N	BK2_IO19	-	31N
AK13	BK2_IO34	-	59P	BK2_IO20	-	36P	BK2_IO20	-	32P
-	GND (Bank 2)	-	-	-	-	-	-	-	-
AH14	BK2_IO35	-	59N	BK2_IO21	-	36N	BK2_IO21	-	32N
AJ14	BK2_IO36	-	60P	BK2_IO22	-	37P	NC	-	-
AK14	BK2_IO37	-	60N	BK2_IO23	-	37N	NC	-	-
AG15	BK2_IO38	-	61P	BK2_IO24	-	38P	NC	-	-
AH15	BK2_IO39	-	61N	BK2_IO25	-	38N	NC	-	-
AJ15	BK2_IO40	-	62P	NC	-	-	NC	-	-
AK15	BK2_IO41	-	62N	NC	-	-	NC	-	-
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-	-	-	-
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-	-	-	-
AK16	BK3_IO0	-	63P	BK3_IO0	-	39P	BK3_IO0	-	33P
AJ16	BK3_IO1	-	63N	BK3_IO1	-	39N	BK3_IO1	-	33N
AH16	BK3_IO2	-	64P	BK3_IO2	-	40P	BK3_IO2	-	34P
AG16	BK3_IO3	-	64N	BK3_IO3	-	40N	BK3_IO3	-	34N
AK17	BK3_IO4	-	65P	BK3_IO4	-	41P	BK3_IO4	-	35P
AJ17	BK3_IO5	-	65N	BK3_IO5	-	41N	BK3_IO5	-	35N
AH17	BK3_IO6	-	66P	BK3_IO6	-	42P	BK3_IO6	-	36P
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-	-	-	-
AJ18	BK3_IO7	-	66N	BK3_IO7	-	42N	BK3_IO7	-	36N
AH18	BK3_IO8	-	67P	BK3_IO8	-	43P	BK3_IO8	-	37P
-	-	-	-	-	-	-	GND (Bank 3)	-	-
AG18	BK3_IO9	-	67N	BK3_IO9	-	43N	BK3_IO9	-	37N
AK18	BK3_IO10	-	68P	BK3_IO10	-	44P	BK3_IO10	-	38P
AK19	BK3_IO11	-	68N	BK3_IO11	-	44N	BK3_IO11	-	38N
AJ19	BK3_IO12	-	69P	BK3_IO12	-	45P	NC	-	-
AH19	BK3_IO13	-	69N	BK3_IO13	-	45N	NC	-	-
AK20	BK3_IO14	-	70P	BK3_IO14	-	46P	NC	-	-
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-	-	-	-
AJ20	BK3_IO15	-	70N	BK3_IO15	-	46N	NC	-	-
AH20	BK3_IO16	-	71P	NC	-	-	NC	-	-
AG20	BK3_IO17	-	71N	NC	-	-	NC	-	-
AK21	BK3_IO18	-	72P	NC	-	-	NC	-	-
AJ21	BK3_IO19	-	72N	NC	-	-	NC	-	-
AH21	BK3_IO20	VREF3	73P	BK3_IO16	VREF3	47P	BK3_IO12	VREF3	39P
AG21	BK3_IO21	-	73N	BK3_IO17	-	47N	BK3_IO13	-	39N
AJ22	BK3_IO22	-	74P	BK3_IO18	-	48P	BK3_IO14	-	40P
-	GND (Bank 3)	-	-	-	-	-	-	-	-
AH22	BK3_IO23	-	74N	BK3_IO19	-	48N	BK3_IO15	-	40N
AK23	BK3_IO24	-	75P	NC	-	-	NC	-	-
AJ23	BK3_IO25	-	75N	NC	-	-	NC	-	-
AH23	BK3_IO26	-	76P	NC	-	-	NC	-	-
AK24	BK3_IO27	-	76N	NC	-	-	NC	-	-
AJ24	BK3_IO28	-	77P	NC	-	-	NC	-	-
AG23	BK3_IO29	-	77N	NC	-	-	NC	-	-
AH24	BK3_IO30	-	78P	NC	-	-	NC	-	-
-	GND (Bank 3)	-	-	-	-	-	-	-	-
AK25	BK3_IO31	-	78N	NC	-	-	NC	-	-

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved ¹
V39	BK2_IO57	-	90N
W37	BK2_IO58	-	91P
-	GND (Bank 2)	-	-
W38	BK2_IO59	-	91N
W39	BK2_IO60	-	92P
AA39	BK2_IO61	-	92N
-	GND (Bank 2)	-	-
-	GND (Bank 3)	-	-
AA38	BK3_IO0	-	93P
Y35	BK3_IO1	-	93N
AA37	BK3_IO2	-	94P
-	GND (Bank 3)	-	-
AA35	BK3_IO3	-	94N
AB39	BK3_IO4	-	95P
AB38	BK3_IO5	-	95N
AA36	BK3_IO6	-	96P
AB37	BK3_IO7	-	96N
AC39	BK3_IO8	-	97P
AC38	BK3_IO9	-	97N
AB36	BK3_IO10	-	98P
-	GND (Bank 3)	-	-
AC37	BK3_IO11	-	98N
AC36	BK3_IO12	-	99P
AD39	BK3_IO13	-	99N
AD37	BK3_IO14	-	100P
AD36	BK3_IO15	-	100N
AD35	BK3_IO16	-	101P
AE38	BK3_IO17	-	101N
AD38	BK3_IO18	-	102P
-	GND (Bank 3)	-	-
AE39	BK3_IO19	-	102N
AF38	BK3_IO20	-	103P
AF37	BK3_IO21	-	103N
AF39	BK3_IO22	-	104P
AE36	BK3_IO23	-	104N
AF36	BK3_IO24	-	105P
AG38	BK3_IO25	-	105N
AG39	BK3_IO26	-	106P
-	GND (Bank 3)	-	-
AG37	BK3_IO27	-	106N
AH37	BK3_IO28	-	107P
AH38	BK3_IO29	-	107N
AG36	BK3_IO30	-	108P

ispXPGA Logic Signal Connections: 900-Ball fpBGA

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹
D3	BK0_IO0	-	0P	NC	-	-
E3	BK0_IO1	-	0N	NC	-	-
C2	BK0_IO2	-	1P	NC	-	-
-	GND (Bank 0)	-	-	-	-	-
C1	BK0_IO3	-	1N	NC	-	-
E4	BK0_IO4	-	2P	BK0_IO0	-	0P
F5	BK0_IO5	-	2N	BK0_IO1	-	0N
D2	BK0_IO6	HSI0A_SOUTP	3P	BK0_IO2	HSI0A_SOUTP	1P/HSI0
-	-	-	-	GND (Bank 0)	-	-
D1	BK0_IO7	HSI0A_SOUTN	3N	BK0_IO3	HSI0A_SOUTN	1N/HSI0
F4	BK0_IO8	-	4P	BK0_IO4	-	2P/HSI0
F3	BK0_IO9	-	4N	BK0_IO5	-	2N/HSI0
E2	BK0_IO10	HSI0A_SINP	5P/HSI0	BK0_IO6	HSI0A_SINP	3P/HSI0
-	GND (Bank 0)	-	-	-	-	-
E1	BK0_IO11	HSI0A_SINN	5N/HSI0	BK0_IO7	HSI0A_SINN	3N/HSI0
G6	BK0_IO12	VREF0	6P/HSI0	BK0_IO9	VREF0	4N/HSI0
G5	BK0_IO13	-	6N/HSI0	BK0_IO8	-	4P/HSI0
F1	BK0_IO14	HSI0B_SOUTP	7P/HSI0	NC	-	-
F2	BK0_IO15	HSI0B_SOUTN	7N/HSI0	NC	-	-
G4	BK0_IO16	-	8P/HSI0	NC	-	-
G3	BK0_IO17	-	8N/HSI0	NC	-	-
G2	BK0_IO18	HSI0B_SINP	9P/HSI0	NC	-	-
-	GND (Bank 0)	-	-	-	-	-
G1	BK0_IO19	HSI0B_SINN	9N/HSI0	NC	-	-
H3	BK0_IO20	-	10P/HSI0	NC	-	-
H4	BK0_IO21	-	10N/HSI0	NC	-	-
H1	BK0_IO22	HSI1A_SOUTP	11P/HSI0	NC	-	-
H2	BK0_IO23	HSI1A_SOUTN	11N/HSI0	NC	-	-
J7	BK0_IO24	-	12P/HSI0	NC	-	-
J6	BK0_IO25	-	12N/HSI0	NC	-	-
J1	BK0_IO26	HSI1A_SINP	13P/HSI1	NC	-	-
-	GND (Bank 0)	-	-	-	-	-
J2	BK0_IO27	HSI1A_SINN	13N/HSI1	NC	-	-
J4	BK0_IO28	-	14P/HSI1	NC	-	-
J5	BK0_IO29	-	14N/HSI1	NC	-	-
K1	BK0_IO30	HSI1B_SOUTP	15P/HSI1	BK0_IO10	HSI0B_SOUTP	5P/HSI0
-	-	-	-	GND (Bank 0)	-	-
K2	BK0_IO31	HSI1B_SOUTN	15N/HSI1	BK0_IO11	HSI0B_SOUTN	5N/HSI0
K5	BK0_IO32	-	16P/HSI1	BK0_IO12	-	6P/HSI0
K4	BK0_IO33	-	16N/HSI1	BK0_IO13	-	6N/HSI0
L1	BK0_IO34	HSI1B_SINP	17P/HSI1	BK0_IO14	HSI0B_SINP	7P/HSI0
-	GND (Bank 0)	-	-	-	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹
B15	BK7_IO1	-	217N	BK7_IO1	-	147N
C15	BK7_IO2	-	218P	BK7_IO2	-	148P
-	GND (Bank 7)	-	-	-	-	-
D15	BK7_IO3	-	218N	BK7_IO3	-	148N
E15	BK7_IO4	-	219P	BK7_IO4	-	149P
F15	BK7_IO5	-	219N	BK7_IO5	-	149N
A14	BK7_IO6	-	220P	BK7_IO6	-	150P
-	-	-	-	GND (Bank 7)	-	-
B14	BK7_IO7	-	220N	BK7_IO7	-	150N
C14	BK7_IO8	-	221P	BK7_IO8	-	151P
D14	BK7_IO9	-	221N	BK7_IO9	-	151N
E14	BK7_IO10	-	222P	BK7_IO10	-	152P
-	GND (Bank 7)	-	-	-	-	-
F14	BK7_IO11	-	222N	BK7_IO11	-	152N
C13	BK7_IO12	-	223P	BK7_IO12	-	153P
D13	BK7_IO13	-	223N	BK7_IO13	-	153N
B13	BK7_IO14	-	224P	BK7_IO14	-	154P
-	-	-	-	GND (Bank 7)	-	-
A13	BK7_IO15	-	224N	BK7_IO15	-	154N
F13	BK7_IO16	-	225P	BK7_IO16	-	155P
G13	BK7_IO17	-	225N	BK7_IO17	-	155N
A12	BK7_IO18	-	226P	BK7_IO18	-	156P
-	GND (Bank 7)	-	-	-	-	-
B12	BK7_IO19	-	226N	BK7_IO19	-	156N
C12	BK7_IO20	-	227P	NC	-	-
D12	BK7_IO21	-	227N	NC	-	-
A11	BK7_IO22	-	228P	NC	-	-
B11	BK7_IO23	-	228N	NC	-	-
E12	BK7_IO24	-	229P	NC	-	-
F12	BK7_IO25	-	229N	NC	-	-
C11	BK7_IO26	-	230P	NC	-	-
-	GND (Bank 7)	-	-	-	-	-
D11	BK7_IO27	-	230N	NC	-	-
E11	BK7_IO28	-	231P	NC	-	-
F11	BK7_IO29	-	231N	NC	-	-
B10	BK7_IO30	-	232P	NC	-	-
A10	BK7_IO31	-	232N	NC	-	-
D10	BK7_IO32	-	233P	NC	-	-
E10	BK7_IO33	-	233N	NC	-	-
A9	BK7_IO34	-	234P	NC	-	-
-	GND (Bank 7)	-	-	-	-	-
B9	BK7_IO35	-	234N	NC	-	-

Commercial (Cont.)

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX200B-05F516C	210K	2.5/3.3	-5	fpBGA	516
LFX200B-04F516C	210K	2.5/3.3	-4	fpBGA	516
LFX200B-03F516C	210K	2.5/3.3	-3	fpBGA	516
LFX200C-04F516C	210K	1.8	-4	fpBGA	516
LFX200C-03F516C	210K	1.8	-3	fpBGA	516
LFX200B-05FH516C ¹	210K	2.5/3.3	-5	fpBGA	516
LFX200B-04FH516C ¹	210K	2.5/3.3	-4	fpBGA	516
LFX200B-03FH516C ¹	210K	2.5/3.3	-3	fpBGA	516
LFX200C-04FH516C ¹	210K	1.8	-4	fpBGA	516
LFX200C-03FH516C ¹	210K	1.8	-3	fpBGA	516
LFX500B-05F516C	476K	2.5/3.3	-5	fpBGA	516
LFX500B-04F516C	476K	2.5/3.3	-4	fpBGA	516
LFX500B-03F516C	476K	2.5/3.3	-3	fpBGA	516
LFX500C-04F516C	476K	1.8	-4	fpBGA	516
LFX500C-03F516C	476K	1.8	-3	fpBGA	516
LFX500B-05FH516C ¹	476K	2.5/3.3	-5	fpBGA	516
LFX500B-04FH516C ¹	476K	2.5/3.3	-4	fpBGA	516
LFX500B-03FH516C ¹	476K	2.5/3.3	-3	fpBGA	516
LFX500C-04FH516C ¹	476K	1.8	-4	fpBGA	516
LFX500C-03FH516C ¹	476K	1.8	-3	fpBGA	516
LFX500B-05F900C	476K	2.5/3.3	-5	fpBGA	900
LFX500B-04F900C	476K	2.5/3.3	-4	fpBGA	900
LFX500B-03F900C	476K	2.5/3.3	-3	fpBGA	900
LFX500C-04F900C	476K	1.8	-4	fpBGA	900
LFX500C-03F900C	476K	1.8	-3	fpBGA	900
LFX1200B-05F900C ²	1.25M	2.5/3.3	-5	fpBGA	900
LFX1200B-04F900C ²	1.25M	2.5/3.3	-4	fpBGA	900
LFX1200B-03F900C ²	1.25M	2.5/3.3	-3	fpBGA	900
LFX1200C-04F900C ²	1.25M	1.8	-4	fpBGA	900
LFX1200C-03F900C ²	1.25M	1.8	-3	fpBGA	900
LFX1200B-05FE680C ²	1.25M	2.5/3.3	-5	fpSBGA	680
LFX1200B-04FE680C ²	1.25M	2.5/3.3	-4	fpSBGA	680
LFX1200B-03FE680C ²	1.25M	2.5/3.3	-3	fpSBGA	680
LFX1200C-04FE680C ²	1.25M	1.8	-4	fpSBGA	680
LFX1200C-03FE680C ²	1.25M	1.8	-3	fpSBGA	680

1. FH516 package was converted to F516 via [PCN #09A-08](#).

2. Discontinued via [PCN #03A-10](#).