Lattice Semiconductor Corporation - LFX1200EC-04FE680C Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	15376
Total RAM Bits	423936
Number of I/O	496
Number of Gates	1250000
Voltage - Supply	1.65V ~ 1.95V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	680-LBGA
Supplier Device Package	680-FPSBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx1200ec-04fe680c

Lattice Semiconductor Corporation

Includes High-Performance, Low-Cost "E-Series"

ispXPGA® Family

February 2010 **Data Sheet DS1026**

■ Non-volatile, Infinitely Reconfigurable

- Instant-on - Powers up in microseconds via on-chip E^2CMOS® based memory
- No external configuration memory
- Excellent design security, no bit stream to intercept
- Reconfigure SRAM based logic in milliseconds

■ High Logic Density for System-level Integration

- 139K to 1.25M functional gates
- 160 to 496 I/O
- 1.8V, 2.5V, and 3.3V V_{CC} operation
- Up to 414Kb sysMEM™ embedded memory

■ High Performance Programmable Function Unit (PFU)

- Four LUT-4 per PFU supports wide and narrow functions
- Dual flip-flops per LUT-4 for extensive pipelining
- Dedicated logic for adders, multipliers, multiplexers, and counters

■ Flexible Memory Resources

- Multiple sysMEM Embedded RAM Blocks
  - Single port, Dual port, and FIFO operation
- 64-bit distributed memory in each PFU
  - Single port, Double port, FIFO, and Shift Register operation

■ Flexible Programming, Reconfiguration, and Testing

- Supports IEEE 1532 and 1149.1
- Microprocessor configuration interface
- Program E^2CMOS while operating from SRAM

■ Eight sysCLOCK™ Phase Locked Loops (PLLs) for Clock Management

- True PLL technology
- 10MHz to 320MHz operation
- Clock multiplication and division
- Phase adjustment
- Shift clocks in 250ps steps

■ sysIO™ for High System Performance

- High speed memory support through SSTL and HSTL
- Advanced buses supported through PCI, GTL+, LVDS, BLVDS, and LVPECL
- Standard logic supported through LVTTL, LVCMOS 3.3, 2.5 and 1.8
- 5V tolerant I/O for LVCMOS 3.3 and LVTTL interfaces
- Programmable drive strength for series termination
- Programmable bus maintenance

■ Two Options Available

- High-performance sysHSI (standard part number)
- Low-cost, no sysHSI ("E-Series")

■ sysHSI™ Capability for Ultra Fast Serial Communications

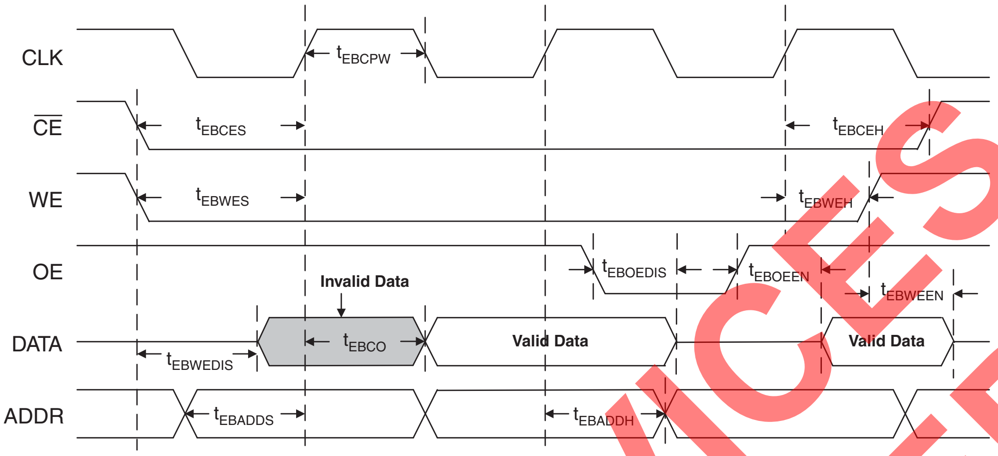
- Up to 800Mbps performance
- Up to 20 channels per device
- Built in Clock Data Recovery (CDR) and Serialization and De-serialization (SERDES)

Table 1. ispXPGA Family Selection Guide

	ispXPGA 125/E	**ispXPGA 200/E**	**ispXPGA 500/E**	**ispXPGA 1200/E**[3]
Functional Gates	139K	210K	476K	1.25M
PFUs	484	676	1764	3844
LUT-4s	1936	2704	7056	15376
Logic FFs	3.8K	5.4K	14.1K	30.7K
sysMEM Memory	92K	111K	184K	414K
Distributed Memory	30K	43K	112K	246K
EBR	20	24	40	90
sysHSI Channels[1]	4	8	12	20
User I/O	160/176	160/208	336	496
Packaging	256 fpBGA 516 fpBGA[2]	256 fpBGA 516 fpBGA[2]	516 fpBGA[2] 900 fpBGA	680 fpSBGA 900 fpBGA

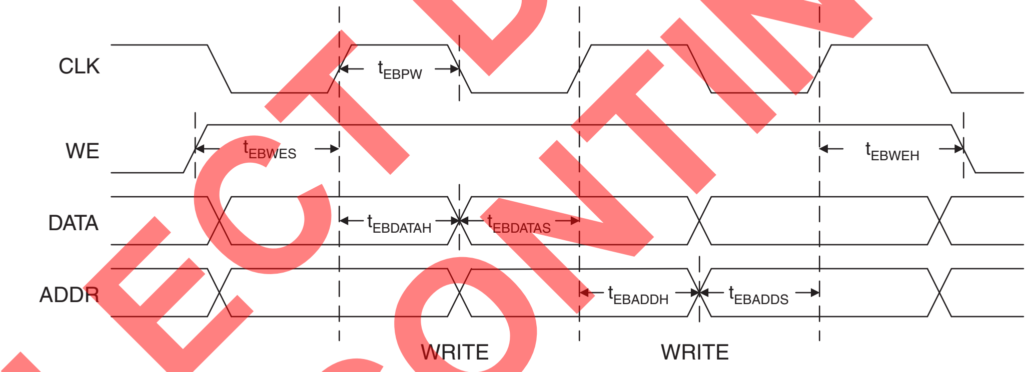
1. "E-Series" does not support sysHSI.
2. FH516 package was converted to F516 via PCN #09A-08.
3. Discontinued via PCN #03A-10.

Figure 13. EBR Synchronous Read Timing Diagram



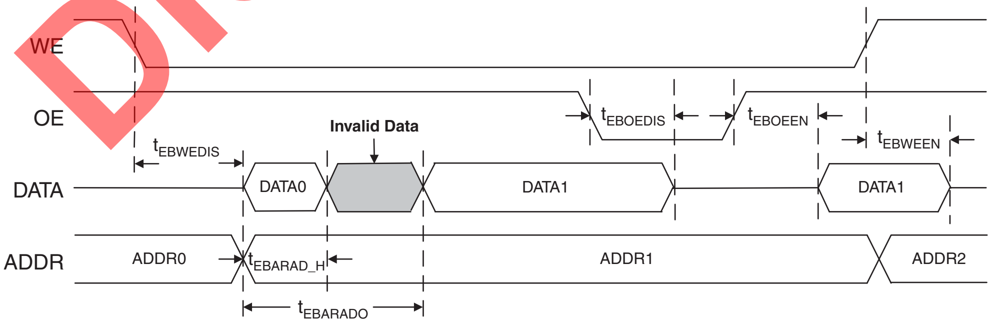
Synchronous Write: The WE signal controls the synchronous write operation. When the WE signal is high, the write operation begins. Once the address and data are present and the Output Enable (OE) is active, a rising clock edge (or falling edge depending on polarity) causes the data to be stored into the EBR. Figure 14 illustrates the synchronous write timing.

Figure 14. EBR Synchronous Write Timing Diagram



Asynchronous Read: The WE signal controls the asynchronous read operation. When the WE signal is low, the read operation begins. Shortly after the address is present, the stored data is available on the DATA port. Figure 15 illustrates the asynchronous read timing. For more information about the EBR, refer to TN1028 [ispXPGA Memory Usage Guidelines].

Figure 15. EBR Asynchronous Read Timing Diagram



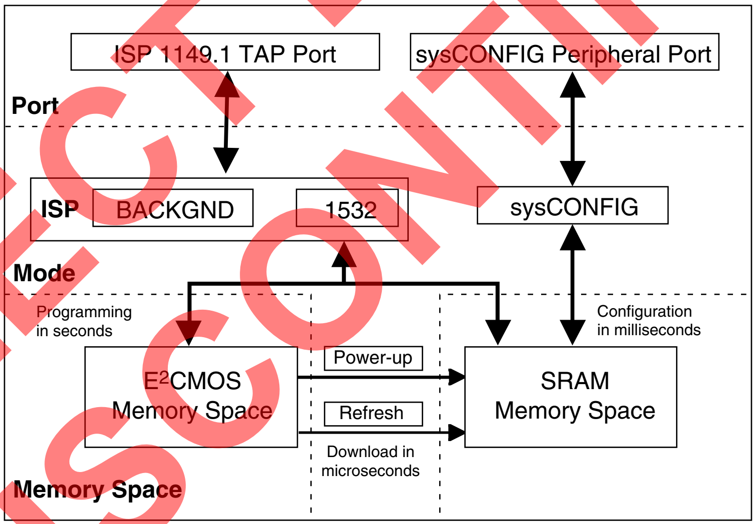
Configuration and Programming

The ispXPGA family of devices takes a unique approach to FPGA configuration memory. It contains two types of memory, Static RAM and non-volatile E^2CMOS cells. The static RAM is used to control the functionality of the device during normal operation and the E^2CMOS memory cells are used to load the SRAM. The E^2CMOS memory module can be thought of as the hard drive for the ispXPGA configuration and the SRAM as the working configuration memory. There is a one-to-one relationship between SRAM memory and the E^2CMOS cells. The SRAM can be configured either from the E^2CMOS memory or from an external source, as shown in Figure 21.

Figure 21 shows the different ports and modes that are used in the configuration and programming of the ispXPGA devices. There are two possible ports that can be used for configuration of the SRAM memory: the ISP port which supports the IEEE 1149.1 Test Access Port (TAP) Std., accommodates bit-wide configuration. The sysCONFIG port allows byte-wide configuration of the SRAM configuration memory. When programming the E^2CMOS memory, only the 1149.1 TAP can be used.

Configuration and programming done through the 1149.1 Test Access Port (TAP) supports both the IEEE Std. 1149.1 Boundary Scan TAP specification and the IEEE Std. 1532 In-System Configuration specification. To configure or program the device using the 1149.1 TAP the device must be in the ISP mode. To configure the SRAM memory using the sysCONFIG Port, the device must be in the sysCONFIG mode. Upon power-up, the device's SRAM memory can be configured either from the E^2CMOS memory or from an external source through the sysCONFIG mode. Additionally, the SRAM can be re-configured from the E^2CMOS memory by executing a "REFRESH." See TN1026, ispXP Configuration Usage Guidelines, for more in depth information on the different programming modes, timing and wake-up.

Figure 21. ispXP Block Diagram



Supports IEEE 1149.1 Boundary Scan Testability

All ispXPGA devices have boundary scan cells and supports the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal boundary scan registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board level testing.

Security Scheme

A programmable security scheme is provided on the ispXPGA devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, the security scheme prevents read-back of the programmed

Absolute Maximum Ratings[1, 2, 3]

	1.8V	2.5V/3.3V
Supply Voltage (V_{CC})	-0.5 to 2.5V	-0.5 to 5.5V
PLL Supply Voltage (V_{CCP})	-0.5 to 2.5V	-0.5 to 5.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V
IEEE 1149.1 TAP Supply Voltage (V_{CCJ})	-0.5 to 4.5V	-0.5 to 4.5V
Input Voltage Applied[4, 5]	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C
Junction Temperature (T_J) with Power Applied	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied (while programming, following the programming specifications).
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to (V_{IH} (MAX) + 2) volts not to exceed 6V is permitted for a duration of <20ns.
5. A maximum of 64 I/Os per device with $V_{IN} > 3.6V$ is allowed.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage for 1.8V device[1]	1.65	1.95	V
	Supply Voltage for 2.5V device	2.3	2.7	V
	Supply Voltage for 3.3V device	3.0	3.6	V
V_{CCP}	Supply Voltage for PLL and sysHSI blocks, 1.8V devices[1]	1.65	1.95	V
	Supply Voltage for PLL and sysHSI blocks, 2.5V devices	2.3	2.7	V
	Supply Voltage for PLL and sysHSI blocks, 3.3V devices	3.0	3.6	V
V_{CCJ}	Supply Voltage for IEEE 1149.1 Test Access Port for LVCMOS 1.8V	1.65	1.95	V
	Supply Voltage for IEEE 1149.1 Test Access Port for LVCMOS 2.5V	2.3	2.7	V
	Supply Voltage for IEEE 1149.1 Test Access Port for LVCMOS 3.3V	3.0	3.6	V
T_J (COM)	Junction Temperature Commercial Operation	0	85	C
T_J (IND)	Junction Temperature Industrial Operation	-40	105	C

1. sysHSI specification is valid for V_{CC} and V_{CCP} = 1.7V to 1.9V.

E^2CMOS Erase Reprogram Specifications

Parameter	Min	Max	Units
Erase/Reprogram Cycle[1]	1,000	—	Cycles

1. Valid over commercial temperature range.

Hot Socketing Characteristics[1, 2, 3, 4]

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DK}	Input or Tristated I/O Leakage Current	0 ð V_{IN} ð 3.0V	—	+/-50	+/-800	µA

1. Insensitive to sequence of V_{CC} and V_{CCO} when V_{CCO} ð 1.0V. For V_{CCO} > 1.0V, V_{CC} min must be present. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO}, provided (V_{IN} - V_{CCO}) ð 3.6V.
2. LVTTL, LVCMOS only.
3. 0 < V_{CC} ð V_{CC} (MAX), 0 < V_{CCO} ð V_{CCO} (MAX).
4. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until non-volatile cells are active.

sysIO Recommended Operating Conditions

Standard	V_{CCO} (V)[1]			V_{REF} (V)		
	Min.	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
LVCMOS 3.3	3.0	3.3	3.6	-	-	-
LVCMOS 2.5	2.3	2.5	2.7	-	-	-
LVCMOS 1.8[2]	1.65	1.8	1.95	-	-	-
LVTTL	3.0	3.3	3.6	-	-	-
PCI 3.3	3.0	3.3	3.6	-	-	-
AGP-1X	3.15	3.3	3.45	-	-	-
SSTL 2	2.3	2.5	2.7	1.15	1.25	1.35
SSTL 3	3.0	3.3	3.6	1.3	1.5	1.7
CTT 3.3	3.0	3.3	3.6	1.35	1.5	1.65
CTT 2.5	2.3	2.5	2.7	1.35	1.5	1.65
HSTL Class I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL Class III	1.4	1.5	1.6	-	0.9	-
GTL+	-	-	-	0.882	1.0	1.122
LVDS	2.3	2.5	2.7	-	-	-
LVPECL	3.0	3.3	3.6	-	-	-
BLVDS	2.3	2.5	2.7	-	-	-

[1] Inputs independent of V_{CCO}.

[2] Design tool default setting.

ispXPGA 125B/C & ispXPGA 125EB/EC PFU Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Functional Delays								
LUTs								
t_{LUT4}	4-Input LUT Delay	—	0.41	—	0.44	—	0.51	ns
t_{LUT5}	5-Input LUT Delay	—	0.73	—	0.79	—	0.91	ns
t_{LUT6}	6-Input LUT Delay	—	0.86	—	0.93	—	1.07	ns
Shift Register (LUT)								
t_{LSR_S}	Shift Register Setup Time	-0.64	—	-0.62	—	-0.53	—	ns
t_{LSR_H}	Shift Register Hold Time	0.61	—	0.63	—	0.72	—	ns
t_{LSR_CO}	Shift Register Clock to Output Delay	—	0.70	—	0.75	—	0.86	ns
Arithmetic Functions								
$t_{LCTHRUR}$	MC (Macro Cell) Carry In to MC Carry Out Delay (Ripple)	—	0.08	—	0.09	—	0.10	ns
$t_{LCTHRUL}$[2]	MC Carry In to MC Carry Out Delay (Look Ahead)	—	0.05	—	0.05	—	0.06	ns
t_{LSTHRU}	MC Sum In to MC Sum Out Delay	—	0.42	—	0.45	—	0.52	ns
$t_{LSINCOUT}$	MC Sum In to MC Carry Out Delay	—	0.29	—	0.31	—	0.36	ns
$t_{LCINSOUTR}$	MC Carry In to MC Sum Out Delay (Ripple)	—	0.36	—	0.39	—	0.45	ns
$t_{LCINSOUTL}$	MC Carry In to MC Sum Out Delay (Look Ahead)	—	0.26	—	0.28	—	0.32	ns
Feed-thru								
t_{LFT}	PFU Feed-Thru Delay	—	0.15	—	0.16	—	0.18	ns
Distributed RAM								
t_{LRAM_CO}	Clock to RAM Output	—	1.24	—	1.33	—	1.53	ns
t_{LRAMAD_S}	Address Setup Time	-0.41	—	-0.40	—	-0.34	—	ns
t_{LRAMD_S}	Data Setup Time	0.21	—	0.22	—	0.25	—	ns
t_{LRAMWE_S}	Write Enable Setup Time	0.45	—	0.46	—	0.53	—	ns
t_{LRAMAD_H}	Address Hold Time	0.58	—	0.60	—	0.69	—	ns
t_{LRAMD_H}	Data Hold Time	0.11	—	0.11	—	0.13	—	ns
t_{LRAMWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{LRAMCPW}$	Clock Pulse Width (High or Low)	2.91	—	3.00	—	3.45	—	ns
$t_{LRAMADO}$	Address to Output Delay	—	0.86	—	0.93	—	1.07	ns
Register/Latch Delays								
Registers								
t_{L_CO}	Register Clock to Output Delay	—	0.58	—	0.62	—	0.71	ns
t_{L_S}	Register Setup Time (Data before Clock)	0.14	—	0.14	—	0.16	—	ns
t_{L_H}	Register Hold Time (Data after Clock)	-0.12	—	-0.12	—	-0.10	—	ns
t_{LCE_S}	Register Clock Enable Setup Time	-0.11	—	-0.11	—	-0.09	—	ns
t_{LCE_H}	Register Clock Enable Hold Time	0.11	—	0.11	—	0.13	—	ns
Latches								
t_{L_GO}	Latch Gate to Output Delay	—	0.09	—	0.10	—	0.12	ns
t_{LL_S}	Latch Setup Time	0.14	—	0.14	—	0.16	—	ns
t_{LL_H}	Latch Hold Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{LLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns

ispXPGA 125B/C & ispXPGA 125EB/EC PFU Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Set								
t_{LASSRO}	Asynchronous Set/Reset to Output	—	1.09	—	1.17	—	1.35	ns
$t_{LASSRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{LASSRR}	Asynchronous Set/Reset Recovery	—	0.51	—	0.55	—	0.63	ns
t_{LSSR_S}	Synchronous Set/Reset Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{LSSR_H}	Synchronous Set/Reset Hold Time	0.03	—	0.03	—	0.03	—	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.
2. $t_{LCTHRUL}$ quoted bit by bit.

Timing v.0.3

ispXPGA 125B/C & ispXPGA 125EB/EC PIC Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Register/Latch Delays								
t_{IO_CO}	Register Clock to Output Delay	—	0.89	—	0.96	—	1.10	ns
t_{IO_S}	Register Setup Time (Data before Clock)	0.05	—	0.05	—	0.06	—	ns
t_{IO_H}	Register Hold Time (Data after Clock)	0.06	—	0.06	—	0.07	—	ns
t_{IOCE_S}	Register Clock Enable Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{IOCE_H}	Register Clock Enable Hold Time	0.13	—	0.13	—	0.15	—	ns
t_{IO_GO}	Latch Gate to Output Delay	—	0.68	—	0.73	—	0.84	ns
t_{IOL_S}	Latch Setup Time	0.05	—	0.05	—	0.06	—	ns
t_{IOL_H}	Latch Hold Time	0.06	—	0.06	—	0.07	—	ns
t_{IOLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns
t_{IOASRO}	Asynchronous Set/Reset to Output	—	1.00	—	1.08	—	1.24	ns
$t_{IOASRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{IOASRR}	Asynchronous Set/Reset Recovery Time	—	0.23	—	0.25	—	0.29	ns
Input/Output Delays								
t_{IOBUF}	Output Buffer Delay	—	0.97	—	1.04	—	1.20	ns
t_{IOIN}	Input Buffer Delay	—	0.57	—	0.61	—	0.70	ns
t_{IOEN}	Output Enable Delay	—	0.53	—	0.57	—	0.66	ns
t_{IODIS}	Output Disable Delay	—	-0.14	—	-0.13	—	-0.11	ns
t_{IOFT}	Feed-thru Delay	—	0.19	—	0.20	—	0.23	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 125B/C & ispXPGA 125EB/EC Timing Adders

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	4.28	—	4.6	—	5.29	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

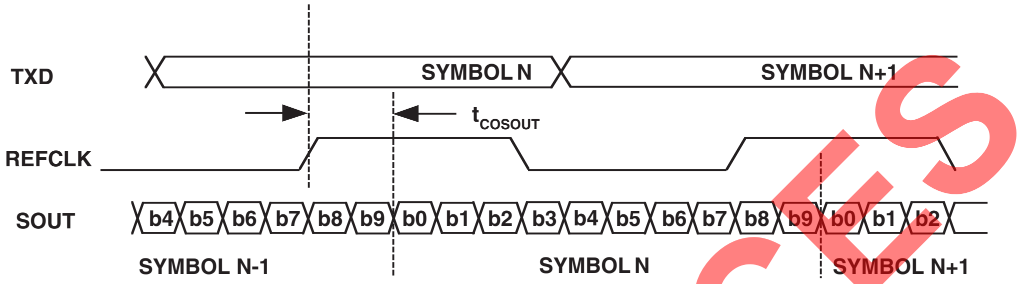
ispXPGA 500B/C & ispXPGA 500EB/EC PFU Timing Parameters

Over Recommended Operating Conditions

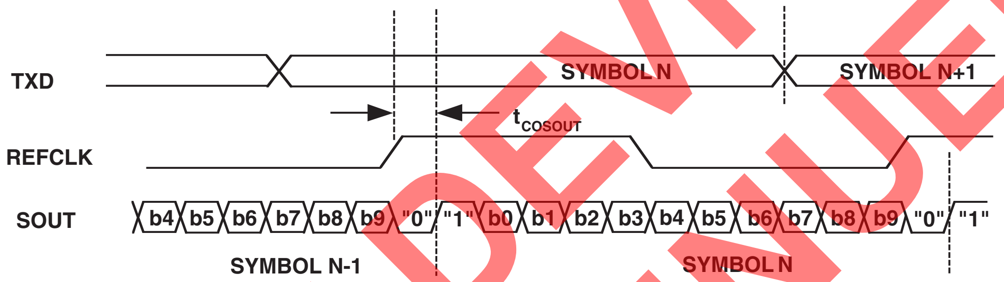
Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Functional Delays								
LUTs								
t_{LUT4}	4-Input LUT Delay	—	0.41	—	0.44	—	0.51	ns
t_{LUT5}	5-Input LUT Delay	—	0.73	—	0.79	—	0.91	ns
t_{LUT6}	6-Input LUT Delay	—	0.86	—	0.93	—	1.07	ns
Shift Register (LUT)								
t_{LSR_S}	Shift Register Setup Time	-0.64	—	-0.62	—	-0.53	—	ns
t_{LSR_H}	Shift Register Hold Time	0.61	—	0.63	—	0.72	—	ns
t_{LSR_CO}	Shift Register Clock to Output Delay	—	0.70	—	0.75	—	0.86	ns
Arithmetic Functions								
$t_{LCTHRUR}$	MC (Macro Cell) Carry In to MC Carry Out Delay (Ripple)	—	0.08	—	0.09	—	0.10	ns
$t_{LCTHRUL}$[2]	MC Carry In to MC Carry Out Delay (Look Ahead)	—	0.05	—	0.05	—	0.06	ns
t_{LSTHRU}	MC Sum In to MC Sum Out Delay	—	0.42	—	0.45	—	0.52	ns
$t_{LSINCOUT}$	MC Sum In to MC Carry Out Delay	—	0.29	—	0.31	—	0.36	ns
$t_{LCINSOUTR}$	MC Carry In to MC Sum Out Delay (Ripple)	—	0.36	—	0.39	—	0.45	ns
$t_{LCINSOUTL}$	MC Carry In to MC Sum Out Delay (Look Ahead)	—	0.26	—	0.28	—	0.32	ns
Feed-thru								
t_{LFT}	PFU Feed-Thru Delay	—	0.15	—	0.16	—	0.18	ns
Distributed RAM								
t_{LRAM_CO}	Clock to RAM Output	—	1.24	—	1.33	—	1.53	ns
t_{LRAMAD_S}	Address Setup Time	-0.41	—	-0.40	—	-0.34	—	ns
t_{LRAMD_S}	Data Setup Time	0.21	—	0.22	—	0.25	—	ns
t_{LRAMWE_S}	Write Enable Setup Time	0.45	—	0.46	—	0.53	—	ns
t_{LRAMAD_H}	Address Hold Time	0.58	—	0.60	—	0.69	—	ns
t_{LRAMD_H}	Data Hold Time	0.11	—	0.11	—	0.13	—	ns
t_{LRAMWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{LRAMCPW}$	Clock Pulse Width (High or Low)	2.91	—	3.00	—	3.45	—	ns
$t_{LRAMADO}$	Address to Output Delay	—	0.86	—	0.93	—	1.07	ns
Register/Latch Delays								
Registers								
t_{L_CO}	Register Clock to Output Delay	—	0.58	—	0.62	—	0.71	ns
t_{L_S}	Register Setup Time (Data before Clock)	0.14	—	0.14	—	0.16	—	ns
t_{L_H}	Register Hold Time (Data after Clock)	-0.12	—	-0.12	—	-0.10	—	ns
t_{LCE_S}	Register Clock Enable Setup Time	-0.11	—	-0.11	—	-0.09	—	ns
t_{LCE_H}	Register Clock Enable Hold Time	0.11	—	0.11	—	0.13	—	ns
Latches								
t_{L_GO}	Latch Gate to Output Delay	—	0.09	—	0.10	—	0.12	ns
t_{LL_S}	Latch Setup Time	0.14	—	0.14	—	0.16	—	ns
t_{LL_H}	Latch Hold Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{LLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns

Serializer Timing

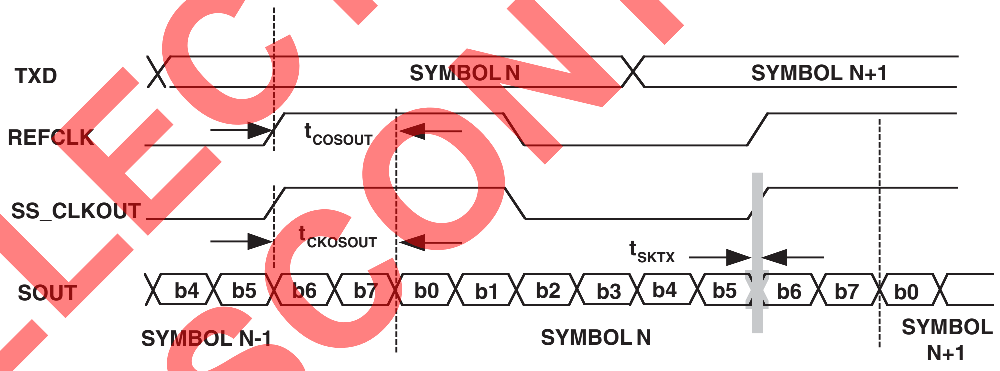
8B/10B SERIALIZER DELAY TIMING



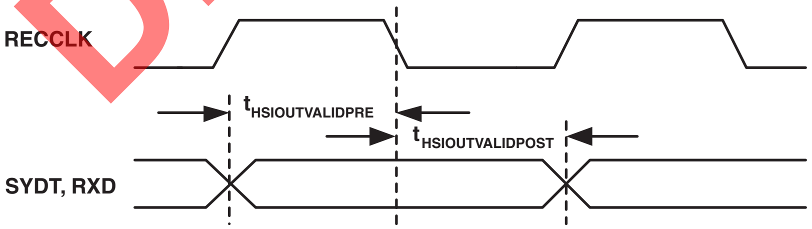
10B/12B SERIALIZER DELAY TIMING



SS Mode SERIALIZER DELAY TIMING



INTERNAL TIMING FOR sysHSI BLOCK



Signal Descriptions[1] (Cont.)

Signal Name	Signal Type	Description
HSI*m*A_CDRRST, HSI*m*B_CDRRST	Input	CDR Reset
HSI*m*_CSLOCK, HSI*m*_CSLOCK	Internal Signal	Indicates when the CSPLL circuit is locked
sysHSI Block (Source Synchronous Mode)[6]		
SS_CLKIN0P, SS_CLKIN1P	Input	P-side of differential clock input
SS_CLKIN0N, SS_CLKIN1N	Input	N-side of differential clock input
SS_CLKOUT0P, SS_CLKOUT1P	Output	P-side of differential clock output
SS_CLKOUT0N, SS_CLKOUT1N	Output	N-side of differential clock output
CAL0, CAL1	Input	Initiates source synchronous calibration sequence

1. x is a variable for the I/O number.
2. y is a variable for the I/O Bank.
3. z is a variable for the PLL number.
4. m is a variable for the sysHSI block number.
5. A and B refer to the sysHSI block channels.
6. 0 and 1 refer to Source Synchronous group 0 and 1
7. n is a variable for the GCLK and Input number
8. See Logic Signal Connections Table for differential pairing.

ispXPGA Power Supply and NC Connections[1]

Signal	256-Ball fpBGA[3]	516-Ball fpBGA[3]
V_{CC}	C3, C14, D4, D13, E5, E12, F6, F11, L6, L11, M5, M12, N4, N13, P3, P14	A9, A22, D4, D27, J1, J30, L11, L12, L15, L16, L19, L20, M11, M20, R11, R20, T11, T20, W11, W20, Y11, Y12, Y15, Y16, Y19, Y20, AB1, AB30, AG4, AG27, AK9, AK22
V_{CCO0}	F5, G5	F4, J4, M4, N11, P4, P11
V_{CCO1}	K5, L5	U4, U11, V11, W4, AB4, AE4
V_{CCO2}	M6, M7	Y13, Y14, AG6, AG9, AG12, AG14
V_{CCO3}	M10, M11	Y17, Y18, AG17, AG19, AG22, AG25
V_{CCO4}	K12, L12	U20, U27, V20, W27, AB27, AE27
V_{CCO5}	G12, F12	F27, J27, M27, N20, P20, P27
V_{CCO6}	E10, E11	D17, D19, D22, D25, L17, L18
V_{CCO7}	E6, E7	D6, D9, D12, D14, L13, L14
V_{CCP}	H3, J15	R4, T30
V_{CCJ}	A2	C4
GND	A1, A16, B2, B15, F7, F8, F9, F10, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L7, L8, L9, L10, R2, R15, T1, T16	A1, A30, B2, B29, C3, C28, M12, M13, M14, M15, M16, M17, M18, M19, N12, N13, N14, N15, N16, N17, N18, N19, P12, P13, P14, P15, P16, P17, P18, P19, R12, R13, R14, R15, R16, R17, R18, R19, T12, T13, T14, T15, T16, T17, T18, T19, U12, U13, U14, U15, U16, U17, U18, U19, V12, V13, V14, V15, V16, V17, V18, V19, W12, W13, W14, W15, W16, W17, W18, W19, AH3, AH28, AJ2, AJ29, AK1, AK30
GND_P	H15, J4	R29, T4
NC[2]	—	**LFX125:** A10, A13, A16, A17, A24, A25, A26, A4, A5, A6, A7, AA1, AA2, AA28, AA29, AA3, AB28, AC1, AC28, AD1, AD27, AD4, AE28, AE29, AE3, AE30, AF27, AF28, AF29, AF3, AF4, AG1, AG10, AG11, AG15, AG2, AG20, AG23, AG24, AG29, AG3, AG8, AH1, AH15, AH19, AH2, AH20, AH23, AH24, AH30, AH7, AH8, AH9, AJ1, AJ12, AJ14, AJ15, AJ19, AJ20, AJ21, AJ23, AJ24, AJ25, AJ27, AJ30, AJ6, AJ7, AJ8, AK11, AK14, AK15, AK20, AK21, AK23, AK24, AK25, AK27, AK5, AK6, AK7, B10, B13, B16, B17, B18, B23, B24, B25, B5, B6, B7, C11, C13, C14, C16, C17, C22, C23, C24, C25, C6, C7, C8, D11, D16, D23, D24, D28, D29, D3, D7, D8, E30, E4, F1, F29, F30, G1, G2, G27, G28, G29, G30, H1, H2, H27, H28, H29, H30, J2, J28, J29, J3, K1, K2, K27, K28, K3, K4, L1, L2, L27, L3, L4, M1, M2, M29, M3, M30, V27, V28, V3, V4, W1, W30, Y1, Y27, Y28, Y3, Y30 **LFX200:** A26, A25, A24, A17, A10, A7, A6, A5, A4, B25, B24, B23, B17, B10, B7, B6, B5, C25, C24, C23, C22, C16, C11, C8, C7, C6, D24, D23, D16, D11, D8, D7, E30, F30, F29, F1, G30, G29, G28, G27, G2, G1, H30, H29, H28, H27, H2, H1, J29, J28, J3, J2, K28, K27, K4, K3, K2, K1, L27, L4, L3, L2, L1, M3, V28, V27, V4, V3, W30, W1, Y30, Y28, Y27, Y3, Y1, AA29, AA28, AA3, AA2, AA1, AD27, AD4, AE28, AE3, AF29, AF28, AF27, AF3, AG29, AG24, AG23, AG20, AG11, AG10, AG8, AG2, AG1, AH30, AH24, AH23, AH20, AH9, AH8, AH7, AH2, AH1, AJ30, AJ27, AJ25, AJ24, AJ23, AJ21, AJ15, AJ12, AJ8, AJ7, AJ6, AJ1, AK27, AK25, AK24, AK23, AK21, AK15, AK11, AK7, AK6, AK5

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, V_{CC} or GND.
3. Balls for GND, V_{CC} and V_{CCOx} are connected within the substrate to their respective common signals. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

	LFX500			LFX200			LFX125		
516-Ball BGA Ball	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
-	-	-	-	GND (Bank 0)	-	-	-	-	-
R2	GCLK0	-	LVDS Pair0P	GCLK0	-	LVDS Pair0P	GCLK0	-	LVDS Pair0P
R3	GCLK1	-	LVDS Pair0N	GCLK1	-	LVDS Pair0N	GCLK1	-	LVDS Pair0N
R4	VCCP0	-	-	VCCP0	-	-	VCCP0	-	-
T4	GNDP0	-	-	GNDP0	-	-	GNDP0	-	-
T3	GCLK2	-	LVDS Pair1P	GCLK2	-	LVDS Pair1P	GCLK2	-	LVDS Pair1P
T2	GCLK3	-	LVDS Pair1N	GCLK3	-	LVDS Pair1N	GCLK3	-	LVDS Pair1N
-	-	-	-	GND (Bank 1)	-	-	-	-	-
T1	BK1_IO0	CLK_OUT2	21P	BK1_IO0	CLK_OUT2	13P	BK1_IO0	CLK_OUT2	11P
-	GND (Bank 1)	-	-	-	-	-	-	-	-
U1	BK1_IO1	CLK_OUT3	21N	BK1_IO1	CLK_OUT3	13N	BK1_IO1	CLK_OUT3	11N
U2	BK1_IO2	SS_CLKOUT0P	22P	BK1_IO2	SS_CLKOUT0P	14P	BK1_IO2	SS_CLKOUT0P	12P
-	-	-	-	-	-	-	GND (Bank 1)	-	-
U3	BK1_IO3	SS_CLKOUT0N	22N	BK1_IO3	SS_CLKOUT0N	14N	BK1_IO3	SS_CLKOUT0N	12N
V1	BK1_IO4	PLL_FBK2	23P	BK1_IO4	PLL_FBK2	15P	BK1_IO4	PLL_FBK2	13P
V2	BK1_IO5	PLL_FBK3	23N	BK1_IO5	PLL_FBK3	15N	BK1_IO5	PLL_FBK3	13N
V3	BK1_IO6	-	24P	NC	-	-	NC	-	-
-	GND (Bank 1)	-	-	-	-	-	-	-	-
V4	BK1_IO7	-	24N	NC	-	-	NC	-	-
W1	BK1_IO8	-	25P	NC	-	-	NC	-	-
Y1	BK1_IO9	-	25N	NC	-	-	NC	-	-
W2	BK1_IO10	SS_CLKIN0P	26P	BK1_IO6	SS_CLKIN0P	16P	BK1_IO6	SS_CLKIN0P	14P
-	-	-	-	GND (Bank 1)	-	-	-	-	-
W3	BK1_IO11	SS_CLKIN0N	26N	BK1_IO7	SS_CLKIN0N	16N	BK1_IO7	SS_CLKIN0N	14N
Y2	BK1_IO12	-	27P	BK1_IO8	-	17P	BK1_IO8	-	15P
-	-	-	-	-	-	-	GND (Bank 1)	-	-
Y4	BK1_IO13	-	27N	BK1_IO9	-	17N	BK1_IO9	-	15N
Y3	BK1_IO14	-	28P	NC	-	-	NC	-	-
-	GND (Bank 1)	-	-	-	-	-	-	-	-
AA1	BK1_IO15	-	28N	NC	-	-	NC	-	-
AA2	BK1_IO16	-	29P	NC	-	-	NC	-	-
AA3	BK1_IO17	-	29N	NC	-	-	NC	-	-
AB2	BK1_IO18	HSI2A_SOUTP	30P	BK1_IO10	HSI1A_SOUTP	18P/HSI1	BK1_IO10	-	16P
AC2	BK1_IO19	HSI2A_SOUTN	30N	BK1_IO11	HSI1A_SOUTN	18N/HSI1	BK1_IO11	-	16N
AB3	BK1_IO20	PLL_RST2	31P	BK1_IO12	PLL_RST2	19P/HSI1	BK1_IO12	PLL_RST2	17P
AA4	BK1_IO21	PLL_RST3	31N	BK1_IO13	PLL_RST3	19N/HSI1	BK1_IO13	PLL_RST3	17N
AC1	BK1_IO22	HSI2A_SINP	32P	BK1_IO14	HSI1A_SINP	20P/HSI1	NC	-	-
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-	-	-	-
AD1	BK1_IO23	HSI2A_SINN	32N	BK1_IO15	HSI1A_SINN	20N/HSI1	NC	-	-
AE1	BK1_IO24	VREF1	33P/HSI2	BK1_IO16	VREF1	21P/HSI1	BK1_IO14	VREF1	18P
AF1	BK1_IO25	-	33N/HSI2	BK1_IO17	-	21N/HSI1	BK1_IO15	-	18N
AC3	BK1_IO26	HSI2B_SOUTP	34P/HSI2	BK1_IO18	HSI1B_SOUTP	22P/HSI1	BK1_IO16	-	19P
-	-	-	-	-	-	-	GND (Bank 1)	-	-
AC4	BK1_IO27	HSI2B_SOUTN	34N/HSI2	BK1_IO19	HSI1B_SOUTN	22N/HSI1	BK1_IO17	-	19N
AD2	BK1_IO28	-	35P/HSI2	BK1_IO20	-	23P/HSI1	BK1_IO18	-	20P
AD3	BK1_IO29	-	35N/HSI2	BK1_IO21	-	23N/HSI1	BK1_IO19	-	20N
AE2	BK1_IO30	HSI2B_SINP	36P/HSI2	BK1_IO22	HSI1B_SINP	24P/HSI1	BK1_IO20	-	21P
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-	-	-	-
AF2	BK1_IO31	HSI2B_SINN	36N/HSI2	BK1_IO23	HSI1B_SINN	24N/HSI1	BK1_IO21	-	21N
AD4	BK1_IO32	-	37P/HSI2	NC	-	-	NC	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AJ13	BK2_IO32	-	58P	BK2_IO18	-	35P	BK2_IO18	-	31P
-	-	-	-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
AK12	BK2_IO33	-	58N	BK2_IO19	-	35N	BK2_IO19	-	31N
AK13	BK2_IO34	-	59P	BK2_IO20	-	36P	BK2_IO20	-	32P
-	GND (Bank 2)	-	-	-	-	-	-	-	-
AH14	BK2_IO35	-	59N	BK2_IO21	-	36N	BK2_IO21	-	32N
AJ14	BK2_IO36	-	60P	BK2_IO22	-	37P	NC	-	-
AK14	BK2_IO37	-	60N	BK2_IO23	-	37N	NC	-	-
AG15	BK2_IO38	-	61P	BK2_IO24	-	38P	NC	-	-
AH15	BK2_IO39	-	61N	BK2_IO25	-	38N	NC	-	-
AJ15	BK2_IO40	-	62P	NC	-	-	NC	-	-
AK15	BK2_IO41	-	62N	NC	-	-	NC	-	-
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-	-	-	-
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-	-	-	-
AK16	BK3_IO0	-	63P	BK3_IO0	-	39P	BK3_IO0	-	33P
AJ16	BK3_IO1	-	63N	BK3_IO1	-	39N	BK3_IO1	-	33N
AH16	BK3_IO2	-	64P	BK3_IO2	-	40P	BK3_IO2	-	34P
AG16	BK3_IO3	-	64N	BK3_IO3	-	40N	BK3_IO3	-	34N
AK17	BK3_IO4	-	65P	BK3_IO4	-	41P	BK3_IO4	-	35P
AJ17	BK3_IO5	-	65N	BK3_IO5	-	41N	BK3_IO5	-	35N
AH17	BK3_IO6	-	66P	BK3_IO6	-	42P	BK3_IO6	-	36P
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-	-	-	-
AJ18	BK3_IO7	-	66N	BK3_IO7	-	42N	BK3_IO7	-	36N
AH18	BK3_IO8	-	67P	BK3_IO8	-	43P	BK3_IO8	-	37P
-	-	-	-	-	-	-	GND (Bank 3)	-	-
AG18	BK3_IO9	-	67N	BK3_IO9	-	43N	BK3_IO9	-	37N
AK18	BK3_IO10	-	68P	BK3_IO10	-	44P	BK3_IO10	-	38P
AK19	BK3_IO11	-	68N	BK3_IO11	-	44N	BK3_IO11	-	38N
AJ19	BK3_IO12	-	69P	BK3_IO12	-	45P	NC	-	-
AH19	BK3_IO13	-	69N	BK3_IO13		45N	NC	-	-
AK20	BK3_IO14	-	70P	BK3_IO14	-	46P	NC	-	-
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-	-	-	-
AJ20	BK3_IO15	-	70N	BK3_IO15	-	46N	NC	-	-
AH20	BK3_IO16	-	71P	NC	-	-	NC	-	-
AG20	BK3_IO17	-	71N	NC	-	-	NC	-	-
AK21	BK3_IO18	-	72P	NC	-	-	NC	-	-
AJ21	BK3_IO19	-	72N	NC	-	-	NC	-	-
AH21	BK3_IO20	VREF3	73P	BK3_IO16	VREF3	47P	BK3_IO12	VREF3	39P
AG21	BK3_IO21	-	73N	BK3_IO17	-	47N	BK3_IO13	-	39N
AJ22	BK3_IO22	-	74P	BK3_IO18	-	48P	BK3_IO14	-	40P
-	GND (Bank 3)	-	-	-	-	-	-	-	-
AH22	BK3_IO23	-	74N	BK3_IO19	-	48N	BK3_IO15	-	40N
AK23	BK3_IO24	-	75P	NC	-	-	NC	-	-
AJ23	BK3_IO25	-	75N	NC	-	-	NC	-	-
AH23	BK3_IO26	-	76P	NC	-	-	NC	-	-
AK24	BK3_IO27	-	76N	NC	-	-	NC	-	-
AJ24	BK3_IO28	-	77P	NC	-	-	NC	-	-
AG23	BK3_IO29	-	77N	NC	-	-	NC	-	-
AH24	BK3_IO30	-	78P	NC	-	-	NC	-	-
-	GND (Bank 3)	-	-		-	-	-	-	-
AK25	BK3_IO31	-	78N	NC	-	-	NC	-	-

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
C24	BK1_IO7	SS_CLKIN0N	34N
A22	BK1_IO8	-	35P
D22	BK1_IO9	-	35N
A23	BK1_IO10	-	36P
-	GND (Bank 1)	-	-
B25	BK1_IO11	-	36N
D23	BK1_IO12	PLL_RST2	37P
A24	BK1_IO13	PLL_RST3	37N
A25	BK1_IO14	-	38P
E24	BK1_IO15	-	38N
D24	BK1_IO16	-	39P
A26	BK1_IO17	-	39N
D25	BK1_IO18	-	40P
-	GND (Bank 1)	-	-
C25	BK1_IO19	-	40N
B26	BK1_IO20	-	41P/HSI3
B27	BK1_IO21	-	41N/HSI3
D26	BK1_IO22	-	42P/HSI3
A27	BK1_IO23	-	42N/HSI3
A28	BK1_IO24	-	43P/HSI3
E26	BK1_IO25	-	43N/HSI3
C27	BK1_IO26	HSI3A_SOUTP	44P/HSI3
-	GND (Bank 1)	-	-
D27	BK1_IO27	HSI3A_SOUTN	44N/HSI3
B28	BK1_IO28	-	45P/HSI3
A30	BK1_IO29	-	45N/HSI3
C28	BK1_IO30	HSI3A_SINP	46P/HSI3
D28	BK1_IO31	HSI3A_SINN	46N/HSI3
A31	BK1_IO32	-	47P/HSI3
B30	BK1_IO33	-	47N/HSI3
E28	BK1_IO34	HSI3B_SOUTP	48P/HSI3
-	GND (Bank 1)	-	-
D29	BK1_IO35	HSI3B_SOUTN	48N/HSI3
C29	BK1_IO36	-	49P/HSI4
B31	BK1_IO37	-	49N/HSI4
D30	BK1_IO38	HSI3B_SINP	50P/HSI4
E30	BK1_IO39	HSI3B_SINN	50N/HSI4
A32	BK1_IO40	-	51P/HSI4
C31	BK1_IO41	-	51N/HSI4
D31	BK1_IO42	HSI4A_SOUTP	52P/HSI4
-	GND (Bank 1)	-	-
C32	BK1_IO43	HSI4A_SOUTN	52N/HSI4
B32	BK1_IO44	-	53P/HSI4

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
V39	BK2_IO57	-	90N
W37	BK2_IO58	-	91P
-	GND (Bank 2)	-	-
W38	BK2_IO59	-	91N
W39	BK2_IO60	-	92P
AA39	BK2_IO61	-	92N
-	GND (Bank 2)	-	-
-	GND (Bank 3)	-	-
AA38	BK3_IO0	-	93P
Y35	BK3_IO1	-	93N
AA37	BK3_IO2	-	94P
-	GND (Bank 3)	-	-
AA35	BK3_IO3	-	94N
AB39	BK3_IO4	-	95P
AB38	BK3_IO5	-	95N
AA36	BK3_IO6	-	96P
AB37	BK3_IO7	-	96N
AC39	BK3_IO8	-	97P
AC38	BK3_IO9	-	97N
AB36	BK3_IO10	-	98P
-	GND (Bank 3)	-	-
AC37	BK3_IO11	-	98N
AC36	BK3_IO12	-	99P
AD39	BK3_IO13	-	99N
AD37	BK3_IO14	-	100P
AD36	BK3_IO15	-	100N
AD35	BK3_IO16	-	101P
AE38	BK3_IO17	-	101N
AD38	BK3_IO18	-	102P
-	GND (Bank 3)	-	-
AE39	BK3_IO19	-	102N
AF38	BK3_IO20	-	103P
AF37	BK3_IO21	-	103N
AF39	BK3_IO22	-	104P
AE36	BK3_IO23	-	104N
AF36	BK3_IO24	-	105P
AG38	BK3_IO25	-	105N
AG39	BK3_IO26	-	106P
-	GND (Bank 3)	-	-
AG37	BK3_IO27	-	106N
AH37	BK3_IO28	-	107P
AH38	BK3_IO29	-	107N
AG36	BK3_IO30	-	108P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AC27	BK4_IO21	-	134N/HSI5	NC	-	-
AD29	BK4_IO22	HSI6A_SINP	135P/HSI5	NC	-	-
AD30	BK4_IO23	HSI6A_SINN	135N/HSI5	NC	-	-
AB24	BK4_IO24	-	136P/HSI5	NC	-	-
AB25	BK4_IO25	-	136N/HSI5	NC	-	-
AC29	BK4_IO26	HSI6A_SOUTP	137P/HSI6	NC	-	-
-	GND (Bank 4)	-	-	-	-	-
AC30	BK4_IO27	HSI6A_SOUTN	137N/HSI6	NC	-	-
AB27	BK4_IO28	-	138P/HSI6	NC	-	-
AB26	BK4_IO29	-	138N/HSI6	NC	-	-
AB30	BK4_IO30	HSI6B_SINP	139P/HSI6	BK4_IO18	HSI3B_SINP	93P
-	-	-	-	GND (Bank 4)	-	-
AB29	BK4_IO31	HSI6B_SINN	139N/HSI6	BK4_IO19	HSI3B_SINN	93N
AA26	BK4_IO32	-	140P/HSI6	NC	-	-
AA27	BK4_IO33	-	140N/HSI6	NC	-	-
AA30	BK4_IO34	HSI6B_SOUTP	141P/HSI6	BK4_IO22	HSI3B_SOUTP	95P
-	GND (Bank 4)	-	-	-	-	-
AA29	BK4_IO35	HSI6B_SOUTN	141N/HSI6	BK4_IO23	HSI3B_SOUTN	95N
Y25	BK4_IO36	-	142P/HSI6	NC	-	-
Y26	BK4_IO37	-	142N/HSI6	NC	-	-
Y28	BK4_IO38	-	143P/HSI6	NC	-	-
Y27	BK4_IO39	-	143N/HSI6	NC	-	-
W25	BK4_IO40	-	144P/HSI6	NC	-	-
W26	BK4_IO41	-	144N/HSI6	NC	-	-
W27	BK4_IO42	-	145P	BK4_IO24	-	96P
-	GND (Bank 4)	-	-	-	-	-
W28	BK4_IO43	-	145N	BK4_IO25	-	96N
V24	BK4_IO44	-	146P	BK4_IO26	-	97P
-	-	-	-	GND (Bank 4)	-	-
V25	BK4_IO45	-	146N	BK4_IO27	-	97N
Y29	BK4_IO46	-	147P	BK4_IO32	-	100P
Y30	BK4_IO47	-	147N	BK4_IO33	-	100N
V27	BK4_IO48	PLL_RST4	148P	BK4_IO20	PLL_RST4	94P
V28	BK4_IO49	PLL_RST5	148N	BK4_IO21	PLL_RST5	94N
W29	BK4_IO50	-	149P	BK4_IO34	-	101P
-	GND (Bank 4)	-	-	GND (Bank 4)	-	-
W30	BK4_IO51	-	149N	BK4_IO35	-	101N
U25	BK4_IO52	-	150P	BK4_IO28	-	98P
U26	BK4_IO53	-	150N	BK4_IO29	-	98N
V29	BK4_IO54	SS_CLKIN1P	151P	BK4_IO30	SS_CLKIN1P	99P
V30	BK4_IO55	SS_CLKIN1N	151N	BK4_IO31	SS_CLKIN1N	99N
U28	BK4_IO56	PLL_FBK4	152P	BK4_IO36	PLL_FBK4	102P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
G25	BK5_IO57	-	183N	NC	-	-
F26	BK5_IO58	-	184P	NC	-	-
-	GND (Bank 5)	-	-	-	-	-
E28	BK5_IO59	-	184N	NC	-	-
E27	BK5_IO60	-	185P	BK5_IO40	-	125P
D28	BK5_IO61	-	185N	BK5_IO41	-	125N
C27	CFG0	-	-	CFG0	-	-
B28	DONE	-	-	DONE	-	-
A28	PROGRAMb	-	-	PROGRAMb	-	-
D26	BK6_IO0	INITb	186P	BK6_IO0	INITb	126P
C26	BK6_IO1	CCLK	186N	BK6_IO1	CCLK	126N
B27	BK6_IO2	-	187P	BK6_IO2	-	127P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
A27	BK6_IO3	-	187N	BK6_IO3	-	127N
D25	BK6_IO4	CSb	188P	BK6_IO4	CSb	128P
C25	BK6_IO5	Read	188N	BK6_IO5	READ	128N
B26	BK6_IO6	-	189P	BK6_IO6	-	129P
A26	BK6_IO7	-	189N	BK6_IO7	-	129N
F24	BK6_IO8	-	190P	BK6_IO8	-	130P
E24	BK6_IO9	-	190N	BK6_IO9	-	130N
A25	BK6_IO10	-	191P	BK6_IO10	-	131P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
B25	BK6_IO11	-	191N	BK6_IO11	-	131N
D24	BK6_IO12	VREF6	192P	BK6_IO21	VREF6	136N
C24	BK6_IO13	-	192N	BK6_IO20	-	136P
A24	BK6_IO14	-	193P	BK6_IO12	-	132P
B24	BK6_IO15	-	193N	BK6_IO13	-	132N
F23	BK6_IO16	-	194P	BK6_IO14	-	133P
E23	BK6_IO17	-	194N	BK6_IO15	-	133N
A23	BK6_IO18	-	195P	BK6_IO16	-	134P
-	GND (Bank 6)	-	-	-	-	-
B23	BK6_IO19	-	195N	BK6_IO17	-	134N
C23	BK6_IO20	-	196P	NC	-	-
D23	BK6_IO21	-	196N	NC	-	-
E22	BK6_IO22	-	197P	NC	-	-
D22	BK6_IO23	-	197N	NC	-	-
G21	BK6_IO24	-	198P	NC	-	-
F21	BK6_IO25	-	198N	NC	-	-
B22	BK6_IO26	-	199P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-
A22	BK6_IO27	-	199N	NC	-	-
E21	BK6_IO28	-	200P	NC	-	-

Part Number Description

LFX XXXX X X – XX XXXXX X

Device Family
LFX

Gates
125 = 139K Gates
200 = 210K Gates
500 = 476K Gates
1200 = 1.25M Gates[1]

sysHSI Support
Blank = Supports sysHSI
E = No sysHSI Support

Power Supply Voltage
B = 2.5/3.3V
C = 1.8V

Grade
C = Commercial
I = Industrial

Package
F256 = 256-Ball fpBGA
FH516 = 516-Ball fpBGA (with Heat Spreader)
F516 = 516-Ball fpBGA (without Heat Spreader)
FE680 = 680-Ball fpSBGA
F900 = 900-Ball fpBGA
FN256 = Lead-Free 256-Ball fpBGA
FN900 = Lead-Free 900-Ball fpBGA[2]

Speed
5 = Fastest
4
3 = Slowest

1. Discontinued via PCN #03A-10.
2. Select products only. See Ordering Information tables below for specific support.

Ordering Information

Conventional Packaging

Commercial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125B-05F256C	139K	2.5/3.3	-5	fpBGA	256
LFX125B-04F256C	139K	2.5/3.3	-4	fpBGA	256
LFX125B-03F256C	139K	2.5/3.3	-3	fpBGA	256
LFX125C-04F256C	139K	1.8	-4	fpBGA	256
LFX125C-03F256C	139K	1.8	-3	fpBGA	256
LFX125B-05F516C	139K	2.5/3.3	-5	fpBGA	516
LFX125B-04F516C	139K	2.5/3.3	-4	fpBGA	516
LFX125B-03F516C	139K	2.5/3.3	-3	fpBGA	516
LFX125C-04F516C	139K	1.8	-4	fpBGA	516
LFX125C-03F516C	139K	1.8	-3	fpBGA	516
LFX125B-05FH516C[1]	139K	2.5/3.3	-5	fpBGA	516
LFX125B-04FH516C[1]	139K	2.5/3.3	-4	fpBGA	516
LFX125B-03FH516C[1]	139K	2.5/3.3	-3	fpBGA	516
LFX125C-04FH516C[1]	139K	1.8	-4	fpBGA	516
LFX125C-03FH516C[1]	139K	1.8	-3	fpBGA	516
LFX200B-05F256C	210K	2.5/3.3	-5	fpBGA	256
LFX200B-04F256C	210K	2.5/3.3	-4	fpBGA	256
LFX200B-03F256C	210K	2.5/3.3	-3	fpBGA	256
LFX200C-04F256C	210K	1.8	-4	fpBGA	256
LFX200C-03F256C	210K	1.8	-3	fpBGA	256

“E-Series” Commercial (Cont.)

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX500EC-04FN900C	476K	1.8	-4	Lead-Free fpBGA	900
LFX500EC-03FN900C	476K	1.8	-3	Lead-Free fpBGA	900

“E-Series” Industrial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125EB-04FN256I	139K	2.5/3.3	-4	Lead-Free fpBGA	256
LFX125EB-03FN256I	139K	2.5/3.3	-3	Lead-Free fpBGA	256
LFX125EC-03FN256I	139K	1.8	-3	Lead-Free fpBGA	256
LFX200EB-04FN256I	210K	2.5/3.3	-4	Lead-Free fpBGA	256
LFX200EB-03FN256I	210K	2.5/3.3	-3	Lead-Free fpBGA	256
LFX200EC-03FN256I	210K	1.8	-3	Lead-Free fpBGA	256
LFX500EB-04FN900I	476K	2.5/3.3	-4	Lead-Free fpBGA	900
LFX500EB-03FN900I	476K	2.5/3.3	-3	Lead-Free fpBGA	900
LFX500EC-03FN900I	476K	1.8	-3	Lead-Free fpBGA	900

For Further Information

In addition to this data sheet, the following Lattice technical notes may be helpful when designing with the ispXPGA Family:

- TN1028, ispXPGA Memory Usage Guidelines
- TN1003, sysCLOCK PLL Usage and Design Guidelines
- TN1000, sysIO Usage Guidelines for Lattice Devices
- TN1026, ispXP Configuration Usage Guidelines
- TN1020, sysHSI Usage Guidelines
- TN1043, Power Estimation in ispXPGA Devices

Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
September 2003	07	Improved typical Icc data for LFX125B/C and LFX500B/C.
		Improved external switching characteristics timing numbers for LFX125B/C.
		Improved PIC timing numbers for LFX125B/C.
		Improved $t_{IOINDLY}$ timing numbers for LFX125B/C.
		Improved external switching characteristics timing numbers for LFX500B/C.
		Improved PIC timing numbers for LFX500B/C.
		Improved $t_{IOINDLY}$ timing numbers for LFX500B/C.
		Enhanced CDR functionality description.
		Logic Signal Connections and Signal Descriptions - removed CDRLOCK, LOSS and EXLOSS descriptions.
January 2004	07.1	Added lead-free package designators.
June 2004	08.0	Updated CDR specifications and reference notes. Removed Source Synchronous (SS:No CAL) mode references for the sysHSI blocks.
		Revised Figures 16 and 24 for clarification.
		Clarification of VCC sysHSI Block for 1.8V devices.
		Updated IIL and IIH max specification.
		Updated LVTTL and PCI 3.3 to support 5V tolerance.