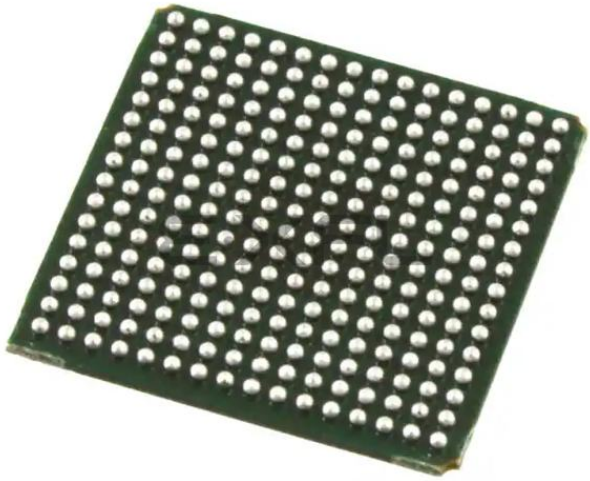


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1936
Total RAM Bits	94208
Number of I/O	160
Number of Gates	139000
Voltage - Supply	2.3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx125eb-03f256i

ispXPGA® Family

Includes High-Performance, Low-Cost "E-Series"

February 2010

Data Sheet DS1026

- **Non-volatile, Infinitely Reconfigurable**
  - Instant-on - Powers up in microseconds via on-chip E²CMOS® based memory
  - No external configuration memory
  - Excellent design security, no bit stream to intercept
  - Reconfigure SRAM based logic in milliseconds
- **High Logic Density for System-level Integration**
  - 139K to 1.25M functional gates
  - 160 to 496 I/O
  - 1.8V, 2.5V, and 3.3V V_{CC} operation
  - Up to 414Kb sysMEM™ embedded memory
- **High Performance Programmable Function Unit (PFU)**
  - Four LUT-4 per PFU supports wide and narrow functions
  - Dual flip-flops per LUT-4 for extensive pipelining
  - Dedicated logic for adders, multipliers, multiplexers, and counters
- **Flexible Memory Resources**
  - Multiple sysMEM Embedded RAM Blocks
    - Single port, Dual port, and FIFO operation
  - 64-bit distributed memory in each PFU
    - Single port, Double port, FIFO, and Shift Register operation
- **Flexible Programming, Reconfiguration, and Testing**
  - Supports IEEE 1532 and 1149.1
  - Microprocessor configuration interface
  - Program E²CMOS while operating from SRAM
- **Eight sysCLOCK™ Phase Locked Loops (PLLs) for Clock Management**
  - True PLL technology
  - 10MHz to 320MHz operation
  - Clock multiplication and division
  - Phase adjustment
  - Shift clocks in 250ps steps
- **sysIO™ for High System Performance**
  - High speed memory support through SSTL and HSTL
  - Advanced buses supported through PCI, GTL+, LVDS, BLVDS, and LVPECL
  - Standard logic supported through LVTTL, LVCMOS 3.3, 2.5 and 1.8
  - 5V tolerant I/O for LVCMOS 3.3 and LVTTL interfaces
  - Programmable drive strength for series termination
  - Programmable bus maintenance
- **Two Options Available**
  - High-performance sysHSI (standard part number)
  - Low-cost, no sysHSI ("E-Series")
- **sysHSI™ Capability for Ultra Fast Serial Communications**
  - Up to 800Mbps performance
  - Up to 20 channels per device
  - Built in Clock Data Recovery (CDR) and Serialization and De-serialization (SERDES)

Table 1. ispXPGA Family Selection Guide

	ispXPGA 125/E	ispXPGA 200/E	ispXPGA 500/E	ispXPGA 1200/E[3]
Functional Gates	139K	210K	476K	1.25M
PFUs	484	676	1764	3844
LUT-4s	1936	2704	7056	15376
Logic FFs	3.8K	5.4K	14.1K	30.7K
sysMEM Memory	92K	111K	184K	414K
Distributed Memory	30K	43K	112K	246K
EBR	20	24	40	90
sysHSI Channels[1]	4	8	12	20
User I/O	160/176	160/208	336	496
Packaging	256 fpBGA 516 fpBGA[2]	256 fpBGA 516 fpBGA[2]	516 fpBGA[2] 900 fpBGA	680 fpSBGA 900 fpBGA

1. "E-Series" does not support sysHSI.
2. FH516 package was converted to F516 via PCN #09A-08.
3. Discontinued via PCN #03A-10.

Set/Reset signal controls all the registers for each PFU. This common Set/Reset signal is composed of the logical OR term of the Global Set/Reset signal (GSR) and the selected signal from routing. The polarity of this signal is not controllable inside the PFU. The polarity of the Global Set/Reset signal (GSR) is programmable. Figure 9 shows the Clock Enable and Output Enable selection for each PFU.

Figure 7. Clock Selection per PFU

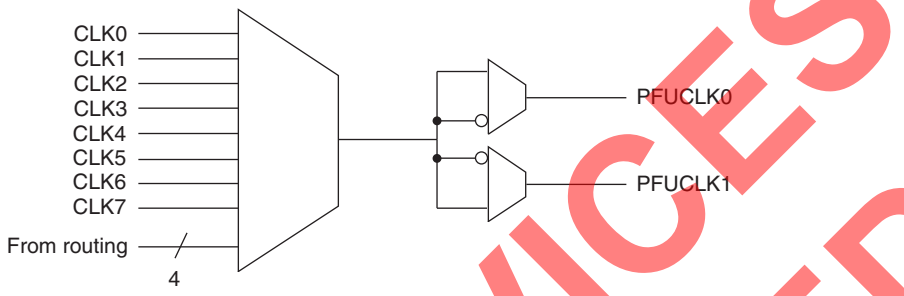


Figure 8. Set/Reset Selection per PFU

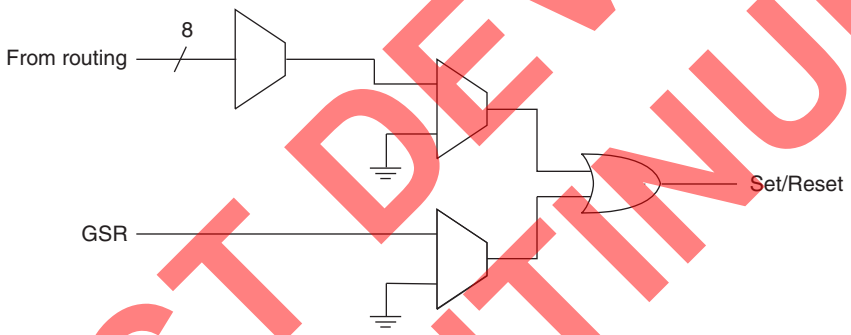
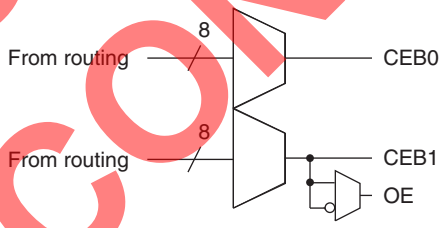


Figure 9. Clock Enable and Output Enable Selection per PFU



Programmable Input/Output Cell

The Programmable Input/Output Cell (PIC) is an essential part of the symmetrical architecture of the ispXPGA Family. The PICs interface the PFUs and EBRs to the sysIO and sysHSI blocks of the device.

Each PIC contains two Programmable Input/Outputs (PIOs) with a total of 21 inputs and 10 outputs. There are 18 inputs from routing, two inputs from the sysIO buffers, and the Global Set/Reset signal. Four outputs of the PIC connect to routing and two outputs are available as Output Enables for the tri-statable Long Lines. The remaining four outputs feed the sysIO buffers directly (one output enable and one output to each). Each PIC associated with a sysHSI block has four additional inputs and six additional outputs to support the sysHSI blocks. The four additional inputs come from the sysHSI block associated with the PIC. The four of the six additional outputs come from the PIC outputs and feed the sysHSI block, while the remaining two outputs feed routing. Figure 10 shows the block diagram of the PIC with the sysHSI block inputs and outputs.

Table 5. ispXPGA Supported I/O Standards

sysIO Standard	V_{CCO}	V_{REF}	V_{TT}
LVTTL	3.3V	N/A	N/A
LVCMOS-3.3	3.3V	N/A	N/A
LVCMOS-2.5	2.5V	N/A	N/A
LVCMOS-1.8	1.8V	N/A	N/A
PCI	3.3V	N/A	N/A
AGP-1X	3.3V	N/A	N/A
SSTL3, Class I, II	3.3V	1.5V	1.5V
SSTL2, Class I, II	2.5V	1.25V	1.25V
HSTL, Class I	1.5V	0.75V	0.75V
HSTL, Class III	1.5V	0.9V	1.5V
GTL+	N/A	1.0V	1.5V
LVPECL	3.3V	N/A	N/A
LVDS[1]	2.5V	N/A	N/A
BLVDS	2.5V	N/A	N/A

1. V_{CCO} must be 2.5V for high speed serial operations (sysHSI block).

Table 6. Differential Interface Standard Support[1]

		sysIO Buffer Not Using sysHSI Block	sysIO Buffer Using sysHSI Block
LVDS	Driver	Supported with external resistor network	Supported
	Receiver	Supported with standard termination	Supported with standard termination
BLVDS	Driver	Supported with external resistor network	Not supported
	Receiver	Supported (may need termination)	Supported (may need termination)
LVPECL	Driver	Supported with external resistor network	Not supported
	Receiver	Supported with termination	Supported with termination

1. For more information, refer to TN1000, sysIO Usage Guidelines for Lattice Devices.

High Speed Serial Interface Block (sysHSI Block)[1]

The High Speed Serial Interface (sysHSI) allows high speed serial data transfer over a pair of LVDS I/O. The ispXPGA devices have multiple sysHSI blocks.

Each sysHSI block has two SERDES blocks which contain two main sub-blocks, Transmitter (with a serializer) and Receiver (with a deserializer) including Clock/Data Recovery Circuit (CDR). Each SERDES can be used as a full duplex channel. The two SERDES in sysHSI blocks share a common clock and must operate at the same nominal frequency. Figure 20 shows the sysHSI block.

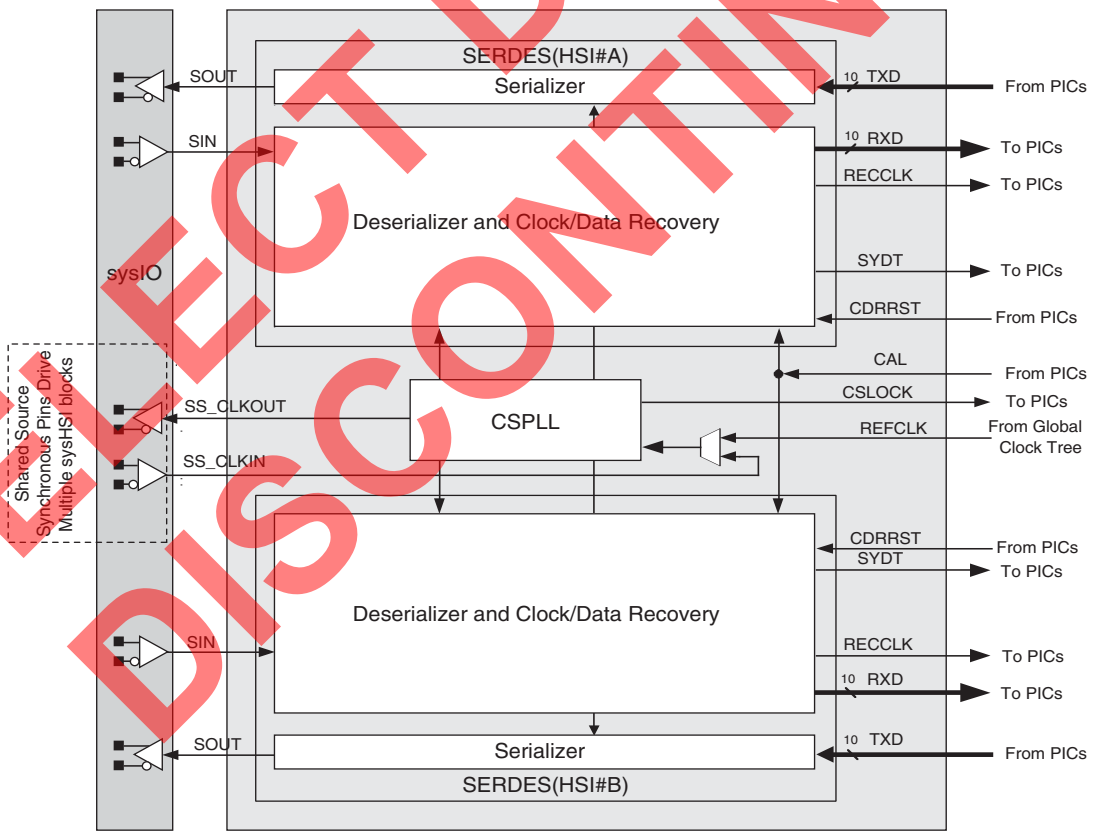
Device features support two data coding modes: 10B/12B and 8B/10B (for use with other encoding schemes, see Lattice's sysHSI technical notes). The encoding and decoding of the 10B/12B standard are performed within the sysHSI block. For the 8B/10B standard, the symbol boundaries are aligned internally but the encoding and decoding are performed outside the sysHSI block.

Each SERDES block receives a single high speed serial data input stream (with embedded clock) from an input, and provide a low speed 10-bit wide data stream and a recovered clock to the device. For transmitting, SERDES converts a 10-bit wide low-speed data stream to a single high-speed data stream with embedded clock for output.

Additionally, multiple sysHSI blocks can be grouped together to form a source synchronous interface of 1-10 channels.

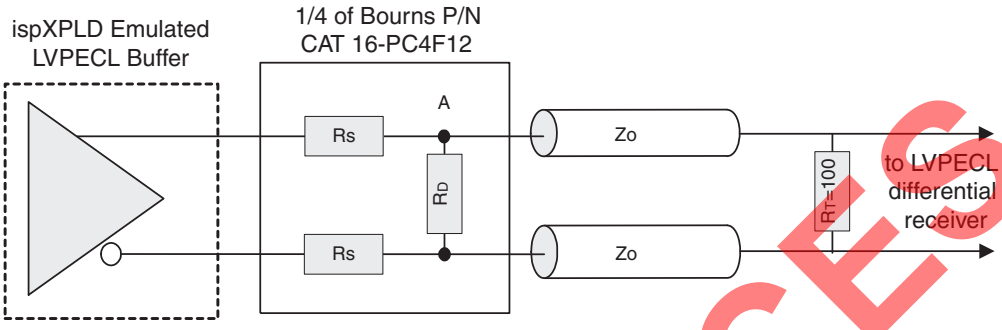
For more information on the SERDES/CDR, refer to TN1020, sysHSI Usage Guidelines.

Figure 20. sysHSI Block Diagram



1. "E-Series" does not support sysHSI.

Figure 23. LVPECL Driver with Three Resistor Pack



ispXPGA 125B/C & ispXPGA 125EB/EC External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Conditions	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{CO}	Global Clock Input to Output	PIO Output Register	—	5.3	—	5.7	—	6.6	ns
t_{S}	Global Clock Input Setup	PIO Input Register without input delay	-1.9	—	-1.8	—	-1.5	—	ns
t_{H}	Global Clock Input Hold	PIO Input Register without input delay	2.7	—	2.9	—	3.3	—	ns
t_{SINDLY}	Global Clock Input Setup	PIO Input Register with input delay	3.1	—	3.3	—	3.8	—	ns
t_{HINDLY}	Global Clock Input Hold	PIO Input Register with input delay	0.0	—	0.0	—	0.0	—	
t_{COPLL}	Global Clock Input to Output	PIO Output Register using PLL without delay	—	3.6	—	3.9	—	4.5	ns
t_{SPLL}	Global Clock Input Setup	PIO Input Register without input delay using PLL without delay	0	—	0.1	—	0.3	—	ns
t_{HPLL}	Global Clock Input Hold	PIO Input Register without input delay using PLL without delay	0.9	—	1.0	—	1.2	—	ns
$t_{SINDLYPLL}$	Global Clock Input Setup	PIO Input Register with input delay using PLL without delay	5.1	—	5.5	—	6.3	—	ns
$t_{HINDLYPLL}$	Global Clock Input Hold	PIO Input Register with input delay using PLL without delay	-3.0	—	-2.8	—	-2.4	—	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 200B/C & ispXPGA 200EB/EC Timing Adders (Cont.)

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LVCMOS_33_4mA_out	Using 3.3V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_33_5.33mA_out	Using 3.3V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_33_8mA_out	Using 3.3V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_33_12mA_out	Using 3.3V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_33_16mA_out	Using 3.3V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_33_24mA_out	Using 3.3V CMOS Standard, 24mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_out	Using AGP 1x Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
CTT25_out	Using CTT 2.5V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
CTT33_out	Using CTT 3.3V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
GTL+_out	Using GTL+	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_out	Using HSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_out	Using HSTL 2.5V, Class III	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVDS_out	Using Low Voltage Differential Signaling (LVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
BLVDS_out	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVPECL_out	Using Low Voltage PECL	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
PCI_out	Using PCI Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL2_I_out	Using SSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL2_II_out	Using SSTL 2.5V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_out	Using SSTL 3.3V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL3_II_out	Using SSTL 3.3V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 500B/C & ispXPGA 500EB/EC External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Conditions	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{CO}	Global Clock Input to Output	PIO Output Register	—	6.4	—	6.9	—	7.9	ns
t_S	Global Clock Input Setup	PIO Input Register without input delay	-2.9	—	-2.7	—	-2.3	—	ns
t_H	Global Clock Input Hold	PIO Input Register without input delay	3.6	—	3.9	—	4.5	—	ns
t_{SINDLY}	Global Clock Input Setup	PIO Input Register with input delay	3.3	—	3.6	—	4.1	—	ns
t_{HINDLY}	Global Clock Input Hold	PIO Input Register with input delay	0.0	—	0.0	—	0.0	—	
t_{COPLL}	Global Clock Input to Output	PIO Output Register using PLL without delay	—	3.2	—	3.4	—	3.9	ns
t_{SPLL}	Global Clock Input Setup	PIO Input Register without input delay using PLL without delay	0.1	—	0.2	—	0.3	—	ns
t_{HPLL}	Global Clock Input Hold	PIO Input Register without input delay using PLL without delay	0.8	—	0.9	—	1.0	—	ns
$t_{SINDLYPLL}$	Global Clock Input Setup	PIO Input Register with input delay using PLL without delay	6.7	—	7.2	—	8.3	—	ns
$t_{HINDLYPLL}$	Global Clock Input Hold	PIO Input Register with input delay using PLL without delay	-4.3	—	-4.0	—	-3.4	—	ns

1. Only available for ispXPGA 500B and ispXPGA 500EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 500B/C & ispXPGA 500EB/EC PFU Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Functional Delays								
LUTs								
t_{LUT4}	4-Input LUT Delay	—	0.41	—	0.44	—	0.51	ns
t_{LUT5}	5-Input LUT Delay	—	0.73	—	0.79	—	0.91	ns
t_{LUT6}	6-Input LUT Delay	—	0.86	—	0.93	—	1.07	ns
Shift Register (LUT)								
t_{LSR_S}	Shift Register Setup Time	-0.64	—	-0.62	—	-0.53	—	ns
t_{LSR_H}	Shift Register Hold Time	0.61	—	0.63	—	0.72	—	ns
t_{LSR_CO}	Shift Register Clock to Output Delay	—	0.70	—	0.75	—	0.86	ns
Arithmetic Functions								
$t_{LCTHRUR}$	MC (Macro Cell) Carry In to MC Carry Out Delay (Ripple)	—	0.08	—	0.09	—	0.10	ns
$t_{LCTHRUL}$[2]	MC Carry In to MC Carry Out Delay (Look Ahead)	—	0.05	—	0.05	—	0.06	ns
t_{LSTHRU}	MC Sum In to MC Sum Out Delay	—	0.42	—	0.45	—	0.52	ns
$t_{LSINCOUT}$	MC Sum In to MC Carry Out Delay	—	0.29	—	0.31	—	0.36	ns
$t_{LCINSOUTR}$	MC Carry In to MC Sum Out Delay (Ripple)	—	0.36	—	0.39	—	0.45	ns
$t_{LCINSOUTL}$	MC Carry In to MC Sum Out Delay (Look Ahead)	—	0.26	—	0.28	—	0.32	ns
Feed-thru								
t_{LFT}	PFU Feed-Thru Delay	—	0.15	—	0.16	—	0.18	ns
Distributed RAM								
t_{LRAM_CO}	Clock to RAM Output	—	1.24	—	1.33	—	1.53	ns
t_{LRAMAD_S}	Address Setup Time	-0.41	—	-0.40	—	-0.34	—	ns
t_{LRAMD_S}	Data Setup Time	0.21	—	0.22	—	0.25	—	ns
t_{LRAMWE_S}	Write Enable Setup Time	0.45	—	0.46	—	0.53	—	ns
t_{LRAMAD_H}	Address Hold Time	0.58	—	0.60	—	0.69	—	ns
t_{LRAMD_H}	Data Hold Time	0.11	—	0.11	—	0.13	—	ns
t_{LRAMWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{LRAMCPW}$	Clock Pulse Width (High or Low)	2.91	—	3.00	—	3.45	—	ns
$t_{LRAMADO}$	Address to Output Delay	—	0.86	—	0.93	—	1.07	ns
Register/Latch Delays								
Registers								
t_{L_CO}	Register Clock to Output Delay	—	0.58	—	0.62	—	0.71	ns
t_{L_S}	Register Setup Time (Data before Clock)	0.14	—	0.14	—	0.16	—	ns
t_{L_H}	Register Hold Time (Data after Clock)	-0.12	—	-0.12	—	-0.10	—	ns
t_{LCE_S}	Register Clock Enable Setup Time	-0.11	—	-0.11	—	-0.09	—	ns
t_{LCE_H}	Register Clock Enable Hold Time	0.11	—	0.11	—	0.13	—	ns
Latches								
t_{L_GO}	Latch Gate to Output Delay	—	0.09	—	0.10	—	0.12	ns
t_{LL_S}	Latch Setup Time	0.14	—	0.14	—	0.16	—	ns
t_{LL_H}	Latch Hold Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{LLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns

ispXPGA 1200B/C & ispXPGA 1200EB/EC PFU Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Set								
t_{LASSRO}	Asynchronous Set/Reset to Output	—	1.09	—	1.17	—	1.35	ns
$t_{LASSRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{LASSRR}	Asynchronous Set/Reset Recovery	—	0.51	—	0.55	—	0.63	ns
t_{LSSR_S}	Synchronous Set/Reset Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{LSSR_H}	Synchronous Set/Reset Hold Time	0.03	—	0.03	—	0.03	—	ns

1. Only available for ispXPGA 1200B and ispXPGA 1200EB (2.5V/3.3V) devices.
2. $t_{LCTHRUL}$ quoted bit by bit.

Timing v.2.1

ispXPGA 1200B/C & ispXPGA 1200EB/EC PIC Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Register/Latch Delays								
t_{IO_CO}	Register Clock to Output Delay	—	1.01	—	1.09	—	1.25	ns
t_{IO_S}	Register Setup Time (Data before Clock)	0.05	—	0.05	—	0.06	—	ns
t_{IO_H}	Register Hold Time (Data after Clock)	0.06	—	0.06	—	0.07	—	ns
t_{IOCE_S}	Register Clock Enable Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{IOCE_H}	Register Clock Enable Hold Time	0.13		0.13	—	0.15	—	ns
t_{IO_GO}	Latch Gate to Output Delay	—	0.85	—	0.91	—	1.05	ns
t_{IOL_S}	Latch Setup Time	0.05	—	0.05	—	0.06	—	ns
t_{IOL_H}	Latch Hold Time	0.06	—	0.06	—	0.07	—	ns
t_{IOLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns
t_{IOASRO}	Asynchronous Set/Reset to Output	—	1.17	—	1.26	—	1.45	ns
$t_{IOASRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{IOASRR}	Asynchronous Set/Reset Recovery Time	—	0.23	—	0.25	—	0.29	ns
Input/Output Delays								
t_{IOBUF}	Output Buffer Delay	—	0.99	—	1.06	—	1.22	ns
t_{IOIN}	Input Buffer Delay	—	0.71	—	0.76	—	0.87	ns
t_{IOEN}	Output Enable Delay	—	0.52	—	0.56	—	0.64	ns
t_{IODIS}	Output Disable Delay	—	-0.11	—	-0.10	—	-0.09	ns
t_{IOFT}	Feed-thru Delay	—	0.19	—	0.20	—	0.23	ns

1. Only available for ispXPGA 1200B and ispXPGA 1200EB (2.5V/3.3V) devices.

Timing v.2.1

ispXP sysCONFIG Port Timing Specifications

Symbol	Timing Parameter	Min.	Typ.	Max.	Units
sysCONFIG Write Cycle Timing					
t_{SUCS}	Input setup time of CS to CCLK rise	10	—	—	ns
t_{HCS}	Hold time of CS to CCLK Rise	0	—	—	ns
t_{SUWD}	Input setup time of write data to CCLK rise	12	—	—	ns
t_{HWD}	Hold time of write data to CCLK rise	0	—	—	ns
t_{PRGM}	Low time to reset device SRAM	5	—	50	ns
t_{WINIT}	INIT pulse width	—	—	5	ms
t_{IODISS}	User I/O disable	—	—	30	ns
t_{IOENSS}	User I/O enable	—	—	30	ns
t_{WH}	Write clock High pulse width	12	—	—	ns
t_{WL}	Write clock Low pulse width	12	—	—	ns
f_{MAXW}	Write f_{MAX}	—	—	33	MHz
sysCONFIG Read Cycle Timing					
t_{HREAD}	Hold time of READ to CCLK rise	0	—	—	ns
t_{SUREAD}	Input setup time of READ High to CCLK rise	30	—	—	ns
t_{RH}	READ clock high pulse width	12	—	—	ns
t_{RL}	READ clock low pulse width	15	—	—	ns
f_{MAXR}	Read f_{MAX}	—	—	33	MHz
t_{CORD}	Clock to out for read data	—	—	25	ns

Boundary Scan Timing

Parameter	Description	Min.	Max.	Units
t_{BTCP}	TCK [BSCAN] Clock Pulse Width	40	—	ns
t_{BTCPH}	TCK [BSCAN] Clock Pulse Width High	20	—	ns
t_{BTCPL}	TCK [BSCAN] Clock Pulse Width Low	20	—	ns
t_{BTS}	TCK [BSCAN] Setup Time	8	—	ns
t_{BTH}	TCK [BSCAN] Hold Time	10	—	ns
t_{BTRF}	TCK [BSCAN] Rise/Fall Time	50	—	mV/ns
t_{BTCO}	TAP Controller Falling Edge of Clock to Valid Output	—	18	ns
$t_{BTCODIS}$	TAP Controller Falling Edge of Clock to Valid Disable	—	18	ns
t_{BTCOEN}	TAP Controller Falling Edge of Clock to Valid Enable	—	18	ns
t_{BTCRS}	BSCAN Test Capture Register Setup Time	8	—	ns
t_{BTCRH}	BSCAN Test Capture Register Hold Time	25	—	ns
t_{BUTCO}	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	45	ns
$t_{BTUODIS}$	BSCAN Test Update Register, Falling Edge of Clock to Valid Disable	—	20	ns
$t_{BTUPOEN}$	BSCAN Test Update Register, Falling Edge of Clock to Valid Enable	—	20	ns

ispXPGA Logic Signal Connections: 256-Ball fpBGA

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
C2	BK0_IO2	HSI0A_SOUTP	1P/HSI0	BK0_IO0	HSI0A_SOUTP	0P
-	GND (Bank 0)	-	-	-	-	-
D2	BK0_IO3	HSI0A_SOUTN	1N/HSI0	BK0_IO1	HSI0A_SOUTN	0N
B1	BK0_IO6	HSI0A_SINP	3P/HSI0	BK0_IO4	HSI0A_SINP	2P/HSI0
-	-	-	-	GND (Bank 0)	-	-
C1	BK0_IO7	HSI0A_SINN	3N/HSI0	BK0_IO5	HSI0A_SINN	2N/HSI0
D3	BK0_IO8	-	4P/HSI0	BK0_IO6	-	3P/HSI0
E3	BK0_IO9	VREF0	4N/HSI0	BK0_IO7	VREF0	3N/HSI0
D1	BK0_IO10	HSI0B_SOUTP	5P/HSI0	BK0_IO8	HSI0B_SOUTP	4P/HSI0
-	GND (Bank 0)	-	-	-	-	-
E1	BK0_IO11	HSI0B_SOUTN	5N/HSI0	BK0_IO9	HSI0B_SOUTN	4N/HSI0
E2	BK0_IO12	-	6P/HSI0	BK0_IO10	-	5P/HSI0
F2	BK0_IO13	-	6N/HSI0	BK0_IO11	-	5N/HSI0
F1	BK0_IO14	HSI0B_SINP	7P/HSI0	BK0_IO12	HSI0B_SINP	6P/HSI0
-	-	-	-	GND (Bank 0)	-	-
G1	BK0_IO15	HSI0B_SINN	7N/HSI0	BK0_IO13	HSI0B_SINN	6N/HSI0
F3	BK0_IO18	PLL_FBK0	9P	BK0_IO14	PLL_FBK0	7P/HSI0
-	GND (Bank 0)	-	-	-	-	-
G2	BK0_IO19	PLL_RST1	9N	BK0_IO15	PLL_RST1	7N/HSI0
E4	BK0_IO20	-	10P	BK0_IO16	-	8P/HSI0
F4	BK0_IO21	PLL_FBK1	10N	BK0_IO17	PLL_FBK1	8N/HSI0
H1	BK0_IO22	PLL_RST0	11P	BK0_IO18	PLL_RST0	9P
-	-	-	-	GND (Bank 0)	-	-
J1	BK0_IO23	-	11N	BK0_IO19	-	9N
H2	BK0_IO24	CLK_OUT0	12P	BK0_IO20	CLK_OUT0	10P
G3	BK0_IO25	CLK_OUT1	12N	BK0_IO21	CLK_OUT1	10N
-	GND (Bank 0)	-	-	-	-	-
G4	GCLK0	-	LVDS Pair0P	GCLK0	-	LVDS Pair0P
H4	GCLK1	-	LVDS Pair0N	GCLK1	-	LVDS Pair0N
H3	VCCP0	-	-	VCCP0	-	-
J4	GNDP0	-	-	GNDP0	-	-
J2	GCLK2	-	LVDS Pair1P	GCLK2	-	LVDS Pair1P
J3	GCLK3	-	LVDS Pair1N	GCLK3	-	LVDS Pair1N
-	GND (Bank 1)	-	-	-	-	-
H5	BK1_IO0	CLK_OUT2	13P	BK1_IO0	CLK_OUT2	11P
J5	BK1_IO1	CLK_OUT3	13N	BK1_IO1	CLK_OUT3	11N
K1	BK1_IO2	SS_CLKOUT0P	14P	BK1_IO2	SS_CLKOUT0P	12P
-	-	-	-	GND (Bank 1)	-	-
L1	BK1_IO3	SS_CLKOUT0N	14N	BK1_IO3	SS_CLKOUT0N	12N
K4	BK1_IO4	PLL_FBK2	15P	BK1_IO4	PLL_FBK2	13P
L4	BK1_IO5	PLL_FBK3	15N	BK1_IO5	PLL_FBK3	13N
K3	BK1_IO6	SS_CLKIN0P	16P	BK1_IO6	SS_CLKIN0P	14P

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
R8	BK2_IO19	-	35N	BK2_IO19	-	31N
N8	BK2_IO20	-	36P	BK2_IO20	-	32P
P8	BK2_IO21	-	36N	BK2_IO21	-	32N
-	GND (Bank 2)	-	-	-	-	-
-	GND (Bank 3)	-	-	-	-	-
T8	BK3_IO0	-	39P	BK3_IO0	-	33P
T9	BK3_IO1	-	39N	BK3_IO1	-	33N
R9	BK3_IO2	-	40P	BK3_IO2	-	34P
-	-	-	-	GND (Bank 3)	-	-
R10	BK3_IO3	-	40N	BK3_IO3	-	34N
P9	BK3_IO4	-	41P	BK3_IO4	-	35P
N9	BK3_IO5	-	41N	BK3_IO5	-	35N
T10	BK3_IO6	-	42P	BK3_IO6	-	36P
-	GND (Bank 3)	-	-	-	-	-
T11	BK3_IO7	-	42N	BK3_IO7	-	36N
P10	BK3_IO8	-	43P	BK3_IO8	-	37P
-	-	-	-	GND (Bank 3)	-	-
N10	BK3_IO9	-	43N	BK3_IO9	-	37N
R11	BK3_IO14	-	46P	BK3_IO10	-	38P
-	GND (Bank 3)	-	-	-	-	-
R12	BK3_IO15	-	46N	BK3_IO11	-	38N
P11	BK3_IO16	VREF3	47P	BK3_IO12	VREF3	39P
N11	BK3_IO17	-	47N	BK3_IO13	-	39N
T12	BK3_IO18	-	48P	BK3_IO14	-	40P
T13	BK3_IO19	-	48N	BK3_IO15	-	40N
R13	BK3_IO20	-	49P	BK3_IO16	-	41P
-	-	-	-	GND (Bank 3)	-	-
R14	BK3_IO21	-	49N	BK3_IO17	-	41N
P12	BK3_IO22	-	50P	BK3_IO18	-	42P
-	GND (Bank 3)	-	-	-	-	-
N12	BK3_IO23	-	50N	BK3_IO19	-	42N
T14	GSR	-	-	GSR	-	-
T15	DXP	-	-	DXP	-	-
P13	DXN	-	-	DXN	-	-
P15	BK4_IO0	-	52P/HSI2	BK4_IO0	-	44P
N14	BK4_IO1	-	52N/HSI2	BK4_IO1	-	44N
R16	BK4_IO2	HSI2A_SINP	53P/HSI2	BK4_IO2	-	45P
-	GND (Bank 4)	-	-	-	-	-
P16	BK4_IO3	HSI2A_SINN	53N/HSI2	BK4_IO3	-	45N
N15	BK4_IO4	-	54P/HSI2	BK4_IO4	-	46P
-	-	-	-	GND (Bank 4)	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
-	-	-	-	GND (Bank 0)	-	-	-	-	-
R2	GCLK0	-	LVDS Pair0P	GCLK0	-	LVDS Pair0P	GCLK0	-	LVDS Pair0P
R3	GCLK1	-	LVDS Pair0N	GCLK1	-	LVDS Pair0N	GCLK1	-	LVDS Pair0N
R4	VCCP0	-	-	VCCP0	-	-	VCCP0	-	-
T4	GNDP0	-	-	GNDP0	-	-	GNDP0	-	-
T3	GCLK2	-	LVDS Pair1P	GCLK2	-	LVDS Pair1P	GCLK2	-	LVDS Pair1P
T2	GCLK3	-	LVDS Pair1N	GCLK3	-	LVDS Pair1N	GCLK3	-	LVDS Pair1N
-	-	-	-	GND (Bank 1)	-	-	-	-	-
T1	BK1_IO0	CLK_OUT2	21P	BK1_IO0	CLK_OUT2	13P	BK1_IO0	CLK_OUT2	11P
-	GND (Bank 1)	-	-	-	-	-	-	-	-
U1	BK1_IO1	CLK_OUT3	21N	BK1_IO1	CLK_OUT3	13N	BK1_IO1	CLK_OUT3	11N
U2	BK1_IO2	SS_CLKOUT0P	22P	BK1_IO2	SS_CLKOUT0P	14P	BK1_IO2	SS_CLKOUT0P	12P
-	-	-	-	-	-	-	GND (Bank 1)	-	-
U3	BK1_IO3	SS_CLKOUT0N	22N	BK1_IO3	SS_CLKOUT0N	14N	BK1_IO3	SS_CLKOUT0N	12N
V1	BK1_IO4	PLL_FBK2	23P	BK1_IO4	PLL_FBK2	15P	BK1_IO4	PLL_FBK2	13P
V2	BK1_IO5	PLL_FBK3	23N	BK1_IO5	PLL_FBK3	15N	BK1_IO5	PLL_FBK3	13N
V3	BK1_IO6	-	24P	NC	-	-	NC	-	-
-	GND (Bank 1)	-	-	-	-	-	-	-	-
V4	BK1_IO7	-	24N	NC	-	-	NC	-	-
W1	BK1_IO8	-	25P	NC	-	-	NC	-	-
Y1	BK1_IO9	-	25N	NC	-	-	NC	-	-
W2	BK1_IO10	SS_CLKINOP	26P	BK1_IO6	SS_CLKIN0P	16P	BK1_IO6	SS_CLKIN0P	14P
-	-	-	-	GND (Bank 1)	-	-	-	-	-
W3	BK1_IO11	SS_CLKINON	26N	BK1_IO7	SS_CLKIN0N	16N	BK1_IO7	SS_CLKIN0N	14N
Y2	BK1_IO12		27P	BK1_IO8		17P	BK1_IO8	-	15P
-	-	-	-	-	-	-	GND (Bank 1)	-	-
Y4	BK1_IO13	-	27N	BK1_IO9	-	17N	BK1_IO9	-	15N
Y3	BK1_IO14	-	28P	NC	-	-	NC	-	-
-	GND (Bank 1)	-	-	-	-	-	-	-	-
AA1	BK1_IO15	-	28N	NC	-	-	NC	-	-
AA2	BK1_IO16	-	29P	NC	-	-	NC	-	-
AA3	BK1_IO17	-	29N	NC	-	-	NC	-	-
AB2	BK1_IO18	HSI2A_SOUTP	30P	BK1_IO10	HSI1A_SOUTP	18P/HSI1	BK1_IO10	-	16P
AC2	BK1_IO19	HSI2A_SOUTN	30N	BK1_IO11	HSI1A_SOUTN	18N/HSI1	BK1_IO11	-	16N
AB3	BK1_IO20	PLL_RST2	31P	BK1_IO12	PLL_RST2	19P/HSI1	BK1_IO12	PLL_RST2	17P
AA4	BK1_IO21	PLL_RST3	31N	BK1_IO13	PLL_RST3	19N/HSI1	BK1_IO13	PLL_RST3	17N
AC1	BK1_IO22	HSI2A_SINP	32P	BK1_IO14	HSI1A_SINP	20P/HSI1	NC	-	-
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-	-	-	-
AD1	BK1_IO23	HSI2A_SINN	32N	BK1_IO15	HSI1A_SINN	20N/HSI1	NC	-	-
AE1	BK1_IO24	VREF1	33P/HSI2	BK1_IO16	VREF1	21P/HSI1	BK1_IO14	VREF1	18P
AF1	BK1_IO25		33N/HSI2	BK1_IO17	-	21N/HSI1	BK1_IO15	-	18N
AC3	BK1_IO26	HSI2B_SOUTP	34P/HSI2	BK1_IO18	HSI1B_SOUTP	22P/HSI1	BK1_IO16	-	19P
-	-	-	-	-	-	-	GND (Bank 1)	-	-
AC4	BK1_IO27	HSI2B_SOUTN	34N/HSI2	BK1_IO19	HSI1B_SOUTN	22N/HSI1	BK1_IO17	-	19N
AD2	BK1_IO28	-	35P/HSI2	BK1_IO20	-	23P/HSI1	BK1_IO18	-	20P
AD3	BK1_IO29	-	35N/HSI2	BK1_IO21	-	23N/HSI1	BK1_IO19	-	20N
AE2	BK1_IO30	HSI2B_SINP	36P/HSI2	BK1_IO22	HSI1B_SINP	24P/HSI1	BK1_IO20	-	21P
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-	-	-	-
AF2	BK1_IO31	HSI2B_SINN	36N/HSI2	BK1_IO23	HSI1B_SINN	24N/HSI1	BK1_IO21	-	21N
AD4	BK1_IO32	-	37P/HSI2	NC	-	-	NC	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AJ25	BK3_IO32	-	79P	NC	-	-	NC	-	-
AG24	BK3_IO33	-	79N	NC	-	-	NC	-	-
AK26	BK3_IO34	-	80P	BK3_IO20	-	49P	BK3_IO16	-	41P
-	-	-	-	-	-	-	GND (Bank 3)	-	-
AH25	BK3_IO35	-	80N	BK3_IO21	-	49N	BK3_IO17	-	41N
AJ26	BK3_IO36	-	81P	BK3_IO22	-	50P	BK3_IO18	-	42P
-	-	-	-	GND (Bank 3)	-	-	-	-	-
AH26	BK3_IO37	-	81N	BK3_IO23	-	50N	BK3_IO19	-	42N
AK27	BK3_IO38	-	82P	NC	-	-	NC	-	-
-	GND (Bank 3)	-	-	-	-	-	-	-	-
AJ27	BK3_IO39	-	82N	NC	-	-	NC	-	-
AG26	BK3_IO40	-	83P	BK3_IO24	-	51P	BK3_IO20	-	43P
AH27	BK3_IO41	-	83N	BK3_IO25	-	51N	BK3_IO21	-	43N
AK28	GSR	-	-	GSR	-	-	GSR	-	-
AJ28	DXP	-	-	DXP	-	-	DXP	-	-
AK29	DXN	-	-	DXN	-	-	DXN	-	-
AH29	BK4_IO0	-	84P	BK4_IO0	-	52P/HSI2	BK4_IO0	-	44P
AG28	BK4_IO1	-	84N	BK4_IO1	-	52N/HSI2	BK4_IO1	-	44N
AF27	BK4_IO2	-	85P/HSI3	NC	-	-	NC	-	-
-	GND (Bank 4)	-	-	-	-	-	-	-	-
AF28	BK4_IO3	-	85N/HSI3	NC	-	-	NC	-	-
AJ30	BK4_IO4	-	86P/HSI3	NC	-	-	NC	-	-
AH30	BK4_IO5	-	86N/HSI3	NC	-	-	NC	-	-
AG29	BK4_IO6	-	87P/HSI3	NC	-	-	NC	-	-
AF29	BK4_IO7	-	87N/HSI3	NC	-	-	NC	-	-
AE28	BK4_IO8	-	88P/HSI3	NC	-	-	NC	-	-
AD27	BK4_IO9	-	88N/HSI3	NC	-	-	NC	-	-
AG30	BK4_IO10	HSI3A_SINP	89P/HSI3	BK4_IO2	HSI2A_SINP	53P/HSI2	BK4_IO2	-	45P
-	GND (Bank 4)	-	-	GND (Bank 4)	-	-	-	-	-
AF30	BK4_IO11	HSI3A_SINN	89N/HSI3	BK4_IO3	HSI2A_SINN	53N/HSI2	BK4_IO3	-	45N
AD28	BK4_IO12	-	90P/HSI3	BK4_IO4	-	54P/HSI2	BK4_IO4	-	46P
-	-	-	-	-	-	-	GND (Bank 4)	-	-
AC27	BK4_IO13	-	90N/HSI3	BK4_IO5	-	54N/HSI2	BK4_IO5	-	46N
AE29	BK4_IO14	HSI3A_SOUTP	91P/HSI3	BK4_IO6	HSI2A_SOUTP	55P/HSI2	NC	-	-
AE30	BK4_IO15	HSI3A_SOUTN	91N/HSI3	BK4_IO7	HSI2A_SOUTN	55N/HSI2	NC	-	-
AD29	BK4_IO16	-	92P/HSI3	BK4_IO8	-	56P/HSI2	BK4_IO6	-	47P
AD30	BK4_IO17	VREF4	92N/HSI3	BK4_IO9	VREF4	56N/HSI2	BK4_IO7	VREF4	47N
AC28	BK4_IO18	HSI3B_SINP	93P	BK4_IO10	HSI2B_SINP	57P/HSI2	NC	-	-
-	GND (Bank 4)	-	-	GND (Bank 4)	-	-	-	-	-
AB28	BK4_IO19	HSI3B_SINN	93N	BK4_IO11	HSI2B_SINN	57N/HSI2	NC	-	-
AA27	BK4_IO20	PLL_RST4	94P	BK4_IO12	PLL_RST4	58P/HSI2	BK4_IO8	PLL_RST4	48P
AB29	BK4_IO21	PLL_RST5	94N	BK4_IO13	PLL_RST5	58N/HSI2	BK4_IO9	PLL_RST5	48N
AC29	BK4_IO22	HSI3B_SOUTP	95P	BK4_IO14	HSI2B_SOUTP	59P/HSI2	BK4_IO10	-	49P
AC30	BK4_IO23	HSI3B_SOUTN	95N	BK4_IO15	HSI2B_SOUTN	59N/HSI2	BK4_IO11	-	49N
AA28	BK4_IO24	-	96P	NC	-	-	NC	-	-
Y27	BK4_IO25	-	96N	NC	-	-	NC	-	-
Y28	BK4_IO26	-	97P	NC	-	-	NC	-	-
-	GND (Bank 4)	-	-	-	-	-	-	-	-
AA29	BK4_IO27	-	97N	NC	-	-	NC	-	-
Y29	BK4_IO28	-	98P	BK4_IO16	-	60P	BK4_IO12	-	50P
-	-	-	-	-	-	-	GND (Bank 4)	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AA30	BK4_IO29	-	98N	BK4_IO17	-	60N	BK4_IO13	-	50N
W28	BK4_IO30	SS_CLKIN1P	99P	BK4_IO18	SS_CLKIN1P	61P	BK4_IO14	SS_CLKIN1P	51P
-	-	-	-	GND (Bank 4)	-	-	-	-	-
W29	BK4_IO31	SS_CLKIN1N	99N	BK4_IO19	SS_CLKIN1N	61N	BK4_IO15	SS_CLKIN1N	51N
Y30	BK4_IO32	-	100P	NC	-	-	NC	-	-
W30	BK4_IO33	-	100N	NC	-	-	NC	-	-
V27	BK4_IO34	-	101P	NC	-	-	NC	-	-
-	GND (Bank 4)	-	-	-	-	-	-	-	-
V28	BK4_IO35	-	101N	NC	-	-	NC	-	-
V29	BK4_IO36	PLL_FBK4	102P	BK4_IO20	PLL_FBK4	62P	BK4_IO16	PLL_FBK4	52P
V30	BK4_IO37	PLL_FBK5	102N	BK4_IO21	PLL_FBK5	62N	BK4_IO17	PLL_FBK5	52N
U30	BK4_IO38	SS_CLKOUT1P	103P	BK4_IO22	SS_CLKOUT1P	63P	BK4_IO18	SS_CLKOUT1P	53P
U29	BK4_IO39	SS_CLKOUT1N	103N	BK4_IO23	SS_CLKOUT1N	63N	BK4_IO19	SS_CLKOUT1N	53N
U28	BK4_IO40	CLK_OUT4	104P	BK4_IO24	CLK_OUT4	64P	BK4_IO20	CLK_OUT4	54P
-	GND (Bank 4)	-	-	-	-	-	-	-	-
T27	BK4_IO41	CLK_OUT5	104N	BK4_IO25	CLK_OUT5	64N	BK4_IO21	CLK_OUT5	54N
-	-	-	-	GND (Bank 4)	-	-	-	-	-
T28	GCLK4	-	LVDS Pair2P	GCLK4	-	LVDS Pair2P	GCLK4	-	LVDS Pair2P
T29	GCLK5	-	LVDS Pair2N	GCLK5	-	LVDS Pair2N	GCLK5	-	LVDS Pair2N
T30	VCCP1	-	-	VCCP1	-	-	VCCP1	-	-
R29	GNDP1	-	-	GNDP1	-	-	GNDP1	-	-
R28	GCLK6	-	LVDS Pair3P	GCLK6	-	LVDS Pair3P	GCLK6	-	LVDS Pair3P
R27	GCLK7	-	LVDS Pair3N	GCLK7	-	LVDS Pair3N	GCLK7	-	LVDS Pair3N
-	-	-	-	GND (Bank 5)	-	-	-	-	-
R30	BK5_IO0	CLK_OUT6	105P	BK5_IO0	CLK_OUT6	65P	BK5_IO0	CLK_OUT6	55P
-	GND (Bank 5)	-	-	-	-	-	-	-	-
P30	BK5_IO1	CLK_OUT7	105N	BK5_IO1	CLK_OUT7	65N	BK5_IO1	CLK_OUT7	55N
P29	BK5_IO2	-	106P	BK5_IO2	-	66P	BK5_IO2	-	56P
-	-	-	-	-	-	-	GND (Bank 5)	-	-
P28	BK5_IO3	PLL_RST7	106N	BK5_IO3	PLL_RST7	66N	BK5_IO3	PLL_RST7	56N
N30	BK5_IO4	PLL_FBK6	107P	BK5_IO4	PLL_FBK6	67P	BK5_IO4	PLL_FBK6	57P/HSI1
N29	BK5_IO5	-	107N	BK5_IO5	-	67N	BK5_IO5	-	57N/HSI1
N28	BK5_IO6	PLL-RST6	108P	BK5_IO6	PLL_RST6	68P	BK5_IO6	PLL_RST6	58P//HSI1
-	GND (Bank 5)	-	-	GND (Bank 5)	-	-	-	-	-
N27	BK5_IO7	PLL_FBK7	108N	BK5_IO7	PLL_FBK7	68N	BK5_IO7	PLL_FBK7	58N/HSI1
M30	BK5_IO8	-	109P/HSI4	BK5_IO8	-	69P	NC	-	-
M29	BK5_IO9	-	109N/HSI4	BK5_IO9	-	69N	NC	-	-
L30	BK5_IO10	HSI4A_SINP	110P/HSI4	BK5_IO10	HSI3A_SINP	70P/HSI3	BK5_IO8	HSI1A_SINP	59P/HSI1
-	-	-	-	-	-	-	GND (Bank 5)	-	-
L29	BK5_IO11	HSI4A_SINN	110N/HSI4	BK5_IO11	HSI3A_SINN	70N/HSI3	BK5_IO9	HSI1A_SINN	59N/HSI1
M28	BK5_IO12	-	111P/HSI4	BK5_IO12	-	71P/HSI3	BK5_IO10	-	60P/HSI1
L28	BK5_IO13	-	111N/HSI4	BK5_IO13		71N/HSI3	BK5_IO11	-	60N/HSI1
K30	BK5_IO14	HSI4A_SOUTP	112P/HSI4	BK5_IO14	HSI3A_SOUTP	72P/HSI3	BK5_IO12	HSI1A_SOUTP	61P/HSI1
-	GND (Bank 5)	-	-	GND (Bank 5)	-	-	-	-	-
K29	BK5_IO15	HSI4A_SOUTN	112N/HSI4	BK5_IO15	HSI3A_SOUTN	72N/HSI3	BK5_IO13	HSI1A_SOUTN	61N/HSI1
L27	BK5_IO16	-	113P/HSI4	NC	-	-	NC	-	-
K28	BK5_IO17	-	113N/HSI4	NC	-	-	NC	-	-
H30	BK5_IO18	HSI4B_SINP	114P/HSI4	NC	-	-	NC	-	-
G30	BK5_IO19	HSI4B_SINN	114N/HSI4	NC	-	-	NC	-	-
J28	BK5_IO20	-	115P/HSI4	NC	-	-	NC	-	-
K27	BK5_IO21	-	115N/HSI4	NC	-	-	NC	-	-

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
V39	BK2_IO57	-	90N
W37	BK2_IO58	-	91P
-	GND (Bank 2)	-	-
W38	BK2_IO59	-	91N
W39	BK2_IO60	-	92P
AA39	BK2_IO61	-	92N
-	GND (Bank 2)	-	-
-	GND (Bank 3)	-	-
AA38	BK3_IO0	-	93P
Y35	BK3_IO1	-	93N
AA37	BK3_IO2	-	94P
-	GND (Bank 3)	-	-
AA35	BK3_IO3	-	94N
AB39	BK3_IO4	-	95P
AB38	BK3_IO5	-	95N
AA36	BK3_IO6	-	96P
AB37	BK3_IO7	-	96N
AC39	BK3_IO8	-	97P
AC38	BK3_IO9	-	97N
AB36	BK3_IO10	-	98P
-	GND (Bank 3)	-	-
AC37	BK3_IO11	-	98N
AC36	BK3_IO12	-	99P
AD39	BK3_IO13	-	99N
AD37	BK3_IO14	-	100P
AD36	BK3_IO15	-	100N
AD35	BK3_IO16	-	101P
AE38	BK3_IO17	-	101N
AD38	BK3_IO18	-	102P
-	GND (Bank 3)	-	-
AE39	BK3_IO19	-	102N
AF38	BK3_IO20	-	103P
AF37	BK3_IO21	-	103N
AF39	BK3_IO22	-	104P
AE36	BK3_IO23	-	104N
AF36	BK3_IO24	-	105P
AG38	BK3_IO25	-	105N
AG39	BK3_IO26	-	106P
-	GND (Bank 3)	-	-
AG37	BK3_IO27	-	106N
AH37	BK3_IO28	-	107P
AH38	BK3_IO29	-	107N
AG36	BK3_IO30	-	108P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
-	GND (Bank 4)	-	-
AW26	BK4_IO43	-	145N
AV25	BK4_IO44	-	146P
AT24	BK4_IO45	-	146N
AU24	BK4_IO46	-	147P
AU25	BK4_IO47	-	147N
AW25	BK4_IO48	PLL_RST4	148P
AW24	BK4_IO49	PLL_RST5	148N
AU23	BK4_IO50	-	149P
-	GND (Bank 4)	-	-
AT23	BK4_IO51	-	149N
AV24	BK4_IO52	-	150P
AW23	BK4_IO53	-	150N
AV23	BK4_IO54	SS_CLKIN1P	151P
AU22	BK4_IO55	SS_CLKIN1N	151N
AR21	BK4_IO56	PLL_FBK4	152P
AT22	BK4_IO57	PLL_FBK5	152N
AV22	BK4_IO58	SS_CLKOUT1P	153P
-	GND (Bank 4)	-	-
AV21	BK4_IO59	SS_CLKOUT1N	153N
AT21	BK4_IO60	CLK_OUT4	154P
AU21	BK4_IO61	CLK_OUT5	154N
-	GND (Bank 4)	-	-
AT19	GCLK4	-	LVDS Pair2P
AU19	GCLK5	-	LVDS Pair2N
AW22	VCCP1	-	-
AR20	GNDP1	-	-
AU18	GCLK6	-	LVDS Pair3P
AT18	GCLK7	-	LVDS Pair3N
-	GND (Bank 5)	-	-
AV17	BK5_IO0	CLK_OUT6	155P
AV18	BK5_IO1	CLK_OUT7	155N
AW21	BK5_IO2	PLL_FBK6	156P
-	GND (Bank 5)	-	-
AV19	BK5_IO3	PLL_FBK7	156N
AR19	BK5_IO4	-	157P/HSI7
AW19	BK5_IO5	-	157N/HSI7
AW18	BK5_IO6	PLL_RST6	158P/HSI7
AW17	BK5_IO7	PLL_RST7	158N/HSI7
AT17	BK5_IO8	-	159P/HSI7
AV16	BK5_IO9	-	159N/HSI7
AU17	BK5_IO10	HSI7A_SINP	160P/HSI7
-	GND (Bank 5)	-	-

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
AU6	BK5_IO50	HSI9B_SINP	180P/HSI9
-	GND (Bank 5)	-	-
AV6	BK5_IO51	HSI9B_SINN	180N/HSI9
AR8	BK5_IO52	-	181P
AT7	BK5_IO53	-	181N
AU5	BK5_IO54	HSI9B_SOUTP	182P
AV5	BK5_IO55	HSI9B_SOUTN	182N
AW5	BK5_IO56	-	183P
AW4	BK5_IO57	-	183N
AT6	BK5_IO58	-	184P
-	GND (Bank 5)	-	-
AV4	BK5_IO59	-	184N
AR6	BK5_IO60	-	185P
AU4	BK5_IO61	-	185N
AT1	CFG0	-	-
AT3	DONE	-	-
AT2	PROGRAMb	-	-
AP4	BK6_IO0	INITb	186P
AP5	BK6_IO1	CCLK	186N
AR3	BK6_IO2	-	187P
-	GND (Bank 6)	-	-
AR2	BK6_IO3	-	187N
AP3	BK6_IO4	CSb	188P
AR1	BK6_IO5	Read	188N
AP2	BK6_IO6	-	189P
AP1	BK6_IO7	-	189N
AN4	BK6_IO8	-	190P
AM5	BK6_IO9	-	190N
AN3	BK6_IO10	-	191P
-	GND (Bank 6)	-	-
AN2	BK6_IO11	-	191N
AM4	BK6_IO12	VREF6	192P
AM3	BK6_IO13	-	192N
AN1	BK6_IO14	-	193P
AM2	BK6_IO15	-	193N
AL4	BK6_IO16	-	194P
AK5	BK6_IO17	-	194N
AM1	BK6_IO18	-	195P
-	GND (Bank 6)	-	-
AK4	BK6_IO19	-	195N
AL3	BK6_IO20	-	196P
AL2	BK6_IO21	-	196N
AL1	BK6_IO22	-	197P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
D21	BK6_IO29	-	200N	NC	-	-
A21	BK6_IO30	-	201P	NC	-	-
B21	BK6_IO31	-	201N	NC	-	-
F20	BK6_IO32	DATA7	202P	BK6_IO18	DATA7	135P
-	-	-	-	GND (Bank 6)	-	-
E20	BK6_IO33	DATA6	202N	BK6_IO19	DATA6	135N
D20	BK6_IO34	-	203P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-
C20	BK6_IO35		203N	NC	-	-
F19	BK6_IO36	DATA5	204P	BK6_IO22	DATA5	137P
E19	BK6_IO37	DATA4	204N	BK6_IO23	DATA4	137N
B20	BK6_IO38	-	205P	NC	-	-
A20	BK6_IO39	-	205N	NC	-	-
D19	BK6_IO40	-	206P	NC	-	-
C19	BK6_IO41	-	206N	NC	-	-
A19	BK6_IO42	-	207P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-
B19	BK6_IO43	-	207N	NC	-	-
G18	BK6_IO44	-	208P	BK6_IO24	-	138P
F18	BK6_IO45	-	208N	BK6_IO25	-	138N
A18	BK6_IO46	-	209P	BK6_IO32	-	142P
B18	BK6_IO47	-	209N	BK6_IO33	-	142N
D18	BK6_IO48	-	210P	BK6_IO34	-	143P
-	-	-	-	GND (Bank 6)	-	-
C18	BK6_IO49	-	210N	BK6_IO35	-	143N
F17	BK6_IO50	DATA3	211P	BK6_IO26	DATA3	139P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
E17	BK6_IO51	DATA2	211N	BK6_IO27	DATA2	139N
D17	BK6_IO52	-	212P	BK6_IO28	-	140P
C17	BK6_IO53	-	212N	BK6_IO29	-	140N
B17	BK6_IO54	DATA1	213P	BK6_IO30	DATA1	141P
A17	BK6_IO55	DATA0	213N	BK6_IO31	DATA0	141N
F16	BK6_IO56	-	214P	BK6_IO36	-	144P
E16	BK6_IO57	-	214N	BK6_IO37	-	144N
D16	BK6_IO58	-	215P	BK6_IO38	-	145P
-	GND (Bank 6)	-	-	-	-	-
C16	BK6_IO59	-	215N	BK6_IO39	-	145N
B16	BK6_IO60	-	216P	BK6_IO40	-	146P
A16	BK6_IO61	-	216N	BK6_IO41	-	146N
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-
A15	BK7_IO0	-	217P	BK7_IO0	-	147P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
B15	BK7_IO1	-	217N	BK7_IO1	-	147N
C15	BK7_IO2	-	218P	BK7_IO2	-	148P
-	GND (Bank 7)	-	-		-	-
D15	BK7_IO3	-	218N	BK7_IO3	-	148N
E15	BK7_IO4	-	219P	BK7_IO4	-	149P
F15	BK7_IO5	-	219N	BK7_IO5	-	149N
A14	BK7_IO6	-	220P	BK7_IO6	-	150P
-	-	-	-	GND (Bank 7)	-	-
B14	BK7_IO7	-	220N	BK7_IO7	-	150N
C14	BK7_IO8	-	221P	BK7_IO8	-	151P
D14	BK7_IO9	-	221N	BK7_IO9	-	151N
E14	BK7_IO10	-	222P	BK7_IO10	-	152P
-	GND (Bank 7)	-	-	-	-	-
F14	BK7_IO11	-	222N	BK7_IO11	-	152N
C13	BK7_IO12	-	223P	BK7_IO12	-	153P
D13	BK7_IO13	-	223N	BK7_IO13	-	153N
B13	BK7_IO14	-	224P	BK7_IO14	-	154P
-	-	-	-	GND (Bank 7)	-	-
A13	BK7_IO15	-	224N	BK7_IO15	-	154N
F13	BK7_IO16	-	225P	BK7_IO16	-	155P
G13	BK7_IO17	-	225N	BK7_IO17	-	155N
A12	BK7_IO18	-	226P	BK7_IO18	-	156P
-	GND (Bank 7)	-	-	-	-	-
B12	BK7_IO19	-	226N	BK7_IO19	-	156N
C12	BK7_IO20	-	227P	NC	-	-
D12	BK7_IO21	-	227N	NC	-	-
A11	BK7_IO22	-	228P	NC	-	-
B11	BK7_IO23	-	228N	NC	-	-
E12	BK7_IO24	-	229P	NC	-	-
F12	BK7_IO25	-	229N	NC	-	-
C11	BK7_IO26	-	230P	NC	-	-
-	GND (Bank 7)	-	-	-	-	-
D11	BK7_IO27	-	230N	NC	-	-
E11	BK7_IO28	-	231P	NC	-	-
F11	BK7_IO29	-	231N	NC	-	-
B10	BK7_IO30	-	232P	NC	-	-
A10	BK7_IO31	-	232N	NC	-	-
D10	BK7_IO32	-	233P	NC	-	-
E10	BK7_IO33	-	233N	NC	-	-
A9	BK7_IO34	-	234P	NC	-	-
-	GND (Bank 7)	-	-	-	-	-
B9	BK7_IO35	-	234N	NC	-	-