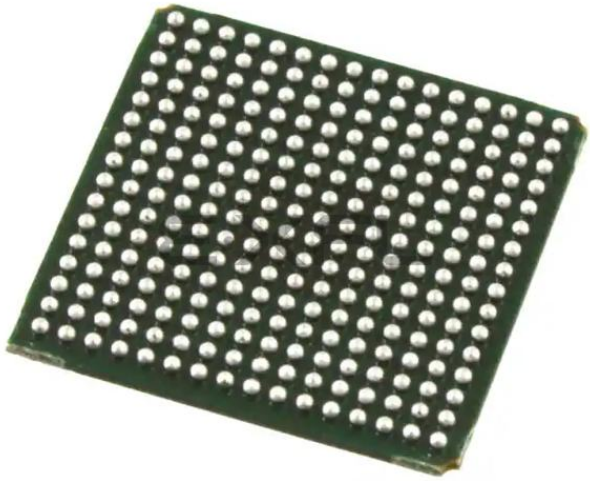
Lattice Semiconductor Corporation - LFX125EB-03FN256I Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1936
Total RAM Bits	94208
Number of I/O	160
Number of Gates	139000
Voltage - Supply	2.3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx125eb-03fn256i

ispXPGA Family Overview

The ispXPGA family of devices provides the ideal vehicle for the creation of high-performance logic designs that are both non-volatile and infinitely re-programmable. Other FPGA solutions force a compromise, being either re-programmable or non-volatile. This family couples this capability with a mainstream architecture containing the features required for today's system-level design.

The ispXPGA family is available in two options. The standard device supports sysHSI capability for ultra fast serial communications while the lower-cost "E-Series" supports the same high-performance FPGA fabric without the sysHSI Block.

Electrically Erasable CMOS (E^2CMOS) memory cells provide the ispXPGA family with non-volatile capability. These allow logic to be functional microseconds after power is applied, allowing easy interfacing in many applications. This capability also means that expensive external configuration memories are not required and that designs can be secured from unauthorized read back. Internal SRAM cells allow the device to be infinitely reconfigured if desired. Both the SRAM and E^2CMOS cells can be programmed and verified through the IEEE 1532 industry standard. Additionally, the SRAM cells can be configured and read-back through the sysCONFIG™ peripheral port.

The family spans the density and I/O range required for the majority of today's logic designs, 139K to 1.25M functional gates and 160 to 496 I/O. The devices are available for operation from 1.8V, 2.5V, and 3.3V power supplies, providing easy integration into the overall system.

System-level design needs are met through the incorporation of sysMEM dual-port memory blocks, sysIO advanced I/O support, and sysCLOCK Phase Locked Loops (PLLs). High-speed serial communications are supported through multiple sysHSI blocks, which provide clock data recovery (CDR) and serialization/de-serialization (SERDES).

The ispLEVER™ design tool from Lattice allows easy implementation of designs using the ispXPGA product. Synthesis library support is available for major logic synthesis tools. The ispLEVER tool takes the output from these common synthesis packages and place and routes the design in the ispXPGA product. The tool supports floor planning and the management of other constraints within the device. The tool also provides outputs to common timing analysis tools for timing analysis.

To increase designer productivity, Lattice provides a variety of pre-designed modules referred to as IP cores for the ispXPGA product. These IP cores allow designers to concentrate on the unique portions of their design while using pre-designed blocks to implement standard functions such as bus interfaces, standard communication interfaces, and memory controllers.

Through the use of advanced technology and innovative architecture the ispXPGA FPGA devices provide designers with excellent speed performance. Although design dependent, many typical designs can run at over 150MHz. Certain designs can run at over 300MHz. Table 2 details the performance of several building blocks commonly used by logic designers.

Table 2. ispXPGA Speed Performance for Typical Building Blocks

Function	Performance
8:1 Asynch MUX	150 MHz
1:32 Asynch Demultiplexer	125 MHz
8 x 8 2-LL Pipelined Multiplier	225 MHz
32-bit Up/Down Counter	290 MHz
32-bit Shift Register	360 MHz

sysCLOCK PLL Description

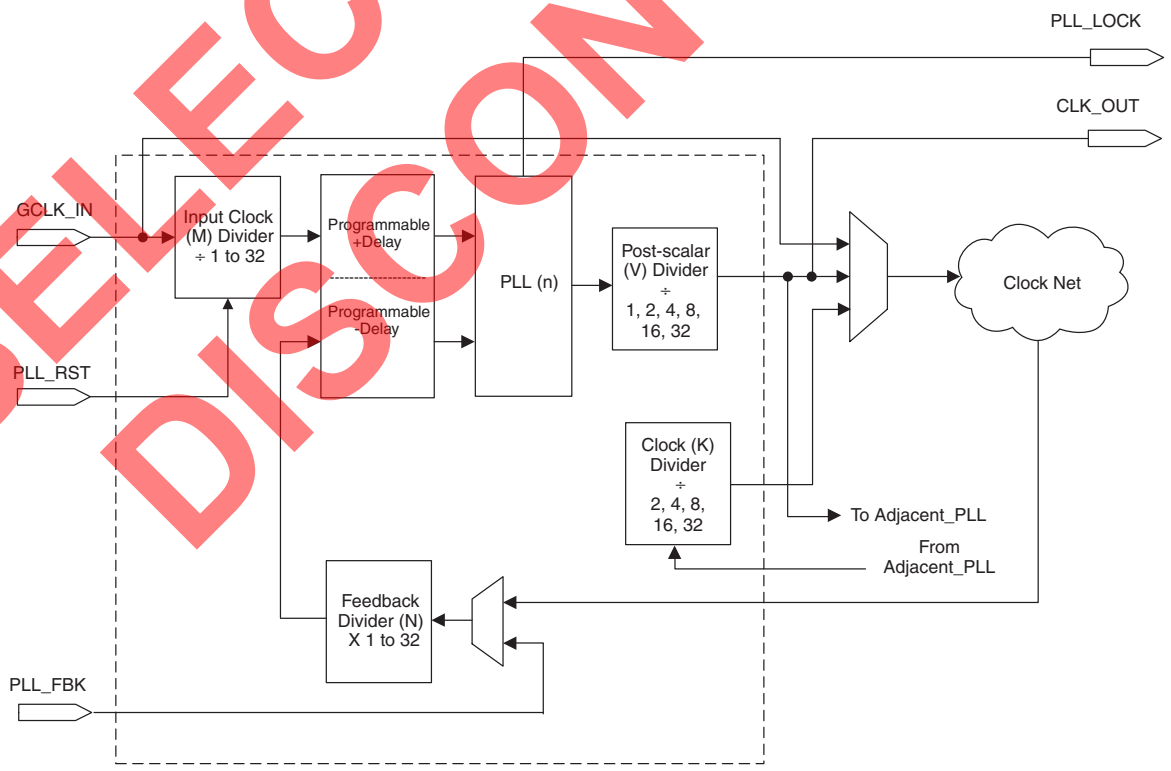
The sysCLOCK PLL circuitry consists of Phase-Lock Loops (PLLs) and the various dividers, reset, and feedback signals associated with the PLLs. This feature gives the user the ability to synthesize clock frequencies and generate multiple clock signals for routing within the device. Furthermore, it can generate clock signals that are aligned either at the board level or the device level.

The ispXPGA devices provide up to eight PLLs. Each PLL receives its input clock from its associated global clock pin, and its output is routed to the associated global clock net. For example, PLL0 receives its clock input from the GCLK0 global clock pin and provides output to the CLK0 global clock net. The PLL also has the ability to output a secondary clock that is a division of the primary clock output. When using the secondary clock, the secondary clock will be routed to the neighboring global clock net. For example, PLL0 will drive its primary clock output on the CLK0 global clock net and its secondary clock output will drive the CLK1 global clock net. Additionally, each PLL has a set of PLL_RST, PLL_FBK, and PLL_LOCK signals. The PLL_RST signal can be generated through routing or a dedicated dual-function I/O pin. The PLL_FBK signal can be generated through a dedicated dual-function I/O pin or internally from the Global Clock net associated with the PLL. The PLL_LOCK signal feeds routing directly from the sysCLOCK PLL circuit. Figure 17 illustrates how the PLL_RST and PLL_FBK signals are generated.

Each PLL has four dividers associated with it, M, N, V, and K. The M divider is used to divide the clock signal, while the N divider is used to multiply the clock signal. The V divider allows the VCO frequency to operate at higher frequencies than the clock output, thereby increasing the frequency range. The K divider is only used when a secondary clock output is needed. This divider divides the primary clock output and feeds to the adjacent global clock net. Different combinations of these dividers allow the user to synthesize clock frequencies. Figure 16 shows the ispXPGA PLL block diagram.

The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. This operates by inserting delay on the input or feedback lines of the PLL. For more information on the PLL, please refer to TN1003, sysCLOCK PLL Usage and Design Guidelines.

Figure 16. ispXPGA PLL Block Diagram



The second type of interface implemented is the terminated, single-ended interface standard. This group of interfaces includes different versions of SSTL and HSTL interfaces along with CTT, and GTL+. Usage of these particular I/O interfaces requires an additional V_{REF} signal. At the system level a termination voltage, V_{TT}, is also required. Typically an output will be terminated to V_{TT} at the receiving end of the transmission line it is driving.

The third type of interface standards are the differential standards LVDS, BLVDS, and LVPECL. The differential standards require two I/O pins to create the differential pair. The logic level is determined by the difference in the two signals. Table 6 lists how these interface standards are implemented in the ispXPGA devices.

For more information on sysIO capability, refer to TN1000, sysIO Usage Guidelines for Lattice Devices.

Figure 19. sysIO Banks per Device

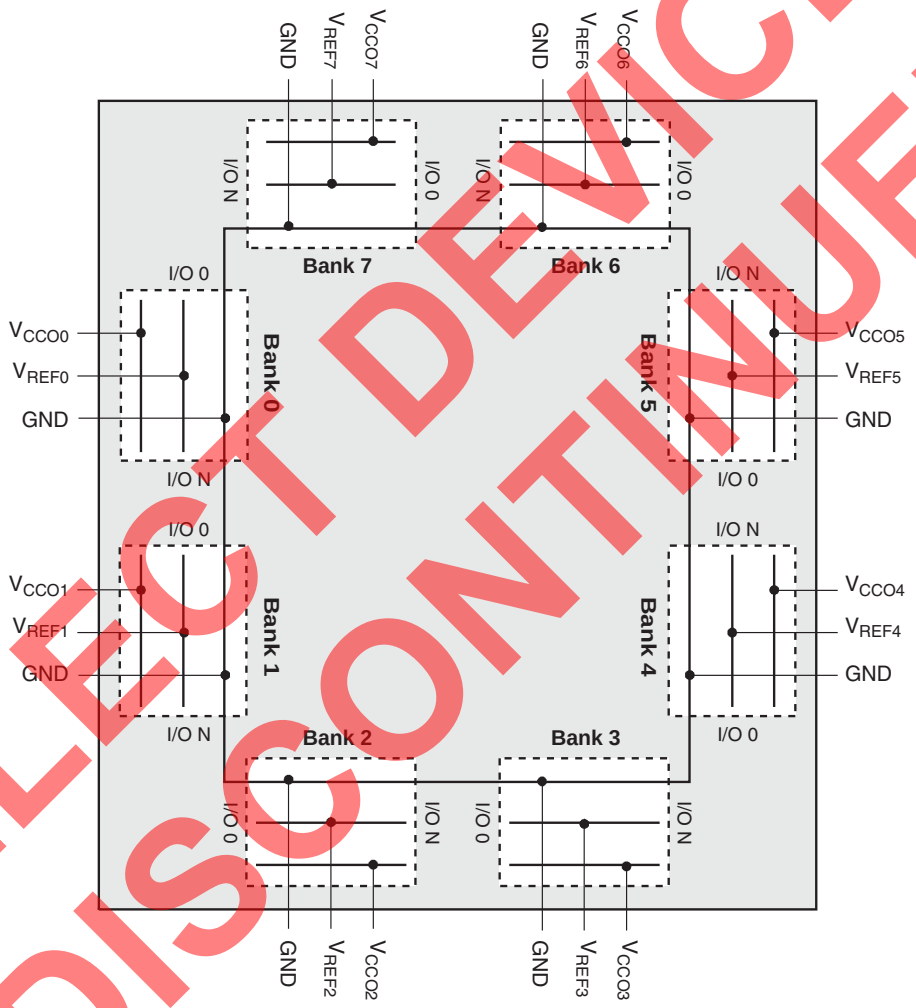


Table 4. Number of I/Os per Bank

Device	Max. Number of I/Os per Bank (N)
XPGA 1200	62
XPGA 500	42
XPGA 200	26
XPGA 125	22

sysIO Differential Standards DC Electrical Characteristics[1]

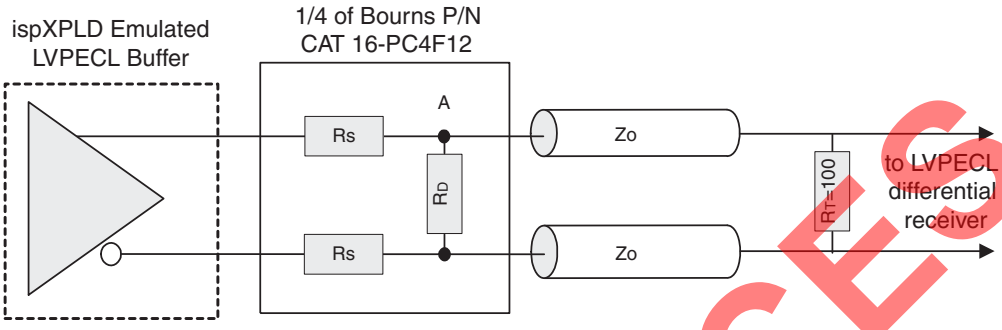
Parameter	Description	Test Conditions	Min.	Typ.	Max.
LVDS[2]					
V_{INP}, V_{INM}	Input voltage		0V	—	2.4V
V_{THD}	Differential input threshold	0.2V ð V_{CM} ð 1.8V	+/-100mV	—	—
I_{IN}	Input current	Power on	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	—	1.38V	1.60V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	0.9V	1.03V	—
V_{OD}	Output Voltage Differential	$\|V_{OP} - V_{OM}\|$, R_T = 100 ohm	250mV	350mV	450mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50mV
V_{OS}	Output Voltage Offset	$\|V_{OP} + V_{OM}\|/2$, R_T = 100 ohm	1.125V	1.25V	1.375V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50mV
I_{OSD}	Output short circuit current	V_{OD} = 0V Driver outputs shorted	—	—	24mA
BLVDS[1]					
V_{INP}, V_{INM}	Input voltage		0V	—	2.4V
V_{THD}	Differential input threshold	0.2V ð V_{CM} ð 1.8V	+/-100mV	—	—
I_{IN}	Input current	Power on	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 27Ω	—	1.4V	1.80V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 27Ω	0.95V	1.1V	—
V_{OD}	Output Voltage Differential	$\|V_{OP} - V_{OM}\|$, RT = 27Ω	240mV	300mV	460mV
ΔV_{OD}	Change in V_{OD} Between H and L				27mV
V_{OS}	Output Voltage Offset	$\|V_{OP} + V_{OM}\|$ /2, RT = 27Ω	1.1V	1.3V	1.5V
ΔV_{OS}	Change in V_{OS} Between H and L				27mV
I_{OSD}	Output Short Circuit Current	V_{OD} = 0. Driver Outputs Shorted.		36mA	65mA

1. Refer to TN1000, sysIO Usage Guidelines for Lattice Devices.
2. V_{OP} and V_{OM} are the two outputs of the LVDS/BLVDS output buffer.

LVPECL[1]								
DC Parameter	**Parameter Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
V_{CCO}		**3.0**		**3.3**		**3.6**		**V**
V_{IH}	Input Voltage High	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	Input Voltage Low	0.86	2.125	0.86	2.125	0.86	2.125	V
V_{OH}	Output Voltage High	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	Output Voltage Low	0.96	1.27	1.06	1.43	1.3	1.57	V
V_{DIFF}[2]	Differential Input threshold	0.3	—	0.3	—	0.3	—	V

1. These values are valid at the output of the source termination pack as shown above with 100-ohm differential load only (see Figure 23). The V_{OH} levels are 200mV below the standard LVPECL levels and are compatible with devices tolerant of the lower common mode ranges.
2. Valid for 0.2 ð V_{CM} ð 1.8V.

Figure 23. LVPECL Driver with Three Resistor Pack



ispXPGA 125B/C & ispXPGA 125EB/EC External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Conditions	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{CO}	Global Clock Input to Output	PIO Output Register	—	5.3	—	5.7	—	6.6	ns
t_{S}	Global Clock Input Setup	PIO Input Register without input delay	-1.9	—	-1.8	—	-1.5	—	ns
t_{H}	Global Clock Input Hold	PIO Input Register without input delay	2.7	—	2.9	—	3.3	—	ns
t_{SINDLY}	Global Clock Input Setup	PIO Input Register with input delay	3.1	—	3.3	—	3.8	—	ns
t_{HINDLY}	Global Clock Input Hold	PIO Input Register with input delay	0.0	—	0.0	—	0.0	—	
t_{COPLL}	Global Clock Input to Output	PIO Output Register using PLL without delay	—	3.6	—	3.9	—	4.5	ns
t_{SPLL}	Global Clock Input Setup	PIO Input Register without input delay using PLL without delay	0	—	0.1	—	0.3	—	ns
t_{HPLL}	Global Clock Input Hold	PIO Input Register without input delay using PLL without delay	0.9	—	1.0	—	1.2	—	ns
$t_{SINDLYPLL}$	Global Clock Input Setup	PIO Input Register with input delay using PLL without delay	5.1	—	5.5	—	6.3	—	ns
$t_{HINDLYPLL}$	Global Clock Input Hold	PIO Input Register with input delay using PLL without delay	-3.0	—	-2.8	—	-2.4	—	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 200B/C & ispXPGA 200EB/EC PFU Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Set								
t_{LASSRO}	Asynchronous Set/Reset to Output	—	1.09	—	1.17	—	1.35	ns
$t_{LASSRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{LASSRR}	Asynchronous Set/Reset Recovery	—	0.51	—	0.55	—	0.63	ns
t_{LSSR_S}	Synchronous Set/Reset Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{LSSR_H}	Synchronous Set/Reset Hold Time	0.03	—	0.03	—	0.03	—	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.
2. $t_{LCTHRUL}$ quoted bit by bit.

Timing v.0.3

ispXPGA 200B/C & ispXPGA 200EB/EC PIC Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Register/Latch Delays								
t_{IO_CO}	Register Clock to Output Delay	—	0.93	—	1.00	—	1.15	ns
t_{IO_S}	Register Setup Time (Data before Clock)	0.05	—	0.05	—	0.06	—	ns
t_{IO_H}	Register Hold Time (Data after Clock)	0.06	—	0.06	—	0.07	—	ns
t_{IOCE_S}	Register Clock Enable Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{IOCE_H}	Register Clock Enable Hold Time	0.13	—	0.13	—	0.15	—	ns
t_{IO_GO}	Latch Gate to Output Delay	—	0.72	—	0.77	—	0.89	ns
t_{IOL_S}	Latch Setup Time	0.05	—	0.05	—	0.06	—	ns
t_{IOL_H}	Latch Hold Time	0.06	—	0.06	—	0.07	—	ns
t_{IOLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns
t_{IOASRO}	Asynchronous Set/Reset to Output	—	1.04	—	1.12	—	1.29	ns
$t_{IOASRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{IOASRR}	Asynchronous Set/Reset Recovery Time	—	0.23	—	0.25	—	0.29	ns
Input/Output Delays								
t_{IOBUF}	Output Buffer Delay	—	0.97	—	1.04	—	1.20	ns
t_{IOIN}	Input Buffer Delay	—	0.60	—	0.64	—	0.74	ns
t_{IOEN}	Output Enable Delay	—	0.53	—	0.57	—	0.66	ns
t_{IODIS}	Output Disable Delay	—	-0.13	—	-0.12	—	-0.10	ns
t_{IOFT}	Feed-thru Delay	—	0.19	—	0.20	—	0.23	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 1200B/C & ispXPGA 1200EB/EC Timing Adders

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	5.58	—	6.0	—	6.90	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

REFCLK and SS_CLKIN Timing

Symbol	Description	Mode	Condition	Min	Max	Unit
$t_{DREFCLK}$	Frequency Deviation Between TX REFCLK and CDRX REFCLK on One Link	8B10B/ 10B12B		-100	100	ppm
$t_{JPPREFCLK}$	REFCLK, SS_CLKIN Peak-to-Peak Period Jitter	All	Random Jitter		0.01	UIPP
$t_{PWREFCLK}$	REFCLK, SS_CLKIN Pulse Width, (80% to 80% or 20% to 20%).	All	40-100MHz	2		ns
			100-200MHz	1		
$t_{RFREFCLK}$	REFCLK, SS_CLKIN Rise/Fall Time (20% to 80% or 80% to 20%)	All			2	ns

Serializer Timing[2]

Symbol	Description	Mode	Condition	Min	Max	Unit
$t_{JPPSOUT}$	SOUT Peak-to-Peak Output Data Jitter	All	f_{CLK} with no jitter		0.25	UIPP
$t_{JPP8B10B}$	SOUT Peak-to-Peak Random Jitter	8B10B	800 Mbps w/K28.7-		130	ps
	SOUT Peak-to-Peak Deterministic Jitter	8B10B	800 Mbps w/K28.5+		160	ps
t_{RFSOUT}	SOUT Output Data Rise/Fall Time (20%, 80%)	LVDS			700	ps
t_{COSOUT}	REFCLK to SOUT Delay	SS/8B10B		$2Bt^{1}$ + 2	$2Bt^{1}$ +10	ns
		10B12B		$1Bt^{1}$ + 2	$1Bt^{1}$ +10	ns
t_{SKTX}	Skew of SOUT with Respect to SS_CLKOUT	SS			300	ps
$t_{CKOSOUT}$	SS_CLKOUT to bit0 of SOUT	SS		$2Bt^{1}$ - t_{SKTX}	$2Bt^{1}$ + t_{SKTX}	ns
$t_{HSITXDDATAS}$	TXD Data Setup Time	All	Note 3	1.5		ns
$t_{HSITXDDATAH}$	TXD Data Hold Time	All	Note 3		1.0	ns

1. Bt: Bit Time Period. High Speed Serial Bit Time.
2. The SIN and SOUT jitter specifications listed above are under the condition that the clock tree that drives the REFCLK to sysHSI Block is in sysCLOCK PLL BYPASS mode.
3. Internal timing for reference only.

Deserializer Timing

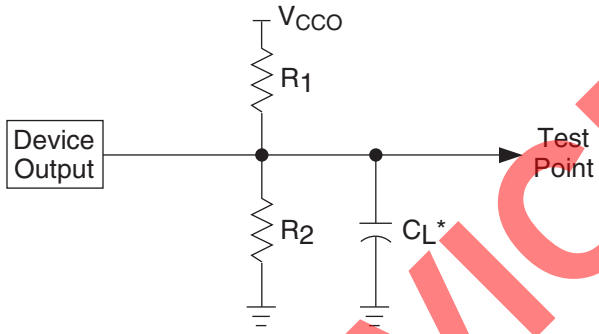
Symbol	Description	Mode	Conditions	Min	Max	Units
f_{DSIN}	SIN Frequency Deviation from REFCLK	8B10B/ 10B12B		-100	100	ppm
eo_{SIN}	SIN Eye Opening Tolerance	All	Notes 1, 2	0.45		UIPP
ber	Bit Error Rate	All			10^{-12}	Bits
$t_{HSIOUTVALIDPRE}$	RXD, SYDT Valid Time Before RECCLK Falling Edge	All	Note 3	$t_{RCP}/2$ - 0.7		ns
$t_{HSIOUTVALIDPOST}$	RXD, SYDT Valid Time After RECCLK Falling Edge	All	Note 3	$t_{RCP}/2$ - 0.7		ns
t_{DSIN}	Bit 0 of SIN Delay to RXD Valid at RECCLK Falling edge	All		1.5 t_{RCP} + 4.5Bt + 3	1.5 t_{RCP} + 4.5Bt + 15	ns

1. Eye opening based on jitter frequency of 100KHz.
2. Lower frequency operation assumes maximum eye closure of 800ps.
3. Internal timing for reference only.

Switching Test Conditions

Figure 25 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 7.

Figure 25. Output Test Load, LVTTL and LVCMOS Standards



*C_L includes test fixture and probe capacitance.

Table 7. Text Fixture Required Components

Test Condition	R_1	R_2	C_L	Timing Reference	VCCO
LVCMOS I/O, (L -> H, H -> L)	106	106	35pF	LVCMOS 3.3 = V_{CCO}/2	LVCMOS 3.3 = 3.0V
				LVCMOS 2.5 = V_{CCO}/2	LVCMOS 2.5 = 2.3V
				LVCMOS 1.8 = V_{CCO}/2	LVCMOS 1.8 = 1.65V
Default LVCMOS 1.8 I/O (Z -> H)	×	106	35pF	0.9V	1.65V
Default LVCMOS 1.8 I/O (Z -> L)	106	×	35pF	0.9V	1.65V
Default LVCMOS 1.8 I/O (H -> Z)	×	106	5pF	V_{OH} - 0.3	1.65V
Default LVCMOS 1.8 I/O (L -> Z)	106	×	5pF	V_{OL} + 0.3	1.65V

Note: Output test conditions for all other interfaces are determined by the respective standards.

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
R8	BK2_IO19	-	35N	BK2_IO19	-	31N
N8	BK2_IO20	-	36P	BK2_IO20	-	32P
P8	BK2_IO21	-	36N	BK2_IO21	-	32N
-	GND (Bank 2)	-	-	-	-	-
-	GND (Bank 3)	-	-	-	-	-
T8	BK3_IO0	-	39P	BK3_IO0	-	33P
T9	BK3_IO1	-	39N	BK3_IO1	-	33N
R9	BK3_IO2	-	40P	BK3_IO2	-	34P
-	-	-	-	GND (Bank 3)	-	-
R10	BK3_IO3	-	40N	BK3_IO3	-	34N
P9	BK3_IO4	-	41P	BK3_IO4	-	35P
N9	BK3_IO5	-	41N	BK3_IO5	-	35N
T10	BK3_IO6	-	42P	BK3_IO6	-	36P
-	GND (Bank 3)	-	-	-	-	-
T11	BK3_IO7	-	42N	BK3_IO7	-	36N
P10	BK3_IO8	-	43P	BK3_IO8	-	37P
-	-	-	-	GND (Bank 3)	-	-
N10	BK3_IO9	-	43N	BK3_IO9	-	37N
R11	BK3_IO14	-	46P	BK3_IO10	-	38P
-	GND (Bank 3)	-	-	-	-	-
R12	BK3_IO15	-	46N	BK3_IO11	-	38N
P11	BK3_IO16	VREF3	47P	BK3_IO12	VREF3	39P
N11	BK3_IO17	-	47N	BK3_IO13	-	39N
T12	BK3_IO18	-	48P	BK3_IO14	-	40P
T13	BK3_IO19	-	48N	BK3_IO15	-	40N
R13	BK3_IO20	-	49P	BK3_IO16	-	41P
-	-	-	-	GND (Bank 3)	-	-
R14	BK3_IO21	-	49N	BK3_IO17	-	41N
P12	BK3_IO22	-	50P	BK3_IO18	-	42P
-	GND (Bank 3)	-	-	-	-	-
N12	BK3_IO23	-	50N	BK3_IO19	-	42N
T14	GSR	-	-	GSR	-	-
T15	DXP	-	-	DXP	-	-
P13	DXN	-	-	DXN	-	-
P15	BK4_IO0	-	52P/HSI2	BK4_IO0	-	44P
N14	BK4_IO1	-	52N/HSI2	BK4_IO1	-	44N
R16	BK4_IO2	HSI2A_SINP	53P/HSI2	BK4_IO2	-	45P
-	GND (Bank 4)	-	-	-	-	-
P16	BK4_IO3	HSI2A_SINN	53N/HSI2	BK4_IO3	-	45N
N15	BK4_IO4	-	54P/HSI2	BK4_IO4	-	46P
-	-	-	-	GND (Bank 4)	-	-

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
C8	BK7_IO1	-	91N	BK7_IO1	-	77N
B8	BK7_IO2	-	92P	BK7_IO2	-	78P
B7	BK7_IO3	-	92N	BK7_IO3	-	78N
A9	BK7_IO6	-	94P	BK7_IO4	-	79P
-	GND (Bank 7)	-	-	-	-	-
A8	BK7_IO7	-	94N	BK7_IO5	-	79N
C7	BK7_IO10	-	96P	BK7_IO6	-	80P
D7	BK7_IO11	-	96N	BK7_IO7	-	80N
D6	BK7_IO12	-	97P	BK7_IO8	-	81P
-	-	-	-	GND (Bank 7)	-	-
C6	BK7_IO13	-	97N	BK7_IO9	-	81N
B6	BK7_IO14	-	98P	BK7_IO10	-	82P
-	GND (Bank 7)	-	-	-	-	-
B5	BK7_IO15	-	98N	BK7_IO11	-	82N
A7	BK7_IO16	VREF7	99P	BK7_IO12	VREF7	83P
A6	BK7_IO17	-	99N	BK7_IO13	-	83N
D5	BK7_IO18	-	100P	BK7_IO14	-	84P
C5	BK7_IO19	-	100N	BK7_IO15	-	84N
A5	BK7_IO20	-	101P	BK7_IO16	-	85P
-	-	-	-	GND (Bank 7)	-	-
A4	BK7_IO21	-	101N	BK7_IO17	-	85N
B4	BK7_IO22	-	102P	BK7_IO18	-	86P
-	GND (Bank 7)	-	-	-	-	-
B3	BK7_IO23	-	102N	BK7_IO19	-	86N
A3	TDO	-	-	TDO	-	-
A2	VCCJ	-	-	VCCJ	-	-
C4	TDI	-	-	TDI	-	-

1. Not available for differential pairs.
2. If a sysHSI Block is used, the indicated sysHSI reserved pins are unavailable for general purpose I/O use.

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
D14	BK0_IO37	-	18N/HSI1
C13	BK0_IO38	HSI2A_SOUTP	19P/HSI1
D13	BK0_IO39	HSI2A_SOUTN	19N/HSI1
B14	BK0_IO40	-	20P/HSI1
A14	BK0_IO41	-	20N/HSI1
C15	BK0_IO42	HSI2A_SINP	21P/HSI2
-	GND (Bank 0)	-	-
D15	BK0_IO43	HSI2A_SINN	21N/HSI2
A15	BK0_IO44	-	22P/HSI2
C16	BK0_IO45	-	22N/HSI2
B15	BK0_IO46	HSI2B_SOUTP	23P/HSI2
B16	BK0_IO47	HSI2B_SOUTN	23N/HSI2
A16	BK0_IO48	-	24P/HSI2
B17	BK0_IO49	-	24N/HSI2
D16	BK0_IO50	HSI2B_SINP	25P/HSI2
-	GND (Bank 0)	-	-
E16	BK0_IO51	HSI2B_SINN	25N/HSI2
D17	BK0_IO52	-	26P/HSI2
C17	BK0_IO53	-	26N/HSI2
A18	BK0_IO54	PLL_RST0	27P/HSI2
D18	BK0_IO55	PLL_RST1	27N/HSI2
A17	BK0_IO56	-	28P/HSI2
E19	BK0_IO57	-	28N/HSI2
A19	BK0_IO58	PLL_FBK0	29P
-	GND (Bank 0)	-	-
B19	BK0_IO59	PLL_FBK1	29N
C18	BK0_IO60	CLK_OUT0	30P
B18	BK0_IO61	CLK_OUT1	30N
-	GND (Bank 0)	-	-
D19	GCLK0	-	LVDS Pair0P
C19	GCLK1	-	LVDS Pair0N
E20	VCCP0	-	-
A21	GNDP0	-	-
B21	GCLK2	-	LVDS Pair1P
C21	GCLK3	-	LVDS Pair1N
B23	BK1_IO0	CLK_OUT2	31P
C23	BK1_IO1	CLK_OUT3	31N
B22	BK1_IO2	SS_CLKOUT0P	32P
-	GND (Bank 1)	-	-
C22	BK1_IO3	SS_CLKOUT0N	32N
D21	BK1_IO4	PLL_FBK2	33P
E21	BK1_IO5	PLL_FBK3	33N
B24	BK1_IO6	SS_CLKIN0P	34P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
-	GND (Bank 4)	-	-
AW26	BK4_IO43	-	145N
AV25	BK4_IO44	-	146P
AT24	BK4_IO45	-	146N
AU24	BK4_IO46	-	147P
AU25	BK4_IO47	-	147N
AW25	BK4_IO48	PLL_RST4	148P
AW24	BK4_IO49	PLL_RST5	148N
AU23	BK4_IO50	-	149P
-	GND (Bank 4)	-	-
AT23	BK4_IO51	-	149N
AV24	BK4_IO52	-	150P
AW23	BK4_IO53	-	150N
AV23	BK4_IO54	SS_CLKIN1P	151P
AU22	BK4_IO55	SS_CLKIN1N	151N
AR21	BK4_IO56	PLL_FBK4	152P
AT22	BK4_IO57	PLL_FBK5	152N
AV22	BK4_IO58	SS_CLKOUT1P	153P
-	GND (Bank 4)	-	-
AV21	BK4_IO59	SS_CLKOUT1N	153N
AT21	BK4_IO60	CLK_OUT4	154P
AU21	BK4_IO61	CLK_OUT5	154N
-	GND (Bank 4)	-	-
AT19	GCLK4	-	LVDS Pair2P
AU19	GCLK5	-	LVDS Pair2N
AW22	VCCP1	-	-
AR20	GNDP1	-	-
AU18	GCLK6	-	LVDS Pair3P
AT18	GCLK7	-	LVDS Pair3N
-	GND (Bank 5)	-	-
AV17	BK5_IO0	CLK_OUT6	155P
AV18	BK5_IO1	CLK_OUT7	155N
AW21	BK5_IO2	PLL_FBK6	156P
-	GND (Bank 5)	-	-
AV19	BK5_IO3	PLL_FBK7	156N
AR19	BK5_IO4	-	157P/HSI7
AW19	BK5_IO5	-	157N/HSI7
AW18	BK5_IO6	PLL_RST6	158P/HSI7
AW17	BK5_IO7	PLL_RST7	158N/HSI7
AT17	BK5_IO8	-	159P/HSI7
AV16	BK5_IO9	-	159N/HSI7
AU17	BK5_IO10	HSI7A_SINP	160P/HSI7
-	GND (Bank 5)	-	-

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
AU6	BK5_IO50	HSI9B_SINP	180P/HSI9
-	GND (Bank 5)	-	-
AV6	BK5_IO51	HSI9B_SINN	180N/HSI9
AR8	BK5_IO52	-	181P
AT7	BK5_IO53	-	181N
AU5	BK5_IO54	HSI9B_SOUTP	182P
AV5	BK5_IO55	HSI9B_SOUTN	182N
AW5	BK5_IO56	-	183P
AW4	BK5_IO57	-	183N
AT6	BK5_IO58	-	184P
-	GND (Bank 5)	-	-
AV4	BK5_IO59	-	184N
AR6	BK5_IO60	-	185P
AU4	BK5_IO61	-	185N
AT1	CFG0	-	-
AT3	DONE	-	-
AT2	PROGRAMb	-	-
AP4	BK6_IO0	INITb	186P
AP5	BK6_IO1	CCLK	186N
AR3	BK6_IO2	-	187P
-	GND (Bank 6)	-	-
AR2	BK6_IO3	-	187N
AP3	BK6_IO4	CSb	188P
AR1	BK6_IO5	Read	188N
AP2	BK6_IO6	-	189P
AP1	BK6_IO7	-	189N
AN4	BK6_IO8	-	190P
AM5	BK6_IO9	-	190N
AN3	BK6_IO10	-	191P
-	GND (Bank 6)	-	-
AN2	BK6_IO11	-	191N
AM4	BK6_IO12	VREF6	192P
AM3	BK6_IO13	-	192N
AN1	BK6_IO14	-	193P
AM2	BK6_IO15	-	193N
AL4	BK6_IO16	-	194P
AK5	BK6_IO17	-	194N
AM1	BK6_IO18	-	195P
-	GND (Bank 6)	-	-
AK4	BK6_IO19	-	195N
AL3	BK6_IO20	-	196P
AL2	BK6_IO21	-	196N
AL1	BK6_IO22	-	197P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
-	-	-	-	GND (Bank 1)	-	-
T1	BK1_IO1	CLK_OUT3	31N	BK1_IO1	CLK_OUT3	21N
U2	BK1_IO2	SS_CLKOUT0P	32P	BK1_IO2	SS_CLKOUT0P	22P
-	GND (Bank 1)	-	-	-	-	-
U1	BK1_IO3	SS_CLKOUT0N	32N	BK1_IO3	SS_CLKOUT0N	22N
U3	BK1_IO4	PLL_FBK2	33P	BK1_IO4	PLL_FBK2	23P
U4	BK1_IO5	PLL_FBK3	33N	BK1_IO5	PLL_FBK3	23N
V1	BK1_IO6	SS_CLKIN0P	34P	BK1_IO10	SS_CLKIN0P	26P
V2	BK1_IO7	SS_CLKIN0N	34N	BK1_IO11	SS_CLKIN0N	26N
U5	BK1_IO8	-	35P	BK1_IO12	-	27P
U6	BK1_IO9	-	35N	BK1_IO13	-	27N
V4	BK1_IO10	-	36P	BK1_IO6	-	24P
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-
V3	BK1_IO11	-	36N	BK1_IO7	-	24N
V6	BK1_IO12	PLL_RST2	37P	BK1_IO20	PLL_RST2	31P
V7	BK1_IO13	PLL_RST3	37N	BK1_IO21	PLL_RST3	31N
W1	BK1_IO14	-	38P	BK1_IO8	-	25P
W2	BK1_IO15	-	38N	BK1_IO9	-	25N
W3	BK1_IO16	-	39P	BK1_IO14	-	28P
-	-	-	-	GND (Bank 1)	-	-
W4	BK1_IO17	-	39N	BK1_IO15	-	28N
W5	BK1_IO18	-	40P	BK1_IO16	-	29P
-	GND (Bank 1)	-	-	-	-	-
W6	BK1_IO19	-	40N	BK1_IO17	-	29N
Y6	BK1_IO20	-	41P/HSI3	NC	-	-
Y5	BK1_IO21	-	41N/HSI3	NC	-	-
Y4	BK1_IO22	-	42P/HSI3	NC	-	-
Y3	BK1_IO23	-	42N/HSI3	NC	-	-
AA5	BK1_IO24	-	43P/HSI3	NC	-	-
AA4	BK1_IO25	-	43N/HSI3	NC	-	-
Y2	BK1_IO26	HSI3A_SOUTP	44P/HSI3	BK1_IO18	HSI2A_SOUTP	30P
-	GND (Bank 1)	-	-	-	-	-
Y1	BK1_IO27	HSI3A_SOUTN	44N/HSI3	BK1_IO19	HSI2A_SOUTN	30N
AB7	BK1_IO28	-	45P/HSI3	NC	-	-
AB6	BK1_IO29	-	45N/HSI3	NC	-	-
AA2	BK1_IO30	HSI3A_SINP	46P/HSI3	BK1_IO22	HSI2A_SINP	32P
-	-	-	-	GND (Bank 1)	-	-
AA1	BK1_IO31	HSI3A_SINN	46N/HSI3	BK1_IO23	HSI2A_SINN	32N
AB5	BK1_IO32	-	47P/HSI3	NC	-	-
AB4	BK1_IO33	-	47N/HSI3	NC	-	-
AB2	BK1_IO34	HSI3B_SOUTP	48P/HSI3	NC	-	-
-	GND (Bank 1)	-	-	-	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AB1	BK1_IO35	HSI3B_SOUTN	48N/HSI3	NC	-	-
AC6	BK1_IO36	-	49P/HSI4	NC	-	-
AC5	BK1_IO37	-	49N/HSI4	NC	-	-
AC2	BK1_IO38	HSI3B_SINP	50P/HSI4	NC	-	-
AC1	BK1_IO39	HSI3B_SINN	50N/HSI4	NC	-	-
AC4	BK1_IO40	-	51P/HSI4	NC	-	-
AC3	BK1_IO41	-	51N/HSI4	NC	-	-
AD2	BK1_IO42	HSI4A_SOUTP	52P/HSI4	NC	-	-
-	GND (Bank 1)	-	-	-	-	-
AD1	BK1_IO43	HSI4A_SOUTN	52N/HSI4	NC	-	-
AD3	BK1_IO44	-	53P/HSI4	BK1_IO32	-	37P/HSI3
AD4	BK1_IO45	-	53N/HSI4	BK1_IO33	-	37N
AE2	BK1_IO46	HSI4A_SINP	54P/HSI4	BK1_IO34	-	38P
AE1	BK1_IO47	HSI4A_SINN	54N/HSI4	BK1_IO35	-	38N
AD5	BK1_IO48	-	55P/HSI4	BK1_IO25	-	33N
AD6	BK1_IO49	VREF1	55N/HSI4	BK1_IO24	VREF1	33P
AF2	BK1_IO50	HSI4B_SOUTP	56P/HSI4	BK1_IO26	HSI2B_SOUTP	34P
-	GND (Bank 1)	-	-	-	-	-
AF1	BK1_IO51	HSI4B_SOUTN	56N/HSI4	BK1_IO27	HSI2B_SOUTN	34N
AE3	BK1_IO52	-	57P	BK1_IO28	-	35P
AE4	BK1_IO53	-	57N	BK1_IO29	-	35N
AG1	BK1_IO54	HSI4B_SINP	58P	BK1_IO30	HSI2B_SINP	36P
-	-	-	-	GND (Bank 1)	-	-
AG2	BK1_IO55	HSI4B_SINN	58N	BK1_IO31	HSI2B_SINN	36N
AE5	BK1_IO56	-	59P	BK1_IO36	-	39P
AF4	BK1_IO57	-	59N	BK1_IO37	-	39N
AH1	BK1_IO58	-	60P	BK1_IO38	-	40P
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-
AH2	BK1_IO59	-	60N	BK1_IO39	-	40N
AF3	BK1_IO60	-	61P	BK1_IO40	-	41P
AG3	BK1_IO61	-	61N	BK1_IO41	-	41N
AH4	TCK	-	-	TCK	-	-
AJ3	TMS	-	-	TMS	-	-
AK3	TOE	-	-	TOE	-	-
AG5	BK2_IO0	-	62P	BK2_IO0	-	42P
AH5	BK2_IO1	-	62N	BK2_IO1	-	42N
AJ4	BK2_IO2	-	63P	BK2_IO2	-	43P
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
AK4	BK2_IO3	-	63N	BK2_IO3	-	43N
AG6	BK2_IO4	-	64P	BK2_IO4	-	44P
AH6	BK2_IO5	-	64N	BK2_IO5	-	44N
AJ5	BK2_IO6	-	65P	BK2_IO6	-	45P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
K30	BK5_IO22	HSI7B_SOUTP	166P/HSI8	BK5_IO22	HSI4B_SOUTP	116P/HSI4
-	-	-	-	GND (Bank 5)	-	-
K29	BK5_IO23	HSI7B_SOUTN	166N/HSI8	BK5_IO23	HSI4B_SOUTN	116N/HSI4
L28	BK5_IO24	-	167P/HSI8	BK5_IO24	-	117P/HSI5
L27	BK5_IO25	-	167N/HSI8	BK5_IO25	-	117N/HSI5
L26	BK5_IO26	HSI8A_SINP	168P/HSI8	BK5_IO26	HSI5A_SINP	118P/HSI5
-	GND (Bank 5)	-	-	-	-	-
L25	BK5_IO27	HSI8A_SINN	168N/HSI8	BK5_IO27	HSI5A_SINN	118N/HSI5
K27	BK5_IO28	-	169P/HSI8	BK5_IO28	-	119P/HSI5
K26	BK5_IO29	-	169N/HSI8	BK5_IO29	-	119N/HSI5
J30	BK5_IO30	HSI8A_SOUTP	170P/HSI8	BK5_IO30	HSI5A_SOUTP	120P/HSI5
-	-	-	-	GND (Bank 5)	-	-
J29	BK5_IO31	HSI8A_SOUTN	170N/HSI8	BK5_IO31	HSI5A_SOUTN	120N/HSI5
J26	BK5_IO32	-	171P/HSI8	NC	-	-
J27	BK5_IO33	-	171N/HSI8	NC	-	-
H30	BK5_IO34	HSI8B_SINP	172P/HSI8	NC	-	-
-	GND (Bank 5)	-	-	-	-	-
H29	BK5_IO35	HSI8B_SINN	172N/HSI8	NC	-	-
J25	BK5_IO36	-	173P/HSI9	NC	-	-
J24	BK5_IO37	-	173N/HSI9	NC	-	-
G30	BK5_IO38	HSI8B_SOUTP	174P/HSI9	NC	-	-
G29	BK5_IO39	HSI8B_SOUTN	174N/HSI9	NC	-	-
H27	BK5_IO40	-	175P/HSI9	NC	-	-
H28	BK5_IO41	-	175N/HSI9	NC	-	-
F30	BK5_IO42	HSI9A_SINP	176P/HSI9	NC	-	-
-	GND (Bank 5)	-	-	-	-	-
F29	BK5_IO43	HSI9A_SINN	176N/HSI9	NC	-	-
G27	BK5_IO44	-	177P/HSI9	NC	-	-
G28	BK5_IO45	-	177N/HSI9	NC	-	-
E30	BK5_IO46	HSI9A_SOUTP	178P/HSI9	NC	-	-
E29	BK5_IO47	HSI9A_SOUTN	178N/HSI9	NC	-	-
H26	BK5_IO48	-	179P/HSI9	BK5_IO33	-	121N/HSI5
H25	BK5_IO49	VREF5	179N/HSI9	BK5_IO32	VREF5	121P/HSI5
D30	BK5_IO50	HSI9B_SINP	180P/HSI9	BK5_IO34	HSI5B_SINP	122P/HSI5
-	GND (Bank 5)	-	-	-	-	-
D29	BK5_IO51	HSI9B_SINN	180N/HSI9	BK5_IO35	HSI5B_SINN	122N/HSI5
F28	BK5_IO52	-	181P	BK5_IO36	-	123P/HSI5
F27	BK5_IO53	-	181N	BK5_IO37	-	123N/HSI5
C30	BK5_IO54	HSI9B_SOUTP	182P	BK5_IO38	HSI5B_SOUTP	124P/HSI5
-	-	-	-	GND (Bank 5)	-	-
C29	BK5_IO55	HSI9B_SOUTN	182N	BK5_IO39	HSI5B_SOUTN	124N/HSI5
G26	BK5_IO56	-	183P	NC	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
D21	BK6_IO29	-	200N	NC	-	-
A21	BK6_IO30	-	201P	NC	-	-
B21	BK6_IO31	-	201N	NC	-	-
F20	BK6_IO32	DATA7	202P	BK6_IO18	DATA7	135P
-	-	-	-	GND (Bank 6)	-	-
E20	BK6_IO33	DATA6	202N	BK6_IO19	DATA6	135N
D20	BK6_IO34	-	203P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-
C20	BK6_IO35		203N	NC	-	-
F19	BK6_IO36	DATA5	204P	BK6_IO22	DATA5	137P
E19	BK6_IO37	DATA4	204N	BK6_IO23	DATA4	137N
B20	BK6_IO38	-	205P	NC	-	-
A20	BK6_IO39	-	205N	NC	-	-
D19	BK6_IO40	-	206P	NC	-	-
C19	BK6_IO41	-	206N	NC	-	-
A19	BK6_IO42	-	207P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-
B19	BK6_IO43	-	207N	NC	-	-
G18	BK6_IO44	-	208P	BK6_IO24	-	138P
F18	BK6_IO45	-	208N	BK6_IO25	-	138N
A18	BK6_IO46	-	209P	BK6_IO32	-	142P
B18	BK6_IO47	-	209N	BK6_IO33	-	142N
D18	BK6_IO48	-	210P	BK6_IO34	-	143P
-	-	-	-	GND (Bank 6)	-	-
C18	BK6_IO49	-	210N	BK6_IO35	-	143N
F17	BK6_IO50	DATA3	211P	BK6_IO26	DATA3	139P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
E17	BK6_IO51	DATA2	211N	BK6_IO27	DATA2	139N
D17	BK6_IO52	-	212P	BK6_IO28	-	140P
C17	BK6_IO53	-	212N	BK6_IO29	-	140N
B17	BK6_IO54	DATA1	213P	BK6_IO30	DATA1	141P
A17	BK6_IO55	DATA0	213N	BK6_IO31	DATA0	141N
F16	BK6_IO56	-	214P	BK6_IO36	-	144P
E16	BK6_IO57	-	214N	BK6_IO37	-	144N
D16	BK6_IO58	-	215P	BK6_IO38	-	145P
-	GND (Bank 6)	-	-	-	-	-
C16	BK6_IO59	-	215N	BK6_IO39	-	145N
B16	BK6_IO60	-	216P	BK6_IO40	-	146P
A16	BK6_IO61	-	216N	BK6_IO41	-	146N
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-
A15	BK7_IO0	-	217P	BK7_IO0	-	147P

"E-Series" Commercial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125EB-05F256C	139K	2.5/3.3	-5	fpBGA	256
LFX125EB-04F256C	139K	2.5/3.3	-4	fpBGA	256
LFX125EB-03F256C	139K	2.5/3.3	-3	fpBGA	256
LFX125EC-04F256C	139K	1.8	-4	fpBGA	256
LFX125EC-03F256C	139K	1.8	-3	fpBGA	256
LFX125EB-05F516C	139K	2.5/3.3	-5	fpBGA	516
LFX125EB-04F516C	139K	2.5/3.3	-4	fpBGA	516
LFX125EB-03F516C	139K	2.5/3.3	-3	fpBGA	516
LFX125EC-04F516C	139K	1.8	-4	fpBGA	516
LFX125EC-03F516C	139K	1.8	-3	fpBGA	516
LFX125EB-05FH516C[1]	139K	2.5/3.3	-5	fpBGA	516
LFX125EB-04FH516C[1]	139K	2.5/3.3	-4	fpBGA	516
LFX125EB-03FH516C[1]	139K	2.5/3.3	-3	fpBGA	516
LFX125EC-04FH516C[1]	139K	1.8	-4	fpBGA	516
LFX125EC-03FH516C[1]	139K	1.8	-3	fpBGA	516
LFX200EB-05F256C	210K	2.5/3.3	-5	fpBGA	256
LFX200EB-04F256C	210K	2.5/3.3	-4	fpBGA	256
LFX200EB-03F256C	210K	2.5/3.3	-3	fpBGA	256
LFX200EC-04F256C	210K	1.8	-4	fpBGA	256
LFX200EC-03F256C	210K	1.8	-3	fpBGA	256
LFX200EB-05F516C	210K	2.5/3.3	-5	fpBGA	516
LFX200EB-04F516C	210K	2.5/3.3	-4	fpBGA	516
LFX200EB-03F516C	210K	2.5/3.3	-3	fpBGA	516
LFX200EC-04F516C	210K	1.8	-4	fpBGA	516
LFX200EC-03F516C	210K	1.8	-3	fpBGA	516
LFX200EB-05FH516C[1]	210K	2.5/3.3	-5	fpBGA	516
LFX200EB-04FH516C[1]	210K	2.5/3.3	-4	fpBGA	516
LFX200EB-03FH516C[1]	210K	2.5/3.3	-3	fpBGA	516
LFX200EC-04FH516C[1]	210K	1.8	-4	fpBGA	516
LFX200EC-03FH516C[1]	210K	1.8	-3	fpBGA	516
LFX500EB-05F516C	476K	2.5/3.3	-5	fpBGA	516
LFX500EB-04F516C	476K	2.5/3.3	-4	fpBGA	516
LFX500EB-03F516C	476K	2.5/3.3	-3	fpBGA	516
LFX500EC-04F516C	476K	1.8	-4	fpBGA	516
LFX500EC-03F516C	476K	1.8	-3	fpBGA	516
LFX500EB-05FH516C[1]	476K	2.5/3.3	-5	fpBGA	516
LFX500EB-04FH516C[1]	476K	2.5/3.3	-4	fpBGA	516
LFX500EB-03FH516C[1]	476K	2.5/3.3	-3	fpBGA	516
LFX500EC-04FH516C[1]	476K	1.8	-4	fpBGA	516
LFX500EC-03FH516C[1]	476K	1.8	-3	fpBGA	516
LFX500EB-05F900C	476K	2.5/3.3	-5	fpBGA	900
LFX500EB-04F900C	476K	2.5/3.3	-4	fpBGA	900
LFX500EB-03F900C	476K	2.5/3.3	-3	fpBGA	900
LFX500EC-04F900C	476K	1.8	-4	fpBGA	900

"E-Series" Industrial (Cont.)

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX1200EB-04F900I[2]	1.25M	2.5/3.3	-4	fpBGA	900
LFX1200EB-03F900I[2]	1.25M	2.5/3.3	-3	fpBGA	900
LFX1200EC-03F900I[2]	1.25M	1.8	-3	fpBGA	900
LFX1200EB-04FE680I[2]	1.25M	2.5/3.3	-4	fpSBGA	680
LFX1200EB-03FE680I[2]	1.25M	2.5/3.3	-3	fpSBGA	680
LFX1200EC-03FE680I[2]	1.25M	1.8	-3	fpSBGA	680

1. FH516 package was converted to F516 via PCN #09A-08.
2. Discontinued via PCN #03A-10.

Lead-Free Packaging

Commercial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125B-05FN256C	139K	2.5/3.3	-5	Lead-Free fpBGA	256
LFX125B-04FN256C	139K	2.5/3.3	-4	Lead-Free fpBGA	256
LFX125B-03FN256C	139K	2.5/3.3	-3	Lead-Free fpBGA	256
LFX125C-04FN256C	139K	1.8	-4	Lead-Free fpBGA	256
LFX125C-03FN256C	139K	1.8	-3	Lead-Free fpBGA	256
LFX200B-05FN256C	210K	2.5/3.3	-5	Lead-Free fpBGA	256
LFX200B-04FN256C	210K	2.5/3.3	-4	Lead-Free fpBGA	256
LFX200B-03FN256C	210K	2.5/3.3	-3	Lead-Free fpBGA	256
LFX200C-04FN256C	210K	1.8	-4	Lead-Free fpBGA	256
LFX200C-03FN256C	210K	1.8	-3	Lead-Free fpBGA	256
LFX500B-05FN900C	476K	2.5/3.3	-5	Lead-Free fpBGA	900
LFX500B-04FN900C	476K	2.5/3.3	-4	Lead-Free fpBGA	900
LFX500B-03FN900C	476K	2.5/3.3	-3	Lead-Free fpBGA	900
LFX500C-04FN900C	476K	1.8	-4	Lead-Free fpBGA	900
LFX500C-03FN900C	476K	1.8	-3	Lead-Free fpBGA	900

"E-Series" Commercial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125EB-05FN256C	139K	2.5/3.3	-5	Lead-Free fpBGA	256
LFX125EB-04FN256C	139K	2.5/3.3	-4	Lead-Free fpBGA	256
LFX125EB-03FN256C	139K	2.5/3.3	-3	Lead-Free fpBGA	256
LFX125EC-04FN256C	139K	1.8	-4	Lead-Free fpBGA	256
LFX125EC-03FN256C	139K	1.8	-3	Lead-Free fpBGA	256
LFX200EB-05FN256C	210K	2.5/3.3	-5	Lead-Free fpBGA	256
LFX200EB-04FN256C	210K	2.5/3.3	-4	Lead-Free fpBGA	256
LFX200EB-03FN256C	210K	2.5/3.3	-3	Lead-Free fpBGA	256
LFX200EC-04FN256C	210K	1.8	-4	Lead-Free fpBGA	256
LFX200EC-03FN256C	210K	1.8	-3	Lead-Free fpBGA	256
LFX500EB-05FN900C	476K	2.5/3.3	-5	Lead-Free fpBGA	900
LFX500EB-04FN900C	476K	2.5/3.3	-4	Lead-Free fpBGA	900
LFX500EB-03FN900C	476K	2.5/3.3	-3	Lead-Free fpBGA	900