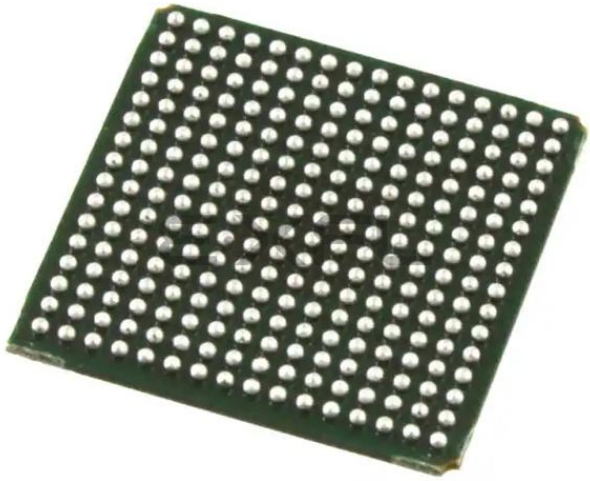


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1936
Total RAM Bits	94208
Number of I/O	160
Number of Gates	139000
Voltage - Supply	2.3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx125eb-04f256c

Product Line	Ordering Part Number	Product Status	Reference PCN
LFX125EC (Cont'd)	LFX125EC-03F516C	**Discontinued**	PCN#09-10
	LFX125EC-04F516C		
	LFX125EC-03F516I		
LFX200EB	LFX200EB-03F256C	Active / Orderable	
	LFX200EB-03FN256C		
	LFX200EB-04F256C		
	LFX200EB-04FN256C		
	LFX200EB-05F256C		
	LFX200EB-05FN256C		
	LFX200EB-03F256I		
	LFX200EB-03FN256I		
	LFX200EB-04F256I		
	LFX200EB-04FN256I		
	LFX200EB-03F516C	**Discontinued**	PCN#09-10
	LFX200EB-04F516C		
	LFX200EB-05F516C		
	LFX200EB-03F516I		
	LFX200EB-04F516I		
LFX200EC	LFX200EC-03F256C	**Discontinued**	PCN#09-10
	LFX200EC-03FN256C		
	LFX200EC-04F256C		
	LFX200EC-04FN256C		
	LFX200EC-03F256I		
	LFX200EC-03FN256I		
	LFX200EC-03F516C		
	LFX200EC-04F516C		
	LFX200EC-03F516I		
LFX500EB	LFX500EB-03F516C	**Discontinued**	PCN#09-10
	LFX500EB-04F516C		
	LFX500EB-05F516C		
	LFX500EB-03F516I		
	LFX500EB-04F516I		
	LFX500EB-03F900C		
	LFX500EB-03FN900C		
	LFX500EB-04F900C		
	LFX500EB-04FN900C		
	LFX500EB-05F900C		
	LFX500EB-05FN900C		
	LFX500EB-03F900I		
	LFX500EB-03FN900I		
	LFX500EB-04F900I		
	LFX500EB-04FN900I		
LFX500EC	LFX500EC-03F516C	**Discontinued**	PCN#09-10
	LFX500EC-04F516C		
	LFX500EC-03F516I		

Product Line	Ordering Part Number	Product Status	Reference PCN
LFX500EC (Cont'd)	LFX500EC-03F900C	**Discontinued**	PCN#09-10
	LFX500EC-03FN900C		
	LFX500EC-04F900C		
	LFX500EC-04FN900C		
	LFX500EC-03F900I		
	LFX500EC-03FN900I		
LFX1200EB	LFX1200EB-03FE680C	**Discontinued**	PCN#03A-10
	LFX1200EB-04FE680C		
	LFX1200EB-05FE680C		
	LFX1200EB-03FE680I		
	LFX1200EB-04FE680I		
	LFX1200EB-03F900C		
	LFX1200EB-04F900C		
	LFX1200EB-05F900C		
	LFX1200EB-03F900I		
	LFX1200EB-04F900I		
LFX1200EC	LFX1200EC-03FE680C	**Discontinued**	PCN#03A-10
	LFX1200EC-04FE680C		
	LFX1200EC-03FE680I		
	LFX1200EC-03F900C		
	LFX1200EC-04F900C		
	LFX1200EC-03F900I		

5555 N.E. Moore Ct. ● Hillsboro, Oregon 97124-6421 ● Phone (503) 268-8000 ● FAX (503) 268-8347
Internet: http://www.latticesemi.com

Architecture Overview

The ispXPGA architecture is a symmetrical architecture consisting of an array of Programmable Function Units (PFUs) enclosed by Input Output Groups (PICs) with columns of sysMEM Embedded Block RAMs (EBRs) distributed throughout the array. Figure 1 illustrates the ispXPGA architecture. Each PIC has two corresponding sysIO blocks, each of which includes one input and output buffer. On two sides of the device, between the PICs and the sysIO blocks, there are sysHSI High-Speed Interface blocks. The symmetrical architecture allows designers to easily implement their designs, since any logic function can be placed in any section of the device.

The PFUs contain the basic building blocks to create logic, memory, arithmetic, and register functions. They are optimized for speed and flexibility allowing complex designs to be implemented quickly and efficiently.

The PICs interface the PFUs and EBRs to the external pins of the device. They allow the signals to be registered quickly to minimize setup times for high-speed designs. They also allow connections directly to the different logic elements for fast access to combinatorial functions.

The sysMEM EBRs are large, fast memory elements that can be configured as RAM, ROM, FIFO, and other storage types. They are designed to facilitate both single and dual-port memory for high-speed applications.

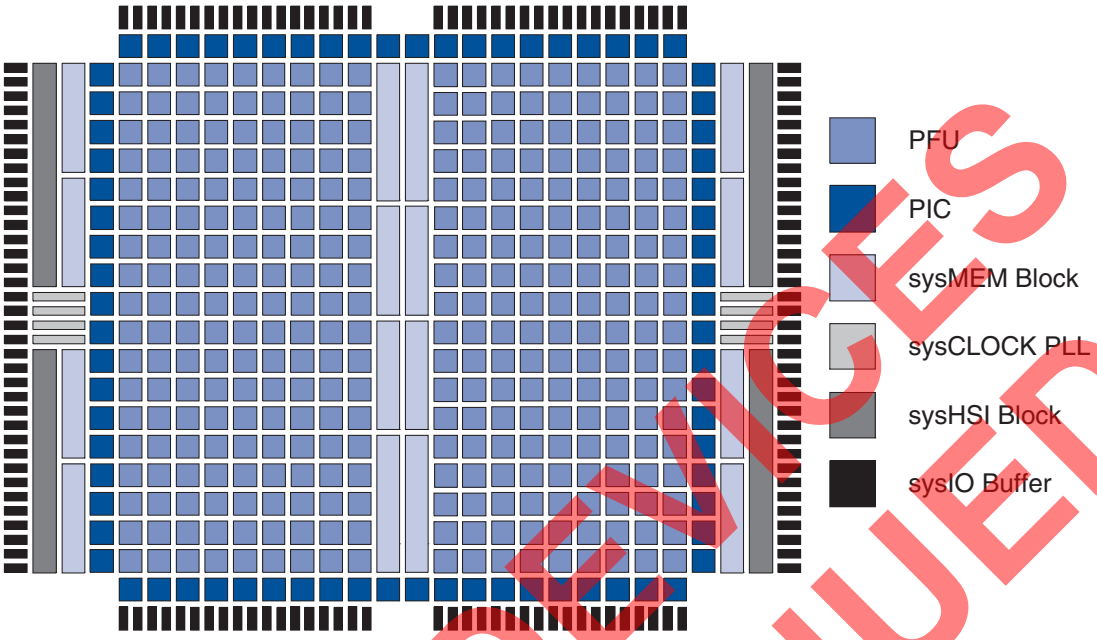
These three components of the architecture are interconnected via a high-speed, flexible routing array. The routing array consists of Variable Length Interconnect (VLI) lines between the PICs, PFUs, and EBRs. There is additional routing available to the PFU for feedback and direct routing of signals to adjacent PFUs or PICs.

The sysIO blocks consist of configurable input and output buffers connected directly to the PICs. These buffers can be configured to interface with 16 different I/O standards. This allows the ispXPGA to interface with other devices without the need for external transceivers.

The sysHSI blocks provide the necessary components to allow the ispXPGA device to transfer data at up to 800Mbps using the LVDS standard. These components include serializing, de-serializing, and clock data recovery (CDR) logic.

The sysCLOCK blocks provide clock multiplication/division, clock distribution, delay compensation, and increased performance through the use of PLL circuitry that manipulates the global clocks. There is one sysCLOCK block for each global clock tree in the device.

Figure 1. ispXPGA Block Diagram



Programmable Function Unit

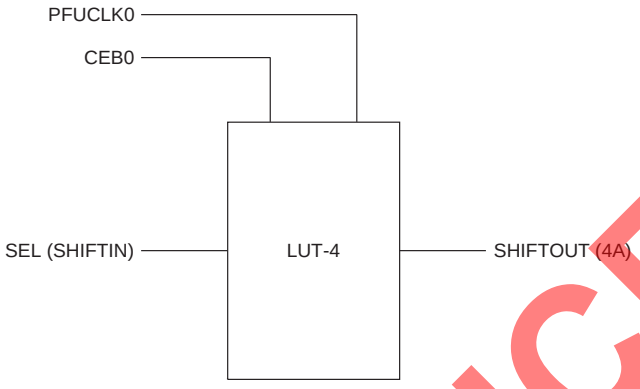
The Programmable Function Unit (PFU) is the basic building block of the ispXPGA architecture. The PFUs are arranged in rows and columns in the device with PFU (1,1) referring to (row 1, column 1). Each PFU consists of four Configurable Logic Elements (CLEs), four Configurable Sequential Elements (CSEs), and a Wide Logic Generator (WLG). By utilizing these components, the PFU can implement a variety of functions. Table 3 lists some of the function capabilities of the PFU.

There are 57 inputs to each PFU and nine outputs. The PFU uses 20 inputs for logic, and 37 inputs drive the control logic from which six control signals are derived for the PFU.

Table 3. Function Capability of ispXPGA PFU

Function	Capability
Look-up table	LUT-4, LUT-5, LUT-6
Wide logic functions	Up to 20 input logic functions
Multiplexing	2:1, 4:1, 8:1
Arithmetic logic	Dedicated carry chain and booth multiplication logic
Single-port RAM	16X1, 16X2, 16X4, 32X1, 32X2, 64X1
Double-port RAM	16X1, 16X2, 32X1
Shift register	8-bit shift registers (up to 32-bit shift capability)

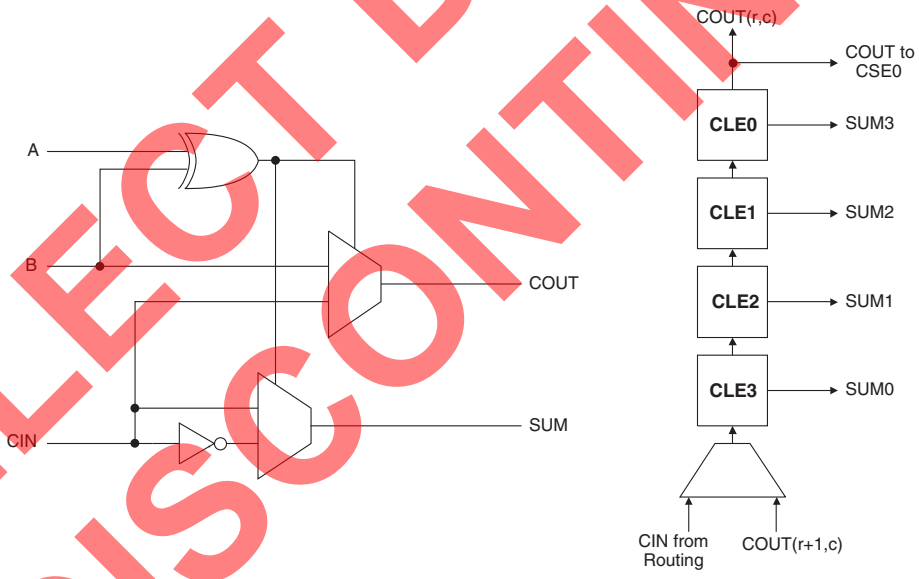
Figure 4. LUT in Shift Register Mode



Carry Chain Generator

The Carry Chain Generator is useful for implementing high-speed arithmetic functions. The CCG consists of a two-input XOR gate whose carryout can be cascaded with the input of the adjacent CCG. As shown in Figure 5, the carryin signal feeds CLE3 of the PFU and is propagated through CLE2 and CLE1 before reaching CLE0. The sum output of the CCG can be fed to the CSE through the WLG. The carryout must propagate to CLE0 for use outside the PFU. The carryout from the PFU can feed the W0 input of CSE0. The CCG also helps to effectively implement wider functions by using its logic elements to expand the capabilities of the LUT-4.

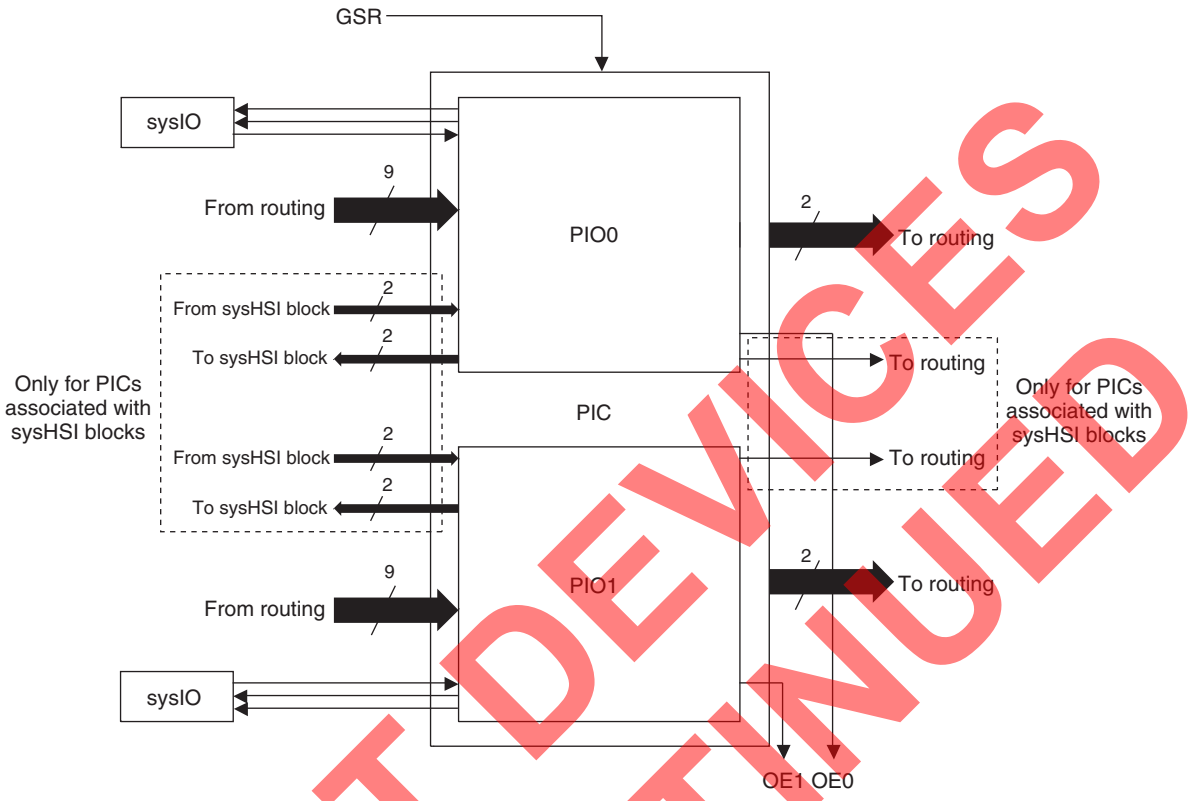
Figure 5. Carry Chain Generator



Wide Logic Generator

The WLG contains the logic necessary to implement wide gate functions. This is made up of a set of multiplexers that are located between the CLE and the CSE. The WLG helps in enhancing the wide gating capability of the PFU. The outputs of each CLE can be cascaded in the WLG to build wide gating functions. Wide multiplexing functions are also possible with a similar use of the WLG. Figure 6 illustrates the WLG.

Figure 10. ispXPGA PIC



Programmable Input/Output

The PIO is the building block of a PIC. The PIO has a total of 11 inputs and five outputs. Nine of the 11 inputs are generated from routing. The inputs from routing are the PIO Input (IN), Feed-Thru (FT), Clock (CLK), Input Clock Enable (ICE), Input Set/Reset (ISR), Output Clock Enable (OCEN), Output Set/Reset (OSR), PIO Output Enable (OEN), and PIO Input Enable (IEN). The remaining inputs are the sysIO input buffer signal and the Global Set/Reset signal. Three of the five outputs (OUT0, OUT1, and OE) feed routing. The last two outputs feed the sysIO buffer directly as the output and output enable of the sysIO output buffer.

PIOs associated with sysHSI blocks contain two additional inputs and outputs to support the sysHSI block. The two inputs come from the sysHSI block associated with the PIO, and the two outputs feed the sysHSI block. One of the inputs routes directly through the PIO to routing, while the other is multiplexed with the Feed-Thru, register bypass, and Q output of the register to form the OUT1 output of the PIO. The outputs to the sysHSI block are the same signals as the outputs which feed the sysIO buffers (sysIO Output and sysIO Output Enable).

Each PIO has an input register, an output register, and an output enable register as shown in Figure 11. The input register path of the PIO has a 'delay' option, which slows the data-flow. A two-input OR function of the Global Set/Reset (GSR) and Set/Reset (ISR or OSR) signals creates the set/reset term for the respective registers. Each PIO has two pairs of set/reset and clock enable signals. One is exclusive to the input register, whereas the other is common for both the output and output enable registers. The clock (CLK) is common to all registers in a PIO, and the polarity of the clock is controllable. The input, output, and the output enable registers can be configured as a latch or D-type flip-flop. Each PIO is capable of generating an output enable signal, which in turn becomes a PIC output.

Supply Current

Over Recommended Operating Conditions

Symbol	Parameter	Device	Condition	Min.	Typ.	Max.	Units
I_{CC}[1, 2]	Standby Core Operating Power Supply Current	LFX125	V_{CC} = 3.3V	—	60	—	mA
			V_{CC} = 2.5V	—	60	—	mA
			V_{CC} = 1.8V	—	40	—	mA
		LFX200	V_{CC} = 3.3V	—	70	—	mA
			V_{CC} = 2.5V	—	70	—	mA
			V_{CC} = 1.8V	—	50	—	mA
		LFX500	V_{CC} = 3.3V	—	120	—	mA
			V_{CC} = 2.5V	—	120	—	mA
			V_{CC} = 1.8V	—	100	—	mA
		LFX1200	V_{CC} = 3.3V	—	220	—	mA
			V_{CC} = 2.5V	—	220	—	mA
			V_{CC} = 1.8V	—	200	—	mA
I_{CCO}[3]	Standby Output Power Supply Current		V_{CCO} = 3.3V	—	2.0	—	mA
			V_{CCO} = 2.5V	—	2.0	—	mA
			V_{CCO} = 1.8V	—	2.0	—	mA
			V_{CCO} = 1.5V	—	2.0	—	mA
I_{CCP}[4]	Standby PLL Operating Supply Current		V_{CCP} = 3.3V	—	17.0	—	mA
			V_{CCP} = 2.5V	—	17.0	—	mA
			V_{CCP} = 1.8V	—	15.0	—	mA
I_{CCJ}[5]	Standby IEEE 1149.1 TAP Power Supply Current		V_{CCJ} = 3.3V	—	2.0	—	mA
			V_{CCJ} = 2.5V	—	1.5	—	mA
			V_{CCJ} = 1.8V	—	1.0	—	mA

1. T_A = 25°C, frequency = 1.0 MHz, device configured with 16-bit counters.
2. I_{CC} varies with specific device configuration and operating frequency. For more accurate power calculation, see TN1043, Power Estimation in ispXPGA Devices.
3. T_A = 25°C, per bank, no DC load, frequency = 0 MHz.
4. T_A = 25°C, per PLL, frequency = 10 MHz.
5. T_A = 25°C

sysIO Recommended Operating Conditions

Standard	V_{CCO} (V)[1]			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.0	3.3	3.6	-	-	-
LVCMOS 2.5	2.3	2.5	2.7	-	-	-
LVCMOS 1.8[2]	1.65	1.8	1.95	-	-	-
LVTTL	3.0	3.3	3.6	-	-	-
PCI 3.3	3.0	3.3	3.6	-	-	-
AGP-1X	3.15	3.3	3.45	-	-	-
SSTL 2	2.3	2.5	2.7	1.15	1.25	1.35
SSTL 3	3.0	3.3	3.6	1.3	1.5	1.7
CTT 3.3	3.0	3.3	3.6	1.35	1.5	1.65
CTT 2.5	2.3	2.5	2.7	1.35	1.5	1.65
HSTL Class I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL Class III	1.4	1.5	1.6	-	0.9	-
GTL+	-	-	-	0.882	1.0	1.122
LVDS	2.3	2.5	2.7	-	-	-
LVPECL	3.0	3.3	3.6	-	-	-
BLVDS	2.3	2.5	2.7	-	-	-

1. Inputs independent of V_{CCO}.
2. Design tool default setting.

ispXPGA 125B/C & ispXPGA 125EB/EC PFU Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Set								
t_{LASSRO}	Asynchronous Set/Reset to Output	—	1.09	—	1.17	—	1.35	ns
$t_{LASSRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{LASSRR}	Asynchronous Set/Reset Recovery	—	0.51	—	0.55	—	0.63	ns
t_{LSSR_S}	Synchronous Set/Reset Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{LSSR_H}	Synchronous Set/Reset Hold Time	0.03	—	0.03	—	0.03	—	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.
2. $t_{LCTHRUL}$ quoted bit by bit.

Timing v.0.3

ispXPGA 125B/C & ispXPGA 125EB/EC PIC Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Register/Latch Delays								
t_{IO_CO}	Register Clock to Output Delay	—	0.89	—	0.96	—	1.10	ns
t_{IO_S}	Register Setup Time (Data before Clock)	0.05	—	0.05	—	0.06	—	ns
t_{IO_H}	Register Hold Time (Data after Clock)	0.06	—	0.06	—	0.07	—	ns
t_{IOCE_S}	Register Clock Enable Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{IOCE_H}	Register Clock Enable Hold Time	0.13	—	0.13	—	0.15	—	ns
t_{IO_GO}	Latch Gate to Output Delay	—	0.68	—	0.73	—	0.84	ns
t_{IOL_S}	Latch Setup Time	0.05	—	0.05	—	0.06	—	ns
t_{IOL_H}	Latch Hold Time	0.06	—	0.06	—	0.07	—	ns
t_{IOLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns
t_{IOASRO}	Asynchronous Set/Reset to Output	—	1.00	—	1.08	—	1.24	ns
$t_{IOASRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{IOASRR}	Asynchronous Set/Reset Recovery Time	—	0.23	—	0.25	—	0.29	ns
Input/Output Delays								
t_{IOBUF}	Output Buffer Delay	—	0.97	—	1.04	—	1.20	ns
t_{IOIN}	Input Buffer Delay	—	0.57	—	0.61	—	0.70	ns
t_{IOEN}	Output Enable Delay	—	0.53	—	0.57	—	0.66	ns
t_{IODIS}	Output Disable Delay	—	-0.14	—	-0.13	—	-0.11	ns
t_{IOFT}	Feed-thru Delay	—	0.19	—	0.20	—	0.23	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 200B/C & ispXPGA 200EB/EC PFU Timing Parameters

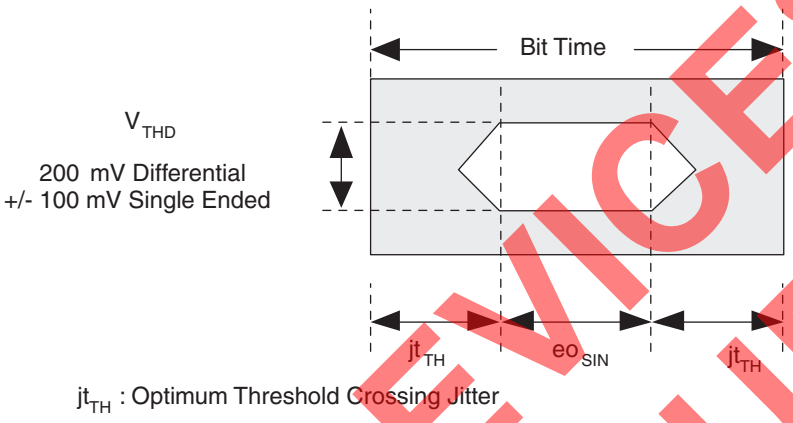
Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Functional Delays								
LUTs								
t_{LUT4}	4-Input LUT Delay	—	0.41	—	0.44	—	0.51	ns
t_{LUT5}	5-Input LUT Delay	—	0.73	—	0.79	—	0.91	ns
t_{LUT6}	6-Input LUT Delay	—	0.86	—	0.93	—	1.07	ns
Shift Register (LUT)								
t_{LSR_S}	Shift Register Setup Time	-0.64	—	-0.62	—	-0.53	—	ns
t_{LSR_H}	Shift Register Hold Time	0.61	—	0.63	—	0.72	—	ns
t_{LSR_CO}	Shift Register Clock to Output Delay	—	0.70	—	0.75	—	0.86	ns
Arithmetic Functions								
$t_{LCTHRUR}$	MC (Macro Cell) Carry In to MC Carry Out Delay (Ripple)	—	0.08	—	0.09	—	0.10	ns
$t_{LCTHRUL}$[2]	MC Carry In to MC Carry Out Delay (Look Ahead)	—	0.05	—	0.05	—	0.06	ns
t_{LSTHRU}	MC Sum In to MC Sum Out Delay	—	0.42	—	0.45	—	0.52	ns
$t_{LSINCOUT}$	MC Sum In to MC Carry Out Delay	—	0.29	—	0.31	—	0.36	ns
$t_{LCINSOUTR}$	MC Carry In to MC Sum Out Delay (Ripple)	—	0.36	—	0.39	—	0.45	ns
$t_{LCINSOUTL}$	MC Carry In to MC Sum Out Delay (Look Ahead)	—	0.26	—	0.28	—	0.32	ns
Feed-thru								
t_{LFT}	PFU Feed-Thru Delay	—	0.15	—	0.16	—	0.18	ns
Distributed RAM								
t_{LRAM_CO}	Clock to RAM Output	—	1.24	—	1.33	—	1.53	ns
t_{LRAMAD_S}	Address Setup Time	-0.41	—	-0.40	—	-0.34	—	ns
t_{LRAMD_S}	Data Setup Time	0.21	—	0.22	—	0.25	—	ns
t_{LRAMWE_S}	Write Enable Setup Time	0.45	—	0.46	—	0.53	—	ns
t_{LRAMAD_H}	Address Hold Time	0.58	—	0.60	—	0.69	—	ns
t_{LRAMD_H}	Data Hold Time	0.11	—	0.11	—	0.13	—	ns
t_{LRAMWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{LRAMCPW}$	Clock Pulse Width (High or Low)	2.91	—	3.00	—	3.45	—	ns
$t_{LRAMADO}$	Address to Output Delay	—	0.86	—	0.93	—	1.07	ns
Register/Latch Delays								
Registers								
t_{L_CO}	Register Clock to Output Delay	—	0.58	—	0.62	—	0.71	ns
t_{L_S}	Register Setup Time (Data before Clock)	0.14	—	0.14	—	0.16	—	ns
t_{L_H}	Register Hold Time (Data after Clock)	-0.12	—	-0.12	—	-0.10	—	ns
t_{LCE_S}	Register Clock Enable Setup Time	-0.11	—	-0.11	—	-0.09	—	ns
t_{LCE_H}	Register Clock Enable Hold Time	0.11	—	0.11	—	0.13	—	ns
Latches								
t_{L_GO}	Latch Gate to Output Delay	—	0.09	—	0.10	—	0.12	ns
t_{LL_S}	Latch Setup Time	0.14	—	0.14	—	0.16	—	ns
t_{LL_H}	Latch Hold Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{LLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns

sysHSI Block Timing

Figure 24 provides a graphical representation of the SERDES receiver input requirements. It provides guidance on a number of input parameters, including signal amplitude and rise time limits, noise and jitter limits, and P and N input skew tolerance.

Figure 24. Receive Data Eye Diagram Template (Differential)



The data pattern eye opening at the receive end of a link is considered the ultimate measure of received signal quality. Almost all detrimental characteristics of a transmit signal and the interconnection link design result in eye closure. This combined with the eye-opening limitations of the line receiver can provide a good indication of a link's ability to transfer error-free data.

Signal jitter is of special interest to system designers. It is often the primary limiting characteristic of long digital links and of systems with high noise level environments. An interesting characteristic of the clock and data recovery (CDR) portion of the ispXPGA SERDES receiver is its ability to filter incoming signal jitter that is below the clock recovery PLL bandwidth. For signals with high levels of low frequency jitter, the receiver can detect incoming data error free, with eye openings significantly less than that shown in Figure 24.

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
R8	BK2_IO19	-	35N	BK2_IO19	-	31N
N8	BK2_IO20	-	36P	BK2_IO20	-	32P
P8	BK2_IO21	-	36N	BK2_IO21	-	32N
-	GND (Bank 2)	-	-	-	-	-
-	GND (Bank 3)	-	-	-	-	-
T8	BK3_IO0	-	39P	BK3_IO0	-	33P
T9	BK3_IO1	-	39N	BK3_IO1	-	33N
R9	BK3_IO2	-	40P	BK3_IO2	-	34P
-	-	-	-	GND (Bank 3)	-	-
R10	BK3_IO3	-	40N	BK3_IO3	-	34N
P9	BK3_IO4	-	41P	BK3_IO4	-	35P
N9	BK3_IO5	-	41N	BK3_IO5	-	35N
T10	BK3_IO6	-	42P	BK3_IO6	-	36P
-	GND (Bank 3)	-	-	-	-	-
T11	BK3_IO7	-	42N	BK3_IO7	-	36N
P10	BK3_IO8	-	43P	BK3_IO8	-	37P
-	-	-	-	GND (Bank 3)	-	-
N10	BK3_IO9	-	43N	BK3_IO9	-	37N
R11	BK3_IO14	-	46P	BK3_IO10	-	38P
-	GND (Bank 3)	-	-	-	-	-
R12	BK3_IO15	-	46N	BK3_IO11	-	38N
P11	BK3_IO16	VREF3	47P	BK3_IO12	VREF3	39P
N11	BK3_IO17	-	47N	BK3_IO13	-	39N
T12	BK3_IO18	-	48P	BK3_IO14	-	40P
T13	BK3_IO19	-	48N	BK3_IO15	-	40N
R13	BK3_IO20	-	49P	BK3_IO16	-	41P
-	-	-	-	GND (Bank 3)	-	-
R14	BK3_IO21	-	49N	BK3_IO17	-	41N
P12	BK3_IO22	-	50P	BK3_IO18	-	42P
-	GND (Bank 3)	-	-	-	-	-
N12	BK3_IO23	-	50N	BK3_IO19	-	42N
T14	GSR	-	-	GSR	-	-
T15	DXP	-	-	DXP	-	-
P13	DXN	-	-	DXN	-	-
P15	BK4_IO0	-	52P/HSI2	BK4_IO0	-	44P
N14	BK4_IO1	-	52N/HSI2	BK4_IO1	-	44N
R16	BK4_IO2	HSI2A_SINP	53P/HSI2	BK4_IO2	-	45P
-	GND (Bank 4)	-	-	-	-	-
P16	BK4_IO3	HSI2A_SINN	53N/HSI2	BK4_IO3	-	45N
N15	BK4_IO4	-	54P/HSI2	BK4_IO4	-	46P
-	-	-	-	GND (Bank 4)	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
-	-	-	-	GND (Bank 0)	-	-	-	-	-
R2	GCLK0	-	LVDS Pair0P	GCLK0	-	LVDS Pair0P	GCLK0	-	LVDS Pair0P
R3	GCLK1	-	LVDS Pair0N	GCLK1	-	LVDS Pair0N	GCLK1	-	LVDS Pair0N
R4	VCCP0	-	-	VCCP0	-	-	VCCP0	-	-
T4	GNDP0	-	-	GNDP0	-	-	GNDP0	-	-
T3	GCLK2	-	LVDS Pair1P	GCLK2	-	LVDS Pair1P	GCLK2	-	LVDS Pair1P
T2	GCLK3	-	LVDS Pair1N	GCLK3	-	LVDS Pair1N	GCLK3	-	LVDS Pair1N
-	-	-	-	GND (Bank 1)	-	-	-	-	-
T1	BK1_IO0	CLK_OUT2	21P	BK1_IO0	CLK_OUT2	13P	BK1_IO0	CLK_OUT2	11P
-	GND (Bank 1)	-	-	-	-	-	-	-	-
U1	BK1_IO1	CLK_OUT3	21N	BK1_IO1	CLK_OUT3	13N	BK1_IO1	CLK_OUT3	11N
U2	BK1_IO2	SS_CLKOUT0P	22P	BK1_IO2	SS_CLKOUT0P	14P	BK1_IO2	SS_CLKOUT0P	12P
-	-	-	-	-	-	-	GND (Bank 1)	-	-
U3	BK1_IO3	SS_CLKOUT0N	22N	BK1_IO3	SS_CLKOUT0N	14N	BK1_IO3	SS_CLKOUT0N	12N
V1	BK1_IO4	PLL_FBK2	23P	BK1_IO4	PLL_FBK2	15P	BK1_IO4	PLL_FBK2	13P
V2	BK1_IO5	PLL_FBK3	23N	BK1_IO5	PLL_FBK3	15N	BK1_IO5	PLL_FBK3	13N
V3	BK1_IO6	-	24P	NC	-	-	NC	-	-
-	GND (Bank 1)	-	-	-	-	-	-	-	-
V4	BK1_IO7	-	24N	NC	-	-	NC	-	-
W1	BK1_IO8	-	25P	NC	-	-	NC	-	-
Y1	BK1_IO9	-	25N	NC	-	-	NC	-	-
W2	BK1_IO10	SS_CLKINOP	26P	BK1_IO6	SS_CLKIN0P	16P	BK1_IO6	SS_CLKIN0P	14P
-	-	-	-	GND (Bank 1)	-	-	-	-	-
W3	BK1_IO11	SS_CLKINON	26N	BK1_IO7	SS_CLKIN0N	16N	BK1_IO7	SS_CLKIN0N	14N
Y2	BK1_IO12		27P	BK1_IO8		17P	BK1_IO8	-	15P
-	-	-	-	-	-	-	GND (Bank 1)	-	-
Y4	BK1_IO13	-	27N	BK1_IO9	-	17N	BK1_IO9	-	15N
Y3	BK1_IO14	-	28P	NC	-	-	NC	-	-
-	GND (Bank 1)	-	-	-	-	-	-	-	-
AA1	BK1_IO15	-	28N	NC	-	-	NC	-	-
AA2	BK1_IO16	-	29P	NC	-	-	NC	-	-
AA3	BK1_IO17	-	29N	NC	-	-	NC	-	-
AB2	BK1_IO18	HSI2A_SOUTP	30P	BK1_IO10	HSI1A_SOUTP	18P/HSI1	BK1_IO10	-	16P
AC2	BK1_IO19	HSI2A_SOUTN	30N	BK1_IO11	HSI1A_SOUTN	18N/HSI1	BK1_IO11	-	16N
AB3	BK1_IO20	PLL_RST2	31P	BK1_IO12	PLL_RST2	19P/HSI1	BK1_IO12	PLL_RST2	17P
AA4	BK1_IO21	PLL_RST3	31N	BK1_IO13	PLL_RST3	19N/HSI1	BK1_IO13	PLL_RST3	17N
AC1	BK1_IO22	HSI2A_SINP	32P	BK1_IO14	HSI1A_SINP	20P/HSI1	NC	-	-
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-	-	-	-
AD1	BK1_IO23	HSI2A_SINN	32N	BK1_IO15	HSI1A_SINN	20N/HSI1	NC	-	-
AE1	BK1_IO24	VREF1	33P/HSI2	BK1_IO16	VREF1	21P/HSI1	BK1_IO14	VREF1	18P
AF1	BK1_IO25		33N/HSI2	BK1_IO17	-	21N/HSI1	BK1_IO15	-	18N
AC3	BK1_IO26	HSI2B_SOUTP	34P/HSI2	BK1_IO18	HSI1B_SOUTP	22P/HSI1	BK1_IO16	-	19P
-	-	-	-	-	-	-	GND (Bank 1)	-	-
AC4	BK1_IO27	HSI2B_SOUTN	34N/HSI2	BK1_IO19	HSI1B_SOUTN	22N/HSI1	BK1_IO17	-	19N
AD2	BK1_IO28	-	35P/HSI2	BK1_IO20	-	23P/HSI1	BK1_IO18	-	20P
AD3	BK1_IO29	-	35N/HSI2	BK1_IO21	-	23N/HSI1	BK1_IO19	-	20N
AE2	BK1_IO30	HSI2B_SINP	36P/HSI2	BK1_IO22	HSI1B_SINP	24P/HSI1	BK1_IO20	-	21P
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-	-	-	-
AF2	BK1_IO31	HSI2B_SINN	36N/HSI2	BK1_IO23	HSI1B_SINN	24N/HSI1	BK1_IO21	-	21N
AD4	BK1_IO32	-	37P/HSI2	NC	-	-	NC	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
D21	BK6_IO20	-	136P	BK6_IO8	-	82P	BK6_IO8	-	70P
C21	BK6_IO21	VREF6	136N	BK6_IO9	VREF6	82N	BK6_IO9	VREF6	70N
B21	BK6_IO22	DATA5	137P	BK6_IO10	DATA5	83P	BK6_IO10	DATA5	71P
-	-	-	-	GND (Bank 6)	-	-	-	-	-
A21	BK6_IO23	DATA4	137N	BK6_IO11	DATA4	83N	BK6_IO11	DATA4	71N
D20	BK6_IO24	-	138P	BK6_IO12	-	84P	BK6_IO12	-	72P
-	-	-	-	-	-	-	GND (Bank 6)	-	-
C20	BK6_IO25	-	138N	BK6_IO13	-	84N	BK6_IO13	-	72N
B20	BK6_IO26	DATA3	139P	BK6_IO14	DATA3	85P	BK6_IO14	DATA3	73P
-	GND (Bank 6)	-	-	-	-	-	-	-	-
A20	BK6_IO27	DATA2	139N	BK6_IO15	DATA2	85N	BK6_IO15	DATA2	73N
C19	BK6_IO28	-	140P	BK6_IO16		86P	BK6_IO16	-	74P
B19	BK6_IO29	-	140N	BK6_IO17		86N	BK6_IO17	-	74N
A19	BK6_IO30	DATA1	141P	BK6_IO18	DATA1	87P	BK6_IO18	DATA1	75P
-	-	-	-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
A18	BK6_IO31	DATA0	141N	BK6_IO19	DATA0	87N	BK6_IO19	DATA0	75N
D18	BK6_IO32	-	142P	BK6_IO20		88P	BK6_IO20	-	76P
C18	BK6_IO33	-	142N	BK6_IO21		88N	BK6_IO21	-	76N
B18	BK6_IO34	-	143P	BK6_IO22		89P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-	-	-	-
C17	BK6_IO35	-	143N	BK6_IO23		89N	NC	-	-
B17	BK6_IO36	-	144P	NC	-	-	NC	-	-
A17	BK6_IO37	-	144N	NC	-	-	NC	-	-
D16	BK6_IO38	-	145P	NC	-	-	NC	-	-
C16	BK6_IO39	-	145N	NC	-	-	NC	-	-
B16	BK6_IO40	-	146P	BK6_IO24	-	90P	NC	-	-
A16	BK6_IO41	-	146N	BK6_IO25	-	90N	NC	-	-
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-	-	-	-
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-	-	-	-
A15	BK7_IO0	-	147P	BK7_IO0	-	91P	BK7_IO0	-	77P
B15	BK7_IO1	-	147N	BK7_IO1	-	91N	BK7_IO1	-	77N
C15	BK7_IO2	-	148P	BK7_IO2	-	92P	BK7_IO2	-	78P
-	-	-	-	-	-	-	GND (Bank 7)	-	-
D15	BK7_IO3	-	148N	BK7_IO3	-	92N	BK7_IO3	-	78N
A14	BK7_IO4	-	149P	BK7_IO4	-	93P	BK7_IO4	-	79P
B14	BK7_IO5	-	149N	BK7_IO5	-	93N	BK7_IO5	-	79N
C14	BK7_IO6	-	150P	BK7_IO6	-	94P	NC	-	-
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-	-	-	-
A13	BK7_IO7	-	150N	BK7_IO7	-	94N	NC	-	-
B13	BK7_IO8	-	151P	BK7_IO8	-	95P	NC	-	-
C13	BK7_IO9	-	151N	BK7_IO9	-	95N	NC	-	-
D13	BK7_IO10	-	152P	BK7_IO10	-	96P	BK7_IO6	-	80P
B12	BK7_IO11	-	152N	BK7_IO11	-	96N	BK7_IO7	-	80N
C12	BK7_IO12	-	153P	BK7_IO12	-	97P	BK7_IO8	-	81P
-	-	-	-	-	-	-	GND (Bank 7)	-	-
A12	BK7_IO13	-	153N	BK7_IO13		97N	BK7_IO9	-	81N
A11	BK7_IO14	-	154P	BK7_IO14	-	98P	BK7_IO10	-	82P
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-	-	-	-
B11	BK7_IO15	-	154N	BK7_IO15	-	98N	BK7_IO11	-	82N
C11	BK7_IO16	-	155P	NC	-	-	NC	-	-
D11	BK7_IO17	-	155N	NC	-	-	NC	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
A10	BK7_IO18	-	156P	NC	-	-	NC	-	-
B10	BK7_IO19	-	156N	NC	-	-	NC	-	-
C10	BK7_IO20	VREF7	157P	BK7_IO16	VREF7	99P	BK7_IO12	VREF7	83P
D10	BK7_IO21	-	157N	BK7_IO17	-	99N	BK7_IO13	-	83N
B9	BK7_IO22	-	158P	BK7_IO18	-	100P	BK7_IO14	-	84P
-	GND (Bank 7)	-	-	-	-	-	-	-	-
C9	BK7_IO23	-	158N	BK7_IO19	-	100N	BK7_IO15	-	84N
A8	BK7_IO24	-	159P	BK7_IO20	-	101P	BK7_IO16	-	85P
-	-	-	-	-	-	-	GND (Bank 7)	-	-
B8	BK7_IO25	-	159N	BK7_IO21	-	101N	BK7_IO17	-	85N
C8	BK7_IO26	-	160P	NC	-	-	NC	-	-
D8	BK7_IO27	-	160N	NC	-	-	NC	-	-
A7	BK7_IO28	-	161P	NC	-	-	NC	-	-
B7	BK7_IO29	-	161N	NC	-	-	NC	-	-
C7	BK7_IO30	-	162P	NC	-	-	NC	-	-
-	GND (Bank 7)	-	-	-	-	-	-	-	-
D7	BK7_IO31	-	162N	NC	-	-	NC	-	-
A6	BK7_IO32	-	163P	NC	-	-	NC	-	-
B6	BK7_IO33	-	163N	NC	-	-	NC	-	-
B5	BK7_IO34	-	164P	NC	-	-	NC	-	-
C6	BK7_IO35	-	164N	NC	-	-	NC	-	-
A5	BK7_IO36	-	165P	NC	-	-	NC	-	-
A4	BK7_IO37	-	165N	NC	-	-	NC	-	-
B4	BK7_IO38	-	166P	BK7_IO22	-	102P	BK7_IO18	-	86P
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-	-	-	-
C5	BK7_IO39	-	166N	BK7_IO23	-	102N	BK7_IO19	-	86N
A3	BK7_IO40	-	167P	BK7_IO24	-	103P	BK7_IO20	-	87P
A2	BK7_IO41	-	167N	BK7_IO25	-	103N	BK7_IO21	-	87N
D5	TDO	-	-	TDO	-	-	TDO	-	-
C4	VCCJ	-	-	VCCJ	-	-	VCCJ	-	-
B3	TDI	-	-	TDI	-	-	TDI	-	-

1. If a sysHSI Block is used, the indicated sysHSI reserved pins are unavailable for general purpose I/O use.

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
AH39	BK3_IO31	-	108N
AK39	BK3_IO32	-	109P
AK38	BK3_IO33	-	109N
AF35	BK3_IO34	-	110P
-	GND (Bank 3)	-	-
AJ37	BK3_IO35	-	110N
AH36	BK3_IO36	-	111P
AM39	BK3_IO37	-	111N
AL38	BK3_IO38	-	112P
AL39	BK3_IO39	-	112N
AJ36	BK3_IO40	-	113P
AH35	BK3_IO41	-	113N
AL37	BK3_IO42	-	114P
-	GND (Bank 3)	-	-
AN38	BK3_IO43	-	114N
AM38	BK3_IO44	-	115P
AK36	BK3_IO45	-	115N
AM37	BK3_IO46	-	116P
AN37	BK3_IO47	-	116N
AN39	BK3_IO48	-	117P
AL36	BK3_IO49	VREF3	117N
AK35	BK3_IO50	-	118P
-	GND (Bank 3)	-	-
AP39	BK3_IO51	-	118N
AM36	BK3_IO52	-	119P
AP38	BK3_IO53	-	119N
AR39	BK3_IO54	-	120P
AN36	BK3_IO55	-	120N
AM35	BK3_IO56	-	121P
AR38	BK3_IO57	-	121N
AP37	BK3_IO58	-	122P
-	GND (Bank 3)	-	-
AT39	BK3_IO59	-	122N
AR37	BK3_IO60	-	123P
AP36	BK3_IO61	-	123N
AT38	GSR	-	-
AP35	DXP	-	-
AT37	DXN	-	-
AU36	BK4_IO0	-	124P
AV36	BK4_IO1	-	124N
AR34	BK4_IO2	-	125P
-	GND (Bank 4)	-	-
AW36	BK4_IO3	-	125N

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
K30	BK5_IO22	HSI7B_SOUTP	166P/HSI8	BK5_IO22	HSI4B_SOUTP	116P/HSI4
-	-	-	-	GND (Bank 5)	-	-
K29	BK5_IO23	HSI7B_SOUTN	166N/HSI8	BK5_IO23	HSI4B_SOUTN	116N/HSI4
L28	BK5_IO24	-	167P/HSI8	BK5_IO24	-	117P/HSI5
L27	BK5_IO25	-	167N/HSI8	BK5_IO25	-	117N/HSI5
L26	BK5_IO26	HSI8A_SINP	168P/HSI8	BK5_IO26	HSI5A_SINP	118P/HSI5
-	GND (Bank 5)	-	-	-	-	-
L25	BK5_IO27	HSI8A_SINN	168N/HSI8	BK5_IO27	HSI5A_SINN	118N/HSI5
K27	BK5_IO28	-	169P/HSI8	BK5_IO28	-	119P/HSI5
K26	BK5_IO29	-	169N/HSI8	BK5_IO29	-	119N/HSI5
J30	BK5_IO30	HSI8A_SOUTP	170P/HSI8	BK5_IO30	HSI5A_SOUTP	120P/HSI5
-	-	-	-	GND (Bank 5)	-	-
J29	BK5_IO31	HSI8A_SOUTN	170N/HSI8	BK5_IO31	HSI5A_SOUTN	120N/HSI5
J26	BK5_IO32	-	171P/HSI8	NC	-	-
J27	BK5_IO33	-	171N/HSI8	NC	-	-
H30	BK5_IO34	HSI8B_SINP	172P/HSI8	NC	-	-
-	GND (Bank 5)	-	-	-	-	-
H29	BK5_IO35	HSI8B_SINN	172N/HSI8	NC	-	-
J25	BK5_IO36	-	173P/HSI9	NC	-	-
J24	BK5_IO37	-	173N/HSI9	NC	-	-
G30	BK5_IO38	HSI8B_SOUTP	174P/HSI9	NC	-	-
G29	BK5_IO39	HSI8B_SOUTN	174N/HSI9	NC	-	-
H27	BK5_IO40	-	175P/HSI9	NC	-	-
H28	BK5_IO41	-	175N/HSI9	NC	-	-
F30	BK5_IO42	HSI9A_SINP	176P/HSI9	NC	-	-
-	GND (Bank 5)	-	-	-	-	-
F29	BK5_IO43	HSI9A_SINN	176N/HSI9	NC	-	-
G27	BK5_IO44	-	177P/HSI9	NC	-	-
G28	BK5_IO45	-	177N/HSI9	NC	-	-
E30	BK5_IO46	HSI9A_SOUTP	178P/HSI9	NC	-	-
E29	BK5_IO47	HSI9A_SOUTN	178N/HSI9	NC	-	-
H26	BK5_IO48	-	179P/HSI9	BK5_IO33	-	121N/HSI5
H25	BK5_IO49	VREF5	179N/HSI9	BK5_IO32	VREF5	121P/HSI5
D30	BK5_IO50	HSI9B_SINP	180P/HSI9	BK5_IO34	HSI5B_SINP	122P/HSI5
-	GND (Bank 5)	-	-	-	-	-
D29	BK5_IO51	HSI9B_SINN	180N/HSI9	BK5_IO35	HSI5B_SINN	122N/HSI5
F28	BK5_IO52	-	181P	BK5_IO36	-	123P/HSI5
F27	BK5_IO53	-	181N	BK5_IO37	-	123N/HSI5
C30	BK5_IO54	HSI9B_SOUTP	182P	BK5_IO38	HSI5B_SOUTP	124P/HSI5
-	-	-	-	GND (Bank 5)	-	-
C29	BK5_IO55	HSI9B_SOUTN	182N	BK5_IO39	HSI5B_SOUTN	124N/HSI5
G26	BK5_IO56	-	183P	NC	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

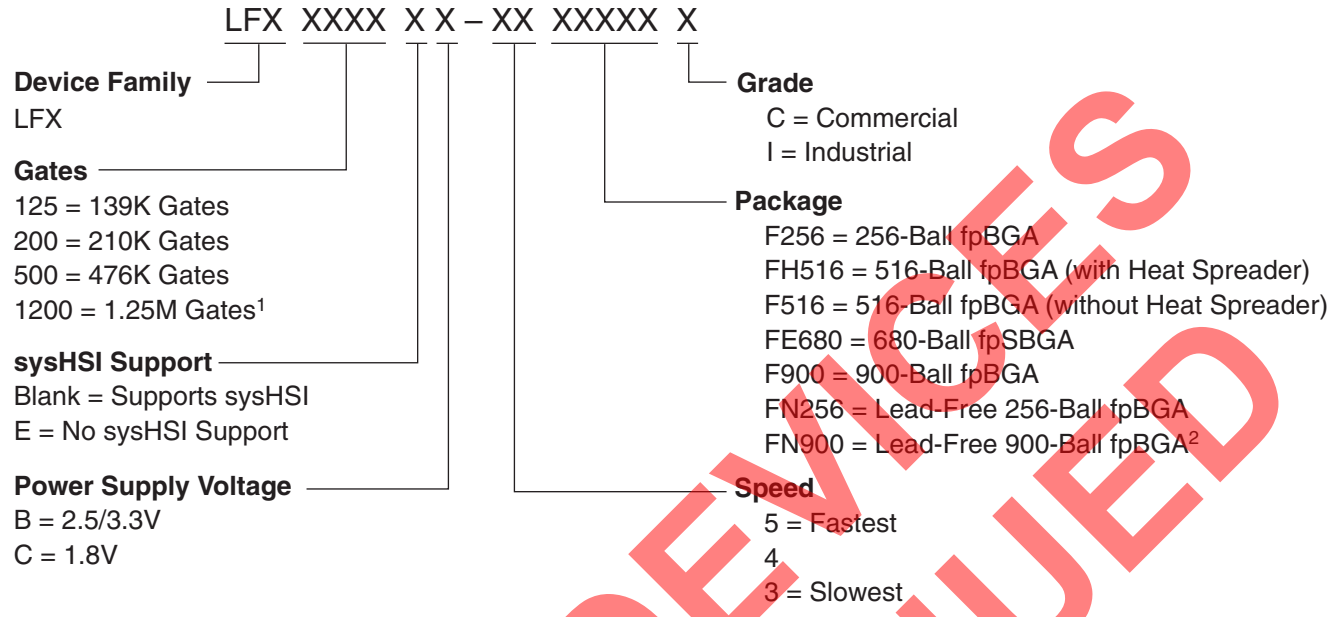
900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
D21	BK6_IO29	-	200N	NC	-	-
A21	BK6_IO30	-	201P	NC	-	-
B21	BK6_IO31	-	201N	NC	-	-
F20	BK6_IO32	DATA7	202P	BK6_IO18	DATA7	135P
-	-	-	-	GND (Bank 6)	-	-
E20	BK6_IO33	DATA6	202N	BK6_IO19	DATA6	135N
D20	BK6_IO34	-	203P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-
C20	BK6_IO35		203N	NC	-	-
F19	BK6_IO36	DATA5	204P	BK6_IO22	DATA5	137P
E19	BK6_IO37	DATA4	204N	BK6_IO23	DATA4	137N
B20	BK6_IO38	-	205P	NC	-	-
A20	BK6_IO39	-	205N	NC	-	-
D19	BK6_IO40	-	206P	NC	-	-
C19	BK6_IO41	-	206N	NC	-	-
A19	BK6_IO42	-	207P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-
B19	BK6_IO43	-	207N	NC	-	-
G18	BK6_IO44	-	208P	BK6_IO24	-	138P
F18	BK6_IO45	-	208N	BK6_IO25	-	138N
A18	BK6_IO46	-	209P	BK6_IO32	-	142P
B18	BK6_IO47	-	209N	BK6_IO33	-	142N
D18	BK6_IO48	-	210P	BK6_IO34	-	143P
-	-	-	-	GND (Bank 6)	-	-
C18	BK6_IO49	-	210N	BK6_IO35	-	143N
F17	BK6_IO50	DATA3	211P	BK6_IO26	DATA3	139P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
E17	BK6_IO51	DATA2	211N	BK6_IO27	DATA2	139N
D17	BK6_IO52	-	212P	BK6_IO28	-	140P
C17	BK6_IO53	-	212N	BK6_IO29	-	140N
B17	BK6_IO54	DATA1	213P	BK6_IO30	DATA1	141P
A17	BK6_IO55	DATA0	213N	BK6_IO31	DATA0	141N
F16	BK6_IO56	-	214P	BK6_IO36	-	144P
E16	BK6_IO57	-	214N	BK6_IO37	-	144N
D16	BK6_IO58	-	215P	BK6_IO38	-	145P
-	GND (Bank 6)	-	-	-	-	-
C16	BK6_IO59	-	215N	BK6_IO39	-	145N
B16	BK6_IO60	-	216P	BK6_IO40	-	146P
A16	BK6_IO61	-	216N	BK6_IO41	-	146N
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-
A15	BK7_IO0	-	217P	BK7_IO0	-	147P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
F10	BK7_IO36	-	235P	NC	-	-
G10	BK7_IO37	-	235N	NC	-	-
A8	BK7_IO38	-	236P	NC	-	-
B8	BK7_IO39	-	236N	NC	-	-
D9	BK7_IO40	-	237P	BK7_IO22	-	158P
-	-	-	-	GND (Bank 7)	-	-
E9	BK7_IO41	-	237N	BK7_IO23	-	158N
A7	BK7_IO42	-	238P	BK7_IO24	-	159P
-	GND (Bank 7)	-	-		-	-
B7	BK7_IO43	-	238N	BK7_IO25	-	159N
C8	BK7_IO44	-	239P	BK7_IO26	-	160P
D8	BK7_IO45	-	239N	BK7_IO27	-	160N
A6	BK7_IO46	-	240P	BK7_IO21	-	157N
B6	BK7_IO47	VREF7	240N	BK7_IO20	VREF7	157P
E8	BK7_IO48	-	241P	BK7_IO28	-	161P
F8	BK7_IO49	-	241N	BK7_IO29	-	161N
C7	BK7_IO50	-	242P	BK7_IO30	-	162P
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-
D7	BK7_IO51	-	242N	BK7_IO31	-	162N
E7	BK7_IO52	-	243P	BK7_IO32	-	163P
F7	BK7_IO53	-	243N	BK7_IO33	-	163N
A5	BK7_IO54	-	244P	BK7_IO34	-	164P
B5	BK7_IO55	-	244N	BK7_IO35	-	164N
C6	BK7_IO56	-	245P	BK7_IO36	-	165P
D6	BK7_IO57	-	245N	BK7_IO37	-	165N
D5	BK7_IO58	-	246P	BK7_IO38	-	166P
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-
C5	BK7_IO59	-	246N	BK7_IO39	-	166N
B4	BK7_IO60	-	247P	BK7_IO40	-	167P
A4	BK7_IO61	-	247N	BK7_IO41	-	167N
A3	TDO	-	-	TDO	-	-
B3	VCCJ	-	-	VCCJ	-	-
C4	TDI	-	-	TDI	-	-

1. If a sysHSI Block is used, the indicated sysHSI reserved pins are unavailable for general purpose I/O use.

Part Number Description



1. Discontinued via PCN #03A-10.
2. Select products only. See Ordering Information tables below for specific support.

Ordering Information

Conventional Packaging

Commercial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125B-05F256C	139K	2.5/3.3	-5	fpBGA	256
LFX125B-04F256C	139K	2.5/3.3	-4	fpBGA	256
LFX125B-03F256C	139K	2.5/3.3	-3	fpBGA	256
LFX125C-04F256C	139K	1.8	-4	fpBGA	256
LFX125C-03F256C	139K	1.8	-3	fpBGA	256
LFX125B-05F516C	139K	2.5/3.3	-5	fpBGA	516
LFX125B-04F516C	139K	2.5/3.3	-4	fpBGA	516
LFX125B-03F516C	139K	2.5/3.3	-3	fpBGA	516
LFX125C-04F516C	139K	1.8	-4	fpBGA	516
LFX125C-03F516C	139K	1.8	-3	fpBGA	516
LFX125B-05FH516C[1]	139K	2.5/3.3	-5	fpBGA	516
LFX125B-04FH516C[1]	139K	2.5/3.3	-4	fpBGA	516
LFX125B-03FH516C[1]	139K	2.5/3.3	-3	fpBGA	516
LFX125C-04FH516C[1]	139K	1.8	-4	fpBGA	516
LFX125C-03FH516C[1]	139K	1.8	-3	fpBGA	516
LFX200B-05F256C	210K	2.5/3.3	-5	fpBGA	256
LFX200B-04F256C	210K	2.5/3.3	-4	fpBGA	256
LFX200B-03F256C	210K	2.5/3.3	-3	fpBGA	256
LFX200C-04F256C	210K	1.8	-4	fpBGA	256
LFX200C-03F256C	210K	1.8	-3	fpBGA	256