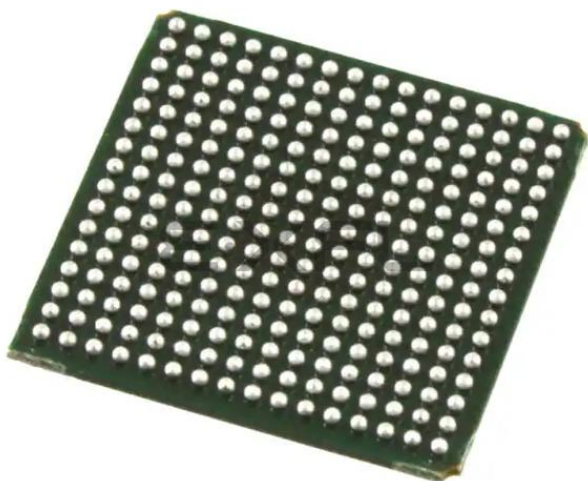




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

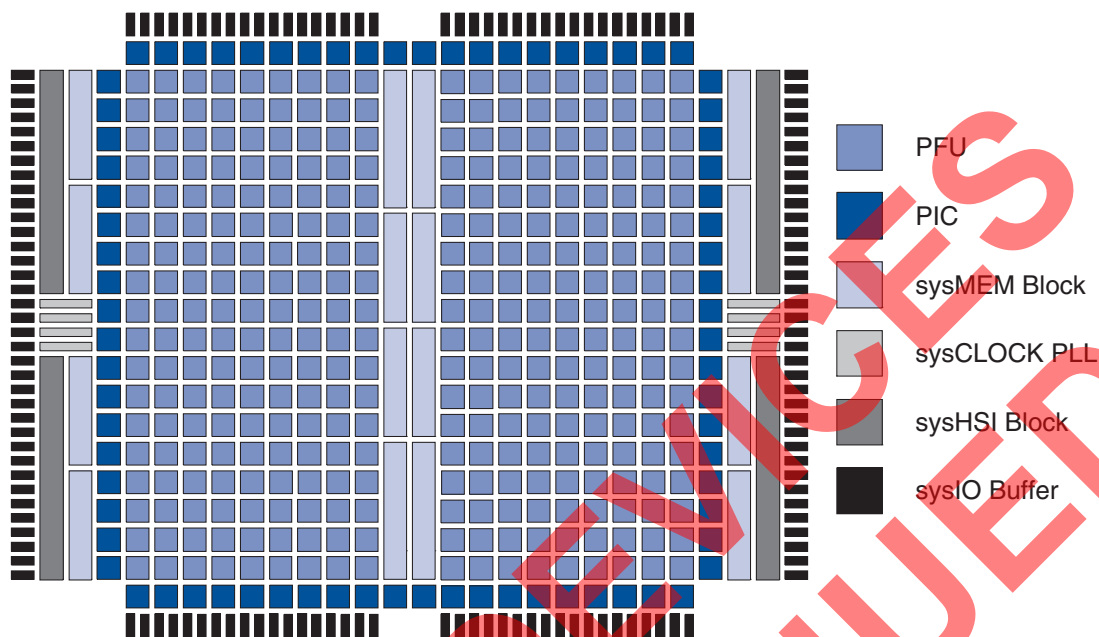
Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1936
Total RAM Bits	94208
Number of I/O	160
Number of Gates	139000
Voltage - Supply	2.3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx125eb-04fn256c



Product Line	Ordering Part Number	Product Status	Reference PCN
LFX125EC (Cont'd)	LFX125EC-03F516C	Discontinued	<u>PCN#09-10</u>
	LFX125EC-04F516C		
	LFX125EC-03F516I		
LFX200EB	LFX200EB-03F256C	Active / Orderable	
	LFX200EB-03FN256C		
	LFX200EB-04F256C		
	LFX200EB-04FN256C		
	LFX200EB-05F256C		
	LFX200EB-05FN256C		
	LFX200EB-03F256I		
	LFX200EB-03FN256I		
	LFX200EB-04F256I	Discontinued	<u>PCN#09-10</u>
	LFX200EB-04FN256I		
	LFX200EB-03F516C		
	LFX200EB-04F516C		
	LFX200EB-05F516C		
	LFX200EB-03F516I		
	LFX200EB-04F516I		
LFX200EC	LFX200EC-03F256C	Discontinued	<u>PCN#09-10</u>
	LFX200EC-03FN256C		
	LFX200EC-04F256C		
	LFX200EC-04FN256C		
	LFX200EC-03F256I		
	LFX200EC-03FN256I		
	LFX200EC-03F516C		
	LFX200EC-04F516C		
	LFX200EC-03F516I		
LFX500EB	LFX500EB-03F516C	Discontinued	<u>PCN#09-10</u>
	LFX500EB-04F516C		
	LFX500EB-05F516C		
	LFX500EB-03F516I		
	LFX500EB-04F516I		
	LFX500EB-03F900C		
	LFX500EB-03FN900C		
	LFX500EB-04F900C		
	LFX500EB-04FN900C		
	LFX500EB-05F900C		
	LFX500EB-05FN900C		
	LFX500EB-03F900I		
	LFX500EB-03FN900I		
	LFX500EB-04F900I		
	LFX500EB-04FN900I		
LFX500EC	LFX500EC-03F516C	Discontinued	<u>PCN#09-10</u>
	LFX500EC-04F516C		
	LFX500EC-03F516I		

Figure 1. ispXPGA Block Diagram



Programmable Function Unit

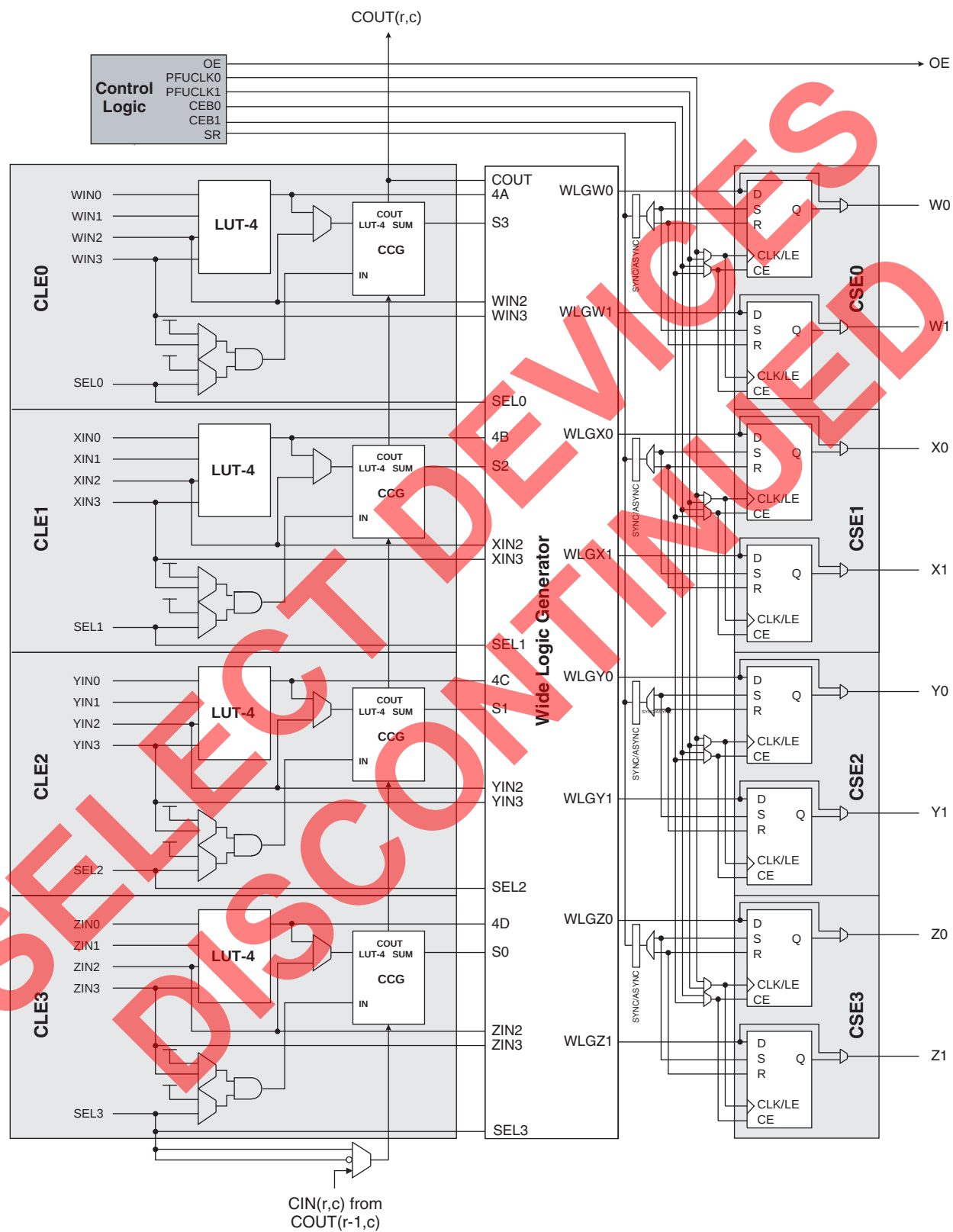
The Programmable Function Unit (PFU) is the basic building block of the ispXPGA architecture. The PFUs are arranged in rows and columns in the device with PFU (1,1) referring to (row 1, column 1). Each PFU consists of four Configurable Logic Elements (CLEs), four Configurable Sequential Elements (CSEs), and a Wide Logic Generator (WLG). By utilizing these components, the PFU can implement a variety of functions. Table 3 lists some of the function capabilities of the PFU.

There are 57 inputs to each PFU and nine outputs. The PFU uses 20 inputs for logic, and 37 inputs drive the control logic from which six control signals are derived for the PFU.

Table 3. Function Capability of ispXPGA PFU

Function	Capability
Look-up table	LUT-4, LUT-5, LUT-6
Wide logic functions	Up to 20 input logic functions
Multiplexing	2:1, 4:1, 8:1
Arithmetic logic	Dedicated carry chain and booth multiplication logic
Single-port RAM	16X1, 16X2, 16X4, 32X1, 32X2, 64X1
Double-port RAM	16X1, 16X2, 32X1
Shift register	8-bit shift registers (up to 32-bit shift capability)

Figure 2. ispXPGA PFU



sysCLOCK PLL Description

The sysCLOCK PLL circuitry consists of Phase-Lock Loops (PLLs) and the various dividers, reset, and feedback signals associated with the PLLs. This feature gives the user the ability to synthesize clock frequencies and generate multiple clock signals for routing within the device. Furthermore, it can generate clock signals that are aligned either at the board level or the device level.

The ispXPGA devices provide up to eight PLLs. Each PLL receives its input clock from its associated global clock pin, and its output is routed to the associated global clock net. For example, PLL0 receives its clock input from the GCLK0 global clock pin and provides output to the CLK0 global clock net. The PLL also has the ability to output a secondary clock that is a division of the primary clock output. When using the secondary clock, the secondary clock will be routed to the neighboring global clock net. For example, PLL0 will drive its primary clock output on the CLK0 global clock net and its secondary clock output will drive the CLK1 global clock net. Additionally, each PLL has a set of PLL_RST, PLL_FBK, and PLL_LOCK signals. The PLL_RST signal can be generated through routing or a dedicated dual-function I/O pin. The PLL_FBK signal can be generated through a dedicated dual-function I/O pin or internally from the Global Clock net associated with the PLL. The PLL_LOCK signal feeds routing directly from the sysCLOCK PLL circuit. Figure 17 illustrates how the PLL_RST and PLL_FBK signals are generated.

Each PLL has four dividers associated with it, M, N, V, and K. The M divider is used to divide the clock signal, while the N divider is used to multiply the clock signal. The V divider allows the VCO frequency to operate at higher frequencies than the clock output, thereby increasing the frequency range. The K divider is only used when a secondary clock output is needed. This divider divides the primary clock output and feeds to the adjacent global clock net. Different combinations of these dividers allow the user to synthesize clock frequencies. Figure 16 shows the ispXPGA PLL block diagram.

The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. This operates by inserting delay on the input or feedback lines of the PLL. For more information on the PLL, please refer to TN1003, [sysCLOCK PLL Usage and Design Guidelines](#).

Figure 16. ispXPGA PLL Block Diagram

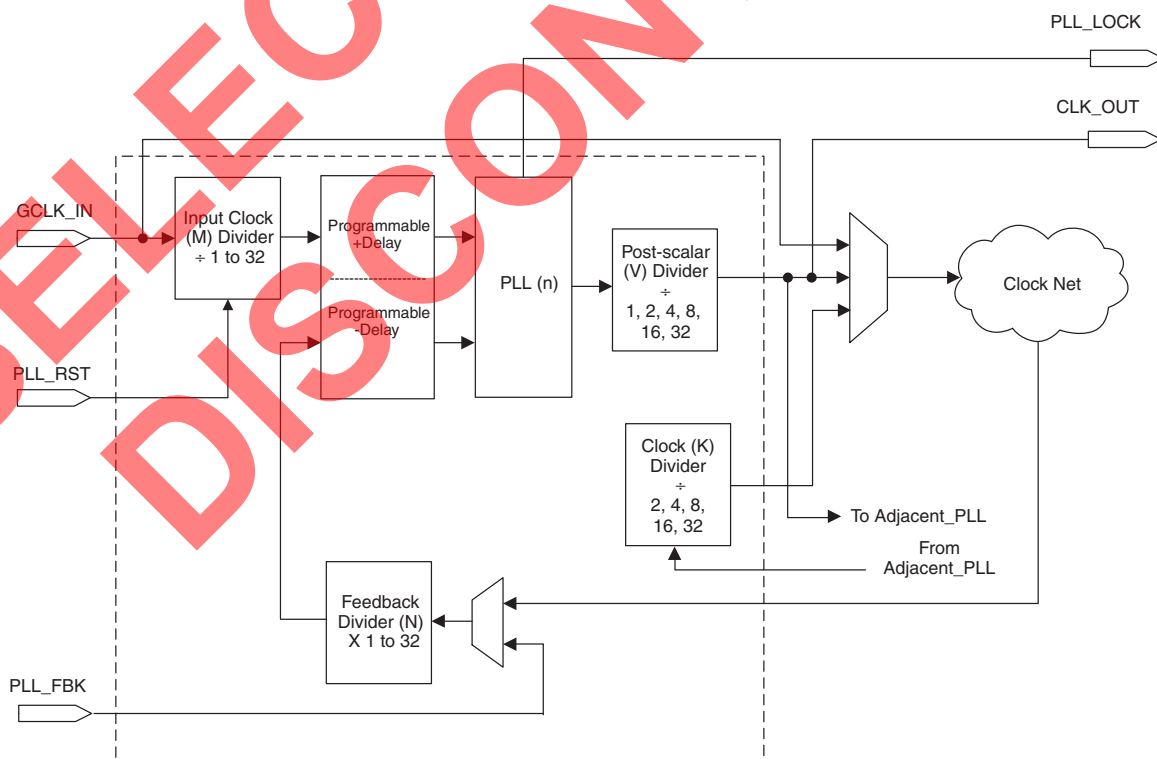
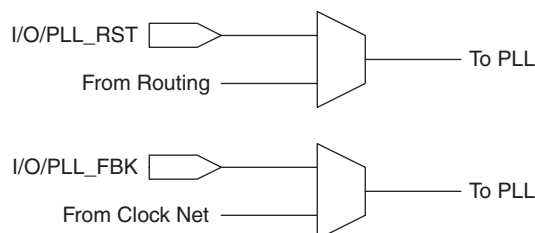
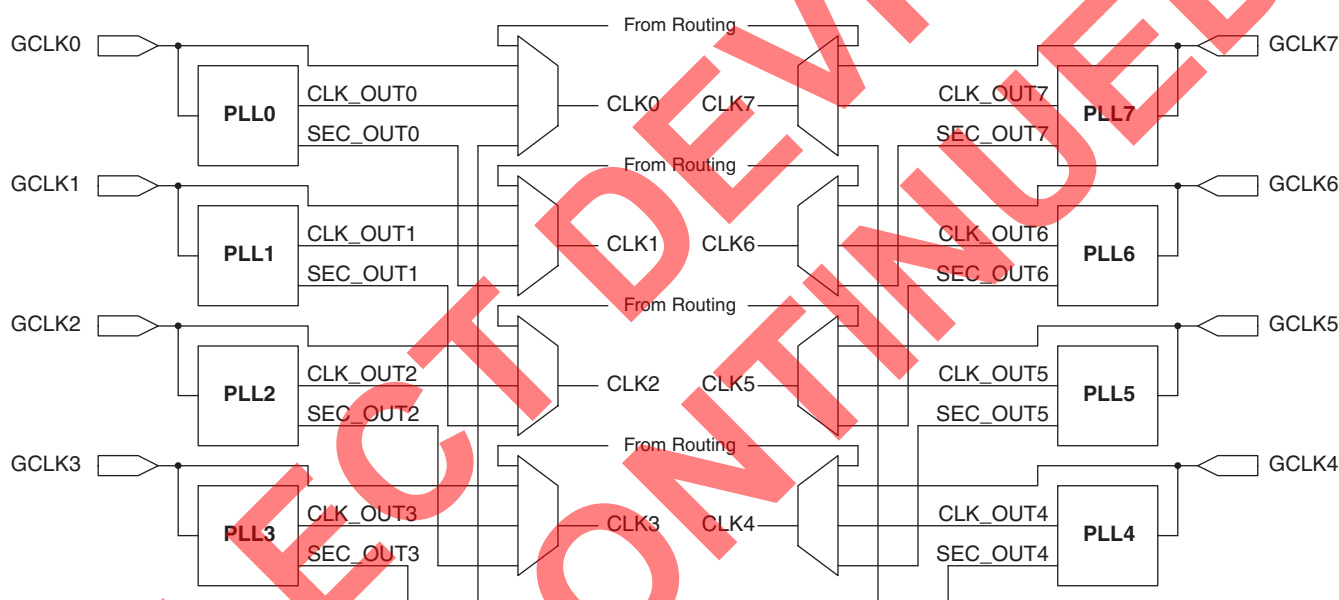


Figure 17. ispXPGA PLL_RST and PLL_FBK Generation

Clock Routing

The Global Clock Lines (GCLK) have two sources, their dedicated pins and the sysCLOCK circuit. Figure 18 illustrates the generation of the Global Clock Lines.

Figure 18. Global Clock Line Generation

sysIO Capability

All the ispXPGA devices have eight sysIO banks, where each bank is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage (V_{CCO}) and reference voltage (V_{REF}) resources allowing each bank complete independence from the others. Each I/O is individually configurable based on the bank's V_{CCO} and V_{REF} settings. In addition, each I/O has configurable drive strength, weak pull-up, weak pull-down, or a bus-keeper latch. Table 4 lists the number of I/Os supported per bank in each of the ispXPGA devices. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to V_{CCO} of 3.0V to 3.6V for LVCMOS 3.3, LVTTL and PCI interfaces.

Table 5 lists the sysIO standards with the typical values for V_{CCO} , V_{REF} and V_{TT} .

The TOE, JTAG TAP pins, PROGRAM, CFG0 and DONE pins of the ispXPGA device are the only pins that do not have the sysIO capabilities. The TOE and CFG0 pins operate off the V_{CC} of the device, supporting only the LVCMOS standard corresponding to the device supply voltage. The TAP pins have a separate supply voltage (V_{CCJ}), which determines the LVCMOS standard corresponding to that supply voltage.

There are three classes of I/O interface standards that are implemented in the ispXPGA devices. The first is the un-terminated, single-ended interface. It includes the 3.3V LVTTL standard along with the 1.8V, 2.5V, and 3.3V LVCMOS interface standards. Additionally, PCI and AGP-1X are subsets of this type of interface.

The second type of interface implemented is the terminated, single-ended interface standard. This group of interfaces includes different versions of SSTL and HSTL interfaces along with CTT, and GTL+. Usage of these particular I/O interfaces requires an additional V_{REF} signal. At the system level a termination voltage, V_{TT} , is also required. Typically an output will be terminated to V_{TT} at the receiving end of the transmission line it is driving.

The third type of interface standards are the differential standards LVDS, BLVDS, and LVPECL. The differential standards require two I/O pins to create the differential pair. The logic level is determined by the difference in the two signals. Table 6 lists how these interface standards are implemented in the ispXPGA devices.

For more information on sysIO capability, refer to TN1000, [sysIO Usage Guidelines for Lattice Devices](#).

Figure 19. sysIO Banks per Device

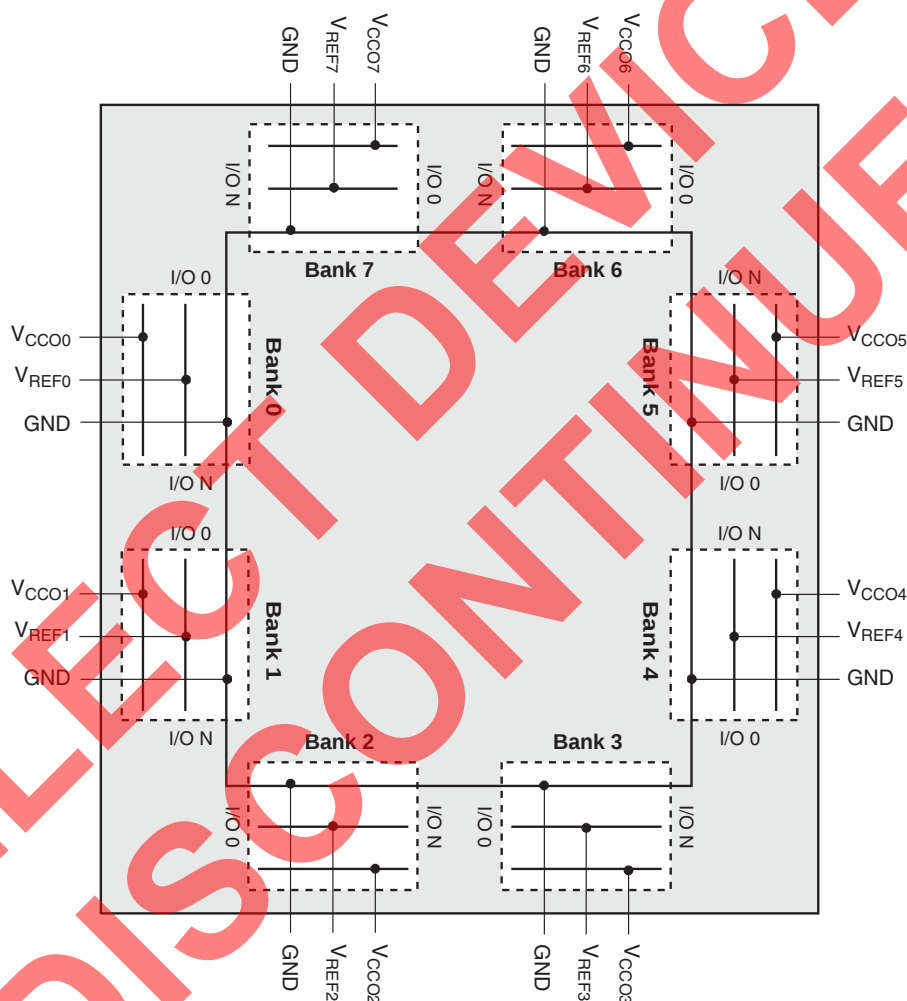


Table 4. Number of I/Os per Bank

Device	Max. Number of I/Os per Bank (N)
XPGA 1200	62
XPGA 500	42
XPGA 200	26
XPGA 125	22

Absolute Maximum Ratings^{1, 2, 3}

	1.8V	2.5V/3.3V
Supply Voltage (V_{CC})	-0.5 to 2.5V	-0.5 to 5.5V
PLL Supply Voltage (V_{CCP})	-0.5 to 2.5V	-0.5 to 5.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V
IEEE 1149.1 TAP Supply Voltage (V_{CCJ})	-0.5 to 4.5V	-0.5 to 4.5V
Input Voltage Applied ^{4, 5}	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C
Junction Temperature (T_J) with Power Applied	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied (while programming, following the programming specifications).
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to (V_{IH} (MAX) + 2) volts not to exceed 6V is permitted for a duration of <20ns.
5. A maximum of 64 I/Os per device with $V_{IN} > 3.6V$ is allowed.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage for 1.8V device ¹	1.65	1.95	V
	Supply Voltage for 2.5V device	2.3	2.7	V
	Supply Voltage for 3.3V device	3.0	3.6	V
V_{CCP}	Supply Voltage for PLL and sysHSI blocks, 1.8V devices ¹	1.65	1.95	V
	Supply Voltage for PLL and sysHSI blocks, 2.5V devices	2.3	2.7	V
	Supply Voltage for PLL and sysHSI blocks, 3.3V devices	3.0	3.6	V
V_{CCJ}	Supply Voltage for IEEE 1149.1 Test Access Port for LVCMOS 1.8V	1.65	1.95	V
	Supply Voltage for IEEE 1149.1 Test Access Port for LVCMOS 2.5V	2.3	2.7	V
	Supply Voltage for IEEE 1149.1 Test Access Port for LVCMOS 3.3V	3.0	3.6	V
T_J (COM)	Junction Temperature Commercial Operation	0	85	C
T_J (IND)	Junction Temperature Industrial Operation	-40	105	C

¹ sysHSI specification is valid for V_{CC} and $V_{CCP} = 1.7V$ to 1.9V.

E²CMOS Erase Reprogram Specifications

Parameter	Min	Max	Units
Erase/Reprogram Cycle ¹	1,000	—	Cycles

¹ Valid over commercial temperature range.

Hot Socketing Characteristics^{1, 2, 3, 4}

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DK}	Input or Tristated I/O Leakage Current	0 δ $V_{IN} \delta$ 3.0V	—	+/-50	+/-800	μA

1. Insensitive to sequence of V_{CC} and V_{CCO} when $V_{CCO} \delta$ 1.0V. For $V_{CCO} > 1.0V$, V_{CC} min must be present. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO} , provided ($V_{IN} - V_{CCO}$) δ 3.6V.
2. LVTTTL, LVCMOS only.
3. 0 < $V_{CC} \delta$ V_{CC} (MAX), 0 < $V_{CCO} \delta$ V_{CCO} (MAX).
4. I_{DK} is additive to I_{PU} , I_{PD} or I_{BH} . Device defaults to pull-up until non-volatile cells are active.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{IL}, I_{IH}^1	Input or I/O Low Leakage	$0 \leq V_{IN} < (V_{CCO} - 0.2V)$	—	—	10	μA
		$(V_{CCO} - 0.2V) \leq V_{IN} \leq 3.6V$	—	—	300	μA
I_{IH}^2	Input High Leakage Current	$3.6V < V_{IN} \leq 5.5V$ and $3.0V \leq V_{CCO} \leq 3.6V$	—	—	3	mA
I_{PU}	I/O Active Pull-up Current	$0 \leq V_{IN} \leq 0.7 V_{CCO}$	-30	—	-150	μA
I_{PD}	I/O Active Pull-down Current	$V_{IL} (MAX) \leq V_{IN} \leq V_{IH} (MAX)$	30	—	150	μA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL} (MAX)$	30	—	—	μA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7 V_{CCO}$	-30	—	—	μA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \leq V_{IN} \leq V_{IH} (MAX)$	—	—	150	μA
I_{BHHO}	Bus Hold High Overdrive Current	$0 \leq V_{IN} \leq V_{IH} (MAX)$	—	—	-150	μA
V_{BHT}	Bus Hold Trip Points		$V_{CCO} * 0.35$	—	$V_{CCO} * 0.65$	V
C_1	I/O Capacitance ³	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	8	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—		—	
C_2	Clock Capacitance ³	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	8	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—		—	
C_3	Global Input Capacitance ³	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	6	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. 5V tolerant inputs and I/Os should be placed in banks where $3.0V \leq V_{CCO} \leq 3.6V$. The JTAG and sysCONFIG ports are not included for the 5V tolerant interface.
3. $T_A = 25^\circ C$, $f = 1.0MHz$.

sysIO DC Electrical Characteristics

Over Recommended Operating Conditions

Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	5.5	0.4	$V_{CCO} - 0.4$	20, 16, 12, 8, 5.33, 4	-20, -16, -12, -8, -5.33, -4
					0.2	$V_{CCO} - 0.2$	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	$V_{CCO} - 0.4$	16, 12, 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	$V_{CCO} - 0.2$	0.1	-0.1
LVCMOS 1.8 ¹	-0.3	0.68 ³	1.07 ³	3.6	0.4	$V_{CCO} - 0.4$	12, 8 ¹ , 5.33, 4	-12, -8 ¹ , -5.33, -4
		0.35 V_{CC}	0.65 V_{CC}		0.2	$V_{CCO} - 0.2$	0.1	-0.1
LVTTTL	-0.3	0.8	2.0	5.5	0.4	$V_{CCO} - 0.4$	4	-4
					0.2	$V_{CCO} - 0.2$	0.1	-0.1
PCI 3.3	-0.3	1.08 ³	1.5 ³	5.5	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
		0.3 V_{CCO}	0.5 V_{CCO}					
AGP-1X	-0.3	1.08 ³	1.5 ³	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
		0.3 V_{CCO}	0.5 V_{CCO}					
SSTL 3 Class I	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.7	$V_{CCO} - 1.1$	8	-8
SSTL 3 Class II	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.5	$V_{CCO} - 0.9$	16	-16
SSTL 2 Class I	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.54	$V_{CCO} - 0.62$	7.6	-7.6
SSTL 2 Class II	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.35	$V_{CCO} - 0.43$	15.2	-15.2
CTT 3.3	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.4$	$V_{REF} + 0.4$	8	-8
CTT 2.5	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.4$	$V_{REF} + 0.4$	8	-8
HSTL Class I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	8	-8
HSTL Class III	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	24	-8
GTL+	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.6	N/A	36	N/A

1. Design tool default setting.
2. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed $n \cdot 8\text{mA}$. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.
3. Applicable for ispXPGA B devices.

sysIO Differential Standards DC Electrical Characteristics¹

Parameter	Description	Test Conditions	Min.	Typ.	Max.
LVDS²					
V_{INP}, V_{INM}	Input voltage		0V	—	2.4V
V_{THD}	Differential input threshold	$0.2V \pm V_{CM} \pm 1.8V$	+/-100mV	—	—
I_{IN}	Input current	Power on	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	$R_T = 100 \text{ Ohm}$	—	1.38V	1.60V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	$R_T = 100 \text{ Ohm}$	0.9V	1.03V	—
V_{OD}	Output Voltage Differential	$ V_{OP} - V_{OM} , R_T = 100 \text{ ohm}$	250mV	350mV	450mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50mV
V_{OS}	Output Voltage Offset	$ V_{OP} + V_{OM} /2, R_T = 100 \text{ ohm}$	1.125V	1.25V	1.375V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50mV
I_{OSD}	Output short circuit current	$V_{OD} = 0V$ Driver outputs shorted	—	—	24mA
BLVDS¹					
V_{INP}, V_{INM}	Input voltage		0V	—	2.4V
V_{THD}	Differential input threshold	$0.2V \pm V_{CM} \pm 1.8V$	+/-100mV	—	—
I_{IN}	Input current	Power on	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	$R_T = 27\Omega$	—	1.4V	1.80V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	$R_T = 27\Omega$	0.95V	1.1V	—
V_{OD}	Output Voltage Differential	$ V_{OP} - V_{OM} , R_T = 27\Omega$	240mV	300mV	460mV
ΔV_{OD}	Change in V_{OD} Between H and L				27mV
V_{OS}	Output Voltage Offset	$ V_{OP} + V_{OM} /2, R_T = 27\Omega$	1.1V	1.3V	1.5V
ΔV_{OS}	Change in V_{OS} Between H and L				27mV
I_{OSD}	Output Short Circuit Current	$V_{OD} = 0$. Driver Outputs Shorted.		36mA	65mA

1. Refer to TN1000, [sysIO Usage Guidelines for Lattice Devices](#).

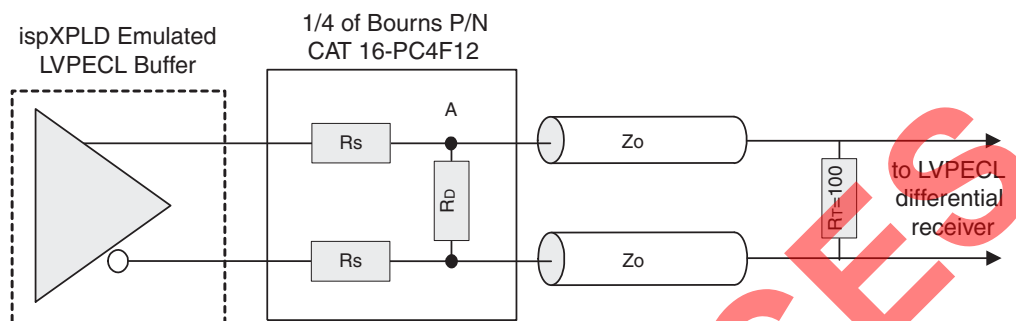
2. V_{OP} and V_{OM} are the two outputs of the LVDS/BLVDS output buffer.

LVPECL¹								
DC Parameter	Parameter Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
V_{CCO}		3.0		3.3		3.6		V
V_{IH}	Input Voltage High	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	Input Voltage Low	0.86	2.125	0.86	2.125	0.86	2.125	V
V_{OH}	Output Voltage High	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	Output Voltage Low	0.96	1.27	1.06	1.43	1.3	1.57	V
V_{DIFF}^2	Differential Input threshold	0.3	—	0.3	—	0.3	—	V

1. These values are valid at the output of the source termination pack as shown above with 100-ohm differential load only (see Figure 23).

The V_{OH} levels are 200mV below the standard LVPECL levels and are compatible with devices tolerant of the lower common mode ranges.

2. Valid for $0.2 \pm V_{CM} \pm 1.8V$.

Figure 23. LVPECL Driver with Three Resistor Pack

ispXPGA 125B/C & ispXPGA 125EB/EC External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Conditions	-5 ¹		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{CO}	Global Clock Input to Output	PIO Output Register	—	5.3	—	5.7	—	6.6	ns
t_S	Global Clock Input Setup	PIO Input Register without input delay	-1.9	—	-1.8	—	-1.5	—	ns
t_H	Global Clock Input Hold	PIO Input Register without input delay	2.7	—	2.9	—	3.3	—	ns
t_{SINDLY}	Global Clock Input Setup	PIO Input Register with input delay	3.1	—	3.3	—	3.8	—	ns
t_{HINDLY}	Global Clock Input Hold	PIO Input Register with input delay	0.0	—	0.0	—	0.0	—	ns
t_{COPLL}	Global Clock Input to Output	PIO Output Register using PLL without delay	—	3.6	—	3.9	—	4.5	ns
t_{SPLL}	Global Clock Input Setup	PIO Input Register without input delay using PLL without delay	0	—	0.1	—	0.3	—	ns
t_{HPLL}	Global Clock Input Hold	PIO Input Register without input delay using PLL without delay	0.9	—	1.0	—	1.2	—	ns
$t_{SINDLYPLL}$	Global Clock Input Setup	PIO Input Register with input delay using PLL without delay	5.1	—	5.5	—	6.3	—	ns
$t_{HINDLYPLL}$	Global Clock Input Hold	PIO Input Register with input delay using PLL without delay	-3.0	—	-2.8	—	-2.4	—	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 500B/C & ispXPGA 500EB/EC EBR Timing Parameters

Parameter	Description	-5 ¹		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Synchronous Write								
t _{EBSWAD_S}	Address Setup Delay	0.59	—	0.61	—	0.70	—	ns
t _{EBSWAD_H}	Address Hold Delay	-0.40	—	-0.39	—	-0.33	—	ns
t _{EBSWCPW}	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t _{EBSWWE_S}	Write Enable Setup Time	-0.12	—	-0.12	—	-0.10	—	ns
t _{EBSWWE_H}	Write Enable Hold Time	0.16	—	0.16	—	0.18	—	ns
t _{EBSWD_S}	Data Setup Time	0.27	—	0.28	—	0.32	—	ns
t _{EBSWD_H}	Data Hold Time	-0.27	—	-0.26	—	-0.22	—	ns
Synchronous Read								
t _{EBSR_CO}	Clock to Data Delay	—	2.04	—	2.19	—	2.52	ns
t _{EBSRAD_S}	Address Setup Delay	0.10	—	0.10	—	0.12	—	ns
t _{EBSRAD_H}	Address Hold Delay	-0.07	—	-0.07	—	-0.06	—	ns
t _{EBSRCPW}	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t _{EBSRCE_S}	Clock Enable Setup Time	-1.76	—	-1.71	—	-1.45	—	ns
t _{EBSRCE_H}	Clock Enable Hold Time	1.64	—	1.69	—	1.94	—	ns
t _{EBSRWE_S}	Write Enable Setup Time	-0.18	—	-0.17	—	-0.14	—	ns
t _{EBSRWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
t _{EBSRWEEN}	Write Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
t _{EBSRWEDIS}	Write Enable to Data Disable Time	—	0.99	—	1.02	—	1.17	ns
t _{EBSREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
t _{EBSRDIS}	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns
Asynchronous Read								
t _{EBARADO}	Address to New Valid Data Delay	—	2.39	—	2.46	—	2.83	ns
t _{EBARAD_H}	Address to Previous Valid Data Delay	—	2.10	—	2.17	—	2.50	ns
t _{EBARWEEN}	Write Enable to Data Enable Time	—	1.01	—	1.04	—	1.20	ns
t _{EBARWEDIS}	Write Enable to Data Disable Time	—	0.98	—	1.01	—	1.16	ns
t _{EBAREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
t _{EBARDIS}	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns

1. Only available for ispXPGA 500B and ispXPGA 500EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 1200B/C & ispXPGA 1200EB/EC External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Conditions	-5 ¹		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{CO}	Global Clock Input to Output	PIO Output Register	—	6.6	—	7.1	—	8.2	ns
t _S	Global Clock Input Setup	PIO Input Register without input delay	-2.7	—	-2.7	—	-2.3	—	ns
t _H	Global Clock Input Hold	PIO Input Register without input delay	4.5	—	4.6	—	5.3	—	ns
t _{SINDLY}	Global Clock Input Setup	PIO Input Register with input delay	3.8	—	3.8	—	4.4	—	ns
t _{HINDLY}	Global Clock Input Hold	PIO Input Register with input delay	0.0	—	0.0	—	0.0	—	
t _{COPLL}	Global Clock Input to Output	PIO Output Register using PLL without delay	—	3.1	—	3.3	—	3.8	ns
t _{SPLL}	Global Clock Input Setup	PIO Input Register without input delay using PLL without delay	0.5	—	0.5	—	0.6	—	ns
t _{HPLL}	Global Clock Input Hold	PIO Input Register without input delay using PLL without delay	0.8	—	0.8	—	1.0	—	ns
t _{SINDLYPLL}	Global Clock Input Setup	PIO Input Register with input delay using PLL without delay	7.6	—	7.6	—	8.8	—	ns
t _{HINDLYPLL}	Global Clock Input Hold	PIO Input Register with input delay using PLL without delay	-4.1	—	-4.0	—	-3.4	—	ns

1. Only available for ispXPGA 1200B and ispXPGA 1200EB (2.5V/3.3V) devices.

Timing v.0.2

ispXPGA 1200B/C & ispXPGA 1200EB/EC EBR Timing Parameters

Parameter	Description	-5 ¹		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Synchronous Write								
t _{EBSWAD_S}	Address Setup Delay	0.59	—	0.61	—	0.70	—	ns
t _{EBSWAD_H}	Address Hold Delay	-0.40	—	-0.39	—	-0.33	—	ns
t _{EBSWCPW}	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t _{EBSWWE_S}	Write Enable Setup Time	-0.12	—	-0.12	—	-0.10	—	ns
t _{EBSWWE_H}	Write Enable Hold Time	0.16	—	0.16	—	0.18	—	ns
t _{EBSWD_S}	Data Setup Time	0.27	—	0.28	—	0.32	—	ns
t _{EBSWD_H}	Data Hold Time	-0.27	—	-0.26	—	-0.22	—	ns
Synchronous Read								
t _{EBSR_CO}	Clock to Data Delay	—	2.04	—	2.19	—	2.52	ns
t _{EBSRAD_S}	Address Setup Delay	0.10	—	0.10	—	0.12	—	ns
t _{EBSRAD_H}	Address Hold Delay	-0.07	—	-0.07	—	-0.06	—	ns
t _{EBSRCPW}	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t _{EBSRCE_S}	Clock Enable Setup Time	-1.76	—	-1.71	—	-1.45	—	ns
t _{EBSRCE_H}	Clock Enable Hold Time	1.64	—	1.69	—	1.94	—	ns
t _{EBSRWE_S}	Write Enable Setup Time	-0.18	—	-0.17	—	-0.14	—	ns
t _{EBSRWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
t _{EBSRWEEN}	Write Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
t _{EBSRWEDIS}	Write Enable to Data Disable Time	—	0.99	—	1.02	—	1.17	ns
t _{EBSREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
t _{EBSRDIS}	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns
Asynchronous Read								
t _{EBARADO}	Address to New Valid Data Delay	—	2.39	—	2.46	—	2.83	ns
t _{EBARAD_H}	Address to Previous Valid Data Delay	—	2.10	—	2.17	—	2.50	ns
t _{EBARWEEN}	Write Enable to Data Enable Time	—	1.01	—	1.04	—	1.20	ns
t _{EBARWEDIS}	Write Enable to Data Disable Time	—	0.98	—	1.01	—	1.16	ns
t _{EBAREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
t _{EBARDIS}	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns

1. Only available for ispXPGA 1200B and ispXPGA 1200EB (2.5V/3.3V) devices.

Timing v.2.1

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹
AE3	BK1_IO33	-	37N/HSI2	NC	-	-	NC	-	-
AG1	BK1_IO34	-	38P/HSI2	NC	-	-	NC	-	-
AH1	BK1_IO35	-	38N/HSI2	NC	-	-	NC	-	-
AG2	BK1_IO36	-	39P/HSI2	NC	-	-	NC	-	-
AF3	BK1_IO37	-	39N/HSI2	NC	-	-	NC	-	-
AJ1	BK1_IO38	-	40P/HSI2	NC	-	-	NC	-	-
-	GND (Bank 1)	-	-	-	-	-	-	-	-
AH2	BK1_IO39	-	40N/HSI2	NC	-	-	NC	-	-
AG3	BK1_IO40	-	41P	BK1_IO24	-	25P/HSI1	NC	-	-
AF4	BK1_IO41	-	41N	BK1_IO25	-	25N/HSI1	NC	-	-
AK2	TCK	-	-	TCK	-	-	TCK	-	-
AJ3	TMS	-	-	TMS	-	-	TMS	-	-
AG5	TOE	-	-	TOE	-	-	TOE	-	-
AH4	BK2_IO0	-	42P	BK2_IO0	-	26P	BK2_IO0	-	22P
AK3	BK2_IO1	-	42N	BK2_IO1	-	26N	BK2_IO1	-	22N
AJ4	BK2_IO2	-	43P	BK2_IO2	-	27P	BK2_IO2	-	23P
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-	-	-	-
AH5	BK2_IO3	-	43N	BK2_IO3	-	27N	BK2_IO3	-	23N
AK4	BK2_IO4	-	44P	BK2_IO4	-	28P	BK2_IO4	-	24P
-	-	-	-	-	-	-	GND (Bank 2)	-	-
AJ5	BK2_IO5	-	44N	BK2_IO5	-	28N	BK2_IO5	-	24N
AG7	BK2_IO6	-	45P	BK2_IO6	-	29P	BK2_IO6	-	25P
AH6	BK2_IO7	-	45N	BK2_IO7	-	29N	BK2_IO7	-	25N
AK5	BK2_IO8	-	46P	NC	-	-	NC	-	-
AJ6	BK2_IO9	-	46N	NC	-	-	NC	-	-
AG8	BK2_IO10	-	47P	NC	-	-	NC	-	-
-	GND (Bank 2)	-	-	-	-	-	-	-	-
AH7	BK2_IO11	-	47N	NC	-	-	NC	-	-
AK6	BK2_IO12	-	48P	NC	-	-	NC	-	-
AJ7	BK2_IO13	-	48N	NC	-	-	NC	-	-
AH8	BK2_IO14	-	49P	NC	-	-	NC	-	-
AG10	BK2_IO15	-	49N	NC	-	-	NC	-	-
AK7	BK2_IO16	-	50P	NC	-	-	NC	-	-
AJ8	BK2_IO17	-	50N	NC	-	-	NC	-	-
AH9	BK2_IO18	-	51P	NC	-	-	NC	-	-
-	GND (Bank 2)	-	-	-	-	-	-	-	-
AG11	BK2_IO19	-	51N	NC	-	-	NC	-	-
AK8	BK2_IO20	-	52P	BK2_IO8	-	30P	BK2_IO8	-	26P
AJ9	BK2_IO21	VREF2	52N	BK2_IO9	VREF2	30N	BK2_IO9	VREF2	26N
AH10	BK2_IO22	-	53P	BK2_IO10	-	31P	BK2_IO10	-	27P
-	-	-	-	GND (Bank 2)	-	-	-	-	-
AH11	BK2_IO23	-	53N	BK2_IO11	-	31N	BK2_IO11	-	27N
AJ10	BK2_IO24	-	54P	BK2_IO12	-	32P	BK2_IO12	-	28P
AK10	BK2_IO25	-	54N	BK2_IO13	-	32N	BK2_IO13	-	28N
AH12	BK2_IO26	-	55P	BK2_IO14	-	33P	BK2_IO14	-	29P
-	GND (Bank 2)	-	-	-	-	-	-	-	-
AJ11	BK2_IO27	-	55N	BK2_IO15	-	33N	BK2_IO15	-	29N
AK11	BK2_IO28	-	56P	NC	-	-	NC	-	-
AJ12	BK2_IO29	-	56N	NC	-	-	NC	-	-
AG13	BK2_IO30	-	57P	BK2_IO16	-	34P	BK2_IO16	-	30P
AH13	BK2_IO31	-	57N	BK2_IO17	-	34N	BK2_IO17	-	30N

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved ¹
L3	BK7_IO35	-	234N
J1	BK7_IO36	-	235P
J2	BK7_IO37	-	235N
M4	BK7_IO38	-	236P
H1	BK7_IO39	-	236N
J3	BK7_IO40	-	237P
L4	BK7_IO41	-	237N
M5	BK7_IO42	-	238P
-	GND (Bank 7)	-	-
H2	BK7_IO43	-	238N
K4	BK7_IO44	-	239P
G1	BK7_IO45	-	239N
H3	BK7_IO46	-	240P
J4	BK7_IO47	VREF7	240N
K5	BK7_IO48	-	241P
G3	BK7_IO49	-	241N
H4	BK7_IO50	-	242P
-	GND (Bank 7)	-	-
F2	BK7_IO51	-	242N
G2	BK7_IO52	-	243P
H5	BK7_IO53	-	243N
F3	BK7_IO54	-	244P
F1	BK7_IO55	-	244N
G4	BK7_IO56	-	245P
E1	BK7_IO57	-	245N
F4	BK7_IO58	-	246P
-	GND (Bank 7)	-	-
E2	BK7_IO59	-	246N
F5	BK7_IO60	-	247P
E3	BK7_IO61	-	247N
D2	TDO	-	-
D3	VCCJ	-	-
D1	TDI	-	-

1. If a sysHSI Block is used, the indicated sysHSI reserved pins are unavailable for general purpose I/O use.

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹
L2	BK0_IO35	HSI1B_SINN	17N/HSI1	BK0_IO15	HSI0B_SINN	7N/HSI0
L6	BK0_IO36	-	18P/HSI1	BK0_IO16	-	8P/HSI0
L5	BK0_IO37	-	18N/HSI1	BK0_IO17	-	8N/HSI0
M1	BK0_IO38	HSI2A_SOUTP	19P/HSI1	BK0_IO18	HSI1A_SOUTP	9P/HSI1
-	-	-	-	GND (Bank 0)	-	-
M2	BK0_IO39	HSI2A_SOUTN	19N/HSI1	BK0_IO19	HSI1A_SOUTN	9N/HSI1
L3	BK0_IO40	-	20P/HSI1	BK0_IO20	-	10P/HSI1
L4	BK0_IO41	-	20N/HSI1	BK0_IO21	-	10N/HSI1
M6	BK0_IO42	HSI2A_SINP	21P/HSI2	BK0_IO22	HSI1A_SINP	11P/HSI1
-	GND (Bank 0)	-	-	-	-	-
M5	BK0_IO43	HSI2A_SINN	21N/HSI2	BK0_IO23	HSI1A_SINN	11N/HSI1
M4	BK0_IO44	-	22P/HSI2	BK0_IO24	-	12P/HSI1
M3	BK0_IO45	-	22N/HSI2	BK0_IO25	-	12N/HSI1
N1	BK0_IO46	HSI2B_SOUTP	23P/HSI2	BK0_IO26	HSI1B_SOUTP	13P/HSI1
-	-	-	-	GND (Bank 0)	-	-
N2	BK0_IO47	HSI2B_SOUTN	23N/HSI2	BK0_IO27	HSI1B_SOUTN	13N/HSI1
N7	BK0_IO48	-	24P/HSI2	BK0_IO28	-	14P/HSI1
N6	BK0_IO49	-	24N/HSI2	BK0_IO29	-	14N/HSI1
P1	BK0_IO50	HSI2B_SINP	25P/HSI2	BK0_IO30	HSI1B_SINP	15P/HSI1
-	GND (Bank 0)	-	-	-	-	-
P2	BK0_IO51	HSI2B_SINN	25N/HSI2	BK0_IO31	HSI1B_SINN	15N/HSI1
N3	BK0_IO52	-	26P/HSI2	BK0_IO32	-	16P/HSI1
N4	BK0_IO53	-	26N/HSI2	BK0_IO33	-	16N/HSI1
P6	BK0_IO54	PLL_RST0	27P/HSI2	BK0_IO38	PLL_RST0	19P
P5	BK0_IO55	PLL_RST1	27N/HSI2	BK0_IO35	PLL_RST1	17N
P3	BK0_IO56	-	28P/HSI2	BK0_IO36	-	18P
P4	BK0_IO57	-	28N/HSI2	BK0_IO39	-	19N
R7	BK0_IO58	PLL_FBK0	29P	BK0_IO34	PLL_FBK0	17P
-	GND (Bank 0)	-	-	GND (Bank 0)	-	-
R6	BK0_IO59	PLL_FBK1	29N	BK0_IO37	PLL_FBK1	18N
R1	BK0_IO60	CLK_OUT0	30P	BK0_IO40	CLK_OUT0	20P
-	-	-	-	GND (Bank 0)	-	-
R2	BK0_IO61	CLK_OUT1	30N	BK0_IO41	CLK_OUT1	20N
-	GND (Bank 0)	-	-	-	-	-
R3	GCLK0	-	LVDS Pair0P	GCLK0	-	LVDS Pair0P
R4	GCLK1	-	LVDS Pair0N	GCLK1	-	LVDS Pair0N
R5	VCCP0	-	-	VCCP0	-	-
T3	GNDP0	-	-	GNDP0	-	-
T4	GCLK2	-	LVDS Pair1P	GCLK2	-	LVDS Pair1P
T5	GCLK3	-	LVDS Pair1N	GCLK3	-	LVDS Pair1N
-	GND (Bank 1)	-	-	-	-	-
T2	BK1_IO0	CLK_OUT2	31P	BK1_IO0	CLK_OUT2	21P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹
AJ12	BK2_IO43	-	83N	BK2_IO23	-	53N
AD13	BK2_IO44	-	84P	BK2_IO24	-	54P
AE13	BK2_IO45	-	84N	BK2_IO25	-	54N
AK13	BK2_IO46	-	85P	BK2_IO26	-	55P
-	-	-	-	GND (Bank 2)	-	-
AJ13	BK2_IO47	-	85N	BK2_IO27	-	55N
AG13	BK2_IO48	-	86P	BK2_IO28	-	56P
AH13	BK2_IO49	-	86N	BK2_IO29	-	56N
AE14	BK2_IO50	-	87P	BK2_IO30	-	57P
-	GND (Bank 2)	-	-	-	-	-
AF14	BK2_IO51	-	87N	BK2_IO31	-	57N
AG14	BK2_IO52	-	88P	BK2_IO32	-	58P
AH14	BK2_IO53	-	88N	BK2_IO33	-	58N
AJ14	BK2_IO54	-	89P	BK2_IO34	-	59P
-	-	-	-	GND (Bank 2)	-	-
AK14	BK2_IO55	-	89N	BK2_IO35	-	59N
AE15	BK2_IO56	-	90P	BK2_IO36	-	60P
AF15	BK2_IO57	-	90N	BK2_IO37	-	60N
AG15	BK2_IO58	-	91P	BK2_IO38	-	61P
-	GND (Bank 2)	-	-	-	-	-
AH15	BK2_IO59	-	91N	BK2_IO39	-	61N
AJ15	BK2_IO60	-	92P	BK2_IO40	-	62P
AK15	BK2_IO61	-	92N	BK2_IO41	-	62N
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-
AK16	BK3_IO0	-	93P	BK3_IO0	-	63P
AJ16	BK3_IO1	-	93N	BK3_IO1	-	63N
AH16	BK3_IO2	-	94P	BK3_IO2	-	64P
-	GND (Bank 3)	-	-	-	-	-
AG16	BK3_IO3	-	94N	BK3_IO3	-	64N
AF16	BK3_IO4	-	95P	BK3_IO4	-	65P
AE16	BK3_IO5	-	95N	BK3_IO5	-	65N
AK17	BK3_IO6	-	96P	BK3_IO6	-	66P
-	-	-	-	GND (Bank 3)	-	-
AJ17	BK3_IO7	-	96N	BK3_IO7	-	66N
AH17	BK3_IO8	-	97P	BK3_IO8	-	67P
AG17	BK3_IO9	-	97N	BK3_IO9	-	67N
AF17	BK3_IO10	-	98P	BK3_IO10	-	68P
-	GND (Bank 3)	-	-	-	-	-
AE17	BK3_IO11	-	98N	BK3_IO11	-	68N
AH18	BK3_IO12	-	99P	BK3_IO12	-	69P
AG18	BK3_IO13	-	99N	BK3_IO13	-	69N

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved ¹
AJ18	BK3_IO14	-	100P	BK3_IO14	-	70P
-	-	-	-	GND (Bank 3)	-	-
AK18	BK3_IO15	-	100N	BK3_IO15	-	70N
AE18	BK3_IO16	-	101P	BK3_IO16	-	71P
AD18	BK3_IO17	-	101N	BK3_IO17	-	71N
AJ19	BK3_IO18	-	102P	BK3_IO18	-	72P
-	GND (Bank 3)	-	-	-	-	-
AK19	BK3_IO19	-	102N	BK3_IO19	-	72N
AH19	BK3_IO20	-	103P	NC	-	-
AG19	BK3_IO21	-	103N	NC	-	-
AK20	BK3_IO22	-	104P	NC	-	-
AJ20	BK3_IO23	-	104N	NC	-	-
AF19	BK3_IO24	-	105P	NC	-	-
AE19	BK3_IO25	-	105N	NC	-	-
AH20	BK3_IO26	-	106P	NC	-	-
-	GND (Bank 3)	-	-	-	-	-
AG20	BK3_IO27	-	106N	NC	-	-
AF20	BK3_IO28	-	107P	NC	-	-
AE20	BK3_IO29	-	107N	NC	-	-
AJ21	BK3_IO30	-	108P	NC	-	-
AK21	BK3_IO31	-	108N	NC	-	-
AG21	BK3_IO32	-	109P	NC	-	-
AF21	BK3_IO33	-	109N	NC	-	-
AK22	BK3_IO34	-	110P	NC	-	-
-	GND (Bank 3)	-	-	-	-	-
AJ22	BK3_IO35	-	110N	NC	-	-
AE21	BK3_IO36	-	111P	NC	-	-
AD21	BK3_IO37	-	111N	NC	-	-
AG22	BK3_IO38	-	112P	NC	-	-
AF22	BK3_IO39	-	112N	NC	-	-
AG23	BK3_IO40	-	113P	BK3_IO22	-	74P
-	-	-	-	GND (Bank 3)	-	-
AH23	BK3_IO41	-	113N	BK3_IO23	-	74N
AJ23	BK3_IO42	-	114P	BK3_IO24	-	75P
-	GND (Bank 3)	-	-	-	-	-
AK23	BK3_IO43	-	114N	BK3_IO25	-	75N
AF23	BK3_IO44	-	115P	BK3_IO26	-	76P
AE23	BK3_IO45	-	115N	BK3_IO27	-	76N
AJ24	BK3_IO46	-	116P	BK3_IO28	-	77P
AK24	BK3_IO47	-	116N	BK3_IO29	-	77N
AH24	BK3_IO48	-	117P	BK3_IO21	-	73N
AG24	BK3_IO49	VREF3	117N	BK3_IO20	VREF3	73P

Commercial (Cont.)

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX200B-05F516C	210K	2.5/3.3	-5	fpBGA	516
LFX200B-04F516C	210K	2.5/3.3	-4	fpBGA	516
LFX200B-03F516C	210K	2.5/3.3	-3	fpBGA	516
LFX200C-04F516C	210K	1.8	-4	fpBGA	516
LFX200C-03F516C	210K	1.8	-3	fpBGA	516
LFX200B-05FH516C ¹	210K	2.5/3.3	-5	fpBGA	516
LFX200B-04FH516C ¹	210K	2.5/3.3	-4	fpBGA	516
LFX200B-03FH516C ¹	210K	2.5/3.3	-3	fpBGA	516
LFX200C-04FH516C ¹	210K	1.8	-4	fpBGA	516
LFX200C-03FH516C ¹	210K	1.8	-3	fpBGA	516
LFX500B-05F516C	476K	2.5/3.3	-5	fpBGA	516
LFX500B-04F516C	476K	2.5/3.3	-4	fpBGA	516
LFX500B-03F516C	476K	2.5/3.3	-3	fpBGA	516
LFX500C-04F516C	476K	1.8	-4	fpBGA	516
LFX500C-03F516C	476K	1.8	-3	fpBGA	516
LFX500B-05FH516C ¹	476K	2.5/3.3	-5	fpBGA	516
LFX500B-04FH516C ¹	476K	2.5/3.3	-4	fpBGA	516
LFX500B-03FH516C ¹	476K	2.5/3.3	-3	fpBGA	516
LFX500C-04FH516C ¹	476K	1.8	-4	fpBGA	516
LFX500C-03FH516C ¹	476K	1.8	-3	fpBGA	516
LFX500B-05F900C	476K	2.5/3.3	-5	fpBGA	900
LFX500B-04F900C	476K	2.5/3.3	-4	fpBGA	900
LFX500B-03F900C	476K	2.5/3.3	-3	fpBGA	900
LFX500C-04F900C	476K	1.8	-4	fpBGA	900
LFX500C-03F900C	476K	1.8	-3	fpBGA	900
LFX1200B-05F900C ²	1.25M	2.5/3.3	-5	fpBGA	900
LFX1200B-04F900C ²	1.25M	2.5/3.3	-4	fpBGA	900
LFX1200B-03F900C ²	1.25M	2.5/3.3	-3	fpBGA	900
LFX1200C-04F900C ²	1.25M	1.8	-4	fpBGA	900
LFX1200C-03F900C ²	1.25M	1.8	-3	fpBGA	900
LFX1200B-05FE680C ²	1.25M	2.5/3.3	-5	fpSBGA	680
LFX1200B-04FE680C ²	1.25M	2.5/3.3	-4	fpSBGA	680
LFX1200B-03FE680C ²	1.25M	2.5/3.3	-3	fpSBGA	680
LFX1200C-04FE680C ²	1.25M	1.8	-4	fpSBGA	680
LFX1200C-03FE680C ²	1.25M	1.8	-3	fpSBGA	680

1. FH516 package was converted to F516 via [PCN #09A-08](#).

2. Discontinued via [PCN #03A-10](#).