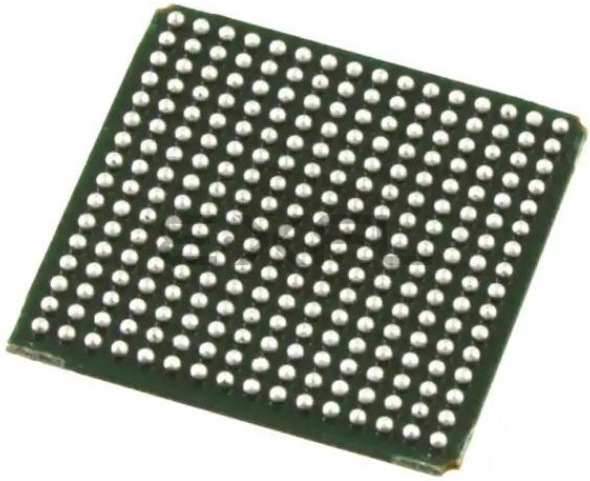
Lattice Semiconductor Corporation - LFX125EB-05F256C Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1936
Total RAM Bits	94208
Number of I/O	160
Number of Gates	139000
Voltage - Supply	2.3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx125eb-05f256c

ispXPGA Family Overview

The ispXPGA family of devices provides the ideal vehicle for the creation of high-performance logic designs that are both non-volatile and infinitely re-programmable. Other FPGA solutions force a compromise, being either re-programmable or non-volatile. This family couples this capability with a mainstream architecture containing the features required for today's system-level design.

The ispXPGA family is available in two options. The standard device supports sysHSI capability for ultra fast serial communications while the lower-cost "E-Series" supports the same high-performance FPGA fabric without the sysHSI Block.

Electrically Erasable CMOS (E^2CMOS) memory cells provide the ispXPGA family with non-volatile capability. These allow logic to be functional microseconds after power is applied, allowing easy interfacing in many applications. This capability also means that expensive external configuration memories are not required and that designs can be secured from unauthorized read back. Internal SRAM cells allow the device to be infinitely reconfigured if desired. Both the SRAM and E^2CMOS cells can be programmed and verified through the IEEE 1532 industry standard. Additionally, the SRAM cells can be configured and read-back through the sysCONFIG™ peripheral port.

The family spans the density and I/O range required for the majority of today's logic designs, 139K to 1.25M functional gates and 160 to 496 I/O. The devices are available for operation from 1.8V, 2.5V, and 3.3V power supplies, providing easy integration into the overall system.

System-level design needs are met through the incorporation of sysMEM dual-port memory blocks, sysIO advanced I/O support, and sysCLOCK Phase Locked Loops (PLLs). High-speed serial communications are supported through multiple sysHSI blocks, which provide clock data recovery (CDR) and serialization/de-serialization (SERDES).

The ispLEVER™ design tool from Lattice allows easy implementation of designs using the ispXPGA product. Synthesis library support is available for major logic synthesis tools. The ispLEVER tool takes the output from these common synthesis packages and place and routes the design in the ispXPGA product. The tool supports floor planning and the management of other constraints within the device. The tool also provides outputs to common timing analysis tools for timing analysis.

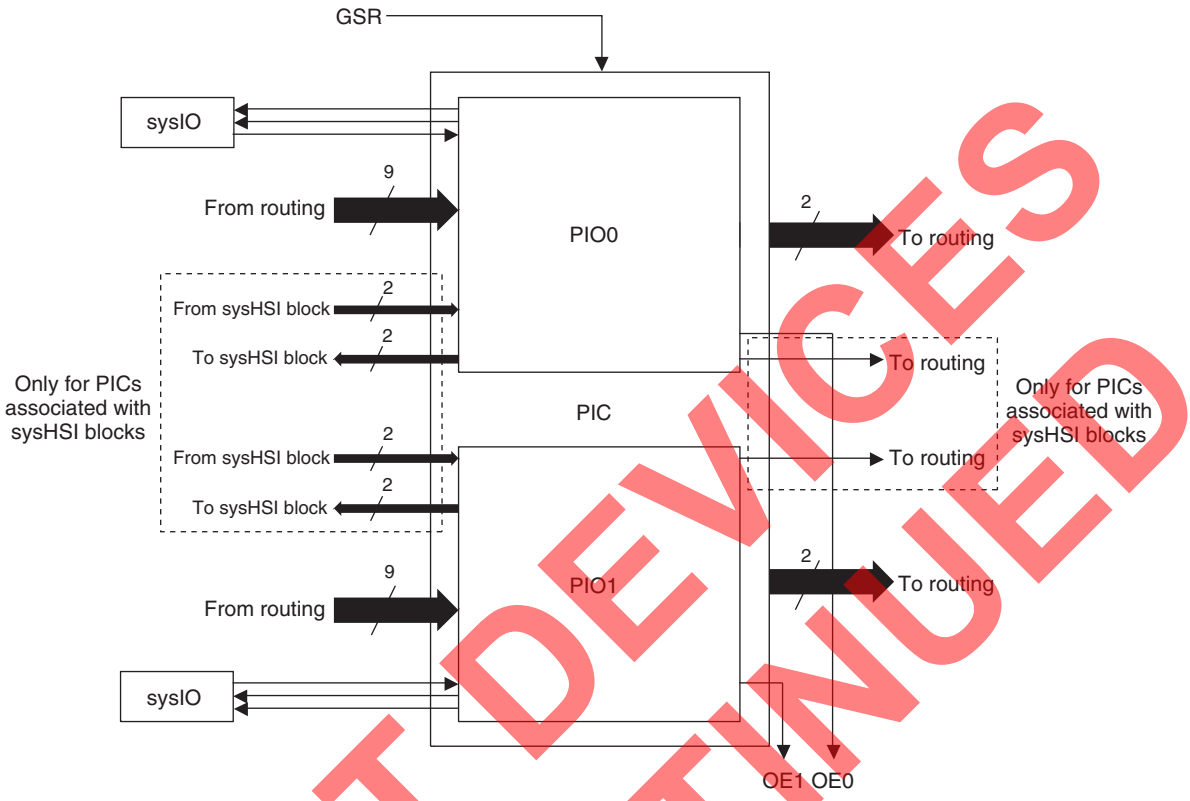
To increase designer productivity, Lattice provides a variety of pre-designed modules referred to as IP cores for the ispXPGA product. These IP cores allow designers to concentrate on the unique portions of their design while using pre-designed blocks to implement standard functions such as bus interfaces, standard communication interfaces, and memory controllers.

Through the use of advanced technology and innovative architecture the ispXPGA FPGA devices provide designers with excellent speed performance. Although design dependent, many typical designs can run at over 150MHz. Certain designs can run at over 300MHz. Table 2 details the performance of several building blocks commonly used by logic designers.

Table 2. ispXPGA Speed Performance for Typical Building Blocks

Function	Performance
8:1 Asynch MUX	150 MHz
1:32 Asynch Demultiplexer	125 MHz
8 x 8 2-LL Pipelined Multiplier	225 MHz
32-bit Up/Down Counter	290 MHz
32-bit Shift Register	360 MHz

Figure 10. ispXPGA PIC



Programmable Input/Output

The PIO is the building block of a PIC. The PIO has a total of 11 inputs and five outputs. Nine of the 11 inputs are generated from routing. The inputs from routing are the PIO Input (IN), Feed-Thru (FT), Clock (CLK), Input Clock Enable (ICE), Input Set/Reset (ISR), Output Clock Enable (OCEN), Output Set/Reset (OSR), PIO Output Enable (OEN), and PIO Input Enable (IEN). The remaining inputs are the sysIO input buffer signal and the Global Set/Reset signal. Three of the five outputs (OUT0, OUT1, and OE) feed routing. The last two outputs feed the sysIO buffer directly as the output and output enable of the sysIO output buffer.

PIOs associated with sysHSI blocks contain two additional inputs and outputs to support the sysHSI block. The two inputs come from the sysHSI block associated with the PIO, and the two outputs feed the sysHSI block. One of the inputs routes directly through the PIO to routing, while the other is multiplexed with the Feed-Thru, register bypass, and Q output of the register to form the OUT1 output of the PIO. The outputs to the sysHSI block are the same signals as the outputs which feed the sysIO buffers (sysIO Output and sysIO Output Enable).

Each PIO has an input register, an output register, and an output enable register as shown in Figure 11. The input register path of the PIO has a 'delay' option, which slows the data-flow. A two-input OR function of the Global Set/Reset (GSR) and Set/Reset (ISR or OSR) signals creates the set/reset term for the respective registers. Each PIO has two pairs of set/reset and clock enable signals. One is exclusive to the input register, whereas the other is common for both the output and output enable registers. The clock (CLK) is common to all registers in a PIO, and the polarity of the clock is controllable. The input, output, and the output enable registers can be configured as a latch or D-type flip-flop. Each PIO is capable of generating an output enable signal, which in turn becomes a PIC output.

Table 5. ispXPGA Supported I/O Standards

sysIO Standard	V_{CCO}	V_{REF}	V_{TT}
LVTTL	3.3V	N/A	N/A
LVCMOS-3.3	3.3V	N/A	N/A
LVCMOS-2.5	2.5V	N/A	N/A
LVCMOS-1.8	1.8V	N/A	N/A
PCI	3.3V	N/A	N/A
AGP-1X	3.3V	N/A	N/A
SSTL3, Class I, II	3.3V	1.5V	1.5V
SSTL2, Class I, II	2.5V	1.25V	1.25V
HSTL, Class I	1.5V	0.75V	0.75V
HSTL, Class III	1.5V	0.9V	1.5V
GTL+	N/A	1.0V	1.5V
LVPECL	3.3V	N/A	N/A
LVDS[1]	2.5V	N/A	N/A
BLVDS	2.5V	N/A	N/A

1. V_{CCO} must be 2.5V for high speed serial operations (sysHSI block).

Table 6. Differential Interface Standard Support[1]

		sysIO Buffer Not Using sysHSI Block	sysIO Buffer Using sysHSI Block
LVDS	Driver	Supported with external resistor network	Supported
	Receiver	Supported with standard termination	Supported with standard termination
BLVDS	Driver	Supported with external resistor network	Not supported
	Receiver	Supported (may need termination)	Supported (may need termination)
LVPECL	Driver	Supported with external resistor network	Not supported
	Receiver	Supported with termination	Supported with termination

1. For more information, refer to TN1000, sysIO Usage Guidelines for Lattice Devices.

ispXPGA 125B/C & ispXPGA 125EB/EC EBR Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Synchronous Write								
t_{EBSWAD_S}	Address Setup Delay	0.59	—	0.61	—	0.70	—	ns
t_{EBSWAD_H}	Address Hold Delay	-0.40	—	-0.39	—	-0.33	—	ns
$t_{EBSWCPW}$	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t_{EBSWWE_S}	Write Enable Setup Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{EBSWWE_H}	Write Enable Hold Time	0.16	—	0.16	—	0.18	—	ns
t_{EBSWD_S}	Data Setup Time	0.27	—	0.28	—	0.32	—	ns
t_{EBSWD_H}	Data Hold Time	-0.27	—	-0.26	—	-0.22	—	ns
Synchronous Read								
t_{EBSR_CO}	Clock to Data Delay	—	2.04	—	2.19	—	2.52	ns
t_{EBSRAD_S}	Address Setup Delay	0.10	—	0.10	—	0.12	—	ns
t_{EBSRAD_H}	Address Hold Delay	-0.07	—	-0.07	—	-0.06	—	ns
$t_{EBSRCPW}$	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t_{EBSRCE_S}	Clock Enable Setup Time	-1.76	—	-1.71	—	-1.45	—	ns
t_{EBSRCE_H}	Clock Enable Hold Time	1.64	—	1.69	—	1.94	—	ns
t_{EBSRWE_S}	Write Enable Setup Time	-0.18	—	-0.17	—	-0.14	—	ns
t_{EBSRWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{EBSRWEEN}$	Write Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBSRWEDIS}$	Write Enable to Data Disable Time	—	0.99	—	1.02	—	1.17	ns
t_{EBSREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBSRDIS}$	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns
Asynchronous Read								
$t_{EBARADO}$	Address to New Valid Data Delay	—	2.39	—	2.46	—	2.83	ns
t_{EBARAD_H}	Address to Previous Valid Data Delay	—	2.10	—	2.17	—	2.50	ns
$t_{EBARWEEN}$	Write Enable to Data Enable Time	—	1.01	—	1.04	—	1.20	ns
$t_{EBARWEDIS}$	Write Enable to Data Disable Time	—	0.98	—	1.01	—	1.16	ns
t_{EBAREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBARDIS}$	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 200B/C & ispXPGA 200EB/EC External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Conditions	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{CO}	Global Clock Input to Output	PIO Output Register	—	5.5	—	5.9	—	6.8	ns
t_S	Global Clock Input Setup	PIO Input Register without input delay	-2.0	—	-2.0	—	-1.7	—	ns
t_H	Global Clock Input Hold	PIO Input Register without input delay	3.7	—	3.8	—	4.4	—	ns
t_{SINDLY}	Global Clock Input Setup	PIO Input Register with input delay	3.8	—	3.8	—	4.4	—	ns
t_{HINDLY}	Global Clock Input Hold	PIO Input Register with input delay	0.0	—	0.0	—	0.0	—	
t_{COPLL}	Global Clock Input to Output	PIO Output Register using PLL without delay	—	3.3	—	3.6	—	4.2	ns
t_{SPLL}	Global Clock Input Setup	PIO Input Register without input delay using PLL without delay	-0.2	—	-0.2	—	0.1	—	ns
t_{HPLL}	Global Clock Input Hold	PIO Input Register without input delay using PLL without delay	1.5	—	1.5	—	1.8	—	ns
$t_{SINDLYPLL}$	Global Clock Input Setup	PIO Input Register with input delay using PLL without delay	6.3	—	6.3	—	7.3	—	ns
$t_{HINDLYPLL}$	Global Clock Input Hold	PIO Input Register with input delay using PLL without delay	-2.7	—	-2.6	—	-2.2	—	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.

Timing v.0.2

ispXPGA 200B/C & ispXPGA 200EB/EC PFU Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Functional Delays								
LUTs								
t_{LUT4}	4-Input LUT Delay	—	0.41	—	0.44	—	0.51	ns
t_{LUT5}	5-Input LUT Delay	—	0.73	—	0.79	—	0.91	ns
t_{LUT6}	6-Input LUT Delay	—	0.86	—	0.93	—	1.07	ns
Shift Register (LUT)								
t_{LSR_S}	Shift Register Setup Time	-0.64	—	-0.62	—	-0.53	—	ns
t_{LSR_H}	Shift Register Hold Time	0.61	—	0.63	—	0.72	—	ns
t_{LSR_CO}	Shift Register Clock to Output Delay	—	0.70	—	0.75	—	0.86	ns
Arithmetic Functions								
$t_{LCTHRUR}$	MC (Macro Cell) Carry In to MC Carry Out Delay (Ripple)	—	0.08	—	0.09	—	0.10	ns
$t_{LCTHRUL}$[2]	MC Carry In to MC Carry Out Delay (Look Ahead)	—	0.05	—	0.05	—	0.06	ns
t_{LSTHRU}	MC Sum In to MC Sum Out Delay	—	0.42	—	0.45	—	0.52	ns
$t_{LSINCOUT}$	MC Sum In to MC Carry Out Delay	—	0.29	—	0.31	—	0.36	ns
$t_{LCINSOUTR}$	MC Carry In to MC Sum Out Delay (Ripple)	—	0.36	—	0.39	—	0.45	ns
$t_{LCINSOUTL}$	MC Carry In to MC Sum Out Delay (Look Ahead)	—	0.26	—	0.28	—	0.32	ns
Feed-thru								
t_{LFT}	PFU Feed-Thru Delay	—	0.15	—	0.16	—	0.18	ns
Distributed RAM								
t_{LRAM_CO}	Clock to RAM Output	—	1.24	—	1.33	—	1.53	ns
t_{LRAMAD_S}	Address Setup Time	-0.41	—	-0.40	—	-0.34	—	ns
t_{LRAMD_S}	Data Setup Time	0.21	—	0.22	—	0.25	—	ns
t_{LRAMWE_S}	Write Enable Setup Time	0.45	—	0.46	—	0.53	—	ns
t_{LRAMAD_H}	Address Hold Time	0.58	—	0.60	—	0.69	—	ns
t_{LRAMD_H}	Data Hold Time	0.11	—	0.11	—	0.13	—	ns
t_{LRAMWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{LRAMCPW}$	Clock Pulse Width (High or Low)	2.91	—	3.00	—	3.45	—	ns
$t_{LRAMADO}$	Address to Output Delay	—	0.86	—	0.93	—	1.07	ns
Register/Latch Delays								
Registers								
t_{L_CO}	Register Clock to Output Delay	—	0.58	—	0.62	—	0.71	ns
t_{L_S}	Register Setup Time (Data before Clock)	0.14	—	0.14	—	0.16	—	ns
t_{L_H}	Register Hold Time (Data after Clock)	-0.12	—	-0.12	—	-0.10	—	ns
t_{LCE_S}	Register Clock Enable Setup Time	-0.11	—	-0.11	—	-0.09	—	ns
t_{LCE_H}	Register Clock Enable Hold Time	0.11	—	0.11	—	0.13	—	ns
Latches								
t_{L_GO}	Latch Gate to Output Delay	—	0.09	—	0.10	—	0.12	ns
t_{LL_S}	Latch Setup Time	0.14	—	0.14	—	0.16	—	ns
t_{LL_H}	Latch Hold Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{LLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns

ispXPGA 200B/C & ispXPGA 200EB/EC EBR Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Synchronous Write								
t_{EBSWAD_S}	Address Setup Delay	0.59	—	0.61	—	0.70	—	ns
t_{EBSWAD_H}	Address Hold Delay	-0.40	—	-0.39	—	-0.33	—	ns
$t_{EBSWCPW}$	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t_{EBSWWE_S}	Write Enable Setup Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{EBSWWE_H}	Write Enable Hold Time	0.16	—	0.16	—	0.18	—	ns
t_{EBSWD_S}	Data Setup Time	0.27	—	0.28	—	0.32	—	ns
t_{EBSWD_H}	Data Hold Time	-0.27	—	-0.26	—	-0.22	—	ns
Synchronous Read								
t_{EBSR_CO}	Clock to Data Delay	—	2.04	—	2.19	—	2.52	ns
t_{EBSRAD_S}	Address Setup Delay	0.10	—	0.10	—	0.12	—	ns
t_{EBSRAD_H}	Address Hold Delay	-0.07	—	-0.07	—	-0.06	—	ns
$t_{EBSRCPW}$	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t_{EBSRCE_S}	Clock Enable Setup Time	-1.76	—	-1.71	—	-1.45	—	ns
t_{EBSRCE_H}	Clock Enable Hold Time	1.64	—	1.69	—	1.94	—	ns
t_{EBSRWE_S}	Write Enable Setup Time	-0.18	—	-0.17	—	-0.14	—	ns
t_{EBSRWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{EBSRWEEN}$	Write Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBSRWEDIS}$	Write Enable to Data Disable Time	—	0.99	—	1.02	—	1.17	ns
t_{EBSREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBSRDIS}$	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns
Asynchronous Read								
$t_{EBARADO}$	Address to New Valid Data Delay	—	2.39	—	2.46	—	2.83	ns
t_{EBARAD_H}	Address to Previous Valid Data Delay	—	2.10	—	2.17	—	2.50	ns
$t_{EBARWEEN}$	Write Enable to Data Enable Time	—	1.01	—	1.04	—	1.20	ns
$t_{EBARWEDIS}$	Write Enable to Data Disable Time	—	0.98	—	1.01	—	1.16	ns
t_{EBAREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBARDIS}$	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 500B/C & ispXPGA 500EB/EC PFU Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Set								
t_{LASSRO}	Asynchronous Set/Reset to Output	—	1.09	—	1.17	—	1.35	ns
$t_{LASSRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{LASSRR}	Asynchronous Set/Reset Recovery	—	0.51	—	0.55	—	0.63	ns
t_{LSSR_S}	Synchronous Set/Reset Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{LSSR_H}	Synchronous Set/Reset Hold Time	0.03	—	0.03	—	0.03	—	ns

1. Only available for ispXPGA 500B and ispXPGA 500EB (2.5V/3.3V) devices.
2. $t_{LCTHRUL}$ quoted bit by bit.

Timing v.0.3

ispXPGA 500B/C & ispXPGA 500EB/EC PIC Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Register/Latch Delays								
t_{IO_CO}	Register Clock to Output Delay	—	1.00	—	1.07	—	1.23	ns
t_{IO_S}	Register Setup Time (Data before Clock)	0.05	—	0.05	—	0.06	—	ns
t_{IO_H}	Register Hold Time (Data after Clock)	0.06	—	0.06	—	0.07	—	ns
t_{IOCE_S}	Register Clock Enable Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{IOCE_H}	Register Clock Enable Hold Time	0.13	—	0.13	—	0.15	—	ns
t_{IO_GO}	Latch Gate to Output Delay	—	0.78	—	0.84	—	0.97	ns
t_{IOL_S}	Latch Setup Time	0.05	—	0.05	—	0.06	—	ns
t_{IOL_H}	Latch Hold Time	0.06	—	0.06	—	0.07	—	ns
t_{IOLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns
t_{IOASRO}	Asynchronous Set/Reset to Output	—	1.11	—	1.19	—	1.37	ns
$t_{IOASRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{IOASRR}	Asynchronous Set/Reset Recovery Time	—	0.23	—	0.25	—	0.29	ns
Input/Output Delays								
t_{IOBUF}	Output Buffer Delay	—	0.98	—	1.05	—	1.21	ns
t_{IOIN}	Input Buffer Delay	—	0.65	—	0.70	—	0.81	ns
t_{IOEN}	Output Enable Delay	—	0.52	—	0.56	—	0.64	ns
t_{IODIS}	Output Disable Delay	—	-0.12	—	-0.11	—	-0.09	ns
t_{IOFT}	Feed-thru Delay	—	0.19	—	0.20	—	0.23	ns

1. Only available for ispXPGA 500B and ispXPGA 500EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 500B/C & ispXPGA 500EB/EC Timing Adders

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	5.21	—	5.60	—	6.44	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

Signal Descriptions[1]

Signal Name	Signal Type	Description
General Purpose		
BK*y*_IO*x*[1,2]	Input/Output	General purpose I/O number x in I/O Bank y
GCLK*n*/I*n*[7]	Input	Global clock/input[8]
GSR	Input	Global Set/Reset
NC	—	No Connect
GND	GND	Ground
V_{CC}	VCC	Core logic power supply
V_{CCJ}	VCC	IEEE 1149.1 TAP power supply
V_{CCOy}[2]	VCC	I/O Bank y power supply
V_{REFy}[2]	Input	I/O Bank y reference voltage
D_{XN}, D_{XP}	Output	Temperature Sensing Diodes, provide a differential voltage, which corresponds to the temperature of the device.
Test and Program/Configuration		
TMS	Input	Test Mode Select
TCK	Input	Test Clock
TDI	Input	Test Data In
TDO	Output	Test Data Out
TOE	Input	Test Output Enable tri-states all I/O pins when driven low
CFG0	Input	Selects the SRAM memory configuration type (Peripheral or E^2CMOS Refresh)
PROGRAMb	Input	Initiates download from E^2CMOS or the peripheral port to SRAM memory (active low)
DONE	Bi-directional	Indicates when configuration is complete
INITb	Bi-directional	Indicates the device is ready for programming (active low)
READ	Input	Selects the READ operation when in sysCONFIG mode
CCLK	Input	sysCONFIG Configuration Clock
CSb	Input	sysCONFIG Chip Select (active low)
DATA[0:7]	Bi-directional	sysCONFIG Peripheral Port Data I/O
sysCLOCK PLL[3]		
PLL_FBK*z*	Input	Optional external feedback
PLL_RST*z*	Input	Optional external M divider reset
CLK_OUT*z*	Internal Signal	Clock output (routable to any I/O)
PLL_LOCK*z*	Internal Signal	Lock output (routable to any I/O)
GND_{P0}	GND	Left side PLL Ground
GND_{P1}	GND	Right side PLL Ground
V_{CCP0}	VCC	Left side PLL power supply
V_{CCP1}	VCC	Right side PLL power supply
sysHSI Block[4, 5]		
HSI*m*A_SINP, HSI*m*B_SINP	Input	P-side of differential serial data input
HSI*m*A_SINN, HSI*m*B_SINN	Input	N-side of differential serial data input
HSI*m*A_SOUTP, HSI*m*B_SOUTP	Output	P-side of differential serial data output
HSI*m*A_SOUTN, HSI*m*B_SOUTN	Output	N-side of differential serial data output
HSI*m*A_SYDT, HSI*m*B_SYDT	Internal Signal	Symbol alignment detect
HSI*m*A_RECCLK, HSI*m*B_RECCLK	Internal Signal	Recovered clock

ispXPGA Power Supply and NC Connections[1] (Continued)

Signal	680-Ball fpBGA[3]	900-Ball fpBGA[3]
V_{CC}	AE35, AE5, AL5, AR15, AR25, AR31, AR35, AR5, AT36, AT4, AU3, AU37, C3, C37, D36, D4, E15, E25, E35, E5, E9, J35, R35, R5	L11, L20, M12, M13, M14, M17, M18, M19, N12, N19, P12, P19, U12, U19, V12, V19, W12, W13, W14, W17, W18, W19, Y11, Y20
V_{CCO0}	E11, E12, E13, E17, E18, E7	K3, L10, M11, N11, N5, P11, R11, R12
V_{CCO1}	E22, E23, E27, E29, E31, E33	AA3, T11, T12, U11, V11, V5, W11, Y10
V_{CCO2}	G35, L35, M35, N35, U35, V35	AA11, AF13, AH10, W15, Y12, Y13, Y14, Y15
V_{CCO3}	AB35, AC35, AG35, AJ35, AL35, AN35	AA20, AF18, AH21, W16, Y16, Y17, Y18, Y19
V_{CCO4}	AR22, AR23, AR27, AR28, AR29, AR33	AA28, T19, T20, U20, V20, V26, W20, Y21
V_{CCO5}	AR11, AR13, AR17, AR18, AR7, AR9	K28, L21, M20, N20, N26, P20, R19, R20
V_{CCO6}	AB5, AC5, AG5, AH5, AJ5, AN5	C21, E18, K20, L16, L17, L18, L19, M16
V_{CCO7}	G5, J5, L5, N5, U5, V5	C10, E13, K11, L12, L13, L14, L15, M15
V_{CCP}	E20, AW22	R5, T26
V_{CCJ}	D3	B3
GND	A1, A2, A20, A38, A39, AE3, AE37, AK3, AK37, AR36, AR4, AT20, AT35, AT5, AU10, AU14, AU20, AU26, AU30, AV1, AV2, AV20, AV38, AV39, AW1, AW2, AW20, AW38, AW39, B1, B2, B20, B38, B39, C10, C14, C20, C26, C30, D20, D35, D5, E36, E4, K3, K37, P37, R3, Y1, Y2, Y3, Y36, Y37, Y38, Y39, Y4	A1, A2, A29, A30, AB28, AB3, AG27, AG4, AH22, AH28, AH3, AH9, AJ1, AJ2, AJ29, AJ30, AK1, AK2, AK29, AK30, B1, B2, B29, B30, C22, C28, C3, C9, D27, D4, J28, J3, N13, N14, N15, N16, N17, N18, P13, P14, P15, P16, P17, P18, R13, R14, R15, R16, R17, R18, T13, T14, T15, T16, T17, T18, U13, U14, U15, U16, U17, U18, V13, V14, V15, V16, V17, V18
GND_P	AR20, A21	R28, T3

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
M15	BK4_IO5	-	54N/HSI2	BK4_IO5	-	46N
M14	BK4_IO8	-	56P/HSI2	BK4_IO6	-	47P
M13	BK4_IO9	VREF4	56N/HSI2	BK4_IO7	VREF4	47N
-	GND (Bank 4)	-	-	-	-	-
L13	BK4_IO12	PLL_RST4	58P/HSI2	BK4_IO8	PLL_RST4	48P
L14	BK4_IO13	PLL_RST5	58N/HSI2	BK4_IO9	PLL_RST5	48N
N16	BK4_IO14	HSI2B_SOUTP	59P/HSI2	BK4_IO10	-	49P
M16	BK4_IO15	HSI2B_SOUTN	59N/HSI2	BK4_IO11	-	49N
-	-	-	-	GND (Bank 4)	-	-
L15	BK4_IO18	SS_CLKIN1P	61P	BK4_IO14	SS_CLKIN1P	51P
-	GND (Bank 4)	-	-	-	-	-
K15	BK4_IO19	SS_CLKIN1N	61N	BK4_IO15	SS_CLKIN1N	51N
K14	BK4_IO20	PLL_FBK4	62P	BK4_IO16	PLL_FBK4	52P
K13	BK4_IO21	PLL_FBK5	62N	BK4_IO17	PLL_FBK5	52N
L16	BK4_IO22	SS_CLKOUT1P	63P	BK4_IO18	SS_CLKOUT1P	53P
-	-	-	-	GND (Bank 4)	-	-
K16	BK4_IO23	SS_CLKOUT1N	63N	BK4_IO19	SS_CLKOUT1N	53N
J13	BK4_IO24	CLK_OUT4	64P	BK4_IO20	CLK_OUT4	54P
J12	BK4_IO25	CLK_OUT5	64N	BK4_IO21	CLK_OUT5	54N
-	GND (Bank 4)	-	-	-	-	-
J14	GCLK4	-	LVDS Pair2P	GCLK4	-	LVDS Pair2P
H14	GCLK5	-	LVDS Pair2N	GCLK5	-	LVDS Pair2N
J15	VCCP1	-	-	VCCP1	-	-
H15	GNDP1	-	-	GNDP1	-	-
J16	GCLK6	-	LVDS Pair3P	GCLK6	-	LVDS Pair3P
H16	GCLK7	-	LVDS Pair3N	GCLK7	-	LVDS Pair3N
-	GND (Bank 5)	-	-	-	-	-
H12	BK5_IO0	CLK_OUT6	65P	BK5_IO0	CLK_OUT6	55P
H13	BK5_IO1	CLK_OUT7	65N	BK5_IO1	CLK_OUT7	55N
G14	BK5_IO2	-	66P	BK5_IO2	-	56P
-	-	-	-	GND (Bank 5)	-	-
G15	BK5_IO3	PLL_RST7	66N	BK5_IO3	PLL_RST7	56N
G13	BK5_IO6	PLL_RST6	68P	BK5_IO6	PLL_RST6	58P/HSI1
-	GND (Bank 5)	-	-	-	-	-
F13	BK5_IO7	PLL_FBK7	68N	BK5_IO7	PLL_FBK7	58N/HSI1
G16	BK5_IO10	HSI3A_SINP	70P	BK5_IO8	HSI1A_SINP	59P/HSI1
-	-	-	-	GND (Bank 5)	-	-
F16	BK5_IO11	HSI3A_SINN	70N/HSI3	BK5_IO9	HSI1A-SINN	59N/HSI1
F14	BK5_IO12	-	71P/HSI3	BK5_IO10	-	60P/HSI1
F15	BK5_IO13	-	71N/HSI3	BK5_IO11	-	60N/HSI1
E16	BK5_IO14	HSI3A_SOUTP	72P/HSI3	BK5_IO12	HSI1A_SOUTP	61P/HSI1
-	GND (Bank 5)	-	-	-	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
E4	BK0_IO0	-	0P	BK0_IO0	-	0P/HSI0	NC	-	-
D3	BK0_IO1	-	0N	BK0_IO1	-	0N/HSI0	NC	-	-
E3	BK0_IO2	HSI0A_SOUTP	1P/HSI0	BK0_IO2	HSI0A_SOUTP	1P/HSI0	BK0_IO0	HSI0A_SOUTP	0P
-	GND (Bank 0)	-	-	GND (Bank 0)	-	-	-	-	-
F3	BK0_IO3	HSI0A_SOUTN	1N/HSI0	BK0_IO3	HSI0A_SOUTN	1N/HSI0	BK0_IO1	HSI0A_SOUTN	0N
C2	BK0_IO4	-	2P/HSI0	BK0_IO4	-	2P/HSI0	BK0_IO2	-	1P/HSI0
B1	BK0_IO5	-	2N/HSI0	BK0_IO5	-	2N/HSI0	BK0_IO3	-	1N/HSI0
G4	BK0_IO6	HSI0A_SINP	3P/HSI0	BK0_IO6	HSI0A_SINP	3P/HSI0	BK0_IO4	HSI0A_SINP	2P/HSI0
-	-	-	-	-	-	-	GND (Bank 0)	-	-
G3	BK0_IO7	HSI0A_SINN	3N/HSI0	BK0_IO7	HSI0A_SINN	3N/HSI0	BK0_IO5	HSI0A_SINN	2N/HSI0
C1	BK0_IO8	-	4P/HSI0	BK0_IO8	-	4P/HSI0	BK0_IO6	-	3P/HSI0
D2	BK0_IO9	VREF0	4N/HSI0	BK0_IO9	VREF0	4N/HSI0	BK0_IO7	VREF0	3N/HSI0
H4	BK0_IO10	HSI0B_SOUTP	5P/HSI0	BK0_IO10	HSI0B_SOUTP	5P/HSI0	BK0_IO8	HSI0B_SOUTP	4P/HSI0
-	GND (Bank 0)	-	-	GND (Bank 0)	-	-	-	-	-
H3	BK0_IO11	HSI0B_SOUTN	5N/HSI0	BK0_IO11	HSI0B_SOUTN	5N/HSI0	BK0_IO9	HSI0B_SOUTN	4N/HSI0
D1	BK0_IO12	-	6P/HSI0	BK0_IO12	-	6P/HSI0	BK0_IO10	-	5P/HSI0
E1	BK0_IO13	-	6N/HSI0	BK0_IO13	-	6N/HSI0	BK0_IO11	-	5N/HSI0
E2	BK0_IO14	HSI0B_SINP	7P/HSI0	BK0_IO14	HSI0B_SINP	7P/HSI0	BK0_IO12	HSI0B_SINP	6P/HSI0
-	-	-	-	-	-	-	GND (Bank 0)	-	-
F2	BK0_IO15	HSI0B_SINN	7N/HSI0	BK0_IO15	HSI0B_SINN	7N/HSI0	BK0_IO13	HSI0B_SINN	6N/HSI0
G2	BK0_IO16	-	8P/HSI0	NC	-	-	NC	-	-
F1	BK0_IO17	-	8N/HSI0	NC	-	-	NC	-	-
J3	BK0_IO18	HSI1A_SOUTP	9P	NC	-	-	NC	-	-
-	GND (Bank 0)	-	-	-	-	-	-	-	-
K3	BK0_IO19	HSI1A_SOUTN	9N	NC	-	-	NC	-	-
K4	BK0_IO20	-	10P	NC	-	-	NC	-	-
L4	BK0_IO21	-	10N	NC	-	-	NC	-	-
H2	BK0_IO22	HSI1A_SINP	11P	NC	-	-	NC	-	-
J2	BK0_IO23	HSI1A_SINN	11N	NC	-	-	NC	-	-
G1	BK0_IO24	-	12P	NC	-	-	NC	-	-
H1	BK0_IO25	-	12N	NC	-	-	NC	-	-
L3	BK0_IO26	HSI1B_SOUTP	13P	NC	-	-	NC	-	-
-	GND (Bank 0)	-	-	-	-	-	-	-	-
M3	BK0_IO27	HSI1B_SOUTN	13N	NC	-	-	NC	-	-
K2	BK0_IO28	-	14P	NC	-	-	NC	-	-
L2	BK0_IO29	-	14N	NC	-	-	NC	-	-
K1	BK0_IO30	HSI1B_SINP	15P	NC	-	-	NC	-	-
L1	BK0_IO31	HSI1B_SINN	15N	NC	-	-	NC	-	-
M2	BK0_IO32	-	16P	BK0_IO16	-	8P	NC	-	-
M1	BK0_IO33	-	16N	BK0_IO17	-	8N	NC	-	-
N3	BK0_IO34	PLL_FBK0	17P	BK0_IO18	PLL_FBK0	9P	BK0_IO14	PLL_FBK0	7P/HSI0
-	GND (Bank 0)	-	-	GND (Bank 0)	-	-	-	-	-
N4	BK0_IO35	PLL_RST1	17N	BK0_IO19	PLL_RST1	9N	BK0_IO15	PLL_RST1	7N/HSI0
N2	BK0_IO36	-	18P	BK0_IO20	-	10P	BK0_IO16	-	8P/HSI0
N1	BK0_IO37	PLL_FBK1	18N	BK0_IO21	PLL_FBK1	10N	BK0_IO17	PLL_FBK1	8N/HSI0
P1	BK0_IO38	PLL_RST0	19P	BK0_IO22	PLL_RST0	11P	BK0_IO18	PLL_RST0	9P
-	-	-	-	-	-	-	GND (Bank 0)	-	-
R1	BK0_IO39	-	19N	BK0_IO23	-	11N	BK0_IO19	-	9N
P3	BK0_IO40	CLK_OUT0	20P	BK0_IO24	CLK_OUT0	12P	BK0_IO20	CLK_OUT0	10P
-	GND (Bank 0)	-	-	-	-	-	-	-	-
P2	BK0_IO41	CLK_OUT1	20N	BK0_IO25	CLK_OUT1	12N	BK0_IO21	CLK_OUT1	10N

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
C24	BK1_IO7	SS_CLKIN0N	34N
A22	BK1_IO8	-	35P
D22	BK1_IO9	-	35N
A23	BK1_IO10	-	36P
-	GND (Bank 1)	-	-
B25	BK1_IO11	-	36N
D23	BK1_IO12	PLL_RST2	37P
A24	BK1_IO13	PLL_RST3	37N
A25	BK1_IO14	-	38P
E24	BK1_IO15	-	38N
D24	BK1_IO16	-	39P
A26	BK1_IO17	-	39N
D25	BK1_IO18	-	40P
-	GND (Bank 1)	-	-
C25	BK1_IO19	-	40N
B26	BK1_IO20	-	41P/HSI3
B27	BK1_IO21	-	41N/HSI3
D26	BK1_IO22	-	42P/HSI3
A27	BK1_IO23	-	42N/HSI3
A28	BK1_IO24	-	43P/HSI3
E26	BK1_IO25	-	43N/HSI3
C27	BK1_IO26	HSI3A_SOUTP	44P/HSI3
-	GND (Bank 1)	-	-
D27	BK1_IO27	HSI3A_SOUTN	44N/HSI3
B28	BK1_IO28	-	45P/HSI3
A30	BK1_IO29	-	45N/HSI3
C28	BK1_IO30	HSI3A_SINP	46P/HSI3
D28	BK1_IO31	HSI3A_SINN	46N/HSI3
A31	BK1_IO32	-	47P/HSI3
B30	BK1_IO33	-	47N/HSI3
E28	BK1_IO34	HSI3B_SOUTP	48P/HSI3
-	GND (Bank 1)	-	-
D29	BK1_IO35	HSI3B_SOUTN	48N/HSI3
C29	BK1_IO36	-	49P/HSI4
B31	BK1_IO37	-	49N/HSI4
D30	BK1_IO38	HSI3B_SINP	50P/HSI4
E30	BK1_IO39	HSI3B_SINN	50N/HSI4
A32	BK1_IO40	-	51P/HSI4
C31	BK1_IO41	-	51N/HSI4
D31	BK1_IO42	HSI4A_SOUTP	52P/HSI4
-	GND (Bank 1)	-	-
C32	BK1_IO43	HSI4A_SOUTN	52N/HSI4
B32	BK1_IO44	-	53P/HSI4

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
V39	BK2_IO57	-	90N
W37	BK2_IO58	-	91P
-	GND (Bank 2)	-	-
W38	BK2_IO59	-	91N
W39	BK2_IO60	-	92P
AA39	BK2_IO61	-	92N
-	GND (Bank 2)	-	-
-	GND (Bank 3)	-	-
AA38	BK3_IO0	-	93P
Y35	BK3_IO1	-	93N
AA37	BK3_IO2	-	94P
-	GND (Bank 3)	-	-
AA35	BK3_IO3	-	94N
AB39	BK3_IO4	-	95P
AB38	BK3_IO5	-	95N
AA36	BK3_IO6	-	96P
AB37	BK3_IO7	-	96N
AC39	BK3_IO8	-	97P
AC38	BK3_IO9	-	97N
AB36	BK3_IO10	-	98P
-	GND (Bank 3)	-	-
AC37	BK3_IO11	-	98N
AC36	BK3_IO12	-	99P
AD39	BK3_IO13	-	99N
AD37	BK3_IO14	-	100P
AD36	BK3_IO15	-	100N
AD35	BK3_IO16	-	101P
AE38	BK3_IO17	-	101N
AD38	BK3_IO18	-	102P
-	GND (Bank 3)	-	-
AE39	BK3_IO19	-	102N
AF38	BK3_IO20	-	103P
AF37	BK3_IO21	-	103N
AF39	BK3_IO22	-	104P
AE36	BK3_IO23	-	104N
AF36	BK3_IO24	-	105P
AG38	BK3_IO25	-	105N
AG39	BK3_IO26	-	106P
-	GND (Bank 3)	-	-
AG37	BK3_IO27	-	106N
AH37	BK3_IO28	-	107P
AH38	BK3_IO29	-	107N
AG36	BK3_IO30	-	108P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
-	GND (Bank 4)	-	-
AW26	BK4_IO43	-	145N
AV25	BK4_IO44	-	146P
AT24	BK4_IO45	-	146N
AU24	BK4_IO46	-	147P
AU25	BK4_IO47	-	147N
AW25	BK4_IO48	PLL_RST4	148P
AW24	BK4_IO49	PLL_RST5	148N
AU23	BK4_IO50	-	149P
-	GND (Bank 4)	-	-
AT23	BK4_IO51	-	149N
AV24	BK4_IO52	-	150P
AW23	BK4_IO53	-	150N
AV23	BK4_IO54	SS_CLKIN1P	151P
AU22	BK4_IO55	SS_CLKIN1N	151N
AR21	BK4_IO56	PLL_FBK4	152P
AT22	BK4_IO57	PLL_FBK5	152N
AV22	BK4_IO58	SS_CLKOUT1P	153P
-	GND (Bank 4)	-	-
AV21	BK4_IO59	SS_CLKOUT1N	153N
AT21	BK4_IO60	CLK_OUT4	154P
AU21	BK4_IO61	CLK_OUT5	154N
-	GND (Bank 4)	-	-
AT19	GCLK4	-	LVDS Pair2P
AU19	GCLK5	-	LVDS Pair2N
AW22	VCCP1	-	-
AR20	GNDP1	-	-
AU18	GCLK6	-	LVDS Pair3P
AT18	GCLK7	-	LVDS Pair3N
-	GND (Bank 5)	-	-
AV17	BK5_IO0	CLK_OUT6	155P
AV18	BK5_IO1	CLK_OUT7	155N
AW21	BK5_IO2	PLL_FBK6	156P
-	GND (Bank 5)	-	-
AV19	BK5_IO3	PLL_FBK7	156N
AR19	BK5_IO4	-	157P/HSI7
AW19	BK5_IO5	-	157N/HSI7
AW18	BK5_IO6	PLL_RST6	158P/HSI7
AW17	BK5_IO7	PLL_RST7	158N/HSI7
AT17	BK5_IO8	-	159P/HSI7
AV16	BK5_IO9	-	159N/HSI7
AU17	BK5_IO10	HSI7A_SINP	160P/HSI7
-	GND (Bank 5)	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AB1	BK1_IO35	HSI3B_SOUTN	48N/HSI3	NC	-	-
AC6	BK1_IO36	-	49P/HSI4	NC	-	-
AC5	BK1_IO37	-	49N/HSI4	NC	-	-
AC2	BK1_IO38	HSI3B_SINP	50P/HSI4	NC	-	-
AC1	BK1_IO39	HSI3B_SINN	50N/HSI4	NC	-	-
AC4	BK1_IO40	-	51P/HSI4	NC	-	-
AC3	BK1_IO41	-	51N/HSI4	NC	-	-
AD2	BK1_IO42	HSI4A_SOUTP	52P/HSI4	NC	-	-
-	GND (Bank 1)	-	-	-	-	-
AD1	BK1_IO43	HSI4A_SOUTN	52N/HSI4	NC	-	-
AD3	BK1_IO44	-	53P/HSI4	BK1_IO32	-	37P/HSI3
AD4	BK1_IO45	-	53N/HSI4	BK1_IO33	-	37N
AE2	BK1_IO46	HSI4A_SINP	54P/HSI4	BK1_IO34	-	38P
AE1	BK1_IO47	HSI4A_SINN	54N/HSI4	BK1_IO35	-	38N
AD5	BK1_IO48	-	55P/HSI4	BK1_IO25	-	33N
AD6	BK1_IO49	VREF1	55N/HSI4	BK1_IO24	VREF1	33P
AF2	BK1_IO50	HSI4B_SOUTP	56P/HSI4	BK1_IO26	HSI2B_SOUTP	34P
-	GND (Bank 1)	-	-	-	-	-
AF1	BK1_IO51	HSI4B_SOUTN	56N/HSI4	BK1_IO27	HSI2B_SOUTN	34N
AE3	BK1_IO52	-	57P	BK1_IO28	-	35P
AE4	BK1_IO53	-	57N	BK1_IO29	-	35N
AG1	BK1_IO54	HSI4B_SINP	58P	BK1_IO30	HSI2B_SINP	36P
-	-	-	-	GND (Bank 1)	-	-
AG2	BK1_IO55	HSI4B_SINN	58N	BK1_IO31	HSI2B_SINN	36N
AE5	BK1_IO56	-	59P	BK1_IO36	-	39P
AF4	BK1_IO57	-	59N	BK1_IO37	-	39N
AH1	BK1_IO58	-	60P	BK1_IO38	-	40P
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-
AH2	BK1_IO59	-	60N	BK1_IO39	-	40N
AF3	BK1_IO60	-	61P	BK1_IO40	-	41P
AG3	BK1_IO61	-	61N	BK1_IO41	-	41N
AH4	TCK	-	-	TCK	-	-
AJ3	TMS	-	-	TMS	-	-
AK3	TOE	-	-	TOE	-	-
AG5	BK2_IO0	-	62P	BK2_IO0	-	42P
AH5	BK2_IO1	-	62N	BK2_IO1	-	42N
AJ4	BK2_IO2	-	63P	BK2_IO2	-	43P
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
AK4	BK2_IO3	-	63N	BK2_IO3	-	43N
AG6	BK2_IO4	-	64P	BK2_IO4	-	44P
AH6	BK2_IO5	-	64N	BK2_IO5	-	44N
AJ5	BK2_IO6	-	65P	BK2_IO6	-	45P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AJ25	BK3_IO50	-	118P	BK3_IO30	-	78P
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-
AK25	BK3_IO51	-	118N	BK3_IO31	-	78N
AF24	BK3_IO52	-	119P	BK3_IO32	-	79P
AE24	BK3_IO53	-	119N	BK3_IO33	-	79N
AK26	BK3_IO54	-	120P	BK3_IO34	-	80P
AJ26	BK3_IO55	-	120N	BK3_IO35	-	80N
AH25	BK3_IO56	-	121P	BK3_IO36	-	81P
AG25	BK3_IO57	-	121N	BK3_IO37	-	81N
AK27	BK3_IO58	-	122P	BK3_IO38	-	82P
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-
AJ27	BK3_IO59	-	122N	BK3_IO39	-	82N
AG26	BK3_IO60	-	123P	BK3_IO40	-	83P
AH26	BK3_IO61	-	123N	BK3_IO41	-	83N
AK28	GSR	-	-	GSR	-	-
AJ28	DXP	-	-	DXP	-	-
AH27	DXN	-	-	DXN	-	-
AG28	BK4_IO0	-	124P	BK4_IO0	-	84P
AF27	BK4_IO1	-	124N	BK4_IO1	-	84N
AF28	BK4_IO2	-	125P	BK4_IO2	-	85P/HSI3
-	GND (Bank 4)	-	-	GND (Bank 4)	-	-
AE26	BK4_IO3	-	125N	BK4_IO3	-	85N/HSI3
AE27	BK4_IO4	-	126P	BK4_IO4	-	86P/HSI3
AE28	BK4_IO5	-	126N	BK4_IO5	-	86N/HSI3
AH30	BK4_IO6	HSI5A_SINP	127P	BK4_IO10	HSI3A_SINP	89P/HSI3
-	-	-	-	GND (Bank 4)	-	-
AH29	BK4_IO7	HSI5A_SINN	127N	BK4_IO11	HSI3A_SINN	89N/HSI3
AD25	BK4_IO8	-	128P	BK4_IO12	-	90P/HSI3
AD26	BK4_IO9	-	128N	BK4_IO13	-	90N/HSI3
AG29	BK4_IO10	HSI5A_SOUTP	129P/HSI5	BK4_IO14	HSI3A_SOUTP	91P/HSI3
-	GND (Bank 4)	-	-	-	-	-
AG30	BK4_IO11	HSI5A_SOUTN	129N/HSI5	BK4_IO15	HSI3A_SOUTN	91N/HSI3
AD27	BK4_IO12	VREF4	130P/HSI5	BK4_IO17	VREF4	92N/HSI3
AD28	BK4_IO13	-	130N/HSI5	BK4_IO16	-	92P/HSI3
AF29	BK4_IO14	HSI5B_SINP	131P/HSI5	BK4_IO6	-	87P/HSI3
AF30	BK4_IO15	HSI5B_SINN	131N/HSI5	BK4_IO7	-	87N/HSI3
AC25	BK4_IO16	-	132P/HSI5	BK4_IO8	-	88P/HSI3
AC26	BK4_IO17	-	132N/HSI5	BK4_IO9	-	88N/HSI3
AE29	BK4_IO18	HSI5B_SOUTP	133P/HSI5	NC	-	-
-	GND (Bank 4)	-	-	-	-	-
AE30	BK4_IO19	HSI5B_SOUTN	133N/HSI5	NC	-	-
AC28	BK4_IO20	-	134P/HSI5	NC	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
U27	BK4_IO57	PLL_FBK5	152N	BK4_IO37	PLL_FBK5	102N
U29	BK4_IO58	SS_CLKOUT1P	153P	BK4_IO38	SS_CLKOUT1P	103P
-	GND (Bank 4)	--	-	-	-	-
U30	BK4_IO59	SS_CLKOUT1N	153N	BK4_IO39	SS_CLKOUT1N	103N
T30	BK4_IO60	CLK_OUT4	154P	BK4_IO40	CLK_OUT4	104P
-	-	-	-	GND (Bank 4)	-	-
T29	BK4_IO61	CLK_OUT5	154N	BK4_IO41	CLK_OUT5	104N
-	GND (Bank 4)	-	-	-	-	-
T28	GCLK4	-	LVDS Pair2P	GCLK4	-	LVDS Pair2P
T27	GCLK5	-	LVDS Pair2N	GCLK5	-	LVDS Pair2N
T26	VCCP1	-	-	VCCP1	-	-
R28	GNDP1	-	-	GNDP1	-	-
R27	GCLK6	-	LVDS Pair3P	GCLK6	-	LVDS Pair3P
R26	GCLK7	-	LVDS Pair3N	GCLK7	-	LVDS Pair3N
-	GND (Bank 5)	-	-	-	-	-
R29	BK5_IO0	CLK_OUT6	155P	BK5_IO0	CLK_OUT6	105P
-	-	-	-	GND (Bank 5)	-	-
R30	BK5_IO1	CLK_OUT7	155N	BK5_IO1	CLK_OUT7	105N
P30	BK5_IO2	PLL_FBK6	156P	BK5_IO4	PLL_FBK6	107P
-	GND (Bank 5)	-	-	GND (Bank 5)	-	-
P29	BK5_IO3	PLL_FBK7	156N	BK5_IO7	PLL_FBK7	108N
P27	BK5_IO4	-	157P/HSI7	BK5_IO2	-	106P
P28	BK5_IO5	-	157N/HSI7	BK5_IO5	-	107N
P26	BK5_IO6	PLL_RST6	158P/HSI7	BK5_IO6	PLL_RST6	108P
P25	BK5_IO7	PLL_RST7	158N/HSI7	BK5_IO3	PLL_RST7	106N
N27	BK5_IO8	-	159P/HSI7	BK5_IO8	-	109P/HSI4
N28	BK5_IO9	-	159N/HSI7	BK5_IO9	-	109N/HSI4
N29	BK5_IO10	HSI7A_SINP	160P/HSI7	BK5_IO10	HSI4A_SINP	110P/HSI4
-	GND (Bank 5)	-	-	-	-	-
N30	BK5_IO11	HSI7A_SINN	160N/HSI7	BK5_IO11	HSI4A_SINN	110N/HSI4
N25	BK5_IO12	-	161P/HSI7	BK5_IO12	-	111P/HSI4
N24	BK5_IO13	-	161N/HSI7	BK5_IO13	-	111N/HSI4
M29	BK5_IO14	HSI7A_SOUTP	162P/HSI7	BK5_IO14	HSI4A_SOUTP	112P/HSI4
-	-	-	-	GND (Bank 5)	-	-
M30	BK5_IO15	HSI7A_SOUTN	162N/HSI7	BK5_IO15	HSI4A_SOUTN	112N/HSI4
M28	BK5_IO16	-	163P/HSI7	BK5_IO16	-	113P/HSI4
M27	BK5_IO17	-	163N/HSI7	BK5_IO17	-	113N/HSI4
L30	BK5_IO18	HSI7B_SINP	164P/HSI7	BK5_IO18	HSI4B_SINP	114P/HSI4
-	GND (Bank 5)	-	-	-	-	-
L29	BK5_IO19	HSI7B_SINN	164N/HSI7	BK5_IO19	HSI4B_SINN	114N/HSI4
M26	BK5_IO20	-	165P/HSI8	BK5_IO20	-	115P/HSI4
M25	BK5_IO21	-	165N/HSI8	BK5_IO21	-	115N/HSI4

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
B15	BK7_IO1	-	217N	BK7_IO1	-	147N
C15	BK7_IO2	-	218P	BK7_IO2	-	148P
-	GND (Bank 7)	-	-		-	-
D15	BK7_IO3	-	218N	BK7_IO3	-	148N
E15	BK7_IO4	-	219P	BK7_IO4	-	149P
F15	BK7_IO5	-	219N	BK7_IO5	-	149N
A14	BK7_IO6	-	220P	BK7_IO6	-	150P
-	-	-	-	GND (Bank 7)	-	-
B14	BK7_IO7	-	220N	BK7_IO7	-	150N
C14	BK7_IO8	-	221P	BK7_IO8	-	151P
D14	BK7_IO9	-	221N	BK7_IO9	-	151N
E14	BK7_IO10	-	222P	BK7_IO10	-	152P
-	GND (Bank 7)	-	-	-	-	-
F14	BK7_IO11	-	222N	BK7_IO11	-	152N
C13	BK7_IO12	-	223P	BK7_IO12	-	153P
D13	BK7_IO13	-	223N	BK7_IO13	-	153N
B13	BK7_IO14	-	224P	BK7_IO14	-	154P
-	-	-	-	GND (Bank 7)	-	-
A13	BK7_IO15	-	224N	BK7_IO15	-	154N
F13	BK7_IO16	-	225P	BK7_IO16	-	155P
G13	BK7_IO17	-	225N	BK7_IO17	-	155N
A12	BK7_IO18	-	226P	BK7_IO18	-	156P
-	GND (Bank 7)	-	-	-	-	-
B12	BK7_IO19	-	226N	BK7_IO19	-	156N
C12	BK7_IO20	-	227P	NC	-	-
D12	BK7_IO21	-	227N	NC	-	-
A11	BK7_IO22	-	228P	NC	-	-
B11	BK7_IO23	-	228N	NC	-	-
E12	BK7_IO24	-	229P	NC	-	-
F12	BK7_IO25	-	229N	NC	-	-
C11	BK7_IO26	-	230P	NC	-	-
-	GND (Bank 7)	-	-	-	-	-
D11	BK7_IO27	-	230N	NC	-	-
E11	BK7_IO28	-	231P	NC	-	-
F11	BK7_IO29	-	231N	NC	-	-
B10	BK7_IO30	-	232P	NC	-	-
A10	BK7_IO31	-	232N	NC	-	-
D10	BK7_IO32	-	233P	NC	-	-
E10	BK7_IO33	-	233N	NC	-	-
A9	BK7_IO34	-	234P	NC	-	-
-	GND (Bank 7)	-	-	-	-	-
B9	BK7_IO35	-	234N	NC	-	-