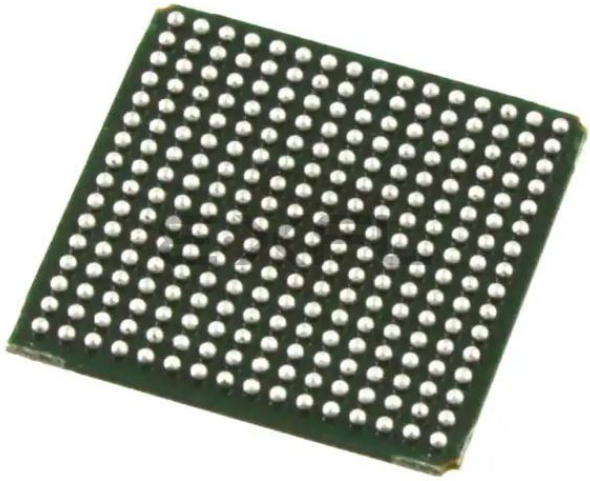

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	2704
Total RAM Bits	113664
Number of I/O	160
Number of Gates	210000
Voltage - Supply	2.3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx200b-03f256c

ispXPGA® Family

Includes High-Performance, Low-Cost "E-Series"

February 2010

Data Sheet DS1026

- **Non-volatile, Infinitely Reconfigurable**
  - Instant-on - Powers up in microseconds via on-chip E²CMOS® based memory
  - No external configuration memory
  - Excellent design security, no bit stream to intercept
  - Reconfigure SRAM based logic in milliseconds
- **High Logic Density for System-level Integration**
  - 139K to 1.25M functional gates
  - 160 to 496 I/O
  - 1.8V, 2.5V, and 3.3V V_{CC} operation
  - Up to 414Kb sysMEM™ embedded memory
- **High Performance Programmable Function Unit (PFU)**
  - Four LUT-4 per PFU supports wide and narrow functions
  - Dual flip-flops per LUT-4 for extensive pipelining
  - Dedicated logic for adders, multipliers, multiplexers, and counters
- **Flexible Memory Resources**
  - Multiple sysMEM Embedded RAM Blocks
    - Single port, Dual port, and FIFO operation
  - 64-bit distributed memory in each PFU
    - Single port, Double port, FIFO, and Shift Register operation
- **Flexible Programming, Reconfiguration, and Testing**
  - Supports IEEE 1532 and 1149.1
  - Microprocessor configuration interface
  - Program E²CMOS while operating from SRAM
- **Eight sysCLOCK™ Phase Locked Loops (PLLs) for Clock Management**
  - True PLL technology
  - 10MHz to 320MHz operation
  - Clock multiplication and division
  - Phase adjustment
  - Shift clocks in 250ps steps
- **sysIO™ for High System Performance**
  - High speed memory support through SSTL and HSTL
  - Advanced buses supported through PCI, GTL+, LVDS, BLVDS, and LVPECL
  - Standard logic supported through LVTTL, LVCMOS 3.3, 2.5 and 1.8
  - 5V tolerant I/O for LVCMOS 3.3 and LVTTL interfaces
  - Programmable drive strength for series termination
  - Programmable bus maintenance
- **Two Options Available**
  - High-performance sysHSI (standard part number)
  - Low-cost, no sysHSI ("E-Series")
- **sysHSI™ Capability for Ultra Fast Serial Communications**
  - Up to 800Mbps performance
  - Up to 20 channels per device
  - Built in Clock Data Recovery (CDR) and Serialization and De-serialization (SERDES)

Table 1. ispXPGA Family Selection Guide

	ispXPGA 125/E	ispXPGA 200/E	ispXPGA 500/E	ispXPGA 1200/E[3]
Functional Gates	139K	210K	476K	1.25M
PFUs	484	676	1764	3844
LUT-4s	1936	2704	7056	15376
Logic FFs	3.8K	5.4K	14.1K	30.7K
sysMEM Memory	92K	111K	184K	414K
Distributed Memory	30K	43K	112K	246K
EBR	20	24	40	90
sysHSI Channels[1]	4	8	12	20
User I/O	160/176	160/208	336	496
Packaging	256 fpBGA 516 fpBGA[2]	256 fpBGA 516 fpBGA[2]	516 fpBGA[2] 900 fpBGA	680 fpSBGA 900 fpBGA

1. "E-Series" does not support sysHSI.
2. FH516 package was converted to F516 via PCN #09A-08.
3. Discontinued via PCN #03A-10.

Architecture Overview

The ispXPGA architecture is a symmetrical architecture consisting of an array of Programmable Function Units (PFUs) enclosed by Input Output Groups (PICs) with columns of sysMEM Embedded Block RAMs (EBRs) distributed throughout the array. Figure 1 illustrates the ispXPGA architecture. Each PIC has two corresponding sysIO blocks, each of which includes one input and output buffer. On two sides of the device, between the PICs and the sysIO blocks, there are sysHSI High-Speed Interface blocks. The symmetrical architecture allows designers to easily implement their designs, since any logic function can be placed in any section of the device.

The PFUs contain the basic building blocks to create logic, memory, arithmetic, and register functions. They are optimized for speed and flexibility allowing complex designs to be implemented quickly and efficiently.

The PICs interface the PFUs and EBRs to the external pins of the device. They allow the signals to be registered quickly to minimize setup times for high-speed designs. They also allow connections directly to the different logic elements for fast access to combinatorial functions.

The sysMEM EBRs are large, fast memory elements that can be configured as RAM, ROM, FIFO, and other storage types. They are designed to facilitate both single and dual-port memory for high-speed applications.

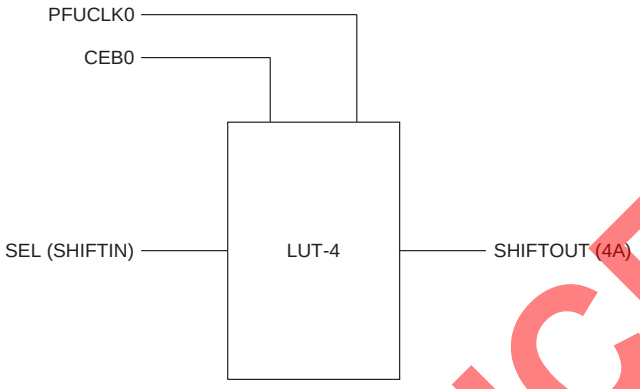
These three components of the architecture are interconnected via a high-speed, flexible routing array. The routing array consists of Variable Length Interconnect (VLI) lines between the PICs, PFUs, and EBRs. There is additional routing available to the PFU for feedback and direct routing of signals to adjacent PFUs or PICs.

The sysIO blocks consist of configurable input and output buffers connected directly to the PICs. These buffers can be configured to interface with 16 different I/O standards. This allows the ispXPGA to interface with other devices without the need for external transceivers.

The sysHSI blocks provide the necessary components to allow the ispXPGA device to transfer data at up to 800Mbps using the LVDS standard. These components include serializing, de-serializing, and clock data recovery (CDR) logic.

The sysCLOCK blocks provide clock multiplication/division, clock distribution, delay compensation, and increased performance through the use of PLL circuitry that manipulates the global clocks. There is one sysCLOCK block for each global clock tree in the device.

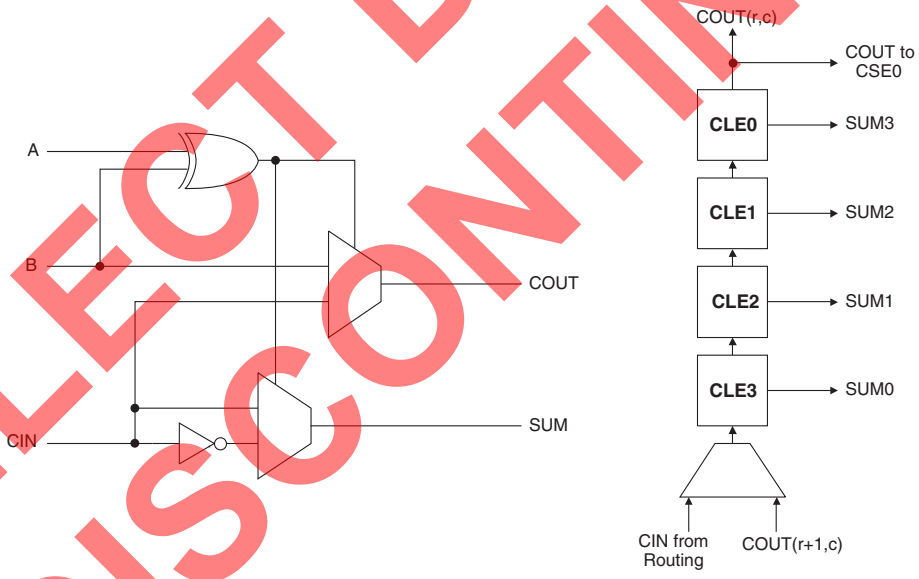
Figure 4. LUT in Shift Register Mode



Carry Chain Generator

The Carry Chain Generator is useful for implementing high-speed arithmetic functions. The CCG consists of a two-input XOR gate whose carryout can be cascaded with the input of the adjacent CCG. As shown in Figure 5, the carryin signal feeds CLE3 of the PFU and is propagated through CLE2 and CLE1 before reaching CLE0. The sum output of the CCG can be fed to the CSE through the WLG. The carryout must propagate to CLE0 for use outside the PFU. The carryout from the PFU can feed the W0 input of CSE0. The CCG also helps to effectively implement wider functions by using its logic elements to expand the capabilities of the LUT-4.

Figure 5. Carry Chain Generator



Wide Logic Generator

The WLG contains the logic necessary to implement wide gate functions. This is made up of a set of multiplexers that are located between the CLE and the CSE. The WLG helps in enhancing the wide gating capability of the PFU. The outputs of each CLE can be cascaded in the WLG to build wide gating functions. Wide multiplexing functions are also possible with a similar use of the WLG. Figure 6 illustrates the WLG.

Memory

The ispXPGA architecture provides a large amount of resources for memory intensive applications. Embedded Block RAMs (EBRs) are available to complement the Distributed Memory that is configured in the PFUs (see Look-Up Table -Distributed Memory Mode in the PFU section above). Each memory element can be configured as RAM or ROM. Additionally, the internal logic of the device can be used to configure the memory elements as FIFO and other storage types. These EBRs are referred to as sysMEM blocks. Refer to Table 1 for memory resources per device.

sysMEM Blocks

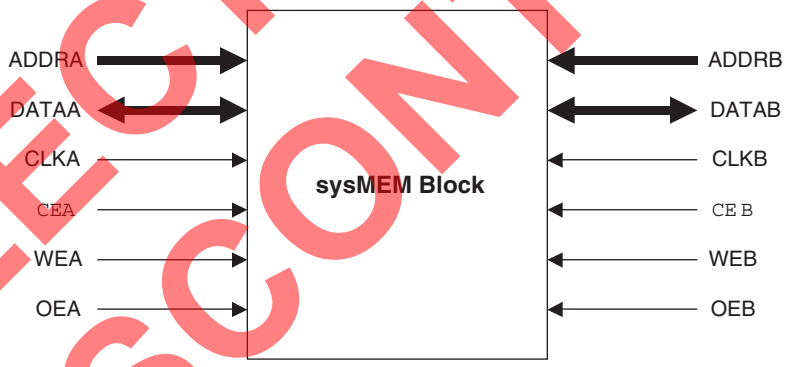
The sysMEM blocks are organized in columns distributed throughout the device. Each EBR contains 4.6K bits of dual-port RAM with dedicated control, address, and data lines for each port. Each column of sysMEM blocks has dedicated address and control lines that can be used by each block separately or cascaded to form larger memory elements. The memory cells are symmetrical and contain two sets of identical control signals. Each port has a read/write clock, clock enable, write enable, and output enable. Figure 12 illustrates the sysMEM block.

The ispXPGA memory block can operate as single-port or dual-port RAM. Supported configurations are:

- 512 x 9 bits single-port (8 bits data / 1 bit parity)
- 256 x 18 bits single-port (16 bits data / 2 bits parity)
- 512 x 9 bits dual-port (8 bits data / 1 bit parity)
- 256 x18 bits dual-port (16 bits data / 2 bits parity)

The data widths of “9” and “18” are ideal for applications where parity is necessary. This allows 9 data bits, 8 data bits plus a parity bit, 18 data bits, or 16 data bits plus two parity bits. The logic for generating and checking the parity must be customized separately.

Figure 12. sysMEM Block Diagram

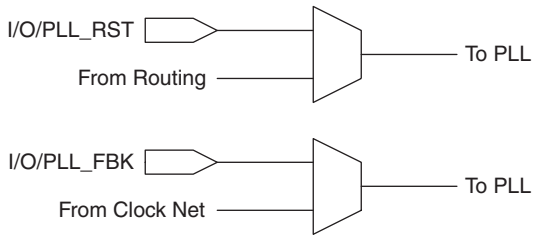


Read and Write Operations

The ispXPGA EBR has fully synchronous read and write operations as well as an asynchronous read operation. These operations allow several different types of memory to be implemented in the device.

Synchronous Read: The Clock Enable ($\overline{CE}$) and Write Enable (WE) signals control the synchronous read operation. When the $\overline{CE}$ signal is low, the clock is enabled. When the WE signal is low the read operation begins. Once the address (ADDR) is present, a rising clock edge (or falling edge depending on polarity) causes the stored data to be available on the DATA port. Figure 13 illustrates the synchronous read timing.

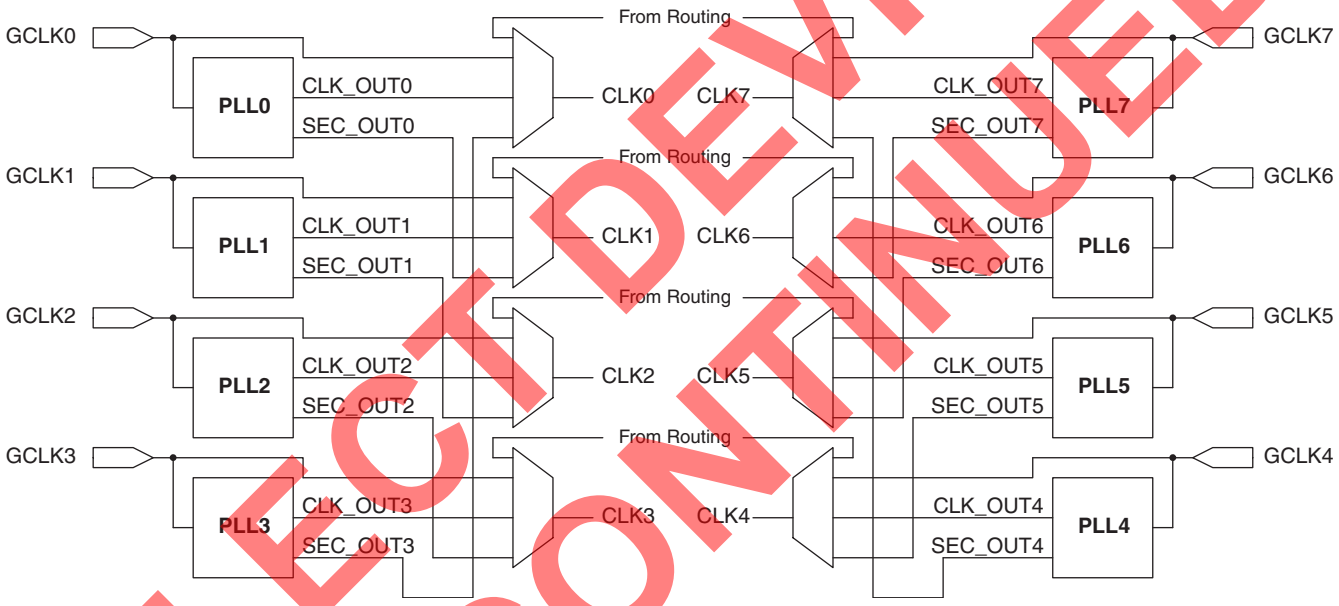
Figure 17. ispXPGA PLL_RST and PLL_FBK Generation



Clock Routing

The Global Clock Lines (GCLK) have two sources, their dedicated pins and the sysCLOCK circuit. Figure 18 illustrates the generation of the Global Clock Lines.

Figure 18. Global Clock Line Generation



sysIO Capability

All the ispXPGA devices have eight sysIO banks, where each bank is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage (V_{CCO}) and reference voltage (V_{REF}) resources allowing each bank complete independence from the others. Each I/O is individually configurable based on the bank's V_{CCO} and V_{REF} settings. In addition, each I/O has configurable drive strength, weak pull-up, weak pull-down, or a bus-keeper latch. Table 4 lists the number of I/Os supported per bank in each of the ispXPGA devices. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to V_{CCO} of 3.0V to 3.6V for LVCMOS 3.3, LVTTL and PCI interfaces.

Table 5 lists the sysIO standards with the typical values for V_{CCO}, V_{REF} and V_{TT}.

The TOE, JTAG TAP pins, PROGRAM, CFG0 and DONE pins of the ispXPGA device are the only pins that do not have the sysIO capabilities. The TOE and CFG0 pins operate off the V_{CC} of the device, supporting only the LVCMOS standard corresponding to the device supply voltage. The TAP pins have a separate supply voltage (V_{CCJ}), which determines the LVCMOS standard corresponding to that supply voltage.

There are three classes of I/O interface standards that are implemented in the ispXPGA devices. The first is the unterminated, single-ended interface. It includes the 3.3V LVTTL standard along with the 1.8V, 2.5V, and 3.3V LVCMOS interface standards. Additionally, PCI and AGP-1X are subsets of this type of interface.

The second type of interface implemented is the terminated, single-ended interface standard. This group of interfaces includes different versions of SSTL and HSTL interfaces along with CTT, and GTL+. Usage of these particular I/O interfaces requires an additional V_{REF} signal. At the system level a termination voltage, V_{TT}, is also required. Typically an output will be terminated to V_{TT} at the receiving end of the transmission line it is driving.

The third type of interface standards are the differential standards LVDS, BLVDS, and LVPECL. The differential standards require two I/O pins to create the differential pair. The logic level is determined by the difference in the two signals. Table 6 lists how these interface standards are implemented in the ispXPGA devices.

For more information on sysIO capability, refer to TN1000, sysIO Usage Guidelines for Lattice Devices.

Figure 19. sysIO Banks per Device

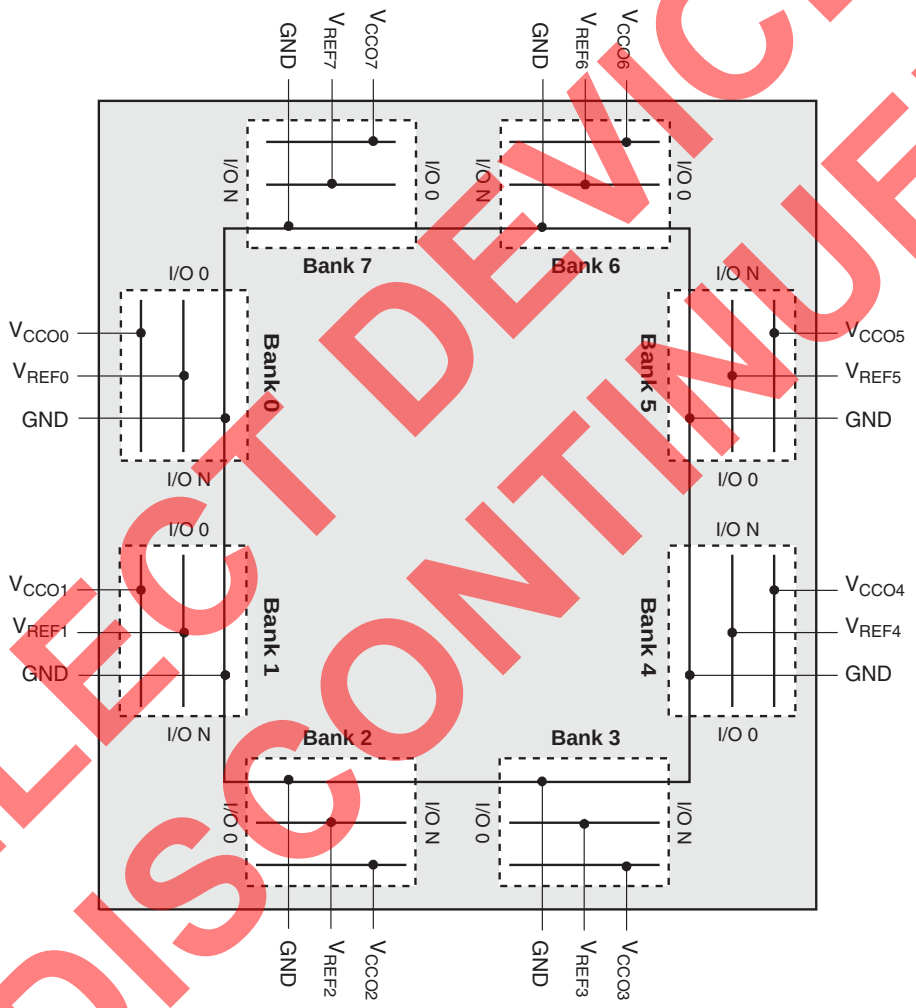


Table 4. Number of I/Os per Bank

Device	Max. Number of I/Os per Bank (N)
XPGA 1200	62
XPGA 500	42
XPGA 200	26
XPGA 125	22

Supply Current

Over Recommended Operating Conditions

Symbol	Parameter	Device	Condition	Min.	Typ.	Max.	Units
I_{CC}[1, 2]	Standby Core Operating Power Supply Current	LFX125	V_{CC} = 3.3V	—	60	—	mA
			V_{CC} = 2.5V	—	60	—	mA
			V_{CC} = 1.8V	—	40	—	mA
		LFX200	V_{CC} = 3.3V	—	70	—	mA
			V_{CC} = 2.5V	—	70	—	mA
			V_{CC} = 1.8V	—	50	—	mA
		LFX500	V_{CC} = 3.3V	—	120	—	mA
			V_{CC} = 2.5V	—	120	—	mA
			V_{CC} = 1.8V	—	100	—	mA
		LFX1200	V_{CC} = 3.3V	—	220	—	mA
			V_{CC} = 2.5V	—	220	—	mA
			V_{CC} = 1.8V	—	200	—	mA
I_{CCO}[3]	Standby Output Power Supply Current		V_{CCO} = 3.3V	—	2.0	—	mA
			V_{CCO} = 2.5V	—	2.0	—	mA
			V_{CCO} = 1.8V	—	2.0	—	mA
			V_{CCO} = 1.5V	—	2.0	—	mA
I_{CCP}[4]	Standby PLL Operating Supply Current		V_{CCP} = 3.3V	—	17.0	—	mA
			V_{CCP} = 2.5V	—	17.0	—	mA
			V_{CCP} = 1.8V	—	15.0	—	mA
I_{CCJ}[5]	Standby IEEE 1149.1 TAP Power Supply Current		V_{CCJ} = 3.3V	—	2.0	—	mA
			V_{CCJ} = 2.5V	—	1.5	—	mA
			V_{CCJ} = 1.8V	—	1.0	—	mA

1. T_A = 25°C, frequency = 1.0 MHz, device configured with 16-bit counters.
2. I_{CC} varies with specific device configuration and operating frequency. For more accurate power calculation, see TN1043, Power Estimation in ispXPGA Devices.
3. T_A = 25°C, per bank, no DC load, frequency = 0 MHz.
4. T_A = 25°C, per PLL, frequency = 10 MHz.
5. T_A = 25°C

sysIO Differential Standards DC Electrical Characteristics[1]

Parameter	Description	Test Conditions	Min.	Typ.	Max.
LVDS[2]					
V_{INP}, V_{INM}	Input voltage		0V	—	2.4V
V_{THD}	Differential input threshold	0.2V ð V_{CM} ð 1.8V	+/-100mV	—	—
I_{IN}	Input current	Power on	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	—	1.38V	1.60V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	0.9V	1.03V	—
V_{OD}	Output Voltage Differential	$\|V_{OP} - V_{OM}\|$, R_T = 100 ohm	250mV	350mV	450mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50mV
V_{OS}	Output Voltage Offset	$\|V_{OP} + V_{OM}\|/2$, R_T = 100 ohm	1.125V	1.25V	1.375V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50mV
I_{OSD}	Output short circuit current	V_{OD} = 0V Driver outputs shorted	—	—	24mA
BLVDS[1]					
V_{INP}, V_{INM}	Input voltage		0V	—	2.4V
V_{THD}	Differential input threshold	0.2V ð V_{CM} ð 1.8V	+/-100mV	—	—
I_{IN}	Input current	Power on	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 27Ω	—	1.4V	1.80V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 27Ω	0.95V	1.1V	—
V_{OD}	Output Voltage Differential	$\|V_{OP} - V_{OM}\|$, RT = 27Ω	240mV	300mV	460mV
ΔV_{OD}	Change in V_{OD} Between H and L				27mV
V_{OS}	Output Voltage Offset	$\|V_{OP} + V_{OM}\|$ /2, RT = 27Ω	1.1V	1.3V	1.5V
ΔV_{OS}	Change in V_{OS} Between H and L				27mV
I_{OSD}	Output Short Circuit Current	V_{OD} = 0. Driver Outputs Shorted.		36mA	65mA

1. Refer to TN1000, sysIO Usage Guidelines for Lattice Devices.
2. V_{OP} and V_{OM} are the two outputs of the LVDS/BLVDS output buffer.

LVPECL[1]								
DC Parameter	**Parameter Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
V_{CCO}		**3.0**		**3.3**		**3.6**		**V**
V_{IH}	Input Voltage High	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	Input Voltage Low	0.86	2.125	0.86	2.125	0.86	2.125	V
V_{OH}	Output Voltage High	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	Output Voltage Low	0.96	1.27	1.06	1.43	1.3	1.57	V
V_{DIFF}[2]	Differential Input threshold	0.3	—	0.3	—	0.3	—	V

1. These values are valid at the output of the source termination pack as shown above with 100-ohm differential load only (see Figure 23). The V_{OH} levels are 200mV below the standard LVPECL levels and are compatible with devices tolerant of the lower common mode ranges.
2. Valid for 0.2 ð V_{CM} ð 1.8V.

ispXPGA 200B/C & ispXPGA 200EB/EC Timing Adders

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	4.84	—	5.2	—	5.98	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

ispXPGA 200B/C & ispXPGA 200EB/EC Timing Adders (Cont.)

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LVCMOS_33_4mA_out	Using 3.3V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_33_5.33mA_out	Using 3.3V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_33_8mA_out	Using 3.3V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_33_12mA_out	Using 3.3V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_33_16mA_out	Using 3.3V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_33_24mA_out	Using 3.3V CMOS Standard, 24mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_out	Using AGP 1x Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
CTT25_out	Using CTT 2.5V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
CTT33_out	Using CTT 3.3V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
GTL+_out	Using GTL+	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_out	Using HSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_out	Using HSTL 2.5V, Class III	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVDS_out	Using Low Voltage Differential Signaling (LVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
BLVDS_out	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVPECL_out	Using Low Voltage PECL	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
PCI_out	Using PCI Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL2_I_out	Using SSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL2_II_out	Using SSTL 2.5V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_out	Using SSTL 3.3V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL3_II_out	Using SSTL 3.3V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.

Timing v.0.3

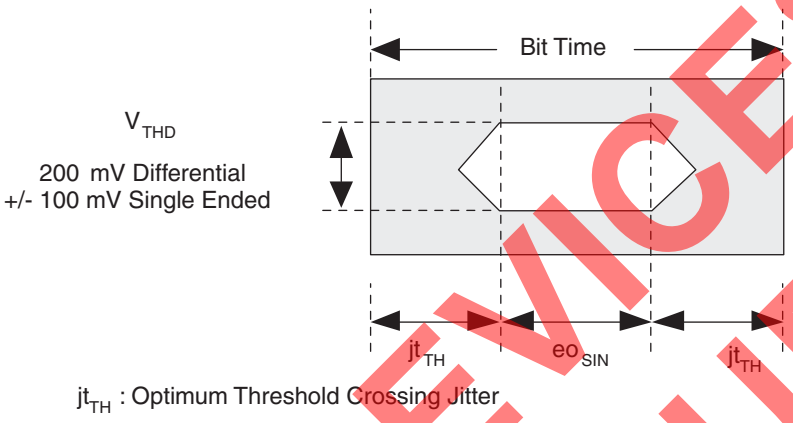
ispXPGA 500B/C & ispXPGA 500EB/EC Timing Adders

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	5.21	—	5.60	—	6.44	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

sysHSI Block Timing

Figure 24 provides a graphical representation of the SERDES receiver input requirements. It provides guidance on a number of input parameters, including signal amplitude and rise time limits, noise and jitter limits, and P and N input skew tolerance.

Figure 24. Receive Data Eye Diagram Template (Differential)



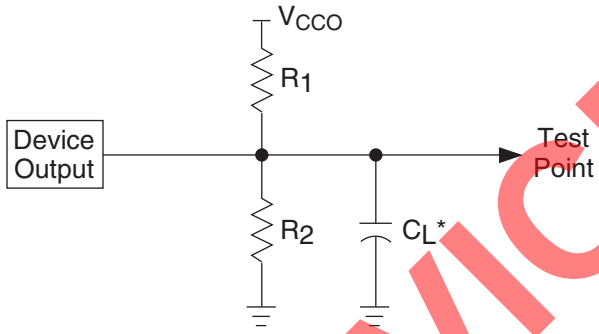
The data pattern eye opening at the receive end of a link is considered the ultimate measure of received signal quality. Almost all detrimental characteristics of a transmit signal and the interconnection link design result in eye closure. This combined with the eye-opening limitations of the line receiver can provide a good indication of a link's ability to transfer error-free data.

Signal jitter is of special interest to system designers. It is often the primary limiting characteristic of long digital links and of systems with high noise level environments. An interesting characteristic of the clock and data recovery (CDR) portion of the ispXPGA SERDES receiver is its ability to filter incoming signal jitter that is below the clock recovery PLL bandwidth. For signals with high levels of low frequency jitter, the receiver can detect incoming data error free, with eye openings significantly less than that shown in Figure 24.

Switching Test Conditions

Figure 25 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 7.

Figure 25. Output Test Load, LVTTL and LVCMOS Standards



*C_L includes test fixture and probe capacitance.

Table 7. Text Fixture Required Components

Test Condition	R_1	R_2	C_L	Timing Reference	VCCO
LVCMOS I/O, (L -> H, H -> L)	106	106	35pF	LVCMOS 3.3 = V_{CCO}/2	LVCMOS 3.3 = 3.0V
				LVCMOS 2.5 = V_{CCO}/2	LVCMOS 2.5 = 2.3V
				LVCMOS 1.8 = V_{CCO}/2	LVCMOS 1.8 = 1.65V
Default LVCMOS 1.8 I/O (Z -> H)	×	106	35pF	0.9V	1.65V
Default LVCMOS 1.8 I/O (Z -> L)	106	×	35pF	0.9V	1.65V
Default LVCMOS 1.8 I/O (H -> Z)	×	106	5pF	V_{OH} - 0.3	1.65V
Default LVCMOS 1.8 I/O (L -> Z)	106	×	5pF	V_{OL} + 0.3	1.65V

Note: Output test conditions for all other interfaces are determined by the respective standards.

ispXPGA Logic Signal Connections: 256-Ball fpBGA

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
C2	BK0_IO2	HSI0A_SOUTP	1P/HSI0	BK0_IO0	HSI0A_SOUTP	0P
-	GND (Bank 0)	-	-	-	-	-
D2	BK0_IO3	HSI0A_SOUTN	1N/HSI0	BK0_IO1	HSI0A_SOUTN	0N
B1	BK0_IO6	HSI0A_SINP	3P/HSI0	BK0_IO4	HSI0A_SINP	2P/HSI0
-	-	-	-	GND (Bank 0)	-	-
C1	BK0_IO7	HSI0A_SINN	3N/HSI0	BK0_IO5	HSI0A_SINN	2N/HSI0
D3	BK0_IO8	-	4P/HSI0	BK0_IO6	-	3P/HSI0
E3	BK0_IO9	VREF0	4N/HSI0	BK0_IO7	VREF0	3N/HSI0
D1	BK0_IO10	HSI0B_SOUTP	5P/HSI0	BK0_IO8	HSI0B_SOUTP	4P/HSI0
-	GND (Bank 0)	-	-	-	-	-
E1	BK0_IO11	HSI0B_SOUTN	5N/HSI0	BK0_IO9	HSI0B_SOUTN	4N/HSI0
E2	BK0_IO12	-	6P/HSI0	BK0_IO10	-	5P/HSI0
F2	BK0_IO13	-	6N/HSI0	BK0_IO11	-	5N/HSI0
F1	BK0_IO14	HSI0B_SINP	7P/HSI0	BK0_IO12	HSI0B_SINP	6P/HSI0
-	-	-	-	GND (Bank 0)	-	-
G1	BK0_IO15	HSI0B_SINN	7N/HSI0	BK0_IO13	HSI0B_SINN	6N/HSI0
F3	BK0_IO18	PLL_FBK0	9P	BK0_IO14	PLL_FBK0	7P/HSI0
-	GND (Bank 0)	-	-	-	-	-
G2	BK0_IO19	PLL_RST1	9N	BK0_IO15	PLL_RST1	7N/HSI0
E4	BK0_IO20	-	10P	BK0_IO16	-	8P/HSI0
F4	BK0_IO21	PLL_FBK1	10N	BK0_IO17	PLL_FBK1	8N/HSI0
H1	BK0_IO22	PLL_RST0	11P	BK0_IO18	PLL_RST0	9P
-	-	-	-	GND (Bank 0)	-	-
J1	BK0_IO23	-	11N	BK0_IO19	-	9N
H2	BK0_IO24	CLK_OUT0	12P	BK0_IO20	CLK_OUT0	10P
G3	BK0_IO25	CLK_OUT1	12N	BK0_IO21	CLK_OUT1	10N
-	GND (Bank 0)	-	-	-	-	-
G4	GCLK0	-	LVDS Pair0P	GCLK0	-	LVDS Pair0P
H4	GCLK1	-	LVDS Pair0N	GCLK1	-	LVDS Pair0N
H3	VCCP0	-	-	VCCP0	-	-
J4	GNDP0	-	-	GNDP0	-	-
J2	GCLK2	-	LVDS Pair1P	GCLK2	-	LVDS Pair1P
J3	GCLK3	-	LVDS Pair1N	GCLK3	-	LVDS Pair1N
-	GND (Bank 1)	-	-	-	-	-
H5	BK1_IO0	CLK_OUT2	13P	BK1_IO0	CLK_OUT2	11P
J5	BK1_IO1	CLK_OUT3	13N	BK1_IO1	CLK_OUT3	11N
K1	BK1_IO2	SS_CLKOUT0P	14P	BK1_IO2	SS_CLKOUT0P	12P
-	-	-	-	GND (Bank 1)	-	-
L1	BK1_IO3	SS_CLKOUT0N	14N	BK1_IO3	SS_CLKOUT0N	12N
K4	BK1_IO4	PLL_FBK2	15P	BK1_IO4	PLL_FBK2	13P
L4	BK1_IO5	PLL_FBK3	15N	BK1_IO5	PLL_FBK3	13N
K3	BK1_IO6	SS_CLKIN0P	16P	BK1_IO6	SS_CLKIN0P	14P

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
-	GND (Bank 1)	-	-	-	-	-
L3	BK1_IO7	SS_CLKIN0N	16N	BK1_IO7	SS_CLKIN0N	14N
K2	BK1_IO8	-	17P	BK1_IO8	-	15P
-	-	-	-	GND (Bank 1)	-	-
L2	BK1_IO9	-	17N	BK1_IO9	-	15N
M1	BK1_IO10	HSI1A_SOUTP	18P/HSI1	BK1_IO10	-	16P
N1	BK1_IO11	HSI1A_SOUTN	18N/HSI1	BK1_IO11	-	16N
M3	BK1_IO12	PLL_RST2	19P/HSI1	BK1_IO12	PLL_RST2	17P
M4	BK1_IO13	PLL_RST3	19N/HSI1	BK1_IO13	PLL_RST3	17N
-	GND (Bank 1)	-	-	-	-	-
M2	BK1_IO16[1]	VREF1	-	BK1_IO14[1]	VREF1	-
P1	BK1_IO18	HSI1B_SOUTP	22P/HSI1	BK1_IO16	-	19P
-	-	-	-	GND (Bank 1)	-	-
R1	BK1_IO19	HSI1B_SOUTN	22N/HSI1	BK1_IO17	-	19N
N3	BK1_IO20[1]	-	-	BK1_IO18[1]	-	-
N2	BK1_IO22	HSI1B_SINP	24P/HSI1	BK1_IO20	-	21P
-	GND (Bank 1)	-	-	-	-	-
P2	BK1_IO23	HSI1B_SINN	24N/HSI1	BK1_IO21	-	21N
P4	TCK	-	-	TCK	-	-
T2	TMS	-	-	TMS	-	-
T3	TOE	-	-	TOE	-	-
R3	BK2_IO0	-	26P	BK2_IO0	-	22P
R4	BK2_IO1	-	26N	BK2_IO1	-	22N
N5	BK2_IO2	-	27P	BK2_IO2	-	23P
-	GND (Bank 2)	-	-	-	-	-
P5	BK2_IO3	-	27N	BK2_IO3	-	23N
-	-	-	-	GND (Bank 2)	-	-
T4	BK2_IO6	-	29P	BK2_IO6	-	25P
T5	BK2_IO7	-	29N	BK2_IO7	-	25N
N6	BK2_IO8	-	30P	BK2_IO8	-	26P
P6	BK2_IO9	VREF2	30N	BK2_IO9	VREF2	26N
R5	BK2_IO10	-	31P	BK2_IO10	-	27P
-	GND (Bank 2)	-	-	-	-	-
R6	BK2_IO11	-	31N	BK2_IO11	-	27N
N7	BK2_IO12	-	32P	BK2_IO12	-	28P
-	-	-	-	GND (Bank 2)	-	-
P7	BK2_IO13	-	32N	BK2_IO13	-	28N
T6	BK2_IO14	-	33P	BK2_IO14	-	29P
T7	BK2_IO15	-	33N	BK2_IO15	-	29N
M8	BK2_IO16	-	34P	BK2_IO16	-	30P
M9	BK2_IO17	-	34N	BK2_IO17	-	30N
R7	BK2_IO18	-	35P	BK2_IO18	-	31P

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AA30	BK4_IO29	-	98N	BK4_IO17	-	60N	BK4_IO13	-	50N
W28	BK4_IO30	SS_CLKIN1P	99P	BK4_IO18	SS_CLKIN1P	61P	BK4_IO14	SS_CLKIN1P	51P
-	-	-	-	GND (Bank 4)	-	-	-	-	-
W29	BK4_IO31	SS_CLKIN1N	99N	BK4_IO19	SS_CLKIN1N	61N	BK4_IO15	SS_CLKIN1N	51N
Y30	BK4_IO32	-	100P	NC	-	-	NC	-	-
W30	BK4_IO33	-	100N	NC	-	-	NC	-	-
V27	BK4_IO34	-	101P	NC	-	-	NC	-	-
-	GND (Bank 4)	-	-	-	-	-	-	-	-
V28	BK4_IO35	-	101N	NC	-	-	NC	-	-
V29	BK4_IO36	PLL_FBK4	102P	BK4_IO20	PLL_FBK4	62P	BK4_IO16	PLL_FBK4	52P
V30	BK4_IO37	PLL_FBK5	102N	BK4_IO21	PLL_FBK5	62N	BK4_IO17	PLL_FBK5	52N
U30	BK4_IO38	SS_CLKOUT1P	103P	BK4_IO22	SS_CLKOUT1P	63P	BK4_IO18	SS_CLKOUT1P	53P
U29	BK4_IO39	SS_CLKOUT1N	103N	BK4_IO23	SS_CLKOUT1N	63N	BK4_IO19	SS_CLKOUT1N	53N
U28	BK4_IO40	CLK_OUT4	104P	BK4_IO24	CLK_OUT4	64P	BK4_IO20	CLK_OUT4	54P
-	GND (Bank 4)	-	-	-	-	-	-	-	-
T27	BK4_IO41	CLK_OUT5	104N	BK4_IO25	CLK_OUT5	64N	BK4_IO21	CLK_OUT5	54N
-	-	-	-	GND (Bank 4)	-	-	-	-	-
T28	GCLK4	-	LVDS Pair2P	GCLK4	-	LVDS Pair2P	GCLK4	-	LVDS Pair2P
T29	GCLK5	-	LVDS Pair2N	GCLK5	-	LVDS Pair2N	GCLK5	-	LVDS Pair2N
T30	VCCP1	-	-	VCCP1	-	-	VCCP1	-	-
R29	GNDP1	-	-	GNDP1	-	-	GNDP1	-	-
R28	GCLK6	-	LVDS Pair3P	GCLK6	-	LVDS Pair3P	GCLK6	-	LVDS Pair3P
R27	GCLK7	-	LVDS Pair3N	GCLK7	-	LVDS Pair3N	GCLK7	-	LVDS Pair3N
-	-	-	-	GND (Bank 5)	-	-	-	-	-
R30	BK5_IO0	CLK_OUT6	105P	BK5_IO0	CLK_OUT6	65P	BK5_IO0	CLK_OUT6	55P
-	GND (Bank 5)	-	-	-	-	-	-	-	-
P30	BK5_IO1	CLK_OUT7	105N	BK5_IO1	CLK_OUT7	65N	BK5_IO1	CLK_OUT7	55N
P29	BK5_IO2	-	106P	BK5_IO2	-	66P	BK5_IO2	-	56P
-	-	-	-	-	-	-	GND (Bank 5)	-	-
P28	BK5_IO3	PLL_RST7	106N	BK5_IO3	PLL_RST7	66N	BK5_IO3	PLL_RST7	56N
N30	BK5_IO4	PLL_FBK6	107P	BK5_IO4	PLL_FBK6	67P	BK5_IO4	PLL_FBK6	57P/HSI1
N29	BK5_IO5	-	107N	BK5_IO5	-	67N	BK5_IO5	-	57N/HSI1
N28	BK5_IO6	PLL-RST6	108P	BK5_IO6	PLL_RST6	68P	BK5_IO6	PLL_RST6	58P//HSI1
-	GND (Bank 5)	-	-	GND (Bank 5)	-	-	-	-	-
N27	BK5_IO7	PLL_FBK7	108N	BK5_IO7	PLL_FBK7	68N	BK5_IO7	PLL_FBK7	58N/HSI1
M30	BK5_IO8	-	109P/HSI4	BK5_IO8	-	69P	NC	-	-
M29	BK5_IO9	-	109N/HSI4	BK5_IO9	-	69N	NC	-	-
L30	BK5_IO10	HSI4A_SINP	110P/HSI4	BK5_IO10	HSI3A_SINP	70P/HSI3	BK5_IO8	HSI1A_SINP	59P/HSI1
-	-	-	-	-	-	-	GND (Bank 5)	-	-
L29	BK5_IO11	HSI4A_SINN	110N/HSI4	BK5_IO11	HSI3A_SINN	70N/HSI3	BK5_IO9	HSI1A_SINN	59N/HSI1
M28	BK5_IO12	-	111P/HSI4	BK5_IO12	-	71P/HSI3	BK5_IO10	-	60P/HSI1
L28	BK5_IO13	-	111N/HSI4	BK5_IO13		71N/HSI3	BK5_IO11	-	60N/HSI1
K30	BK5_IO14	HSI4A_SOUTP	112P/HSI4	BK5_IO14	HSI3A_SOUTP	72P/HSI3	BK5_IO12	HSI1A_SOUTP	61P/HSI1
-	GND (Bank 5)	-	-	GND (Bank 5)	-	-	-	-	-
K29	BK5_IO15	HSI4A_SOUTN	112N/HSI4	BK5_IO15	HSI3A_SOUTN	72N/HSI3	BK5_IO13	HSI1A_SOUTN	61N/HSI1
L27	BK5_IO16	-	113P/HSI4	NC	-	-	NC	-	-
K28	BK5_IO17	-	113N/HSI4	NC	-	-	NC	-	-
H30	BK5_IO18	HSI4B_SINP	114P/HSI4	NC	-	-	NC	-	-
G30	BK5_IO19	HSI4B_SINN	114N/HSI4	NC	-	-	NC	-	-
J28	BK5_IO20	-	115P/HSI4	NC	-	-	NC	-	-
K27	BK5_IO21	-	115N/HSI4	NC	-	-	NC	-	-

ispXPGA Logic Signal Connections: 680-Ball fpBGA

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
C4	BK0_IO0	-	0P
B4	BK0_IO1	-	0N
E6	BK0_IO2	-	1P
-	GND (Bank 0)	-	-
D6	BK0_IO3	-	1N
A4	BK0_IO4	-	2P
E8	BK0_IO5	-	2N
C5	BK0_IO6	HSI0A_SOUTP	3P
C6	BK0_IO7	HSI0A_SOUTN	3N
A6	BK0_IO8	-	4P
A5	BK0_IO9	-	4N
B6	BK0_IO10	HSI0A_SINP	5P/HSI0
-	GND (Bank 0)	-	-
B5	BK0_IO11	HSI0A_SINN	5N/HSI0
B7	BK0_IO12	VREF0	6P/HSI0
A7	BK0_IO13	-	6N/HSI0
D8	BK0_IO14	HSI0B_SOUTP	7P/HSI0
D7	BK0_IO15	HSI0B_SOUTN	7N/HSI0
D9	BK0_IO16	-	8P/HSI0
E10	BK0_IO17	-	8N/HSI0
C8	BK0_IO18	HSI0B_SINP	9P/HSI0
-	GND (Bank 0)	-	-
C7	BK0_IO19	HSI0B_SINN	9N/HSI0
A8	BK0_IO20	-	10P/HSI0
A9	BK0_IO21	-	10N/HSI0
C9	BK0_IO22	HSI1A_SOUTP	11P/HSI0
B8	BK0_IO23	HSI1A_SOUTN	11N/HSI0
B9	BK0_IO24	-	12P/HSI0
B10	BK0_IO25	-	12N/HSI0
D11	BK0_IO26	HSI1A_SINP	13P/HSI1
-	GND (Bank 0)	-	-
D10	BK0_IO27	HSI1A_SINN	13N/HSI1
A10	BK0_IO28	-	14P/HSI1
C12	BK0_IO29	-	14N/HSI1
D12	BK0_IO30	HSI1B_SOUTP	15P/HSI1
C11	BK0_IO31	HSI1B_SOUTN	15N/HSI1
A12	BK0_IO32	-	16P/HSI1
A13	BK0_IO33	-	16N/HSI1
B13	BK0_IO34	HSI1B_SINP	17P/HSI1
-	GND (Bank 0)	-	-
B12	BK0_IO35	HSI1B_SINN	17N/HSI1
E14	BK0_IO36	-	18P/HSI1

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
AK2	BK6_IO23	-	197N
AK1	BK6_IO24	-	198P
AJ4	BK6_IO25	-	198N
AJ3	BK6_IO26	-	199P
-	GND (Bank 6)	-	-
AH4	BK6_IO27	-	199N
AH3	BK6_IO28	-	200P
AH2	BK6_IO29	-	200N
AH1	BK6_IO30	-	201P
AG4	BK6_IO31	-	201N
AF5	BK6_IO32	DATA7	202P
AG3	BK6_IO33	DATA6	202N
AG2	BK6_IO34	-	203P
-	GND (Bank 6)	-	-
AF4	BK6_IO35	-	203N
AF3	BK6_IO36	DATA5	204P
AG1	BK6_IO37	DATA4	204N
AE2	BK6_IO38	-	205P
AF1	BK6_IO39	-	205N
AF2	BK6_IO40	-	206P
AE1	BK6_IO41	-	206N
AE4	BK6_IO42	-	207P
-	GND (Bank 6)	-	-
AD4	BK6_IO43	-	207N
AD5	BK6_IO44	-	208P
AD3	BK6_IO45	-	208N
AD2	BK6_IO46	-	209P
AD1	BK6_IO47	-	209N
AC4	BK6_IO48	-	210P
AC3	BK6_IO49	-	210N
AC2	BK6_IO50	DATA3	211P
-	GND (Bank 6)	-	-
AC1	BK6_IO51	DATA2	211N
AB3	BK6_IO52	-	212P
AB4	BK6_IO53	-	212N
AB2	BK6_IO54	DATA1	213P
AB1	BK6_IO55	DATA0	213N
AA3	BK6_IO56	-	214P
AA4	BK6_IO57	-	214N
AA5	BK6_IO58	-	215P
-	GND (Bank 6)	-	-
AA2	BK6_IO59	-	215N
AA1	BK6_IO60	-	216P

ispXPGA Logic Signal Connections: 900-Ball fpBGA

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
D3	BK0_IO0	-	0P	NC	-	-
E3	BK0_IO1	-	0N	NC	-	-
C2	BK0_IO2	-	1P	NC	-	-
-	GND (Bank 0)	-	-	-	-	-
C1	BK0_IO3	-	1N	NC	-	-
E4	BK0_IO4	-	2P	BK0_IO0	-	0P
F5	BK0_IO5	-	2N	BK0_IO1	-	0N
D2	BK0_IO6	HSI0A_SOUTP	3P	BK0_IO2	HSI0A_SOUTP	1P/HSI0
-	-	-	-	GND (Bank 0)	-	-
D1	BK0_IO7	HSI0A_SOUTN	3N	BK0_IO3	HSI0A_SOUTN	1N/HSI0
F4	BK0_IO8	-	4P	BK0_IO4	-	2P/HSI0
F3	BK0_IO9	-	4N	BK0_IO5	-	2N/HSI0
E2	BK0_IO10	HSI0A_SINP	5P/HSI0	BK0_IO6	HSI0A_SINP	3P/HSI0
-	GND (Bank 0)	-	-	-	-	-
E1	BK0_IO11	HSI0A_SINN	5N/HSI0	BK0_IO7	HSI0A_SINN	3N/HSI0
G6	BK0_IO12	VREF0	6P/HSI0	BK0_IO9	VREF0	4N/HSI0
G5	BK0_IO13	-	6N/HSI0	BK0_IO8	-	4P/HSI0
F1	BK0_IO14	HSI0B_SOUTP	7P/HSI0	NC	-	-
F2	BK0_IO15	HSI0B_SOUTN	7N/HSI0	NC	-	-
G4	BK0_IO16	-	8P/HSI0	NC	-	-
G3	BK0_IO17	-	8N/HSI0	NC	-	-
G2	BK0_IO18	HSI0B_SINP	9P/HSI0	NC	-	-
-	GND (Bank 0)	-	-	-	-	-
G1	BK0_IO19	HSI0B_SINN	9N/HSI0	NC	-	-
H3	BK0_IO20	-	10P/HSI0	NC	-	-
H4	BK0_IO21	-	10N/HSI0	NC	-	-
H1	BK0_IO22	HSI1A_SOUTP	11P/HSI0	NC	-	-
H2	BK0_IO23	HSI1A_SOUTN	11N/HSI0	NC	-	-
J7	BK0_IO24	-	12P/HSI0	NC	-	-
J6	BK0_IO25	-	12N/HSI0	NC	-	-
J1	BK0_IO26	HSI1A_SINP	13P/HSI1	NC	-	-
-	GND (Bank 0)	-	-	-	-	-
J2	BK0_IO27	HSI1A_SINN	13N/HSI1	NC	-	-
J4	BK0_IO28	-	14P/HSI1	NC	-	-
J5	BK0_IO29	-	14N/HSI1	NC	-	-
K1	BK0_IO30	HSI1B_SOUTP	15P/HSI1	BK0_IO10	HSI0B_SOUTP	5P/HSI0
-	-	-	-	GND (Bank 0)	-	-
K2	BK0_IO31	HSI1B_SOUTN	15N/HSI1	BK0_IO11	HSI0B_SOUTN	5N/HSI0
K5	BK0_IO32	-	16P/HSI1	BK0_IO12	-	6P/HSI0
K4	BK0_IO33	-	16N/HSI1	BK0_IO13	-	6N/HSI0
L1	BK0_IO34	HSI1B_SINP	17P/HSI1	BK0_IO14	HSI0B_SINP	7P/HSI0
-	GND (Bank 0)	-	-	-	-	-

"E-Series" Commercial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125EB-05F256C	139K	2.5/3.3	-5	fpBGA	256
LFX125EB-04F256C	139K	2.5/3.3	-4	fpBGA	256
LFX125EB-03F256C	139K	2.5/3.3	-3	fpBGA	256
LFX125EC-04F256C	139K	1.8	-4	fpBGA	256
LFX125EC-03F256C	139K	1.8	-3	fpBGA	256
LFX125EB-05F516C	139K	2.5/3.3	-5	fpBGA	516
LFX125EB-04F516C	139K	2.5/3.3	-4	fpBGA	516
LFX125EB-03F516C	139K	2.5/3.3	-3	fpBGA	516
LFX125EC-04F516C	139K	1.8	-4	fpBGA	516
LFX125EC-03F516C	139K	1.8	-3	fpBGA	516
LFX125EB-05FH516C[1]	139K	2.5/3.3	-5	fpBGA	516
LFX125EB-04FH516C[1]	139K	2.5/3.3	-4	fpBGA	516
LFX125EB-03FH516C[1]	139K	2.5/3.3	-3	fpBGA	516
LFX125EC-04FH516C[1]	139K	1.8	-4	fpBGA	516
LFX125EC-03FH516C[1]	139K	1.8	-3	fpBGA	516
LFX200EB-05F256C	210K	2.5/3.3	-5	fpBGA	256
LFX200EB-04F256C	210K	2.5/3.3	-4	fpBGA	256
LFX200EB-03F256C	210K	2.5/3.3	-3	fpBGA	256
LFX200EC-04F256C	210K	1.8	-4	fpBGA	256
LFX200EC-03F256C	210K	1.8	-3	fpBGA	256
LFX200EB-05F516C	210K	2.5/3.3	-5	fpBGA	516
LFX200EB-04F516C	210K	2.5/3.3	-4	fpBGA	516
LFX200EB-03F516C	210K	2.5/3.3	-3	fpBGA	516
LFX200EC-04F516C	210K	1.8	-4	fpBGA	516
LFX200EC-03F516C	210K	1.8	-3	fpBGA	516
LFX200EB-05FH516C[1]	210K	2.5/3.3	-5	fpBGA	516
LFX200EB-04FH516C[1]	210K	2.5/3.3	-4	fpBGA	516
LFX200EB-03FH516C[1]	210K	2.5/3.3	-3	fpBGA	516
LFX200EC-04FH516C[1]	210K	1.8	-4	fpBGA	516
LFX200EC-03FH516C[1]	210K	1.8	-3	fpBGA	516
LFX500EB-05F516C	476K	2.5/3.3	-5	fpBGA	516
LFX500EB-04F516C	476K	2.5/3.3	-4	fpBGA	516
LFX500EB-03F516C	476K	2.5/3.3	-3	fpBGA	516
LFX500EC-04F516C	476K	1.8	-4	fpBGA	516
LFX500EC-03F516C	476K	1.8	-3	fpBGA	516
LFX500EB-05FH516C[1]	476K	2.5/3.3	-5	fpBGA	516
LFX500EB-04FH516C[1]	476K	2.5/3.3	-4	fpBGA	516
LFX500EB-03FH516C[1]	476K	2.5/3.3	-3	fpBGA	516
LFX500EC-04FH516C[1]	476K	1.8	-4	fpBGA	516
LFX500EC-03FH516C[1]	476K	1.8	-3	fpBGA	516
LFX500EB-05F900C	476K	2.5/3.3	-5	fpBGA	900
LFX500EB-04F900C	476K	2.5/3.3	-4	fpBGA	900
LFX500EB-03F900C	476K	2.5/3.3	-3	fpBGA	900
LFX500EC-04F900C	476K	1.8	-4	fpBGA	900