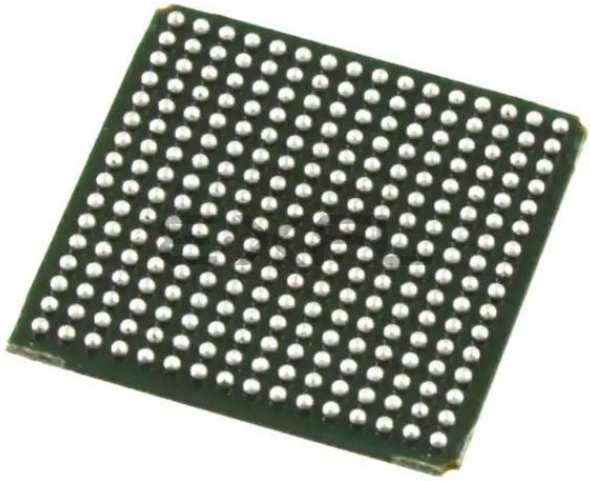


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	2704
Total RAM Bits	113664
Number of I/O	160
Number of Gates	210000
Voltage - Supply	2.3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx200b-04f256c

ispXPGA Family Overview

The ispXPGA family of devices provides the ideal vehicle for the creation of high-performance logic designs that are both non-volatile and infinitely re-programmable. Other FPGA solutions force a compromise, being either re-programmable or non-volatile. This family couples this capability with a mainstream architecture containing the features required for today's system-level design.

The ispXPGA family is available in two options. The standard device supports sysHSI capability for ultra fast serial communications while the lower-cost "E-Series" supports the same high-performance FPGA fabric without the sysHSI Block.

Electrically Erasable CMOS (E^2CMOS) memory cells provide the ispXPGA family with non-volatile capability. These allow logic to be functional microseconds after power is applied, allowing easy interfacing in many applications. This capability also means that expensive external configuration memories are not required and that designs can be secured from unauthorized read back. Internal SRAM cells allow the device to be infinitely reconfigured if desired. Both the SRAM and E^2CMOS cells can be programmed and verified through the IEEE 1532 industry standard. Additionally, the SRAM cells can be configured and read-back through the sysCONFIG™ peripheral port.

The family spans the density and I/O range required for the majority of today's logic designs, 139K to 1.25M functional gates and 160 to 496 I/O. The devices are available for operation from 1.8V, 2.5V, and 3.3V power supplies, providing easy integration into the overall system.

System-level design needs are met through the incorporation of sysMEM dual-port memory blocks, sysIO advanced I/O support, and sysCLOCK Phase Locked Loops (PLLs). High-speed serial communications are supported through multiple sysHSI blocks, which provide clock data recovery (CDR) and serialization/de-serialization (SERDES).

The ispLEVER™ design tool from Lattice allows easy implementation of designs using the ispXPGA product. Synthesis library support is available for major logic synthesis tools. The ispLEVER tool takes the output from these common synthesis packages and place and routes the design in the ispXPGA product. The tool supports floor planning and the management of other constraints within the device. The tool also provides outputs to common timing analysis tools for timing analysis.

To increase designer productivity, Lattice provides a variety of pre-designed modules referred to as IP cores for the ispXPGA product. These IP cores allow designers to concentrate on the unique portions of their design while using pre-designed blocks to implement standard functions such as bus interfaces, standard communication interfaces, and memory controllers.

Through the use of advanced technology and innovative architecture the ispXPGA FPGA devices provide designers with excellent speed performance. Although design dependent, many typical designs can run at over 150MHz. Certain designs can run at over 300MHz. Table 2 details the performance of several building blocks commonly used by logic designers.

Table 2. ispXPGA Speed Performance for Typical Building Blocks

Function	Performance
8:1 Asynch MUX	150 MHz
1:32 Asynch Demultiplexer	125 MHz
8 x 8 2-LL Pipelined Multiplier	225 MHz
32-bit Up/Down Counter	290 MHz
32-bit Shift Register	360 MHz

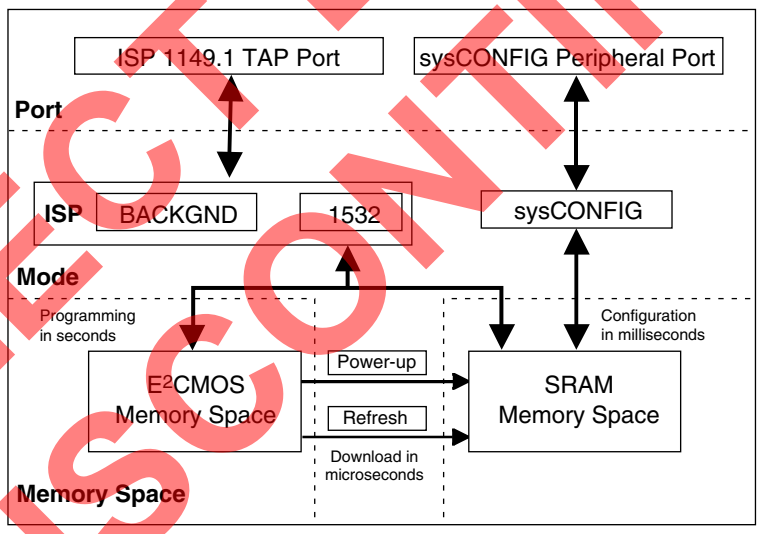
Configuration and Programming

The ispXPGA family of devices takes a unique approach to FPGA configuration memory. It contains two types of memory, Static RAM and non-volatile E²CMOS cells. The static RAM is used to control the functionality of the device during normal operation and the E²CMOS memory cells are used to load the SRAM. The E²CMOS memory module can be thought of as the hard drive for the ispXPGA configuration and the SRAM as the working configuration memory. There is a one-to-one relationship between SRAM memory and the E²CMOS cells. The SRAM can be configured either from the E²CMOS memory or from an external source, as shown in Figure 21.

Figure 21 shows the different ports and modes that are used in the configuration and programming of the ispXPGA devices. There are two possible ports that can be used for configuration of the SRAM memory: the ISP port which supports the IEEE 1149.1 Test Access Port (TAP) Std., accommodates bit-wide configuration. The sysCONFIG port allows byte-wide configuration of the SRAM configuration memory. When programming the E²CMOS memory, only the 1149.1 TAP can be used.

Configuration and programming done through the 1149.1 Test Access Port (TAP) supports both the IEEE Std. 1149.1 Boundary Scan TAP specification and the IEEE Std. 1532 In-System Configuration specification. To configure or program the device using the 1149.1 TAP the device must be in the ISP mode. To configure the SRAM memory using the sysCONFIG Port, the device must be in the sysCONFIG mode. Upon power-up, the device's SRAM memory can be configured either from the E²CMOS memory or from an external source through the sysCONFIG mode. Additionally, the SRAM can be re-configured from the E²CMOS memory by executing a "REFRESH." See TN1026, ispXP Configuration Usage Guidelines, for more in depth information on the different programming modes, timing and wake-up.

Figure 21. ispXP Block Diagram



Supports IEEE 1149.1 Boundary Scan Testability

All ispXPGA devices have boundary scan cells and supports the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal boundary scan registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board level testing.

Security Scheme

A programmable security scheme is provided on the ispXPGA devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, the security scheme prevents read-back of the programmed

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{IL}, I_{IH}[1]	Input or I/O Low Leakage	0 ð V_{IN} < (V_{CCO} - 0.2V)	—	—	10	µA
		(V_{CCO} - 0.2V) ð V_{IN} ð 3.6V	—	—	300	µA
I_{IH}[2]	Input High Leakage Current	3.6V < V_{IN} ð 5.5V and 3.0V ð V_{CCO} ð 3.6V	—	—	3	mA
I_{PU}	I/O Active Pull-up Current	0 ð V_{IN} ð 0.7 V_{CCO}	-30	—	-150	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) ð V_{IN} ð V_{IH} (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	V_{IN} = V_{IL} (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	V_{IN} = 0.7 V_{CCO}	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	0 ð V_{IN} ð V_{IH} (MAX)	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive Current	0 ð V_{IN} ð V_{IH} (MAX)	—	—	-150	µA
V_{BHT}	Bus Hold Trip Points		V_{CCO} * 0.35	—	V_{CCO} * 0.65	V
C_1	I/O Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_2	Clock Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_3	Global Input Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. 5V tolerant inputs and I/Os should be placed in banks where 3.0V ð V_{CCO} ð 3.6V. The JTAG and sysCONFIG ports are not included for the 5V tolerant interface.
3. T_A = 25°C, f = 1.0MHz.

ispXPGA 125B/C & ispXPGA 125EB/EC PFU Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Set								
t_{LASSRO}	Asynchronous Set/Reset to Output	—	1.09	—	1.17	—	1.35	ns
$t_{LASSRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{LASSRR}	Asynchronous Set/Reset Recovery	—	0.51	—	0.55	—	0.63	ns
t_{LSSR_S}	Synchronous Set/Reset Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{LSSR_H}	Synchronous Set/Reset Hold Time	0.03	—	0.03	—	0.03	—	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.
2. $t_{LCTHRUL}$ quoted bit by bit.

Timing v.0.3

ispXPGA 125B/C & ispXPGA 125EB/EC PIC Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Register/Latch Delays								
t_{IO_CO}	Register Clock to Output Delay	—	0.89	—	0.96	—	1.10	ns
t_{IO_S}	Register Setup Time (Data before Clock)	0.05	—	0.05	—	0.06	—	ns
t_{IO_H}	Register Hold Time (Data after Clock)	0.06	—	0.06	—	0.07	—	ns
t_{IOCE_S}	Register Clock Enable Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{IOCE_H}	Register Clock Enable Hold Time	0.13	—	0.13	—	0.15	—	ns
t_{IO_GO}	Latch Gate to Output Delay	—	0.68	—	0.73	—	0.84	ns
t_{IOL_S}	Latch Setup Time	0.05	—	0.05	—	0.06	—	ns
t_{IOL_H}	Latch Hold Time	0.06	—	0.06	—	0.07	—	ns
t_{IOLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns
t_{IOASRO}	Asynchronous Set/Reset to Output	—	1.00	—	1.08	—	1.24	ns
$t_{IOASRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{IOASRR}	Asynchronous Set/Reset Recovery Time	—	0.23	—	0.25	—	0.29	ns
Input/Output Delays								
t_{IOBUF}	Output Buffer Delay	—	0.97	—	1.04	—	1.20	ns
t_{IOIN}	Input Buffer Delay	—	0.57	—	0.61	—	0.70	ns
t_{IOEN}	Output Enable Delay	—	0.53	—	0.57	—	0.66	ns
t_{IODIS}	Output Disable Delay	—	-0.14	—	-0.13	—	-0.11	ns
t_{IOFT}	Feed-thru Delay	—	0.19	—	0.20	—	0.23	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 125B/C & ispXPGA 125EB/EC EBR Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Synchronous Write								
t_{EBSWAD_S}	Address Setup Delay	0.59	—	0.61	—	0.70	—	ns
t_{EBSWAD_H}	Address Hold Delay	-0.40	—	-0.39	—	-0.33	—	ns
$t_{EBSWCPW}$	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t_{EBSWWE_S}	Write Enable Setup Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{EBSWWE_H}	Write Enable Hold Time	0.16	—	0.16	—	0.18	—	ns
t_{EBSWD_S}	Data Setup Time	0.27	—	0.28	—	0.32	—	ns
t_{EBSWD_H}	Data Hold Time	-0.27	—	-0.26	—	-0.22	—	ns
Synchronous Read								
t_{EBSR_CO}	Clock to Data Delay	—	2.04	—	2.19	—	2.52	ns
t_{EBSRAD_S}	Address Setup Delay	0.10	—	0.10	—	0.12	—	ns
t_{EBSRAD_H}	Address Hold Delay	-0.07	—	-0.07	—	-0.06	—	ns
$t_{EBSRCPW}$	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t_{EBSRCE_S}	Clock Enable Setup Time	-1.76	—	-1.71	—	-1.45	—	ns
t_{EBSRCE_H}	Clock Enable Hold Time	1.64	—	1.69	—	1.94	—	ns
t_{EBSRWE_S}	Write Enable Setup Time	-0.18	—	-0.17	—	-0.14	—	ns
t_{EBSRWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{EBSRWEEN}$	Write Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBSRWEDIS}$	Write Enable to Data Disable Time	—	0.99	—	1.02	—	1.17	ns
t_{EBSREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBSRDIS}$	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns
Asynchronous Read								
$t_{EBARADO}$	Address to New Valid Data Delay	—	2.39	—	2.46	—	2.83	ns
t_{EBARAD_H}	Address to Previous Valid Data Delay	—	2.10	—	2.17	—	2.50	ns
$t_{EBARWEEN}$	Write Enable to Data Enable Time	—	1.01	—	1.04	—	1.20	ns
$t_{EBARWEDIS}$	Write Enable to Data Disable Time	—	0.98	—	1.01	—	1.16	ns
t_{EBAREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBARDIS}$	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 125B/C & ispXPGA 125EB/EC Timing Adders (Cont.)

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LVCMOS_33_4mA_out	Using 3.3V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_33_5.33mA_out	Using 3.3V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_33_8mA_out	Using 3.3V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_33_12mA_out	Using 3.3V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_33_16mA_out	Using 3.3V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_33_24mA_out	Using 3.3V CMOS Standard, 24mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_out	Using AGP 1x Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
CTT25_out	Using CTT 2.5V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
CTT33_out	Using CTT 3.3V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
GTL+_out	Using GTL+	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_out	Using HSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_out	Using HSTL 2.5V, Class III	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVDS_out	Using Low Voltage Differential Signaling (LVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
BLVDS_out	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVPECL_out	Using Low Voltage PECL	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
PCI_out	Using PCI Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL2_I_out	Using SSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL2_II_out	Using SSTL 2.5V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_out	Using SSTL 3.3V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL3_II_out	Using SSTL 3.3V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 200B/C & ispXPGA 200EB/EC External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Conditions	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{CO}	Global Clock Input to Output	PIO Output Register	—	5.5	—	5.9	—	6.8	ns
t_S	Global Clock Input Setup	PIO Input Register without input delay	-2.0	—	-2.0	—	-1.7	—	ns
t_H	Global Clock Input Hold	PIO Input Register without input delay	3.7	—	3.8	—	4.4	—	ns
t_{SINDLY}	Global Clock Input Setup	PIO Input Register with input delay	3.8	—	3.8	—	4.4	—	ns
t_{HINDLY}	Global Clock Input Hold	PIO Input Register with input delay	0.0	—	0.0	—	0.0	—	
t_{COPLL}	Global Clock Input to Output	PIO Output Register using PLL without delay	—	3.3	—	3.6	—	4.2	ns
t_{SPLL}	Global Clock Input Setup	PIO Input Register without input delay using PLL without delay	-0.2	—	-0.2	—	0.1	—	ns
t_{HPLL}	Global Clock Input Hold	PIO Input Register without input delay using PLL without delay	1.5	—	1.5	—	1.8	—	ns
$t_{SINDLYPLL}$	Global Clock Input Setup	PIO Input Register with input delay using PLL without delay	6.3	—	6.3	—	7.3	—	ns
$t_{HINDLYPLL}$	Global Clock Input Hold	PIO Input Register with input delay using PLL without delay	-2.7	—	-2.6	—	-2.2	—	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.

Timing v.0.2

ispXPGA 200B/C & ispXPGA 200EB/EC PFU Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Set								
t_{LASSRO}	Asynchronous Set/Reset to Output	—	1.09	—	1.17	—	1.35	ns
$t_{LASSRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{LASSRR}	Asynchronous Set/Reset Recovery	—	0.51	—	0.55	—	0.63	ns
t_{LSSR_S}	Synchronous Set/Reset Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{LSSR_H}	Synchronous Set/Reset Hold Time	0.03	—	0.03	—	0.03	—	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.
2. $t_{LCTHRUL}$ quoted bit by bit.

Timing v.0.3

ispXPGA 200B/C & ispXPGA 200EB/EC PIC Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Register/Latch Delays								
t_{IO_CO}	Register Clock to Output Delay	—	0.93	—	1.00	—	1.15	ns
t_{IO_S}	Register Setup Time (Data before Clock)	0.05	—	0.05	—	0.06	—	ns
t_{IO_H}	Register Hold Time (Data after Clock)	0.06	—	0.06	—	0.07	—	ns
t_{IOCE_S}	Register Clock Enable Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{IOCE_H}	Register Clock Enable Hold Time	0.13	—	0.13	—	0.15	—	ns
t_{IO_GO}	Latch Gate to Output Delay	—	0.72	—	0.77	—	0.89	ns
t_{IOL_S}	Latch Setup Time	0.05	—	0.05	—	0.06	—	ns
t_{IOL_H}	Latch Hold Time	0.06	—	0.06	—	0.07	—	ns
t_{IOLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns
t_{IOASRO}	Asynchronous Set/Reset to Output	—	1.04	—	1.12	—	1.29	ns
$t_{IOASRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{IOASRR}	Asynchronous Set/Reset Recovery Time	—	0.23	—	0.25	—	0.29	ns
Input/Output Delays								
t_{IOBUF}	Output Buffer Delay	—	0.97	—	1.04	—	1.20	ns
t_{IOIN}	Input Buffer Delay	—	0.60	—	0.64	—	0.74	ns
t_{IOEN}	Output Enable Delay	—	0.53	—	0.57	—	0.66	ns
t_{IODIS}	Output Disable Delay	—	-0.13	—	-0.12	—	-0.10	ns
t_{IOFT}	Feed-thru Delay	—	0.19	—	0.20	—	0.23	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 200B/C & ispXPGA 200EB/EC EBR Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Synchronous Write								
t_{EBSWAD_S}	Address Setup Delay	0.59	—	0.61	—	0.70	—	ns
t_{EBSWAD_H}	Address Hold Delay	-0.40	—	-0.39	—	-0.33	—	ns
$t_{EBSWCPW}$	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t_{EBSWWE_S}	Write Enable Setup Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{EBSWWE_H}	Write Enable Hold Time	0.16	—	0.16	—	0.18	—	ns
t_{EBSWD_S}	Data Setup Time	0.27	—	0.28	—	0.32	—	ns
t_{EBSWD_H}	Data Hold Time	-0.27	—	-0.26	—	-0.22	—	ns
Synchronous Read								
t_{EBSR_CO}	Clock to Data Delay	—	2.04	—	2.19	—	2.52	ns
t_{EBSRAD_S}	Address Setup Delay	0.10	—	0.10	—	0.12	—	ns
t_{EBSRAD_H}	Address Hold Delay	-0.07	—	-0.07	—	-0.06	—	ns
$t_{EBSRCPW}$	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t_{EBSRCE_S}	Clock Enable Setup Time	-1.76	—	-1.71	—	-1.45	—	ns
t_{EBSRCE_H}	Clock Enable Hold Time	1.64	—	1.69	—	1.94	—	ns
t_{EBSRWE_S}	Write Enable Setup Time	-0.18	—	-0.17	—	-0.14	—	ns
t_{EBSRWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{EBSRWEEN}$	Write Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBSRWEDIS}$	Write Enable to Data Disable Time	—	0.99	—	1.02	—	1.17	ns
t_{EBSREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBSRDIS}$	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns
Asynchronous Read								
$t_{EBARADO}$	Address to New Valid Data Delay	—	2.39	—	2.46	—	2.83	ns
t_{EBARAD_H}	Address to Previous Valid Data Delay	—	2.10	—	2.17	—	2.50	ns
$t_{EBARWEEN}$	Write Enable to Data Enable Time	—	1.01	—	1.04	—	1.20	ns
$t_{EBARWEDIS}$	Write Enable to Data Disable Time	—	0.98	—	1.01	—	1.16	ns
t_{EBAREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBARDIS}$	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 200B/C & ispXPGA 200EB/EC Timing Adders

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	4.84	—	5.2	—	5.98	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

ispXPGA 500B/C & ispXPGA 500EB/EC PFU Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Functional Delays								
LUTs								
t_{LUT4}	4-Input LUT Delay	—	0.41	—	0.44	—	0.51	ns
t_{LUT5}	5-Input LUT Delay	—	0.73	—	0.79	—	0.91	ns
t_{LUT6}	6-Input LUT Delay	—	0.86	—	0.93	—	1.07	ns
Shift Register (LUT)								
t_{LSR_S}	Shift Register Setup Time	-0.64	—	-0.62	—	-0.53	—	ns
t_{LSR_H}	Shift Register Hold Time	0.61	—	0.63	—	0.72	—	ns
t_{LSR_CO}	Shift Register Clock to Output Delay	—	0.70	—	0.75	—	0.86	ns
Arithmetic Functions								
$t_{LCTHRUR}$	MC (Macro Cell) Carry In to MC Carry Out Delay (Ripple)	—	0.08	—	0.09	—	0.10	ns
$t_{LCTHRUL}$[2]	MC Carry In to MC Carry Out Delay (Look Ahead)	—	0.05	—	0.05	—	0.06	ns
t_{LSTHRU}	MC Sum In to MC Sum Out Delay	—	0.42	—	0.45	—	0.52	ns
$t_{LSINCOUT}$	MC Sum In to MC Carry Out Delay	—	0.29	—	0.31	—	0.36	ns
$t_{LCINSOUTR}$	MC Carry In to MC Sum Out Delay (Ripple)	—	0.36	—	0.39	—	0.45	ns
$t_{LCINSOUTL}$	MC Carry In to MC Sum Out Delay (Look Ahead)	—	0.26	—	0.28	—	0.32	ns
Feed-thru								
t_{LFT}	PFU Feed-Thru Delay	—	0.15	—	0.16	—	0.18	ns
Distributed RAM								
t_{LRAM_CO}	Clock to RAM Output	—	1.24	—	1.33	—	1.53	ns
t_{LRAMAD_S}	Address Setup Time	-0.41	—	-0.40	—	-0.34	—	ns
t_{LRAMD_S}	Data Setup Time	0.21	—	0.22	—	0.25	—	ns
t_{LRAMWE_S}	Write Enable Setup Time	0.45	—	0.46	—	0.53	—	ns
t_{LRAMAD_H}	Address Hold Time	0.58	—	0.60	—	0.69	—	ns
t_{LRAMD_H}	Data Hold Time	0.11	—	0.11	—	0.13	—	ns
t_{LRAMWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{LRAMCPW}$	Clock Pulse Width (High or Low)	2.91	—	3.00	—	3.45	—	ns
$t_{LRAMADO}$	Address to Output Delay	—	0.86	—	0.93	—	1.07	ns
Register/Latch Delays								
Registers								
t_{L_CO}	Register Clock to Output Delay	—	0.58	—	0.62	—	0.71	ns
t_{L_S}	Register Setup Time (Data before Clock)	0.14	—	0.14	—	0.16	—	ns
t_{L_H}	Register Hold Time (Data after Clock)	-0.12	—	-0.12	—	-0.10	—	ns
t_{LCE_S}	Register Clock Enable Setup Time	-0.11	—	-0.11	—	-0.09	—	ns
t_{LCE_H}	Register Clock Enable Hold Time	0.11	—	0.11	—	0.13	—	ns
Latches								
t_{L_GO}	Latch Gate to Output Delay	—	0.09	—	0.10	—	0.12	ns
t_{LL_S}	Latch Setup Time	0.14	—	0.14	—	0.16	—	ns
t_{LL_H}	Latch Hold Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{LLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns

ispXPGA 1200B/C & ispXPGA 1200EB/EC PFU Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Functional Delays								
LUTs								
t_{LUT4}	4-Input LUT Delay	—	0.41	—	0.44	—	0.51	ns
t_{LUT5}	5-Input LUT Delay	—	0.73	—	0.79	—	0.91	ns
t_{LUT6}	6-Input LUT Delay	—	0.86	—	0.93	—	1.07	ns
Shift Register (LUT)								
t_{LSR_S}	Shift Register Setup Time	-0.64	—	-0.62	—	-0.53	—	ns
t_{LSR_H}	Shift Register Hold Time	0.61	—	0.63	—	0.72	—	ns
t_{LSR_CO}	Shift Register Clock to Output Delay	—	0.70	—	0.75	—	0.86	ns
Arithmetic Functions								
$t_{LCTHRUR}$	MC (Macro Cell) Carry In to MC Carry Out Delay (Ripple)	—	0.08	—	0.09	—	0.10	ns
$t_{LCTHRUL}$[2]	MC Carry In to MC Carry Out Delay (Look Ahead)	—	0.05	—	0.05	—	0.06	ns
t_{LSTHRU}	MC Sum In to MC Sum Out Delay	—	0.42	—	0.45	—	0.52	ns
$t_{LSINCOUT}$	MC Sum In to MC Carry Out Delay	—	0.29	—	0.31	—	0.36	ns
$t_{LCINSOUTR}$	MC Carry In to MC Sum Out Delay (Ripple)	—	0.36	—	0.39	—	0.45	ns
$t_{LCINSOUTL}$	MC Carry In to MC Sum Out Delay (Look Ahead)	—	0.26	—	0.28	—	0.32	ns
Feed-thru								
t_{LFT}	PFU Feed-Thru Delay	—	0.15	—	0.16	—	0.18	ns
Distributed RAM								
t_{LRAM_CO}	Clock to RAM Output	—	1.24	—	1.33	—	1.53	ns
t_{LRAMAD_S}	Address Setup Time	-0.41	—	-0.40	—	-0.34	—	ns
t_{LRAMD_S}	Data Setup Time	0.21	—	0.22	—	0.25	—	ns
t_{LRAMWE_S}	Write Enable Setup Time	0.45	—	0.46	—	0.53	—	ns
t_{LRAMAD_H}	Address Hold Time	0.58	—	0.60	—	0.69	—	ns
t_{LRAMD_H}	Data Hold Time	0.11	—	0.11	—	0.13	—	ns
t_{LRAMWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{LRAMCPW}$	Clock Pulse Width (High or Low)	2.91	—	3.00	—	3.45	—	ns
$t_{LRAMADO}$	Address to Output Delay	—	0.86	—	0.93	—	1.07	ns
Register/Latch Delays								
Registers								
t_{L_CO}	Register Clock to Output Delay	—	0.58	—	0.62	—	0.71	ns
t_{L_S}	Register Setup Time (Data before Clock)	0.14	—	0.14	—	0.16	—	ns
t_{L_H}	Register Hold Time (Data after Clock)	-0.12	—	-0.12	—	-0.10	—	ns
t_{LCE_S}	Register Clock Enable Setup Time	-0.11	—	-0.11	—	-0.09	—	ns
t_{LCE_H}	Register Clock Enable Hold Time	0.11	—	0.11	—	0.13	—	ns
Latches								
t_{L_GO}	Latch Gate to Output Delay	—	0.09	—	0.10	—	0.12	ns
t_{LL_S}	Latch Setup Time	0.14	—	0.14	—	0.16	—	ns
t_{LL_H}	Latch Hold Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{LLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns

ispXPGA Power Supply and NC Connections[1] (Continued)

Signal	680-Ball fpBGA[3]	900-Ball fpBGA[3]
V_{CC}	AE35, AE5, AL5, AR15, AR25, AR31, AR35, AR5, AT36, AT4, AU3, AU37, C3, C37, D36, D4, E15, E25, E35, E5, E9, J35, R35, R5	L11, L20, M12, M13, M14, M17, M18, M19, N12, N19, P12, P19, U12, U19, V12, V19, W12, W13, W14, W17, W18, W19, Y11, Y20
V_{CCO0}	E11, E12, E13, E17, E18, E7	K3, L10, M11, N11, N5, P11, R11, R12
V_{CCO1}	E22, E23, E27, E29, E31, E33	AA3, T11, T12, U11, V11, V5, W11, Y10
V_{CCO2}	G35, L35, M35, N35, U35, V35	AA11, AF13, AH10, W15, Y12, Y13, Y14, Y15
V_{CCO3}	AB35, AC35, AG35, AJ35, AL35, AN35	AA20, AF18, AH21, W16, Y16, Y17, Y18, Y19
V_{CCO4}	AR22, AR23, AR27, AR28, AR29, AR33	AA28, T19, T20, U20, V20, V26, W20, Y21
V_{CCO5}	AR11, AR13, AR17, AR18, AR7, AR9	K28, L21, M20, N20, N26, P20, R19, R20
V_{CCO6}	AB5, AC5, AG5, AH5, AJ5, AN5	C21, E18, K20, L16, L17, L18, L19, M16
V_{CCO7}	G5, J5, L5, N5, U5, V5	C10, E13, K11, L12, L13, L14, L15, M15
V_{CCP}	E20, AW22	R5, T26
V_{CCJ}	D3	B3
GND	A1, A2, A20, A38, A39, AE3, AE37, AK3, AK37, AR36, AR4, AT20, AT35, AT5, AU10, AU14, AU20, AU26, AU30, AV1, AV2, AV20, AV38, AV39, AW1, AW2, AW20, AW38, AW39, B1, B2, B20, B38, B39, C10, C14, C20, C26, C30, D20, D35, D5, E36, E4, K3, K37, P37, R3, Y1, Y2, Y3, Y36, Y37, Y38, Y39, Y4	A1, A2, A29, A30, AB28, AB3, AG27, AG4, AH22, AH28, AH3, AH9, AJ1, AJ2, AJ29, AJ30, AK1, AK2, AK29, AK30, B1, B2, B29, B30, C22, C28, C3, C9, D27, D4, J28, J3, N13, N14, N15, N16, N17, N18, P13, P14, P15, P16, P17, P18, R13, R14, R15, R16, R17, R18, T13, T14, T15, T16, T17, T18, U13, U14, U15, U16, U17, U18, V13, V14, V15, V16, V17, V18
GND_P	AR20, A21	R28, T3

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
R8	BK2_IO19	-	35N	BK2_IO19	-	31N
N8	BK2_IO20	-	36P	BK2_IO20	-	32P
P8	BK2_IO21	-	36N	BK2_IO21	-	32N
-	GND (Bank 2)	-	-	-	-	-
-	GND (Bank 3)	-	-	-	-	-
T8	BK3_IO0	-	39P	BK3_IO0	-	33P
T9	BK3_IO1	-	39N	BK3_IO1	-	33N
R9	BK3_IO2	-	40P	BK3_IO2	-	34P
-	-	-	-	GND (Bank 3)	-	-
R10	BK3_IO3	-	40N	BK3_IO3	-	34N
P9	BK3_IO4	-	41P	BK3_IO4	-	35P
N9	BK3_IO5	-	41N	BK3_IO5	-	35N
T10	BK3_IO6	-	42P	BK3_IO6	-	36P
-	GND (Bank 3)	-	-	-	-	-
T11	BK3_IO7	-	42N	BK3_IO7	-	36N
P10	BK3_IO8	-	43P	BK3_IO8	-	37P
-	-	-	-	GND (Bank 3)	-	-
N10	BK3_IO9	-	43N	BK3_IO9	-	37N
R11	BK3_IO14	-	46P	BK3_IO10	-	38P
-	GND (Bank 3)	-	-	-	-	-
R12	BK3_IO15	-	46N	BK3_IO11	-	38N
P11	BK3_IO16	VREF3	47P	BK3_IO12	VREF3	39P
N11	BK3_IO17	-	47N	BK3_IO13	-	39N
T12	BK3_IO18	-	48P	BK3_IO14	-	40P
T13	BK3_IO19	-	48N	BK3_IO15	-	40N
R13	BK3_IO20	-	49P	BK3_IO16	-	41P
-	-	-	-	GND (Bank 3)	-	-
R14	BK3_IO21	-	49N	BK3_IO17	-	41N
P12	BK3_IO22	-	50P	BK3_IO18	-	42P
-	GND (Bank 3)	-	-	-	-	-
N12	BK3_IO23	-	50N	BK3_IO19	-	42N
T14	GSR	-	-	GSR	-	-
T15	DXP	-	-	DXP	-	-
P13	DXN	-	-	DXN	-	-
P15	BK4_IO0	-	52P/HSI2	BK4_IO0	-	44P
N14	BK4_IO1	-	52N/HSI2	BK4_IO1	-	44N
R16	BK4_IO2	HSI2A_SINP	53P/HSI2	BK4_IO2	-	45P
-	GND (Bank 4)	-	-	-	-	-
P16	BK4_IO3	HSI2A_SINN	53N/HSI2	BK4_IO3	-	45N
N15	BK4_IO4	-	54P/HSI2	BK4_IO4	-	46P
-	-	-	-	GND (Bank 4)	-	-

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
-	GND (Bank 2)	-	-
K36	BK2_IO19	-	71N
H38	BK2_IO20	-	72P
J38	BK2_IO21	-	72N
J39	BK2_IO22	-	73P
L36	BK2_IO23	-	73N
K38	BK2_IO24	-	74P
M36	BK2_IO25	-	74N
L37	BK2_IO26	-	75P
-	GND (Bank 2)	-	-
K39	BK2_IO27	-	75N
L38	BK2_IO28	-	76P
P35	BK2_IO29	-	76N
N36	BK2_IO30	-	77P
M37	BK2_IO31	-	77N
L39	BK2_IO32	-	78P
M38	BK2_IO33	-	78N
M39	BK2_IO34	-	79P
-	GND (Bank 2)	-	-
P36	BK2_IO35	-	79N
R36	BK2_IO36	-	80P
N37	BK2_IO37	-	80N
P38	BK2_IO38	-	81P
T35	BK2_IO39	-	81N
R37	BK2_IO40	-	82P
R38	BK2_IO41	-	82N
P39	BK2_IO42	-	83P
-	GND (Bank 2)	-	-
R39	BK2_IO43	-	83N
T38	BK2_IO44	-	84P
T36	BK2_IO45	-	84N
T37	BK2_IO46	-	85P
U36	BK2_IO47	-	85N
U37	BK2_IO48	-	86P
T39	BK2_IO49	-	86N
V36	BK2_IO50	-	87P
-	GND (Bank 2)	-	-
U38	BK2_IO51	-	87N
U39	BK2_IO52	-	88P
V38	BK2_IO53	-	88N
V37	BK2_IO54	-	89P
W36	BK2_IO55	-	89N
W35	BK2_IO56	-	90P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AJ25	BK3_IO50	-	118P	BK3_IO30	-	78P
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-
AK25	BK3_IO51	-	118N	BK3_IO31	-	78N
AF24	BK3_IO52	-	119P	BK3_IO32	-	79P
AE24	BK3_IO53	-	119N	BK3_IO33	-	79N
AK26	BK3_IO54	-	120P	BK3_IO34	-	80P
AJ26	BK3_IO55	-	120N	BK3_IO35	-	80N
AH25	BK3_IO56	-	121P	BK3_IO36	-	81P
AG25	BK3_IO57	-	121N	BK3_IO37	-	81N
AK27	BK3_IO58	-	122P	BK3_IO38	-	82P
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-
AJ27	BK3_IO59	-	122N	BK3_IO39	-	82N
AG26	BK3_IO60	-	123P	BK3_IO40	-	83P
AH26	BK3_IO61	-	123N	BK3_IO41	-	83N
AK28	GSR	-	-	GSR	-	-
AJ28	DXP	-	-	DXP	-	-
AH27	DXN	-	-	DXN	-	-
AG28	BK4_IO0	-	124P	BK4_IO0	-	84P
AF27	BK4_IO1	-	124N	BK4_IO1	-	84N
AF28	BK4_IO2	-	125P	BK4_IO2	-	85P/HSI3
-	GND (Bank 4)	-	-	GND (Bank 4)	-	-
AE26	BK4_IO3	-	125N	BK4_IO3	-	85N/HSI3
AE27	BK4_IO4	-	126P	BK4_IO4	-	86P/HSI3
AE28	BK4_IO5	-	126N	BK4_IO5	-	86N/HSI3
AH30	BK4_IO6	HSI5A_SINP	127P	BK4_IO10	HSI3A_SINP	89P/HSI3
-	-	-	-	GND (Bank 4)	-	-
AH29	BK4_IO7	HSI5A_SINN	127N	BK4_IO11	HSI3A_SINN	89N/HSI3
AD25	BK4_IO8	-	128P	BK4_IO12	-	90P/HSI3
AD26	BK4_IO9	-	128N	BK4_IO13	-	90N/HSI3
AG29	BK4_IO10	HSI5A_SOUTP	129P/HSI5	BK4_IO14	HSI3A_SOUTP	91P/HSI3
-	GND (Bank 4)	-	-	-	-	-
AG30	BK4_IO11	HSI5A_SOUTN	129N/HSI5	BK4_IO15	HSI3A_SOUTN	91N/HSI3
AD27	BK4_IO12	VREF4	130P/HSI5	BK4_IO17	VREF4	92N/HSI3
AD28	BK4_IO13	-	130N/HSI5	BK4_IO16	-	92P/HSI3
AF29	BK4_IO14	HSI5B_SINP	131P/HSI5	BK4_IO6	-	87P/HSI3
AF30	BK4_IO15	HSI5B_SINN	131N/HSI5	BK4_IO7	-	87N/HSI3
AC25	BK4_IO16	-	132P/HSI5	BK4_IO8	-	88P/HSI3
AC26	BK4_IO17	-	132N/HSI5	BK4_IO9	-	88N/HSI3
AE29	BK4_IO18	HSI5B_SOUTP	133P/HSI5	NC	-	-
-	GND (Bank 4)	-	-	-	-	-
AE30	BK4_IO19	HSI5B_SOUTN	133N/HSI5	NC	-	-
AC28	BK4_IO20	-	134P/HSI5	NC	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
U27	BK4_IO57	PLL_FBK5	152N	BK4_IO37	PLL_FBK5	102N
U29	BK4_IO58	SS_CLKOUT1P	153P	BK4_IO38	SS_CLKOUT1P	103P
-	GND (Bank 4)	--	-	-	-	-
U30	BK4_IO59	SS_CLKOUT1N	153N	BK4_IO39	SS_CLKOUT1N	103N
T30	BK4_IO60	CLK_OUT4	154P	BK4_IO40	CLK_OUT4	104P
-	-	-	-	GND (Bank 4)	-	-
T29	BK4_IO61	CLK_OUT5	154N	BK4_IO41	CLK_OUT5	104N
-	GND (Bank 4)	-	-	-	-	-
T28	GCLK4	-	LVDS Pair2P	GCLK4	-	LVDS Pair2P
T27	GCLK5	-	LVDS Pair2N	GCLK5	-	LVDS Pair2N
T26	VCCP1	-	-	VCCP1	-	-
R28	GNDP1	-	-	GNDP1	-	-
R27	GCLK6	-	LVDS Pair3P	GCLK6	-	LVDS Pair3P
R26	GCLK7	-	LVDS Pair3N	GCLK7	-	LVDS Pair3N
-	GND (Bank 5)	-	-	-	-	-
R29	BK5_IO0	CLK_OUT6	155P	BK5_IO0	CLK_OUT6	105P
-	-	-	-	GND (Bank 5)	-	-
R30	BK5_IO1	CLK_OUT7	155N	BK5_IO1	CLK_OUT7	105N
P30	BK5_IO2	PLL_FBK6	156P	BK5_IO4	PLL_FBK6	107P
-	GND (Bank 5)	-	-	GND (Bank 5)	-	-
P29	BK5_IO3	PLL_FBK7	156N	BK5_IO7	PLL_FBK7	108N
P27	BK5_IO4	-	157P/HSI7	BK5_IO2	-	106P
P28	BK5_IO5	-	157N/HSI7	BK5_IO5	-	107N
P26	BK5_IO6	PLL_RST6	158P/HSI7	BK5_IO6	PLL_RST6	108P
P25	BK5_IO7	PLL_RST7	158N/HSI7	BK5_IO3	PLL_RST7	106N
N27	BK5_IO8	-	159P/HSI7	BK5_IO8	-	109P/HSI4
N28	BK5_IO9	-	159N/HSI7	BK5_IO9	-	109N/HSI4
N29	BK5_IO10	HSI7A_SINP	160P/HSI7	BK5_IO10	HSI4A_SINP	110P/HSI4
-	GND (Bank 5)	-	-	-	-	-
N30	BK5_IO11	HSI7A_SINN	160N/HSI7	BK5_IO11	HSI4A_SINN	110N/HSI4
N25	BK5_IO12	-	161P/HSI7	BK5_IO12	-	111P/HSI4
N24	BK5_IO13	-	161N/HSI7	BK5_IO13	-	111N/HSI4
M29	BK5_IO14	HSI7A_SOUTP	162P/HSI7	BK5_IO14	HSI4A_SOUTP	112P/HSI4
-	-	-	-	GND (Bank 5)	-	-
M30	BK5_IO15	HSI7A_SOUTN	162N/HSI7	BK5_IO15	HSI4A_SOUTN	112N/HSI4
M28	BK5_IO16	-	163P/HSI7	BK5_IO16	-	113P/HSI4
M27	BK5_IO17	-	163N/HSI7	BK5_IO17	-	113N/HSI4
L30	BK5_IO18	HSI7B_SINP	164P/HSI7	BK5_IO18	HSI4B_SINP	114P/HSI4
-	GND (Bank 5)	-	-	-	-	-
L29	BK5_IO19	HSI7B_SINN	164N/HSI7	BK5_IO19	HSI4B_SINN	114N/HSI4
M26	BK5_IO20	-	165P/HSI8	BK5_IO20	-	115P/HSI4
M25	BK5_IO21	-	165N/HSI8	BK5_IO21	-	115N/HSI4

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
B15	BK7_IO1	-	217N	BK7_IO1	-	147N
C15	BK7_IO2	-	218P	BK7_IO2	-	148P
-	GND (Bank 7)	-	-		-	-
D15	BK7_IO3	-	218N	BK7_IO3	-	148N
E15	BK7_IO4	-	219P	BK7_IO4	-	149P
F15	BK7_IO5	-	219N	BK7_IO5	-	149N
A14	BK7_IO6	-	220P	BK7_IO6	-	150P
-	-	-	-	GND (Bank 7)	-	-
B14	BK7_IO7	-	220N	BK7_IO7	-	150N
C14	BK7_IO8	-	221P	BK7_IO8	-	151P
D14	BK7_IO9	-	221N	BK7_IO9	-	151N
E14	BK7_IO10	-	222P	BK7_IO10	-	152P
-	GND (Bank 7)	-	-	-	-	-
F14	BK7_IO11	-	222N	BK7_IO11	-	152N
C13	BK7_IO12	-	223P	BK7_IO12	-	153P
D13	BK7_IO13	-	223N	BK7_IO13	-	153N
B13	BK7_IO14	-	224P	BK7_IO14	-	154P
-	-	-	-	GND (Bank 7)	-	-
A13	BK7_IO15	-	224N	BK7_IO15	-	154N
F13	BK7_IO16	-	225P	BK7_IO16	-	155P
G13	BK7_IO17	-	225N	BK7_IO17	-	155N
A12	BK7_IO18	-	226P	BK7_IO18	-	156P
-	GND (Bank 7)	-	-	-	-	-
B12	BK7_IO19	-	226N	BK7_IO19	-	156N
C12	BK7_IO20	-	227P	NC	-	-
D12	BK7_IO21	-	227N	NC	-	-
A11	BK7_IO22	-	228P	NC	-	-
B11	BK7_IO23	-	228N	NC	-	-
E12	BK7_IO24	-	229P	NC	-	-
F12	BK7_IO25	-	229N	NC	-	-
C11	BK7_IO26	-	230P	NC	-	-
-	GND (Bank 7)	-	-	-	-	-
D11	BK7_IO27	-	230N	NC	-	-
E11	BK7_IO28	-	231P	NC	-	-
F11	BK7_IO29	-	231N	NC	-	-
B10	BK7_IO30	-	232P	NC	-	-
A10	BK7_IO31	-	232N	NC	-	-
D10	BK7_IO32	-	233P	NC	-	-
E10	BK7_IO33	-	233N	NC	-	-
A9	BK7_IO34	-	234P	NC	-	-
-	GND (Bank 7)	-	-	-	-	-
B9	BK7_IO35	-	234N	NC	-	-

Commercial (Cont.)

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX200B-05F516C	210K	2.5/3.3	-5	fpBGA	516
LFX200B-04F516C	210K	2.5/3.3	-4	fpBGA	516
LFX200B-03F516C	210K	2.5/3.3	-3	fpBGA	516
LFX200C-04F516C	210K	1.8	-4	fpBGA	516
LFX200C-03F516C	210K	1.8	-3	fpBGA	516
LFX200B-05FH516C[1]	210K	2.5/3.3	-5	fpBGA	516
LFX200B-04FH516C[1]	210K	2.5/3.3	-4	fpBGA	516
LFX200B-03FH516C[1]	210K	2.5/3.3	-3	fpBGA	516
LFX200C-04FH516C[1]	210K	1.8	-4	fpBGA	516
LFX200C-03FH516C[1]	210K	1.8	-3	fpBGA	516
LFX500B-05F516C	476K	2.5/3.3	-5	fpBGA	516
LFX500B-04F516C	476K	2.5/3.3	-4	fpBGA	516
LFX500B-03F516C	476K	2.5/3.3	-3	fpBGA	516
LFX500C-04F516C	476K	1.8	-4	fpBGA	516
LFX500C-03F516C	476K	1.8	-3	fpBGA	516
LFX500B-05FH516C[1]	476K	2.5/3.3	-5	fpBGA	516
LFX500B-04FH516C[1]	476K	2.5/3.3	-4	fpBGA	516
LFX500B-03FH516C[1]	476K	2.5/3.3	-3	fpBGA	516
LFX500C-04FH516C[1]	476K	1.8	-4	fpBGA	516
LFX500C-03FH516C[1]	476K	1.8	-3	fpBGA	516
LFX500B-05F900C	476K	2.5/3.3	-5	fpBGA	900
LFX500B-04F900C	476K	2.5/3.3	-4	fpBGA	900
LFX500B-03F900C	476K	2.5/3.3	-3	fpBGA	900
LFX500C-04F900C	476K	1.8	-4	fpBGA	900
LFX500C-03F900C	476K	1.8	-3	fpBGA	900
LFX1200B-05F900C[2]	1.25M	2.5/3.3	-5	fpBGA	900
LFX1200B-04F900C[2]	1.25M	2.5/3.3	-4	fpBGA	900
LFX1200B-03F900C[2]	1.25M	2.5/3.3	-3	fpBGA	900
LFX1200C-04F900C[2]	1.25M	1.8	-4	fpBGA	900
LFX1200C-03F900C[2]	1.25M	1.8	-3	fpBGA	900
LFX1200B-05FE680C[2]	1.25M	2.5/3.3	-5	fpSBGA	680
LFX1200B-04FE680C[2]	1.25M	2.5/3.3	-4	fpSBGA	680
LFX1200B-03FE680C[2]	1.25M	2.5/3.3	-3	fpSBGA	680
LFX1200C-04FE680C[2]	1.25M	1.8	-4	fpSBGA	680
LFX1200C-03FE680C[2]	1.25M	1.8	-3	fpSBGA	680

1. FH516 package was converted to F516 via PCN #09A-08.
2. Discontinued via PCN #03A-10.

"E-Series" Commercial (Cont.)

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX500EC-03F900C	476K	1.8	-3	fpBGA	900
LFX1200EB-05F900C[2]	1.25M	2.5/3.3	-5	fpBGA	900
LFX1200EB-04F900C[2]	1.25M	2.5/3.3	-4	fpBGA	900
LFX1200EB-03F900C[2]	1.25M	2.5/3.3	-3	fpBGA	900
LFX1200EC-04F900C[2]	1.25M	1.8	-4	fpBGA	900
LFX1200EC-03F900C[2]	1.25M	1.8	-3	fpBGA	900
LFX1200EB-05FE680C[2]	1.25M	2.5/3.3	-5	fpSBGA	680
LFX1200EB-04FE680C[2]	1.25M	2.5/3.3	-4	fpSBGA	680
LFX1200EB-03FE680C[2]	1.25M	2.5/3.3	-3	fpSBGA	680
LFX1200EC-04FE680C[2]	1.25M	1.8	-4	fpSBGA	680
LFX1200EC-03FE680C[2]	1.25M	1.8	-3	fpSBGA	680

1. FH516 package was converted to F516 via PCN #09A-08.
2. Discontinued via PCN #03A-10.

"E-Series" Industrial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125EB-04F256I	139K	2.5/3.3	-4	fpBGA	256
LFX125EB-03F256I	139K	2.5/3.3	-3	fpBGA	256
LFX125EC-03F256I	139K	1.8	-3	fpBGA	256
LFX125EB-04F516I	139K	2.5/3.3	-4	fpBGA	516
LFX125EB-03F516I	139K	2.5/3.3	-3	fpBGA	516
LFX125EC-03F516I	139K	1.8	-3	fpBGA	516
LFX125EB-04FH516I[1]	139K	2.5/3.3	-4	fpBGA	516
LFX125EB-03FH516I[1]	139K	2.5/3.3	-3	fpBGA	516
LFX125EC-03FH516I[1]	139K	1.8	-3	fpBGA	516
LFX200EB-04F256I	210K	2.5/3.3	-4	fpBGA	256
LFX200EB-03F256I	210K	2.5/3.3	-3	fpBGA	256
LFX200EC-03F256I	210K	1.8	-3	fpBGA	256
LFX200EB-04F516I	210K	2.5/3.3	-4	fpBGA	516
LFX200EB-03F516I	210K	2.5/3.3	-3	fpBGA	516
LFX200EC-03F516I	210K	1.8	-3	fpBGA	516
LFX200EB-04FH516I[1]	210K	2.5/3.3	-4	fpBGA	516
LFX200EB-03FH516I[1]	210K	2.5/3.3	-3	fpBGA	516
LFX200EC-03FH516I[1]	210K	1.8	-3	fpBGA	516
LFX500EB-04F516I	476K	2.5/3.3	-4	fpBGA	516
LFX500EB-03F516I	476K	2.5/3.3	-3	fpBGA	516
LFX500EC-03F516I	476K	1.8	-3	fpBGA	516
LFX500EB-04FH516I[1]	476K	2.5/3.3	-4	fpBGA	516
LFX500EB-03FH516I[1]	476K	2.5/3.3	-3	fpBGA	516
LFX500EC-03FH516I[1]	476K	1.8	-3	fpBGA	516
LFX500EB-04F900I	476K	2.5/3.3	-4	fpBGA	900
LFX500EB-03F900I	476K	2.5/3.3	-3	fpBGA	900
LFX500EC-03F900I	476K	1.8	-3	fpBGA	900