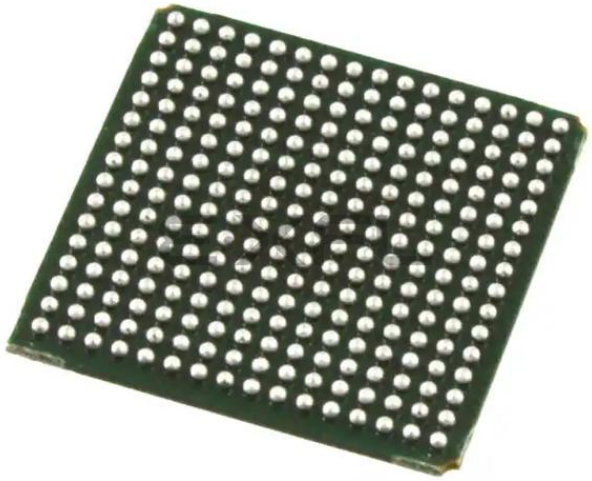
Lattice Semiconductor Corporation - LFX200B-05FN256C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

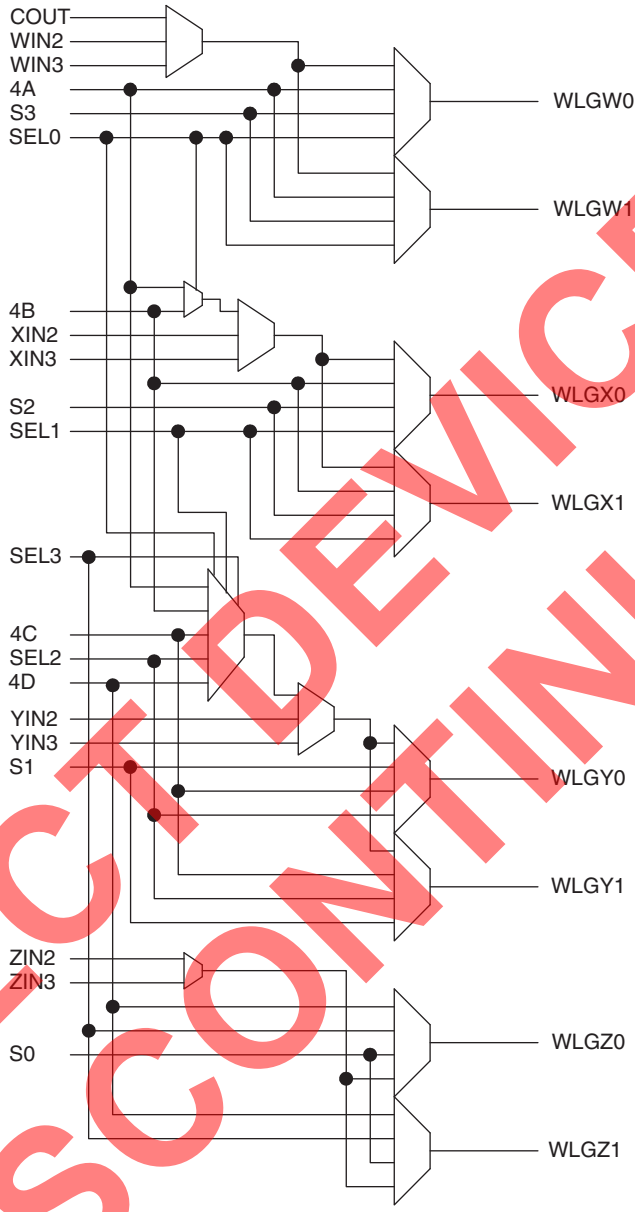
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	2704
Total RAM Bits	113664
Number of I/O	160
Number of Gates	210000
Voltage - Supply	2.3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx200b-05fn256c

Product Line	Ordering Part Number	Product Status	Reference PCN
LFX125EC (Cont'd)	LFX125EC-03F516C	**Discontinued**	PCN#09-10
	LFX125EC-04F516C		
	LFX125EC-03F516I		
LFX200EB	LFX200EB-03F256C	Active / Orderable	
	LFX200EB-03FN256C		
	LFX200EB-04F256C		
	LFX200EB-04FN256C		
	LFX200EB-05F256C		
	LFX200EB-05FN256C		
	LFX200EB-03F256I		
	LFX200EB-03FN256I		
	LFX200EB-04F256I		
	LFX200EB-04FN256I		
	LFX200EB-03F516C	**Discontinued**	PCN#09-10
	LFX200EB-04F516C		
	LFX200EB-05F516C		
	LFX200EB-03F516I		
	LFX200EB-04F516I		
LFX200EC	LFX200EC-03F256C	**Discontinued**	PCN#09-10
	LFX200EC-03FN256C		
	LFX200EC-04F256C		
	LFX200EC-04FN256C		
	LFX200EC-03F256I		
	LFX200EC-03FN256I		
	LFX200EC-03F516C		
	LFX200EC-04F516C		
	LFX200EC-03F516I		
LFX500EB	LFX500EB-03F516C	**Discontinued**	PCN#09-10
	LFX500EB-04F516C		
	LFX500EB-05F516C		
	LFX500EB-03F516I		
	LFX500EB-04F516I		
	LFX500EB-03F900C		
	LFX500EB-03FN900C		
	LFX500EB-04F900C		
	LFX500EB-04FN900C		
	LFX500EB-05F900C		
	LFX500EB-05FN900C		
	LFX500EB-03F900I		
	LFX500EB-03FN900I		
	LFX500EB-04F900I		
	LFX500EB-04FN900I		
LFX500EC	LFX500EC-03F516C	**Discontinued**	PCN#09-10
	LFX500EC-04F516C		
	LFX500EC-03F516I		

Figure 6. ispXPGA Wide Logic Generator



Configurable Sequential Element

There are two registers in each CSE for a total of eight registers in each PFU. This high register count assists in implementing efficient pipelined applications with no utilization penalty. Each register can be configured as a latch or D type flip-flop with either synchronous or asynchronous set or reset. Figure 2 shows the signals that feed the register's D inputs. Feed-through signals in the architecture ensure that registers are efficiently utilized even if the accompanying LUT is occupied.

Control Logic

The control signals available to the registers in a PFU are Clock, Clock Enable, and Set/Reset. Figure 7 shows the various options available to generate the clock signal. As can be seen, the clock signal is the output of a 12:1 MUX with true and compliment versions available from the 12:1 MUX. Each CSE can chose whether it uses the true or complement form of the clock. Figure 8 shows the Set/Reset selection for each PFU in the ispXPGA. A common

Set/Reset signal controls all the registers for each PFU. This common Set/Reset signal is composed of the logical OR term of the Global Set/Reset signal (GSR) and the selected signal from routing. The polarity of this signal is not controllable inside the PFU. The polarity of the Global Set/Reset signal (GSR) is programmable. Figure 9 shows the Clock Enable and Output Enable selection for each PFU.

Figure 7. Clock Selection per PFU

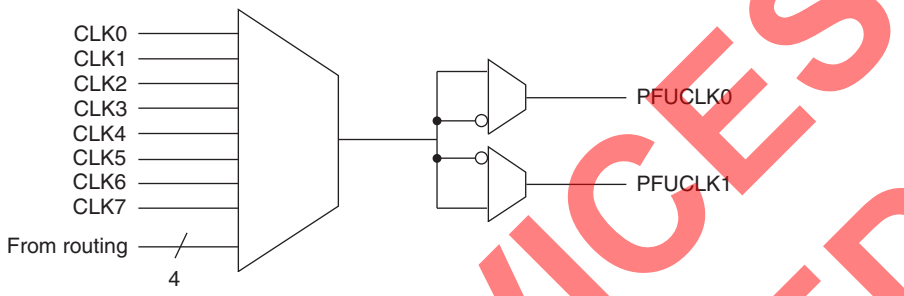


Figure 8. Set/Reset Selection per PFU

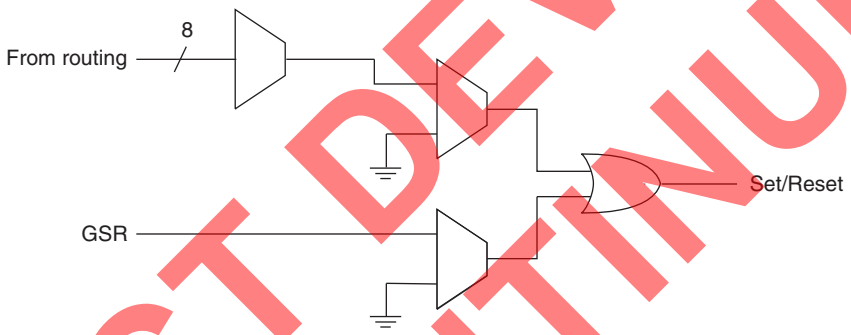
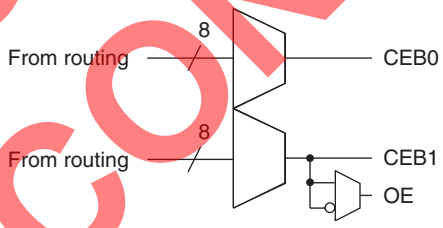


Figure 9. Clock Enable and Output Enable Selection per PFU

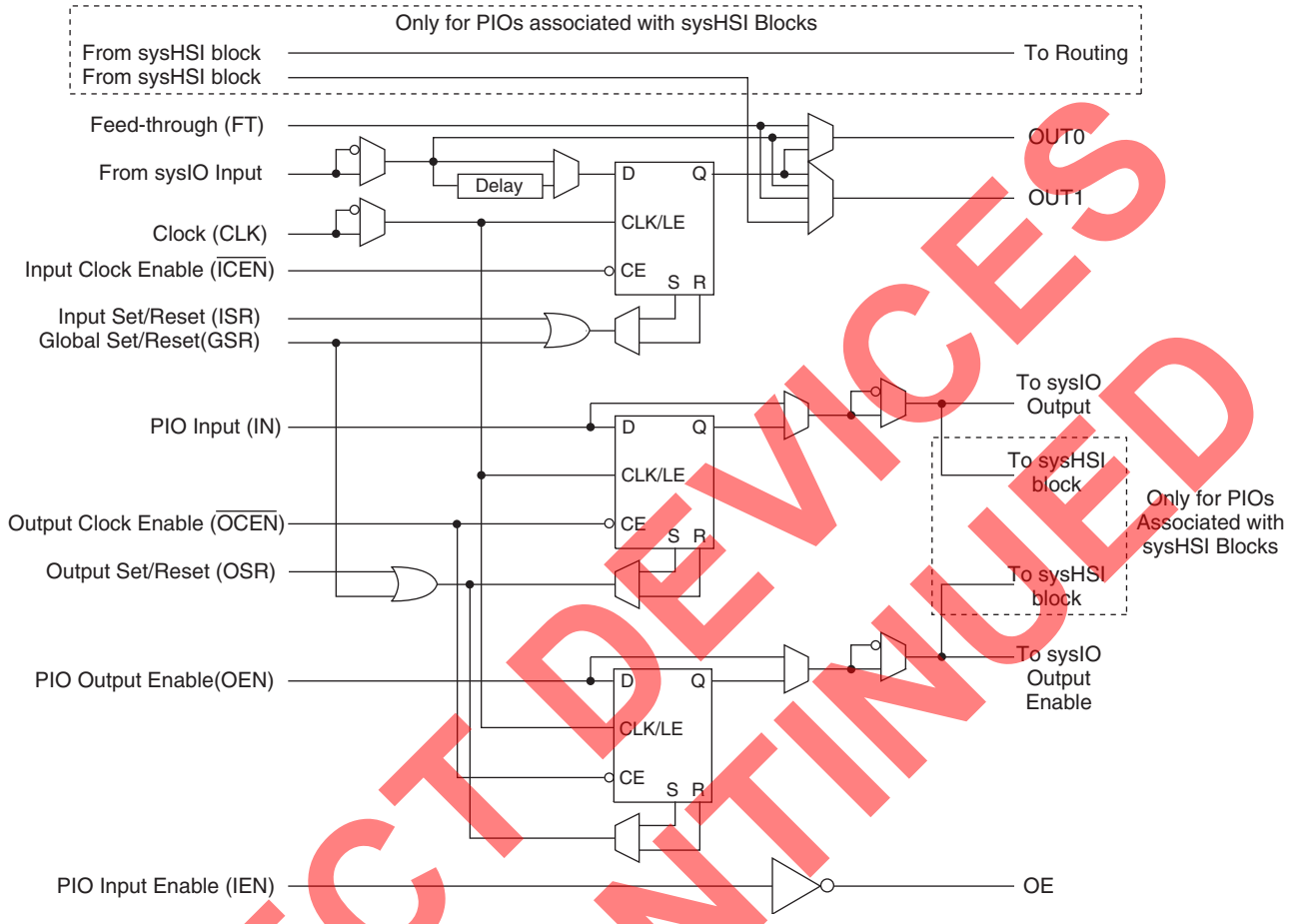


Programmable Input/Output Cell

The Programmable Input/Output Cell (PIC) is an essential part of the symmetrical architecture of the ispXPGA Family. The PICs interface the PFUs and EBRs to the sysIO and sysHSI blocks of the device.

Each PIC contains two Programmable Input/Outputs (PIOs) with a total of 21 inputs and 10 outputs. There are 18 inputs from routing, two inputs from the sysIO buffers, and the Global Set/Reset signal. Four outputs of the PIC connect to routing and two outputs are available as Output Enables for the tri-statable Long Lines. The remaining four outputs feed the sysIO buffers directly (one output enable and one output to each). Each PIC associated with a sysHSI block has four additional inputs and six additional outputs to support the sysHSI blocks. The four additional inputs come from the sysHSI block associated with the PIC. The four of the six additional outputs come from the PIC outputs and feed the sysHSI block, while the remaining two outputs feed routing. Figure 10 shows the block diagram of the PIC with the sysHSI block inputs and outputs.

Figure 11. ispXPGA PIO



VLI Routing Resources

The ispXPGA architecture contains a Variable-Length-Interconnect (VLI) routing technology connecting the PFUs, PICs, and EBRs in the device. There are four types of routing resources, Global Lines, Long Lines, General Interconnect, and Local Lines forming the global routing structure. This allows a signal to be routed to any element in the device with the optimal delay.

The Global Lines consist of global clock lines and a global set/reset line. These lines are routed to all elements in the device. They are specifically designed for high speed, predictable timing regardless of fan-out. The global clock lines can also be used as dedicated inputs.

The Long Lines consist of Horizontal and Vertical Long Lines (HLL and VLL). The VLL and HLL are tri-statable lines spanning the entire device. These lines allow fast routing for high fan-out nets and general-purpose functions.

The General Interconnect consists of Double and Deca Lines. The Double Lines connect up to three elements (two plus the driving element), while the Deca Lines connect up to eleven elements (ten plus the driving element).

The Local Lines are extremely fast routing paths consisting of Feedback and Direct Connect Lines. The Feedback Lines are internal routing paths from the PFU outputs to the PFU inputs. The Direct Connect Lines connect all adjacent elements.

The Common Interface Block (CIB) provides the link between the logic element (PFU, PIC, or EBR) and the VLI Routing resources. The CIB is a switch matrix that can be programmed to connect virtually any routing resource to any input or output of the logic element.

Table 5. ispXPGA Supported I/O Standards

sysIO Standard	V_{CCO}	V_{REF}	V_{TT}
LVTTL	3.3V	N/A	N/A
LVCMOS-3.3	3.3V	N/A	N/A
LVCMOS-2.5	2.5V	N/A	N/A
LVCMOS-1.8	1.8V	N/A	N/A
PCI	3.3V	N/A	N/A
AGP-1X	3.3V	N/A	N/A
SSTL3, Class I, II	3.3V	1.5V	1.5V
SSTL2, Class I, II	2.5V	1.25V	1.25V
HSTL, Class I	1.5V	0.75V	0.75V
HSTL, Class III	1.5V	0.9V	1.5V
GTL+	N/A	1.0V	1.5V
LVPECL	3.3V	N/A	N/A
LVDS[1]	2.5V	N/A	N/A
BLVDS	2.5V	N/A	N/A

1. V_{CCO} must be 2.5V for high speed serial operations (sysHSI block).

Table 6. Differential Interface Standard Support[1]

		sysIO Buffer Not Using sysHSI Block	sysIO Buffer Using sysHSI Block
LVDS	Driver	Supported with external resistor network	Supported
	Receiver	Supported with standard termination	Supported with standard termination
BLVDS	Driver	Supported with external resistor network	Not supported
	Receiver	Supported (may need termination)	Supported (may need termination)
LVPECL	Driver	Supported with external resistor network	Not supported
	Receiver	Supported with termination	Supported with termination

1. For more information, refer to TN1000, sysIO Usage Guidelines for Lattice Devices.

pattern by a device programmer, securing proprietary designs from competitors. The entire device must be erased in order to erase the security scheme.

Density Shifting

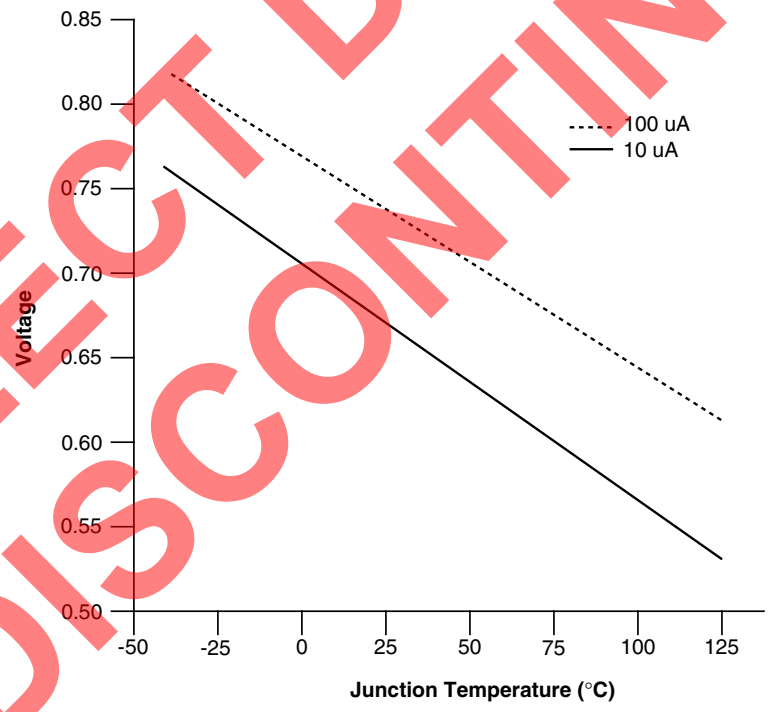
The ispXPGA family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

Temperature Sensing Diode

The built-in temperature-sensing diodes allow junction temperature to be measured during device operation. A pair of pins (DXp and DXn) are dedicated for monitoring device junction temperature. The measurement is done by forcing 10 µA and 100 µA current in the forward direction, and then measuring the resulting voltage. The voltage decreases with increasing temperature at approximately 1.64 mV/°C. A typical device with a 85°C junction temperature will measure approximately 593 mV.

The temperature-sensing diode works for the entire operating range as shown in Figure 22 - Sensing Diode Voltage-Temperature Relationship. Refer to the Lattice Thermal Management document for thermal coefficients. Also refer to TN1043, Power Estimation in ispXPGA Devices.

Figure 22. Sensing Diode Voltage-Temperature Relationship



sysIO Differential Standards DC Electrical Characteristics[1]

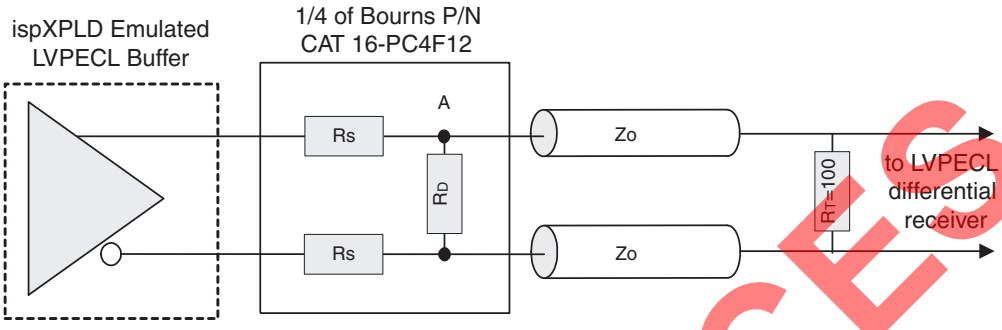
Parameter	Description	Test Conditions	Min.	Typ.	Max.
LVDS[2]					
V_{INP}, V_{INM}	Input voltage		0V	—	2.4V
V_{THD}	Differential input threshold	0.2V ð V_{CM} ð 1.8V	+/-100mV	—	—
I_{IN}	Input current	Power on	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	—	1.38V	1.60V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	0.9V	1.03V	—
V_{OD}	Output Voltage Differential	$\|V_{OP} - V_{OM}\|$, R_T = 100 ohm	250mV	350mV	450mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50mV
V_{OS}	Output Voltage Offset	$\|V_{OP} + V_{OM}\|/2$, R_T = 100 ohm	1.125V	1.25V	1.375V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50mV
I_{OSD}	Output short circuit current	V_{OD} = 0V Driver outputs shorted	—	—	24mA
BLVDS[1]					
V_{INP}, V_{INM}	Input voltage		0V	—	2.4V
V_{THD}	Differential input threshold	0.2V ð V_{CM} ð 1.8V	+/-100mV	—	—
I_{IN}	Input current	Power on	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 27Ω	—	1.4V	1.80V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 27Ω	0.95V	1.1V	—
V_{OD}	Output Voltage Differential	$\|V_{OP} - V_{OM}\|$, RT = 27Ω	240mV	300mV	460mV
ΔV_{OD}	Change in V_{OD} Between H and L				27mV
V_{OS}	Output Voltage Offset	$\|V_{OP} + V_{OM}\|$ /2, RT = 27Ω	1.1V	1.3V	1.5V
ΔV_{OS}	Change in V_{OS} Between H and L				27mV
I_{OSD}	Output Short Circuit Current	V_{OD} = 0. Driver Outputs Shorted.		36mA	65mA

1. Refer to TN1000, sysIO Usage Guidelines for Lattice Devices.
2. V_{OP} and V_{OM} are the two outputs of the LVDS/BLVDS output buffer.

LVPECL[1]								
DC Parameter	**Parameter Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
V_{CCO}		**3.0**		**3.3**		**3.6**		**V**
V_{IH}	Input Voltage High	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	Input Voltage Low	0.86	2.125	0.86	2.125	0.86	2.125	V
V_{OH}	Output Voltage High	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	Output Voltage Low	0.96	1.27	1.06	1.43	1.3	1.57	V
V_{DIFF}[2]	Differential Input threshold	0.3	—	0.3	—	0.3	—	V

1. These values are valid at the output of the source termination pack as shown above with 100-ohm differential load only (see Figure 23). The V_{OH} levels are 200mV below the standard LVPECL levels and are compatible with devices tolerant of the lower common mode ranges.
2. Valid for 0.2 ð V_{CM} ð 1.8V.

Figure 23. LVPECL Driver with Three Resistor Pack



ispXPGA 125B/C & ispXPGA 125EB/EC External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Conditions	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{CO}	Global Clock Input to Output	PIO Output Register	—	5.3	—	5.7	—	6.6	ns
t_{S}	Global Clock Input Setup	PIO Input Register without input delay	-1.9	—	-1.8	—	-1.5	—	ns
t_{H}	Global Clock Input Hold	PIO Input Register without input delay	2.7	—	2.9	—	3.3	—	ns
t_{SINDLY}	Global Clock Input Setup	PIO Input Register with input delay	3.1	—	3.3	—	3.8	—	ns
t_{HINDLY}	Global Clock Input Hold	PIO Input Register with input delay	0.0	—	0.0	—	0.0	—	
t_{COPLL}	Global Clock Input to Output	PIO Output Register using PLL without delay	—	3.6	—	3.9	—	4.5	ns
t_{SPLL}	Global Clock Input Setup	PIO Input Register without input delay using PLL without delay	0	—	0.1	—	0.3	—	ns
t_{HPLL}	Global Clock Input Hold	PIO Input Register without input delay using PLL without delay	0.9	—	1.0	—	1.2	—	ns
$t_{SINDLYPLL}$	Global Clock Input Setup	PIO Input Register with input delay using PLL without delay	5.1	—	5.5	—	6.3	—	ns
$t_{HINDLYPLL}$	Global Clock Input Hold	PIO Input Register with input delay using PLL without delay	-3.0	—	-2.8	—	-2.4	—	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 125B/C & ispXPGA 125EB/EC Timing Adders

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	4.28	—	4.6	—	5.29	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

ispXPGA 500B/C & ispXPGA 500EB/EC Timing Adders

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	5.21	—	5.60	—	6.44	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

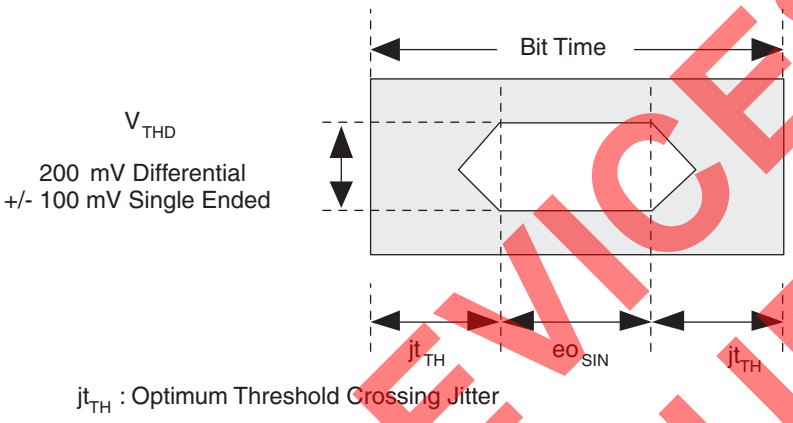
ispXPGA 1200B/C & ispXPGA 1200EB/EC Timing Adders

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	5.58	—	6.0	—	6.90	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

sysHSI Block Timing

Figure 24 provides a graphical representation of the SERDES receiver input requirements. It provides guidance on a number of input parameters, including signal amplitude and rise time limits, noise and jitter limits, and P and N input skew tolerance.

Figure 24. Receive Data Eye Diagram Template (Differential)



The data pattern eye opening at the receive end of a link is considered the ultimate measure of received signal quality. Almost all detrimental characteristics of a transmit signal and the interconnection link design result in eye closure. This combined with the eye-opening limitations of the line receiver can provide a good indication of a link's ability to transfer error-free data.

Signal jitter is of special interest to system designers. It is often the primary limiting characteristic of long digital links and of systems with high noise level environments. An interesting characteristic of the clock and data recovery (CDR) portion of the ispXPGA SERDES receiver is its ability to filter incoming signal jitter that is below the clock recovery PLL bandwidth. For signals with high levels of low frequency jitter, the receiver can detect incoming data error free, with eye openings significantly less than that shown in Figure 24.

sysHSI Block AC Specifications

Operating Frequency Ranges

Symbol	Description	Mode	Test Condition	Device	-5[1]		-4		-3		Units
					Min.	Max.	Min.	Max.	Min.	Max.	
f_{CLK}	Reference Clock Frequency	SS:CAL		LFX125B/C	50	200	50	200	50	200	MHz
				LFX200B/C	50	188	50	188	50	188	
				LFX500B/C	50	188	50	188	50	188	
				LFX1200B/C	50	175	50	175	50	175	
		10B12B		LFX125B/C	33	67	33	67	33	67	MHz
				LFX200B/C	33	63	33	63	33	63	
				LFX500B/C	33	63	33	63	33	63	
				LFX1200B/C	33	58	33	58	33	58	
		8B10B		LFX125B/C	40	80	40	80	40	80	MHz
				LFX200B/C	40	75	40	75	40	75	
				LFX500B/C	40	75	40	75	40	75	
				LFX1200B/C	40	70	40	70	40	70	
f_{SIN}[2]	Serial Input	SS:CAL	with eoSIN	LFX125B/C	400	800	400	800	400	800	Mbps
				LFX200B/C	400	750	400	750	400	750	
				LFX500B/C	400	750	400	750	400	750	
				LFX1200B/C	400	700	400	700	400	700	
		10B12B	with eoSIN	LFX125B/C	400	800	400	800	400	800	Mbps
				LFX200B/C	400	750	400	750	400	750	
				LFX500B/C	400	750	400	750	400	750	
				LFX1200B/C	400	700	400	700	400	700	
		8B10B	with eoSIN	LFX125B/C	400	800	400	800	400	800	Mbps
				LFX200B/C	400	750	400	750	400	750	
				LFX500B/C	400	750	400	750	400	750	
				LFX1200B/C	400	700	400	700	400	700	
f_{OUT}[2]	Serial Out	LVDS	CL = 5 pF, RL = 100¾ f_{CLK} with no jitter	LFX125B/C	400	800	400	800	400	800	Mbps
				LFX200B/C	400	750	400	750	400	750	
				LFX500B/C	400	750	400	750	400	750	
				LFX1200B/C	400	700	400	700	400	700	

1. Only available for ispXPGA 125B, 200B, 500B and 1200B (2.5V/3.3V) devices.
2. f_{SIN} and f_{SOUT} speeds are supported at V_{CC} and V_{CCP} at 1.7V to 1.9V for ispXPGA 1.8V devices.

LOCKIN Time

Symbol	Description	Mode	Condition	Min	Max	Unit
t_{SCLOCK}	CSPLL Lock Time	All	After input is stabilized		25	µS
$t_{CDRLOCK}$	CDRPLL Lock-in Time	SS	With SS mode sync pattern		1024	t_{RCP}[1]
		10B12B	With 10B12B sync pattern		1024	t_{RCP}
		8B10B	With 8B10B idle pattern		960	t_{RCP}
t_{SYNC}	SyncPat Length	SS		1200		t_{RCP}
t_{CAL}	CAL Duration	SS		1100		t_{RCP}
t_{SUSYNC}	SyncPat Set-up Time to CAL	SS		50		t_{RCP}
t_{HDSYNC}	SyncPat Hold Time from CAL	SS		50		t_{RCP}

1. REFCLK clock period.

REFCLK and SS_CLKIN Timing

Symbol	Description	Mode	Condition	Min	Max	Unit
$t_{DREFCLK}$	Frequency Deviation Between TX REFCLK and CDRX REFCLK on One Link	8B10B/ 10B12B		-100	100	ppm
$t_{JPPREFCLK}$	REFCLK, SS_CLKIN Peak-to-Peak Period Jitter	All	Random Jitter		0.01	UIPP
$t_{PWREFCLK}$	REFCLK, SS_CLKIN Pulse Width, (80% to 80% or 20% to 20%).	All	40-100MHz	2		ns
			100-200MHz	1		
$t_{RFREFCLK}$	REFCLK, SS_CLKIN Rise/Fall Time (20% to 80% or 80% to 20%)	All			2	ns

Serializer Timing[2]

Symbol	Description	Mode	Condition	Min	Max	Unit
$t_{JPPSOUT}$	SOUT Peak-to-Peak Output Data Jitter	All	f_{CLK} with no jitter		0.25	UIPP
$t_{JPP8B10B}$	SOUT Peak-to-Peak Random Jitter	8B10B	800 Mbps w/K28.7-		130	ps
	SOUT Peak-to-Peak Deterministic Jitter	8B10B	800 Mbps w/K28.5+		160	ps
t_{RFSOUT}	SOUT Output Data Rise/Fall Time (20%, 80%)	LVDS			700	ps
t_{COSOUT}	REFCLK to SOUT Delay	SS/8B10B		$2Bt^{1}$ + 2	$2Bt^{1}$ +10	ns
		10B12B		$1Bt^{1}$ + 2	$1Bt^{1}$ +10	ns
t_{SKTX}	Skew of SOUT with Respect to SS_CLKOUT	SS			300	ps
$t_{CKOSOUT}$	SS_CLKOUT to bit0 of SOUT	SS		$2Bt^{1}$ - t_{SKTX}	$2Bt^{1}$ + t_{SKTX}	ns
$t_{HSITXDDATAS}$	TXD Data Setup Time	All	Note 3	1.5		ns
$t_{HSITXDDATAH}$	TXD Data Hold Time	All	Note 3		1.0	ns

1. Bt: Bit Time Period. High Speed Serial Bit Time.
2. The SIN and SOUT jitter specifications listed above are under the condition that the clock tree that drives the REFCLK to sysHSI Block is in sysCLOCK PLL BYPASS mode.
3. Internal timing for reference only.

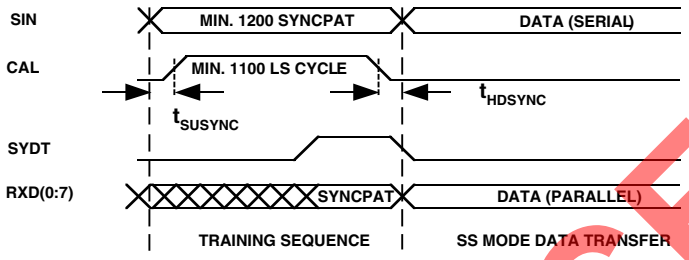
Deserializer Timing

Symbol	Description	Mode	Conditions	Min	Max	Units
f_{DSIN}	SIN Frequency Deviation from REFCLK	8B10B/ 10B12B		-100	100	ppm
eo_{SIN}	SIN Eye Opening Tolerance	All	Notes 1, 2	0.45		UIPP
ber	Bit Error Rate	All			10^{-12}	Bits
$t_{HSIOUTVALIDPRE}$	RXD, SYDT Valid Time Before RECCLK Falling Edge	All	Note 3	$t_{RCP}/2$ - 0.7		ns
$t_{HSIOUTVALIDPOST}$	RXD, SYDT Valid Time After RECCLK Falling Edge	All	Note 3	$t_{RCP}/2$ - 0.7		ns
t_{DSIN}	Bit 0 of SIN Delay to RXD Valid at RECCLK Falling edge	All		1.5 t_{RCP} + 4.5Bt + 3	1.5 t_{RCP} + 4.5Bt + 15	ns

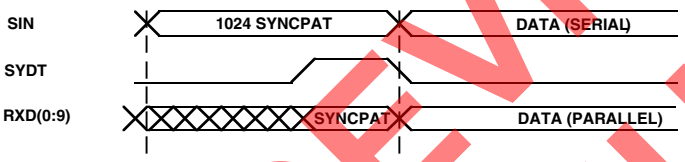
1. Eye opening based on jitter frequency of 100KHz.
2. Lower frequency operation assumes maximum eye closure of 800ps.
3. Internal timing for reference only.

Lock-in Timing

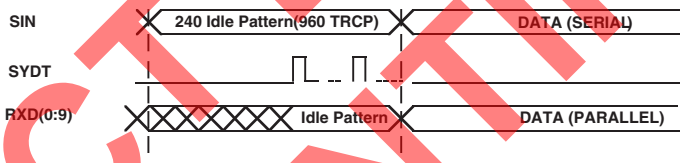
CDRX_SS LOCK-IN (DE-SKEW) TIMING



CDR_10B12B LOCK-IN TIMING

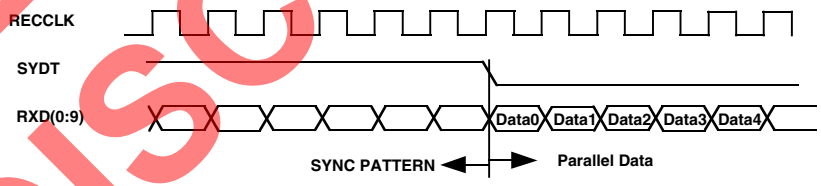


CDR_8B10B LOCK-IN TIMING

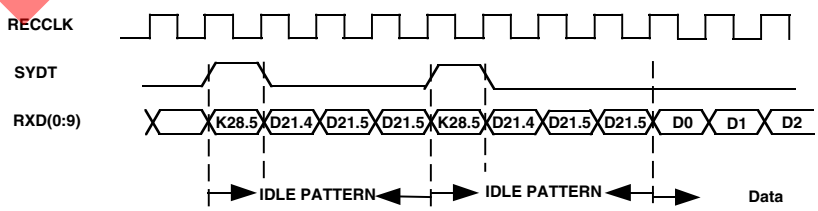


SYDT Timing

SYDT TIMING FOR CDRX_10B12B



SYDT TIMING FOR CDRX_8B10B



ispXPGA Power Supply and NC Connections[1]

Signal	256-Ball fpBGA[3]	516-Ball fpBGA[3]
V_{CC}	C3, C14, D4, D13, E5, E12, F6, F11, L6, L11, M5, M12, N4, N13, P3, P14	A9, A22, D4, D27, J1, J30, L11, L12, L15, L16, L19, L20, M11, M20, R11, R20, T11, T20, W11, W20, Y11, Y12, Y15, Y16, Y19, Y20, AB1, AB30, AG4, AG27, AK9, AK22
V_{CCO0}	F5, G5	F4, J4, M4, N11, P4, P11
V_{CCO1}	K5, L5	U4, U11, V11, W4, AB4, AE4
V_{CCO2}	M6, M7	Y13, Y14, AG6, AG9, AG12, AG14
V_{CCO3}	M10, M11	Y17, Y18, AG17, AG19, AG22, AG25
V_{CCO4}	K12, L12	U20, U27, V20, W27, AB27, AE27
V_{CCO5}	G12, F12	F27, J27, M27, N20, P20, P27
V_{CCO6}	E10, E11	D17, D19, D22, D25, L17, L18
V_{CCO7}	E6, E7	D6, D9, D12, D14, L13, L14
V_{CCP}	H3, J15	R4, T30
V_{CCJ}	A2	C4
GND	A1, A16, B2, B15, F7, F8, F9, F10, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L7, L8, L9, L10, R2, R15, T1, T16	A1, A30, B2, B29, C3, C28, M12, M13, M14, M15, M16, M17, M18, M19, N12, N13, N14, N15, N16, N17, N18, N19, P12, P13, P14, P15, P16, P17, P18, P19, R12, R13, R14, R15, R16, R17, R18, R19, T12, T13, T14, T15, T16, T17, T18, T19, U12, U13, U14, U15, U16, U17, U18, U19, V12, V13, V14, V15, V16, V17, V18, V19, W12, W13, W14, W15, W16, W17, W18, W19, AH3, AH28, AJ2, AJ29, AK1, AK30
GND_P	H15, J4	R29, T4
NC[2]	—	**LFX125:** A10, A13, A16, A17, A24, A25, A26, A4, A5, A6, A7, AA1, AA2, AA28, AA29, AA3, AB28, AC1, AC28, AD1, AD27, AD4, AE28, AE29, AE3, AE30, AF27, AF28, AF29, AF3, AF4, AG1, AG10, AG11, AG15, AG2, AG20, AG23, AG24, AG29, AG3, AG8, AH1, AH15, AH19, AH2, AH20, AH23, AH24, AH30, AH7, AH8, AH9, AJ1, AJ12, AJ14, AJ15, AJ19, AJ20, AJ21, AJ23, AJ24, AJ25, AJ27, AJ30, AJ6, AJ7, AJ8, AK11, AK14, AK15, AK20, AK21, AK23, AK24, AK25, AK27, AK5, AK6, AK7, B10, B13, B16, B17, B18, B23, B24, B25, B5, B6, B7, C11, C13, C14, C16, C17, C22, C23, C24, C25, C6, C7, C8, D11, D16, D23, D24, D28, D29, D3, D7, D8, E30, E4, F1, F29, F30, G1, G2, G27, G28, G29, G30, H1, H2, H27, H28, H29, H30, J2, J28, J29, J3, K1, K2, K27, K28, K3, K4, L1, L2, L27, L3, L4, M1, M2, M29, M3, M30, V27, V28, V3, V4, W1, W30, Y1, Y27, Y28, Y3, Y30 **LFX200:** A26, A25, A24, A17, A10, A7, A6, A5, A4, B25, B24, B23, B17, B10, B7, B6, B5, C25, C24, C23, C22, C16, C11, C8, C7, C6, D24, D23, D16, D11, D8, D7, E30, F30, F29, F1, G30, G29, G28, G27, G2, G1, H30, H29, H28, H27, H2, H1, J29, J28, J3, J2, K28, K27, K4, K3, K2, K1, L27, L4, L3, L2, L1, M3, V28, V27, V4, V3, W30, W1, Y30, Y28, Y27, Y3, Y1, AA29, AA28, AA3, AA2, AA1, AD27, AD4, AE28, AE3, AF29, AF28, AF27, AF3, AG29, AG24, AG23, AG20, AG11, AG10, AG8, AG2, AG1, AH30, AH24, AH23, AH20, AH9, AH8, AH7, AH2, AH1, AJ30, AJ27, AJ25, AJ24, AJ23, AJ21, AJ15, AJ12, AJ8, AJ7, AJ6, AJ1, AK27, AK25, AK24, AK23, AK21, AK15, AK11, AK7, AK6, AK5

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, V_{CC} or GND.
3. Balls for GND, V_{CC} and V_{CCOx} are connected within the substrate to their respective common signals. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
C8	BK7_IO1	-	91N	BK7_IO1	-	77N
B8	BK7_IO2	-	92P	BK7_IO2	-	78P
B7	BK7_IO3	-	92N	BK7_IO3	-	78N
A9	BK7_IO6	-	94P	BK7_IO4	-	79P
-	GND (Bank 7)	-	-	-	-	-
A8	BK7_IO7	-	94N	BK7_IO5	-	79N
C7	BK7_IO10	-	96P	BK7_IO6	-	80P
D7	BK7_IO11	-	96N	BK7_IO7	-	80N
D6	BK7_IO12	-	97P	BK7_IO8	-	81P
-	-	-	-	GND (Bank 7)	-	-
C6	BK7_IO13	-	97N	BK7_IO9	-	81N
B6	BK7_IO14	-	98P	BK7_IO10	-	82P
-	GND (Bank 7)	-	-	-	-	-
B5	BK7_IO15	-	98N	BK7_IO11	-	82N
A7	BK7_IO16	VREF7	99P	BK7_IO12	VREF7	83P
A6	BK7_IO17	-	99N	BK7_IO13	-	83N
D5	BK7_IO18	-	100P	BK7_IO14	-	84P
C5	BK7_IO19	-	100N	BK7_IO15	-	84N
A5	BK7_IO20	-	101P	BK7_IO16	-	85P
-	-	-	-	GND (Bank 7)	-	-
A4	BK7_IO21	-	101N	BK7_IO17	-	85N
B4	BK7_IO22	-	102P	BK7_IO18	-	86P
-	GND (Bank 7)	-	-	-	-	-
B3	BK7_IO23	-	102N	BK7_IO19	-	86N
A3	TDO	-	-	TDO	-	-
A2	VCCJ	-	-	VCCJ	-	-
C4	TDI	-	-	TDI	-	-

1. Not available for differential pairs.
2. If a sysHSI Block is used, the indicated sysHSI reserved pins are unavailable for general purpose I/O use.

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
A10	BK7_IO18	-	156P	NC	-	-	NC	-	-
B10	BK7_IO19	-	156N	NC	-	-	NC	-	-
C10	BK7_IO20	VREF7	157P	BK7_IO16	VREF7	99P	BK7_IO12	VREF7	83P
D10	BK7_IO21	-	157N	BK7_IO17	-	99N	BK7_IO13	-	83N
B9	BK7_IO22	-	158P	BK7_IO18	-	100P	BK7_IO14	-	84P
-	GND (Bank 7)	-	-	-	-	-	-	-	-
C9	BK7_IO23	-	158N	BK7_IO19	-	100N	BK7_IO15	-	84N
A8	BK7_IO24	-	159P	BK7_IO20	-	101P	BK7_IO16	-	85P
-	-	-	-	-	-	-	GND (Bank 7)	-	-
B8	BK7_IO25	-	159N	BK7_IO21	-	101N	BK7_IO17	-	85N
C8	BK7_IO26	-	160P	NC	-	-	NC	-	-
D8	BK7_IO27	-	160N	NC	-	-	NC	-	-
A7	BK7_IO28	-	161P	NC	-	-	NC	-	-
B7	BK7_IO29	-	161N	NC	-	-	NC	-	-
C7	BK7_IO30	-	162P	NC	-	-	NC	-	-
-	GND (Bank 7)	-	-	-	-	-	-	-	-
D7	BK7_IO31	-	162N	NC	-	-	NC	-	-
A6	BK7_IO32	-	163P	NC	-	-	NC	-	-
B6	BK7_IO33	-	163N	NC	-	-	NC	-	-
B5	BK7_IO34	-	164P	NC	-	-	NC	-	-
C6	BK7_IO35	-	164N	NC	-	-	NC	-	-
A5	BK7_IO36	-	165P	NC	-	-	NC	-	-
A4	BK7_IO37	-	165N	NC	-	-	NC	-	-
B4	BK7_IO38	-	166P	BK7_IO22	-	102P	BK7_IO18	-	86P
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-	-	-	-
C5	BK7_IO39	-	166N	BK7_IO23	-	102N	BK7_IO19	-	86N
A3	BK7_IO40	-	167P	BK7_IO24	-	103P	BK7_IO20	-	87P
A2	BK7_IO41	-	167N	BK7_IO25	-	103N	BK7_IO21	-	87N
D5	TDO	-	-	TDO	-	-	TDO	-	-
C4	VCCJ	-	-	VCCJ	-	-	VCCJ	-	-
B3	TDI	-	-	TDI	-	-	TDI	-	-

1. If a sysHSI Block is used, the indicated sysHSI reserved pins are unavailable for general purpose I/O use.

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
C24	BK1_IO7	SS_CLKIN0N	34N
A22	BK1_IO8	-	35P
D22	BK1_IO9	-	35N
A23	BK1_IO10	-	36P
-	GND (Bank 1)	-	-
B25	BK1_IO11	-	36N
D23	BK1_IO12	PLL_RST2	37P
A24	BK1_IO13	PLL_RST3	37N
A25	BK1_IO14	-	38P
E24	BK1_IO15	-	38N
D24	BK1_IO16	-	39P
A26	BK1_IO17	-	39N
D25	BK1_IO18	-	40P
-	GND (Bank 1)	-	-
C25	BK1_IO19	-	40N
B26	BK1_IO20	-	41P/HSI3
B27	BK1_IO21	-	41N/HSI3
D26	BK1_IO22	-	42P/HSI3
A27	BK1_IO23	-	42N/HSI3
A28	BK1_IO24	-	43P/HSI3
E26	BK1_IO25	-	43N/HSI3
C27	BK1_IO26	HSI3A_SOUTP	44P/HSI3
-	GND (Bank 1)	-	-
D27	BK1_IO27	HSI3A_SOUTN	44N/HSI3
B28	BK1_IO28	-	45P/HSI3
A30	BK1_IO29	-	45N/HSI3
C28	BK1_IO30	HSI3A_SINP	46P/HSI3
D28	BK1_IO31	HSI3A_SINN	46N/HSI3
A31	BK1_IO32	-	47P/HSI3
B30	BK1_IO33	-	47N/HSI3
E28	BK1_IO34	HSI3B_SOUTP	48P/HSI3
-	GND (Bank 1)	-	-
D29	BK1_IO35	HSI3B_SOUTN	48N/HSI3
C29	BK1_IO36	-	49P/HSI4
B31	BK1_IO37	-	49N/HSI4
D30	BK1_IO38	HSI3B_SINP	50P/HSI4
E30	BK1_IO39	HSI3B_SINN	50N/HSI4
A32	BK1_IO40	-	51P/HSI4
C31	BK1_IO41	-	51N/HSI4
D31	BK1_IO42	HSI4A_SOUTP	52P/HSI4
-	GND (Bank 1)	-	-
C32	BK1_IO43	HSI4A_SOUTN	52N/HSI4
B32	BK1_IO44	-	53P/HSI4

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
-	GND (Bank 4)	-	-
AW26	BK4_IO43	-	145N
AV25	BK4_IO44	-	146P
AT24	BK4_IO45	-	146N
AU24	BK4_IO46	-	147P
AU25	BK4_IO47	-	147N
AW25	BK4_IO48	PLL_RST4	148P
AW24	BK4_IO49	PLL_RST5	148N
AU23	BK4_IO50	-	149P
-	GND (Bank 4)	-	-
AT23	BK4_IO51	-	149N
AV24	BK4_IO52	-	150P
AW23	BK4_IO53	-	150N
AV23	BK4_IO54	SS_CLKIN1P	151P
AU22	BK4_IO55	SS_CLKIN1N	151N
AR21	BK4_IO56	PLL_FBK4	152P
AT22	BK4_IO57	PLL_FBK5	152N
AV22	BK4_IO58	SS_CLKOUT1P	153P
-	GND (Bank 4)	-	-
AV21	BK4_IO59	SS_CLKOUT1N	153N
AT21	BK4_IO60	CLK_OUT4	154P
AU21	BK4_IO61	CLK_OUT5	154N
-	GND (Bank 4)	-	-
AT19	GCLK4	-	LVDS Pair2P
AU19	GCLK5	-	LVDS Pair2N
AW22	VCCP1	-	-
AR20	GNDP1	-	-
AU18	GCLK6	-	LVDS Pair3P
AT18	GCLK7	-	LVDS Pair3N
-	GND (Bank 5)	-	-
AV17	BK5_IO0	CLK_OUT6	155P
AV18	BK5_IO1	CLK_OUT7	155N
AW21	BK5_IO2	PLL_FBK6	156P
-	GND (Bank 5)	-	-
AV19	BK5_IO3	PLL_FBK7	156N
AR19	BK5_IO4	-	157P/HSI7
AW19	BK5_IO5	-	157N/HSI7
AW18	BK5_IO6	PLL_RST6	158P/HSI7
AW17	BK5_IO7	PLL_RST7	158N/HSI7
AT17	BK5_IO8	-	159P/HSI7
AV16	BK5_IO9	-	159N/HSI7
AU17	BK5_IO10	HSI7A_SINP	160P/HSI7
-	GND (Bank 5)	-	-