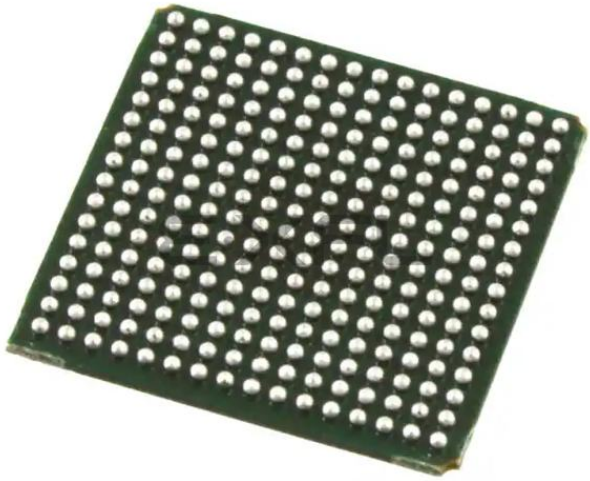
# Lattice Semiconductor Corporation - LFX200EB-03F256C Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 2704 |
| Total RAM Bits | 113664 |
| Number of I/O | 160 |
| Number of Gates | 210000 |
| Voltage - Supply | 2.3V ~ 3.6V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 256-BGA |
| Supplier Device Package | 256-FPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx200eb-03f256c |

## Architecture Overview

The ispXPGA architecture is a symmetrical architecture consisting of an array of Programmable Function Units (PFUs) enclosed by Input Output Groups (PICs) with columns of sysMEM Embedded Block RAMs (EBRs) distributed throughout the array. Figure 1 illustrates the ispXPGA architecture. Each PIC has two corresponding sysIO blocks, each of which includes one input and output buffer. On two sides of the device, between the PICs and the sysIO blocks, there are sysHSI High-Speed Interface blocks. The symmetrical architecture allows designers to easily implement their designs, since any logic function can be placed in any section of the device.

The PFUs contain the basic building blocks to create logic, memory, arithmetic, and register functions. They are optimized for speed and flexibility allowing complex designs to be implemented quickly and efficiently.

The PICs interface the PFUs and EBRs to the external pins of the device. They allow the signals to be registered quickly to minimize setup times for high-speed designs. They also allow connections directly to the different logic elements for fast access to combinatorial functions.

The sysMEM EBRs are large, fast memory elements that can be configured as RAM, ROM, FIFO, and other storage types. They are designed to facilitate both single and dual-port memory for high-speed applications.

These three components of the architecture are interconnected via a high-speed, flexible routing array. The routing array consists of Variable Length Interconnect (VLI) lines between the PICs, PFUs, and EBRs. There is additional routing available to the PFU for feedback and direct routing of signals to adjacent PFUs or PICs.

The sysIO blocks consist of configurable input and output buffers connected directly to the PICs. These buffers can be configured to interface with 16 different I/O standards. This allows the ispXPGA to interface with other devices without the need for external transceivers.

The sysHSI blocks provide the necessary components to allow the ispXPGA device to transfer data at up to 800Mbps using the LVDS standard. These components include serializing, de-serializing, and clock data recovery (CDR) logic.

The sysCLOCK blocks provide clock multiplication/division, clock distribution, delay compensation, and increased performance through the use of PLL circuitry that manipulates the global clocks. There is one sysCLOCK block for each global clock tree in the device.

Set/Reset signal controls all the registers for each PFU. This common Set/Reset signal is composed of the logical OR term of the Global Set/Reset signal (GSR) and the selected signal from routing. The polarity of this signal is not controllable inside the PFU. The polarity of the Global Set/Reset signal (GSR) is programmable. Figure 9 shows the Clock Enable and Output Enable selection for each PFU.

***Figure 7. Clock Selection per PFU***

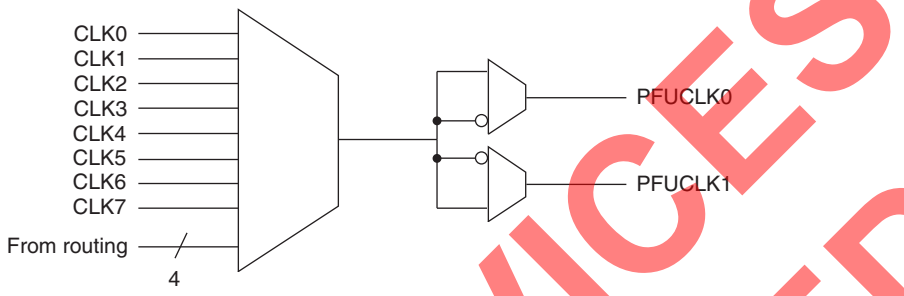



***Figure 8. Set/Reset Selection per PFU***

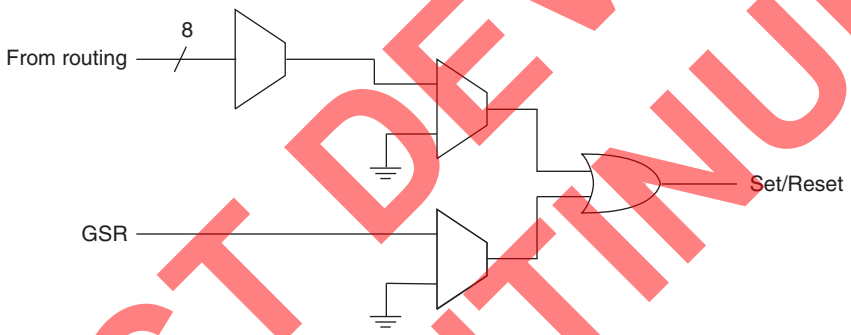
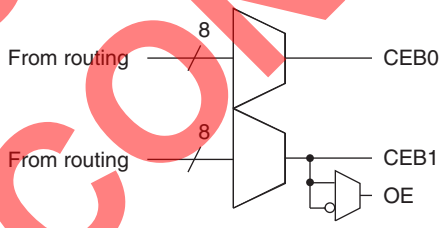



***Figure 9. Clock Enable and Output Enable Selection per PFU***

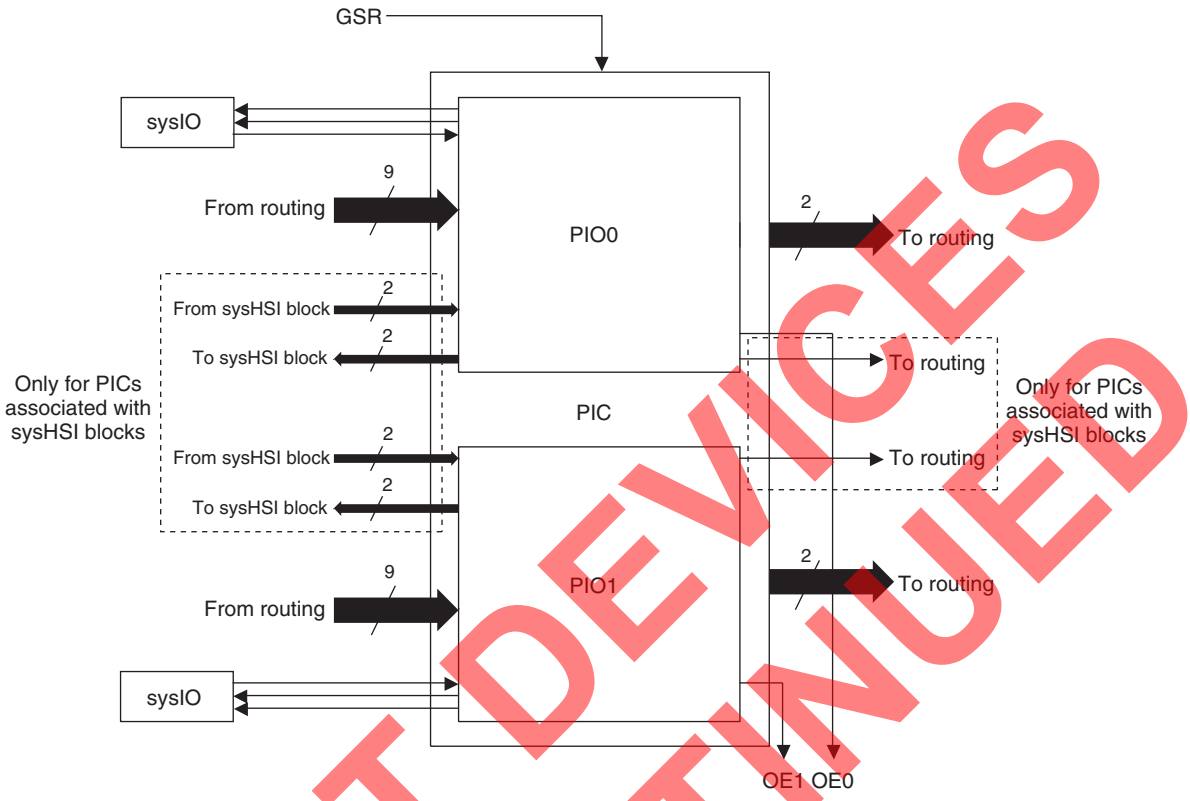



## Programmable Input/Output Cell

The Programmable Input/Output Cell (PIC) is an essential part of the symmetrical architecture of the ispXPGA Family. The PICs interface the PFUs and EBRs to the sysIO and sysHSI blocks of the device.

Each PIC contains two Programmable Input/Outputs (PIOs) with a total of 21 inputs and 10 outputs. There are 18 inputs from routing, two inputs from the sysIO buffers, and the Global Set/Reset signal. Four outputs of the PIC connect to routing and two outputs are available as Output Enables for the tri-statable Long Lines. The remaining four outputs feed the sysIO buffers directly (one output enable and one output to each). Each PIC associated with a sysHSI block has four additional inputs and six additional outputs to support the sysHSI blocks. The four additional inputs come from the sysHSI block associated with the PIC. The four of the six additional outputs come from the PIC outputs and feed the sysHSI block, while the remaining two outputs feed routing. Figure 10 shows the block diagram of the PIC with the sysHSI block inputs and outputs.

*Figure 10. ispXPGA PIC*



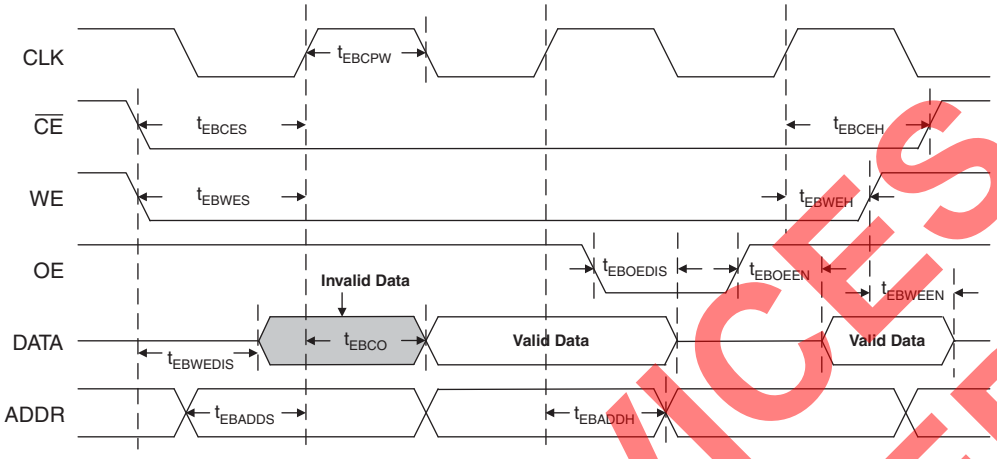

## Programmable Input/Output

The PIO is the building block of a PIC. The PIO has a total of 11 inputs and five outputs. Nine of the 11 inputs are generated from routing. The inputs from routing are the PIO Input (IN), Feed-Thru (FT), Clock (CLK), Input Clock Enable (ICE), Input Set/Reset (ISR), Output Clock Enable (OCEN), Output Set/Reset (OSR), PIO Output Enable (OEN), and PIO Input Enable (IEN). The remaining inputs are the sysIO input buffer signal and the Global Set/Reset signal. Three of the five outputs (OUT0, OUT1, and OE) feed routing. The last two outputs feed the sysIO buffer directly as the output and output enable of the sysIO output buffer.

PIOs associated with sysHSI blocks contain two additional inputs and outputs to support the sysHSI block. The two inputs come from the sysHSI block associated with the PIO, and the two outputs feed the sysHSI block. One of the inputs routes directly through the PIO to routing, while the other is multiplexed with the Feed-Thru, register bypass, and Q output of the register to form the OUT1 output of the PIO. The outputs to the sysHSI block are the same signals as the outputs which feed the sysIO buffers (sysIO Output and sysIO Output Enable).

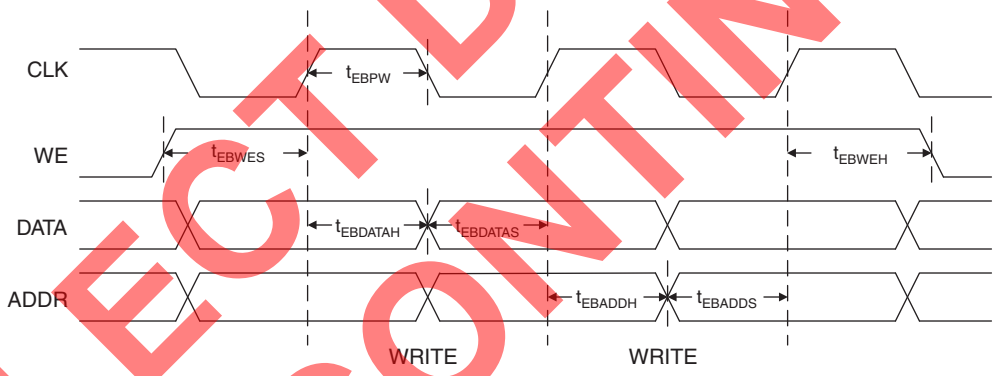
Each PIO has an input register, an output register, and an output enable register as shown in Figure 11. The input register path of the PIO has a 'delay' option, which slows the data-flow. A two-input OR function of the Global Set/Reset (GSR) and Set/Reset (ISR or OSR) signals creates the set/reset term for the respective registers. Each PIO has two pairs of set/reset and clock enable signals. One is exclusive to the input register, whereas the other is common for both the output and output enable registers. The clock (CLK) is common to all registers in a PIO, and the polarity of the clock is controllable. The input, output, and the output enable registers can be configured as a latch or D-type flip-flop. Each PIO is capable of generating an output enable signal, which in turn becomes a PIC output.

*Figure 13. EBR Synchronous Read Timing Diagram*




**Synchronous Write:** The WE signal controls the synchronous write operation. When the WE signal is high, the write operation begins. Once the address and data are present and the Output Enable (OE) is active, a rising clock edge (or falling edge depending on polarity) causes the data to be stored into the EBR. Figure 14 illustrates the synchronous write timing.

*Figure 14. EBR Synchronous Write Timing Diagram*




**Asynchronous Read:** The WE signal controls the asynchronous read operation. When the WE signal is low, the read operation begins. Shortly after the address is present, the stored data is available on the DATA port. Figure 15 illustrates the asynchronous read timing. For more information about the EBR, refer to TN1028 ispXPGA Memory Usage Guidelines.

*Figure 15. EBR Asynchronous Read Timing Diagram*

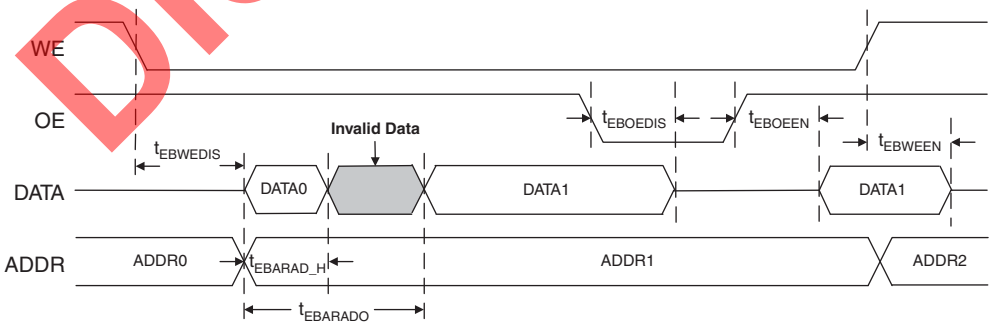
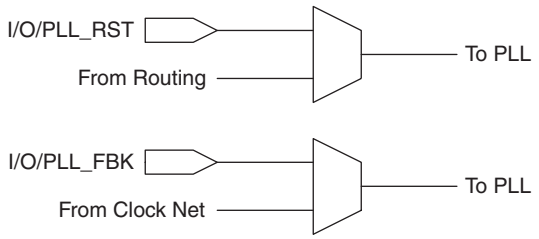


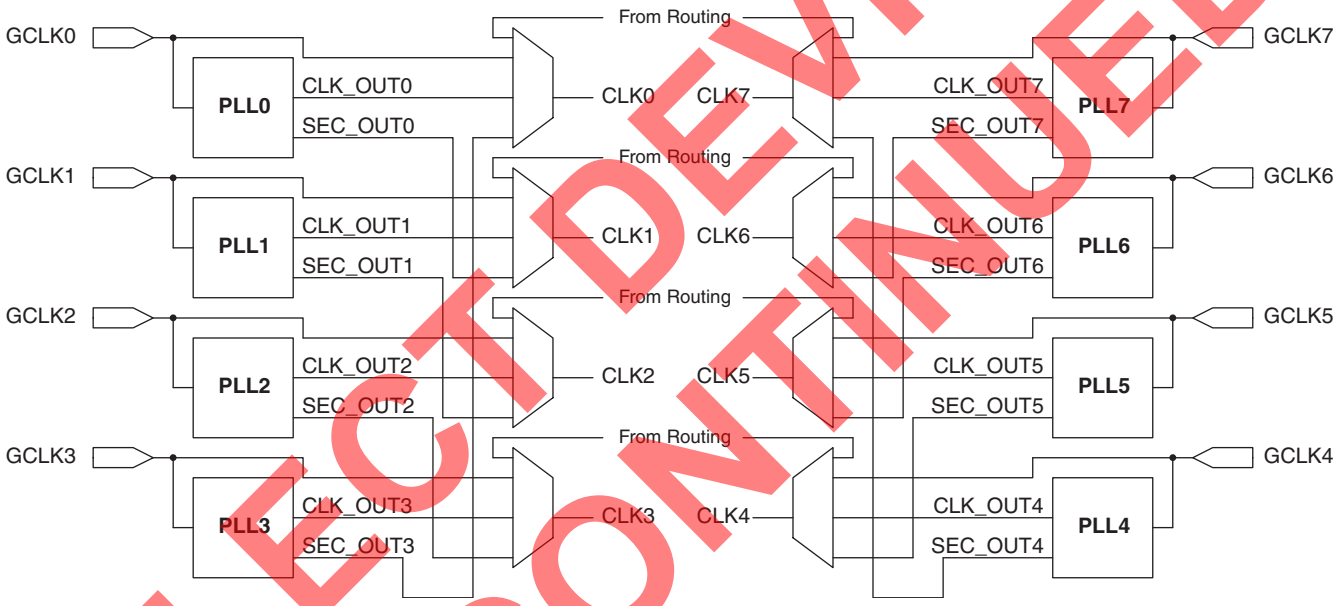
*Figure 17. ispXPGA PLL_RST and PLL_FBK Generation*




## Clock Routing

The Global Clock Lines (GCLK) have two sources, their dedicated pins and the sysCLOCK circuit. Figure 18 illustrates the generation of the Global Clock Lines.

*Figure 18. Global Clock Line Generation*




## sysIO Capability

All the ispXPGA devices have eight sysIO banks, where each bank is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage ($V_{CCO}$) and reference voltage ($V_{REF}$) resources allowing each bank complete independence from the others. Each I/O is individually configurable based on the bank's $V_{CCO}$ and $V_{REF}$ settings. In addition, each I/O has configurable drive strength, weak pull-up, weak pull-down, or a bus-keeper latch. Table 4 lists the number of I/Os supported per bank in each of the ispXPGA devices. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to $V_{CCO}$ of 3.0V to 3.6V for LVCMOS 3.3, LVTTL and PCI interfaces.

Table 5 lists the sysIO standards with the typical values for $V_{CCO}$, $V_{REF}$ and $V_{TT}$.

The TOE, JTAG TAP pins, PROGRAM, CFG0 and DONE pins of the ispXPGA device are the only pins that do not have the sysIO capabilities. The TOE and CFG0 pins operate off the $V_{CC}$ of the device, supporting only the LVCMOS standard corresponding to the device supply voltage. The TAP pins have a separate supply voltage ($V_{CCJ}$), which determines the LVCMOS standard corresponding to that supply voltage.

There are three classes of I/O interface standards that are implemented in the ispXPGA devices. The first is the unterminated, single-ended interface. It includes the 3.3V LVTTL standard along with the 1.8V, 2.5V, and 3.3V LVCMOS interface standards. Additionally, PCI and AGP-1X are subsets of this type of interface.

# DC Electrical Characteristics

**Over Recommended Operating Conditions**

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$[1] | Input or I/O Low Leakage | 0 ð $V_{IN}$ < ($V_{CCO}$ - 0.2V) | — | — | 10 | µA |
| | | ($V_{CCO}$ - 0.2V) ð $V_{IN}$ ð 3.6V | — | — | 300 | µA |
| $I_{IH}$[2] | Input High Leakage Current | 3.6V < $V_{IN}$ ð 5.5V and 3.0V ð $V_{CCO}$ ð 3.6V | — | — | 3 | mA |
| $I_{PU}$ | I/O Active Pull-up Current | 0 ð $V_{IN}$ ð 0.7 $V_{CCO}$ | -30 | — | -150 | µA |
| $I_{PD}$ | I/O Active Pull-down Current | $V_{IL}$ (MAX) ð $V_{IN}$ ð $V_{IH}$ (MAX) | 30 | — | 150 | µA |
| $I_{BHLS}$ | Bus Hold Low Sustaining Current | $V_{IN}$ = $V_{IL}$ (MAX) | 30 | — | — | µA |
| $I_{BHHS}$ | Bus Hold High Sustaining Current | $V_{IN}$ = 0.7 $V_{CCO}$ | -30 | — | — | µA |
| $I_{BHLO}$ | Bus Hold Low Overdrive Current | 0 ð $V_{IN}$ ð $V_{IH}$ (MAX) | — | — | 150 | µA |
| $I_{BHHO}$ | Bus Hold High Overdrive Current | 0 ð $V_{IN}$ ð $V_{IH}$ (MAX) | — | — | -150 | µA |
| $V_{BHT}$ | Bus Hold Trip Points | | $V_{CCO}$ * 0.35 | — | $V_{CCO}$ * 0.65 | V |
| $C_1$ | I/O Capacitance[3] | $V_{CCO}$ = 3.3V, 2.5V, 1.8V | — | 8 | — | pf |
| | | $V_{CC}$ = 1.8V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | | — | |
| $C_2$ | Clock Capacitance[3] | $V_{CCO}$ = 3.3V, 2.5V, 1.8V | — | 8 | — | pf |
| | | $V_{CC}$ = 1.8V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | | — | |
| $C_3$ | Global Input Capacitance[3] | $V_{CCO}$ = 3.3V, 2.5V, 1.8V | — | 6 | — | pf |
| | | $V_{CC}$ = 1.8V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | | — | |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. 5V tolerant inputs and I/Os should be placed in banks where 3.0V ð $V_{CCO}$ ð 3.6V. The JTAG and sysCONFIG ports are not included for the 5V tolerant interface.
3. $T_A$ = 25°C, f = 1.0MHz.

## sysIO Recommended Operating Conditions

| Standard | $V_{CCO}$ (V)[1] | | | $V_{REF}$ (V) | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| LVCMOS 3.3 | 3.0 | 3.3 | 3.6 | - | - | - |
| LVCMOS 2.5 | 2.3 | 2.5 | 2.7 | - | - | - |
| LVCMOS 1.8[2] | 1.65 | 1.8 | 1.95 | - | - | - |
| LVTTL | 3.0 | 3.3 | 3.6 | - | - | - |
| PCI 3.3 | 3.0 | 3.3 | 3.6 | - | - | - |
| AGP-1X | 3.15 | 3.3 | 3.45 | - | - | - |
| SSTL 2 | 2.3 | 2.5 | 2.7 | 1.15 | 1.25 | 1.35 |
| SSTL 3 | 3.0 | 3.3 | 3.6 | 1.3 | 1.5 | 1.7 |
| CTT 3.3 | 3.0 | 3.3 | 3.6 | 1.35 | 1.5 | 1.65 |
| CTT 2.5 | 2.3 | 2.5 | 2.7 | 1.35 | 1.5 | 1.65 |
| HSTL Class I | 1.4 | 1.5 | 1.6 | 0.68 | 0.75 | 0.9 |
| HSTL Class III | 1.4 | 1.5 | 1.6 | - | 0.9 | - |
| GTL+ | - | - | - | 0.882 | 1.0 | 1.122 |
| LVDS | 2.3 | 2.5 | 2.7 | - | - | - |
| LVPECL | 3.0 | 3.3 | 3.6 | - | - | - |
| BLVDS | 2.3 | 2.5 | 2.7 | - | - | - |

1. Inputs independent of $V_{CCO}$.
2. Design tool default setting.

## ispXPGA 500B/C & ispXPGA 500EB/EC PFU Timing Parameters (Cont.)

**Over Recommended Operating Conditions**

| Parameter | Description | -5[1] | | -4 | | -3 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| ***Reset/Set*** | | | | | | | | |
| $t_{LASSRO}$ | Asynchronous Set/Reset to Output | — | 1.09 | — | 1.17 | — | 1.35 | ns |
| $t_{LASSRPW}$ | Asynchronous Set/Reset Pulse Width | 4.19 | — | 4.50 | — | 5.18 | — | ns |
| $t_{LASSRR}$ | Asynchronous Set/Reset Recovery | — | 0.51 | — | 0.55 | — | 0.63 | ns |
| $t_{LSSR\_S}$ | Synchronous Set/Reset Setup Time | -0.03 | — | -0.03 | — | -0.03 | — | ns |
| $t_{LSSR\_H}$ | Synchronous Set/Reset Hold Time | 0.03 | — | 0.03 | — | 0.03 | — | ns |

1. Only available for ispXPGA 500B and ispXPGA 500EB (2.5V/3.3V) devices.
2. $t_{LCTHRUL}$ quoted bit by bit.

Timing v.0.3

## ispXPGA 500B/C & ispXPGA 500EB/EC PIC Timing Parameters

| Parameter | Description | -5[1] | | -4 | | -3 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Register/Latch Delays** | | | | | | | | |
| $t_{IO\_CO}$ | Register Clock to Output Delay | — | 1.00 | — | 1.07 | — | 1.23 | ns |
| $t_{IO\_S}$ | Register Setup Time (Data before Clock) | 0.05 | — | 0.05 | — | 0.06 | — | ns |
| $t_{IO\_H}$ | Register Hold Time (Data after Clock) | 0.06 | — | 0.06 | — | 0.07 | — | ns |
| $t_{IOCE\_S}$ | Register Clock Enable Setup Time | -0.03 | — | -0.03 | — | -0.03 | — | ns |
| $t_{IOCE\_H}$ | Register Clock Enable Hold Time | 0.13 | — | 0.13 | — | 0.15 | — | ns |
| $t_{IO\_GO}$ | Latch Gate to Output Delay | — | 0.78 | — | 0.84 | — | 0.97 | ns |
| $t_{IOL\_S}$ | Latch Setup Time | 0.05 | — | 0.05 | — | 0.06 | — | ns |
| $t_{IOL\_H}$ | Latch Hold Time | 0.06 | — | 0.06 | — | 0.07 | — | ns |
| $t_{IOLPD}$ | Latch Propagation Delay (Transparent Mode) | — | 0.09 | — | 0.10 | — | 0.12 | ns |
| $t_{IOASRO}$ | Asynchronous Set/Reset to Output | — | 1.11 | — | 1.19 | — | 1.37 | ns |
| $t_{IOASRPW}$ | Asynchronous Set/Reset Pulse Width | 4.19 | — | 4.50 | — | 5.18 | — | ns |
| $t_{IOASRR}$ | Asynchronous Set/Reset Recovery Time | — | 0.23 | — | 0.25 | — | 0.29 | ns |
| **Input/Output Delays** | | | | | | | | |
| $t_{IOBUF}$ | Output Buffer Delay | — | 0.98 | — | 1.05 | — | 1.21 | ns |
| $t_{IOIN}$ | Input Buffer Delay | — | 0.65 | — | 0.70 | — | 0.81 | ns |
| $t_{IOEN}$ | Output Enable Delay | — | 0.52 | — | 0.56 | — | 0.64 | ns |
| $t_{IODIS}$ | Output Disable Delay | — | -0.12 | — | -0.11 | — | -0.09 | ns |
| $t_{IOFT}$ | Feed-thru Delay | — | 0.19 | — | 0.20 | — | 0.23 | ns |

1. Only available for ispXPGA 500B and ispXPGA 500EB (2.5V/3.3V) devices.

Timing v.0.3

## ispXPGA 1200B/C & ispXPGA 1200EB/EC PFU Timing Parameters (Cont.)

**Over Recommended Operating Conditions**

| Parameter | Description | -5[1] | | -4 | | -3 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Reset/Set** | | | | | | | | |
| $t_{LASSRO}$ | Asynchronous Set/Reset to Output | — | 1.09 | — | 1.17 | — | 1.35 | ns |
| $t_{LASSRPW}$ | Asynchronous Set/Reset Pulse Width | 4.19 | — | 4.50 | — | 5.18 | — | ns |
| $t_{LASSRR}$ | Asynchronous Set/Reset Recovery | — | 0.51 | — | 0.55 | — | 0.63 | ns |
| $t_{LSSR\_S}$ | Synchronous Set/Reset Setup Time | -0.03 | — | -0.03 | — | -0.03 | — | ns |
| $t_{LSSR\_H}$ | Synchronous Set/Reset Hold Time | 0.03 | — | 0.03 | — | 0.03 | — | ns |

1. Only available for ispXPGA 1200B and ispXPGA 1200EB (2.5V/3.3V) devices.
2. $t_{LCTHRUL}$ quoted bit by bit.

Timing v.2.1

## ispXPGA 1200B/C & ispXPGA 1200EB/EC PIC Timing Parameters

| Parameter | Description | -5[1] | | -4 | | -3 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Register/Latch Delays** | | | | | | | | |
| $t_{IO\_CO}$ | Register Clock to Output Delay | — | 1.01 | — | 1.09 | — | 1.25 | ns |
| $t_{IO\_S}$ | Register Setup Time (Data before Clock) | 0.05 | — | 0.05 | — | 0.06 | — | ns |
| $t_{IO\_H}$ | Register Hold Time (Data after Clock) | 0.06 | — | 0.06 | — | 0.07 | — | ns |
| $t_{IOCE\_S}$ | Register Clock Enable Setup Time | -0.03 | — | -0.03 | — | -0.03 | — | ns |
| $t_{IOCE\_H}$ | Register Clock Enable Hold Time | 0.13 | | 0.13 | — | 0.15 | — | ns |
| $t_{IO\_GO}$ | Latch Gate to Output Delay | — | 0.85 | — | 0.91 | — | 1.05 | ns |
| $t_{IOL\_S}$ | Latch Setup Time | 0.05 | — | 0.05 | — | 0.06 | — | ns |
| $t_{IOL\_H}$ | Latch Hold Time | 0.06 | — | 0.06 | — | 0.07 | — | ns |
| $t_{IOLPD}$ | Latch Propagation Delay (Transparent Mode) | — | 0.09 | — | 0.10 | — | 0.12 | ns |
| $t_{IOASRO}$ | Asynchronous Set/Reset to Output | — | 1.17 | — | 1.26 | — | 1.45 | ns |
| $t_{IOASRPW}$ | Asynchronous Set/Reset Pulse Width | 4.19 | — | 4.50 | — | 5.18 | — | ns |
| $t_{IOASRR}$ | Asynchronous Set/Reset Recovery Time | — | 0.23 | — | 0.25 | — | 0.29 | ns |
| **Input/Output Delays** | | | | | | | | |
| $t_{IOBUF}$ | Output Buffer Delay | — | 0.99 | — | 1.06 | — | 1.22 | ns |
| $t_{IOIN}$ | Input Buffer Delay | — | 0.71 | — | 0.76 | — | 0.87 | ns |
| $t_{IOEN}$ | Output Enable Delay | — | 0.52 | — | 0.56 | — | 0.64 | ns |
| $t_{IODIS}$ | Output Disable Delay | — | -0.11 | — | -0.10 | — | -0.09 | ns |
| $t_{IOFT}$ | Feed-thru Delay | — | 0.19 | — | 0.20 | — | 0.23 | ns |

1. Only available for ispXPGA 1200B and ispXPGA 1200EB (2.5V/3.3V) devices.

Timing v.2.1

## sysHSI Block AC Specifications

### Operating Frequency Ranges

| Symbol | Description | Mode | Test Condition | Device | -5[1] | | -4 | | -3 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $f_{CLK}$ | Reference Clock Frequency | SS:CAL | | LFX125B/C | 50 | 200 | 50 | 200 | 50 | 200 | MHz |
| | | | | LFX200B/C | 50 | 188 | 50 | 188 | 50 | 188 | |
| | | | | LFX500B/C | 50 | 188 | 50 | 188 | 50 | 188 | |
| | | | | LFX1200B/C | 50 | 175 | 50 | 175 | 50 | 175 | |
| | | 10B12B | | LFX125B/C | 33 | 67 | 33 | 67 | 33 | 67 | MHz |
| | | | | LFX200B/C | 33 | 63 | 33 | 63 | 33 | 63 | |
| | | | | LFX500B/C | 33 | 63 | 33 | 63 | 33 | 63 | |
| | | | | LFX1200B/C | 33 | 58 | 33 | 58 | 33 | 58 | |
| | | 8B10B | | LFX125B/C | 40 | 80 | 40 | 80 | 40 | 80 | MHz |
| | | | | LFX200B/C | 40 | 75 | 40 | 75 | 40 | 75 | |
| | | | | LFX500B/C | 40 | 75 | 40 | 75 | 40 | 75 | |
| | | | | LFX1200B/C | 40 | 70 | 40 | 70 | 40 | 70 | |
| $f_{SIN}$[2] | Serial Input | SS:CAL | with eoSIN | LFX125B/C | 400 | 800 | 400 | 800 | 400 | 800 | Mbps |
| | | | | LFX200B/C | 400 | 750 | 400 | 750 | 400 | 750 | |
| | | | | LFX500B/C | 400 | 750 | 400 | 750 | 400 | 750 | |
| | | | | LFX1200B/C | 400 | 700 | 400 | 700 | 400 | 700 | |
| | | 10B12B | with eoSIN | LFX125B/C | 400 | 800 | 400 | 800 | 400 | 800 | Mbps |
| | | | | LFX200B/C | 400 | 750 | 400 | 750 | 400 | 750 | |
| | | | | LFX500B/C | 400 | 750 | 400 | 750 | 400 | 750 | |
| | | | | LFX1200B/C | 400 | 700 | 400 | 700 | 400 | 700 | |
| | | 8B10B | with eoSIN | LFX125B/C | 400 | 800 | 400 | 800 | 400 | 800 | Mbps |
| | | | | LFX200B/C | 400 | 750 | 400 | 750 | 400 | 750 | |
| | | | | LFX500B/C | 400 | 750 | 400 | 750 | 400 | 750 | |
| | | | | LFX1200B/C | 400 | 700 | 400 | 700 | 400 | 700 | |
| $f_{OUT}$[2] | Serial Out | LVDS | CL = 5 pF, RL = 100¾ $f_{CLK}$ with no jitter | LFX125B/C | 400 | 800 | 400 | 800 | 400 | 800 | Mbps |
| | | | | LFX200B/C | 400 | 750 | 400 | 750 | 400 | 750 | |
| | | | | LFX500B/C | 400 | 750 | 400 | 750 | 400 | 750 | |
| | | | | LFX1200B/C | 400 | 700 | 400 | 700 | 400 | 700 | |

1. Only available for ispXPGA 125B, 200B, 500B and 1200B (2.5V/3.3V) devices.
2. $f_{SIN}$ and $f_{SOUT}$ speeds are supported at $V_{CC}$ and $V_{CCP}$ at 1.7V to 1.9V for ispXPGA 1.8V devices.

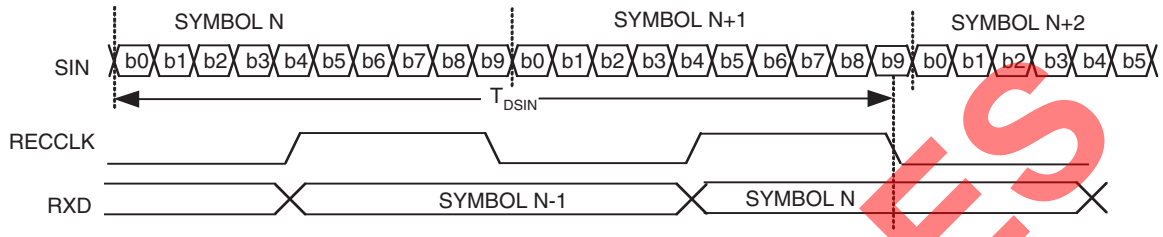
### LOCKIN Time

| Symbol | Description | Mode | Condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{SCLOCK}$ | CSPLL Lock Time | All | After input is stabilized | | 25 | µS |
| $t_{CDRLOCK}$ | CDRPLL Lock-in Time | SS | With SS mode sync pattern | | 1024 | $t_{RCP}$[1] |
| | | 10B12B | With 10B12B sync pattern | | 1024 | $t_{RCP}$ |
| | | 8B10B | With 8B10B idle pattern | | 960 | $t_{RCP}$ |
| $t_{SYNC}$ | SyncPat Length | SS | | 1200 | | $t_{RCP}$ |
| $t_{CAL}$ | CAL Duration | SS | | 1100 | | $t_{RCP}$ |
| $t_{SUSYNC}$ | SyncPat Set-up Time to CAL | SS | | 50 | | $t_{RCP}$ |
| $t_{HDSYNC}$ | SyncPat Hold Time from CAL | SS | | 50 | | $t_{RCP}$ |

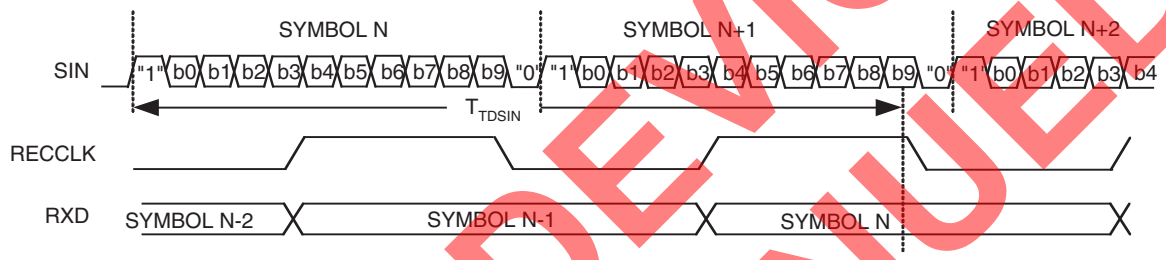
1. REFCLK clock period.

## Deserializer Timing

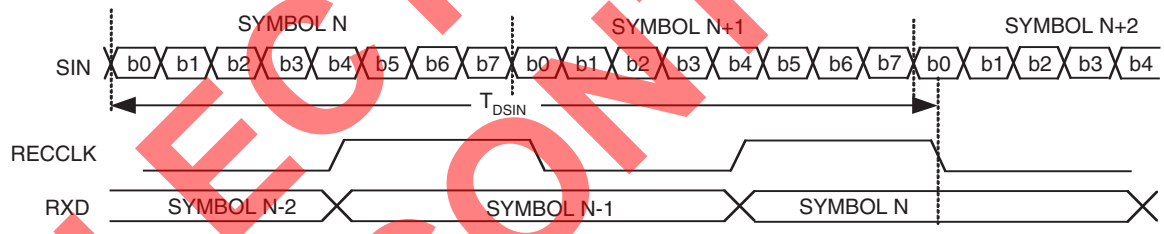
**8B/10B DESERIALIZER DELAY TIMING**



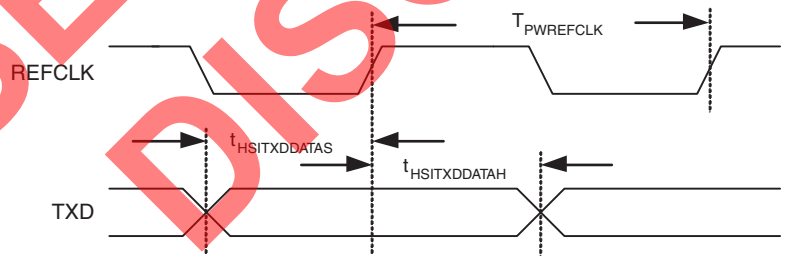

**10B/12B DESERIALIZER DELAY TIMING**




**CDRX_SS DESERIALIZER DELAY TIMING**




**INTERNAL TIMING FOR sysHSI BLOCK**



## ispXP sysCONFIG Port Timing Specifications

| Symbol | Timing Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **sysCONFIG Write Cycle Timing** | | | | | |
| $t_{SUCS}$ | Input setup time of CS to CCLK rise | 10 | — | — | ns |
| $t_{HCS}$ | Hold time of CS to CCLK Rise | 0 | — | — | ns |
| $t_{SUWD}$ | Input setup time of write data to CCLK rise | 12 | — | — | ns |
| $t_{HWD}$ | Hold time of write data to CCLK rise | 0 | — | — | ns |
| $t_{PRGM}$ | Low time to reset device SRAM | 5 | — | 50 | ns |
| $t_{WINIT}$ | INIT pulse width | — | — | 5 | ms |
| $t_{IODISS}$ | User I/O disable | — | — | 30 | ns |
| $t_{IOENSS}$ | User I/O enable | — | — | 30 | ns |
| $t_{WH}$ | Write clock High pulse width | 12 | — | — | ns |
| $t_{WL}$ | Write clock Low pulse width | 12 | — | — | ns |
| $f_{MAXW}$ | Write $f_{MAX}$ | — | — | 33 | MHz |
| **sysCONFIG Read Cycle Timing** | | | | | |
| $t_{HREAD}$ | Hold time of READ to CCLK rise | 0 | — | — | ns |
| $t_{SUREAD}$ | Input setup time of READ High to CCLK rise | 30 | — | — | ns |
| $t_{RH}$ | READ clock high pulse width | 12 | — | — | ns |
| $t_{RL}$ | READ clock low pulse width | 15 | — | — | ns |
| $f_{MAXR}$ | Read $f_{MAX}$ | — | — | 33 | MHz |
| $t_{CORD}$ | Clock to out for read data | — | — | 25 | ns |

## Boundary Scan Timing

| Parameter | Description | Min. | Max. | Units |
|---|---|---|---|---|
| $t_{BTCP}$ | TCK [BSCAN] Clock Pulse Width | 40 | — | ns |
| $t_{BTCPH}$ | TCK [BSCAN] Clock Pulse Width High | 20 | — | ns |
| $t_{BTCPL}$ | TCK [BSCAN] Clock Pulse Width Low | 20 | — | ns |
| $t_{BTS}$ | TCK [BSCAN] Setup Time | 8 | — | ns |
| $t_{BTH}$ | TCK [BSCAN] Hold Time | 10 | — | ns |
| $t_{BTRF}$ | TCK [BSCAN] Rise/Fall Time | 50 | — | mV/ns |
| $t_{BTCO}$ | TAP Controller Falling Edge of Clock to Valid Output | — | 18 | ns |
| $t_{BTCODIS}$ | TAP Controller Falling Edge of Clock to Valid Disable | — | 18 | ns |
| $t_{BTCOEN}$ | TAP Controller Falling Edge of Clock to Valid Enable | — | 18 | ns |
| $t_{BTCRS}$ | BSCAN Test Capture Register Setup Time | 8 | — | ns |
| $t_{BTCRH}$ | BSCAN Test Capture Register Hold Time | 25 | — | ns |
| $t_{BUTCO}$ | BSCAN Test Update Register, Falling Edge of Clock to Valid Output | — | 45 | ns |
| $t_{BTUODIS}$ | BSCAN Test Update Register, Falling Edge of Clock to Valid Disable | — | 20 | ns |
| $t_{BTUPOEN}$ | BSCAN Test Update Register, Falling Edge of Clock to Valid Enable | — | 20 | ns |

## Signal Descriptions[1]

| Signal Name | Signal Type | Description |
|---|---|---|
| **General Purpose** | | |
| BK*y*_IO*x*[1,2] | Input/Output | General purpose I/O number x in I/O Bank y |
| GCLK*n*/I*n*[7] | Input | Global clock/input[8] |
| GSR | Input | Global Set/Reset |
| NC | — | No Connect |
| GND | GND | Ground |
| $V_{CC}$ | VCC | Core logic power supply |
| $V_{CCJ}$ | VCC | IEEE 1149.1 TAP power supply |
| $V_{CCOy}$[2] | VCC | I/O Bank y power supply |
| $V_{REFy}$[2] | Input | I/O Bank y reference voltage |
| $D_{XN}$, $D_{XP}$ | Output | Temperature Sensing Diodes, provide a differential voltage, which corresponds to the temperature of the device. |
| **Test and Program/Configuration** | | |
| TMS | Input | Test Mode Select |
| TCK | Input | Test Clock |
| TDI | Input | Test Data In |
| TDO | Output | Test Data Out |
| TOE | Input | Test Output Enable tri-states all I/O pins when driven low |
| CFG0 | Input | Selects the SRAM memory configuration type (Peripheral or $E^2$CMOS Refresh) |
| PROGRAMb | Input | Initiates download from $E^2$CMOS or the peripheral port to SRAM memory (active low) |
| DONE | Bi-directional | Indicates when configuration is complete |
| INITb | Bi-directional | Indicates the device is ready for programming (active low) |
| READ | Input | Selects the READ operation when in sysCONFIG mode |
| CCLK | Input | sysCONFIG Configuration Clock |
| CSb | Input | sysCONFIG Chip Select (active low) |
| DATA[0:7] | Bi-directional | sysCONFIG Peripheral Port Data I/O |
| **sysCLOCK PLL**[3] | | |
| PLL_FBK*z* | Input | Optional external feedback |
| PLL_RST*z* | Input | Optional external M divider reset |
| CLK_OUT*z* | Internal Signal | Clock output (routable to any I/O) |
| PLL_LOCK*z* | Internal Signal | Lock output (routable to any I/O) |
| $GND_{P0}$ | GND | Left side PLL Ground |
| $GND_{P1}$ | GND | Right side PLL Ground |
| $V_{CCP0}$ | VCC | Left side PLL power supply |
| $V_{CCP1}$ | VCC | Right side PLL power supply |
| **sysHSI Block**[4, 5] | | |
| HSI*m*A_SINP, HSI*m*B_SINP | Input | P-side of differential serial data input |
| HSI*m*A_SINN, HSI*m*B_SINN | Input | N-side of differential serial data input |
| HSI*m*A_SOUTP, HSI*m*B_SOUTP | Output | P-side of differential serial data output |
| HSI*m*A_SOUTN, HSI*m*B_SOUTN | Output | N-side of differential serial data output |
| HSI*m*A_SYDT, HSI*m*B_SYDT | Internal Signal | Symbol alignment detect |
| HSI*m*A_RECCLK, HSI*m*B_RECCLK | Internal Signal | Recovered clock |

## ispXPGA Logic Signal Connections: 256-Ball fpBGA

| 256-fpBGA Ball | LFX200 | | | LFX125 | | |
|---|---|---|---|---|---|---|
| | Signal Name | Second Function | LVDS Pair/ sysHSI Reserved[2] | Signal Name | Second Function | LVDS Pair/ sysHSI Reserved[2] |
| C2 | BK0_IO2 | HSI0A_SOUTP | 1P/HSI0 | BK0_IO0 | HSI0A_SOUTP | 0P |
| - | GND (Bank 0) | - | - | - | - | - |
| D2 | BK0_IO3 | HSI0A_SOUTN | 1N/HSI0 | BK0_IO1 | HSI0A_SOUTN | 0N |
| B1 | BK0_IO6 | HSI0A_SINP | 3P/HSI0 | BK0_IO4 | HSI0A_SINP | 2P/HSI0 |
| - | - | - | - | GND (Bank 0) | - | - |
| C1 | BK0_IO7 | HSI0A_SINN | 3N/HSI0 | BK0_IO5 | HSI0A_SINN | 2N/HSI0 |
| D3 | BK0_IO8 | - | 4P/HSI0 | BK0_IO6 | - | 3P/HSI0 |
| E3 | BK0_IO9 | VREF0 | 4N/HSI0 | BK0_IO7 | VREF0 | 3N/HSI0 |
| D1 | BK0_IO10 | HSI0B_SOUTP | 5P/HSI0 | BK0_IO8 | HSI0B_SOUTP | 4P/HSI0 |
| - | GND (Bank 0) | - | - | - | - | - |
| E1 | BK0_IO11 | HSI0B_SOUTN | 5N/HSI0 | BK0_IO9 | HSI0B_SOUTN | 4N/HSI0 |
| E2 | BK0_IO12 | - | 6P/HSI0 | BK0_IO10 | - | 5P/HSI0 |
| F2 | BK0_IO13 | - | 6N/HSI0 | BK0_IO11 | - | 5N/HSI0 |
| F1 | BK0_IO14 | HSI0B_SINP | 7P/HSI0 | BK0_IO12 | HSI0B_SINP | 6P/HSI0 |
| - | - | - | - | GND (Bank 0) | - | - |
| G1 | BK0_IO15 | HSI0B_SINN | 7N/HSI0 | BK0_IO13 | HSI0B_SINN | 6N/HSI0 |
| F3 | BK0_IO18 | PLL_FBK0 | 9P | BK0_IO14 | PLL_FBK0 | 7P/HSI0 |
| - | GND (Bank 0) | - | - | - | - | - |
| G2 | BK0_IO19 | PLL_RST1 | 9N | BK0_IO15 | PLL_RST1 | 7N/HSI0 |
| E4 | BK0_IO20 | - | 10P | BK0_IO16 | - | 8P/HSI0 |
| F4 | BK0_IO21 | PLL_FBK1 | 10N | BK0_IO17 | PLL_FBK1 | 8N/HSI0 |
| H1 | BK0_IO22 | PLL_RST0 | 11P | BK0_IO18 | PLL_RST0 | 9P |
| - | - | - | - | GND (Bank 0) | - | - |
| J1 | BK0_IO23 | - | 11N | BK0_IO19 | - | 9N |
| H2 | BK0_IO24 | CLK_OUT0 | 12P | BK0_IO20 | CLK_OUT0 | 10P |
| G3 | BK0_IO25 | CLK_OUT1 | 12N | BK0_IO21 | CLK_OUT1 | 10N |
| - | GND (Bank 0) | - | - | - | - | - |
| G4 | GCLK0 | - | LVDS Pair0P | GCLK0 | - | LVDS Pair0P |
| H4 | GCLK1 | - | LVDS Pair0N | GCLK1 | - | LVDS Pair0N |
| H3 | VCCP0 | - | - | VCCP0 | - | - |
| J4 | GNDP0 | - | - | GNDP0 | - | - |
| J2 | GCLK2 | - | LVDS Pair1P | GCLK2 | - | LVDS Pair1P |
| J3 | GCLK3 | - | LVDS Pair1N | GCLK3 | - | LVDS Pair1N |
| - | GND (Bank 1) | - | - | - | - | - |
| H5 | BK1_IO0 | CLK_OUT2 | 13P | BK1_IO0 | CLK_OUT2 | 11P |
| J5 | BK1_IO1 | CLK_OUT3 | 13N | BK1_IO1 | CLK_OUT3 | 11N |
| K1 | BK1_IO2 | SS_CLKOUT0P | 14P | BK1_IO2 | SS_CLKOUT0P | 12P |
| - | - | - | - | GND (Bank 1) | - | - |
| L1 | BK1_IO3 | SS_CLKOUT0N | 14N | BK1_IO3 | SS_CLKOUT0N | 12N |
| K4 | BK1_IO4 | PLL_FBK2 | 15P | BK1_IO4 | PLL_FBK2 | 13P |
| L4 | BK1_IO5 | PLL_FBK3 | 15N | BK1_IO5 | PLL_FBK3 | 13N |
| K3 | BK1_IO6 | SS_CLKIN0P | 16P | BK1_IO6 | SS_CLKIN0P | 14P |

## ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

| 256-fpBGA Ball | LFX200 | | | LFX125 | | |
|---|---|---|---|---|---|---|
| | Signal Name | Second Function | LVDS Pair/ sysHSI Reserved[2] | Signal Name | Second Function | LVDS Pair/ sysHSI Reserved[2] |
| C8 | BK7_IO1 | - | 91N | BK7_IO1 | - | 77N |
| B8 | BK7_IO2 | - | 92P | BK7_IO2 | - | 78P |
| B7 | BK7_IO3 | - | 92N | BK7_IO3 | - | 78N |
| A9 | BK7_IO6 | - | 94P | BK7_IO4 | - | 79P |
| - | GND (Bank 7) | - | - | - | - | - |
| A8 | BK7_IO7 | - | 94N | BK7_IO5 | - | 79N |
| C7 | BK7_IO10 | - | 96P | BK7_IO6 | - | 80P |
| D7 | BK7_IO11 | - | 96N | BK7_IO7 | - | 80N |
| D6 | BK7_IO12 | - | 97P | BK7_IO8 | - | 81P |
| - | - | - | - | GND (Bank 7) | - | - |
| C6 | BK7_IO13 | - | 97N | BK7_IO9 | - | 81N |
| B6 | BK7_IO14 | - | 98P | BK7_IO10 | - | 82P |
| - | GND (Bank 7) | - | - | - | - | - |
| B5 | BK7_IO15 | - | 98N | BK7_IO11 | - | 82N |
| A7 | BK7_IO16 | VREF7 | 99P | BK7_IO12 | VREF7 | 83P |
| A6 | BK7_IO17 | - | 99N | BK7_IO13 | - | 83N |
| D5 | BK7_IO18 | - | 100P | BK7_IO14 | - | 84P |
| C5 | BK7_IO19 | - | 100N | BK7_IO15 | - | 84N |
| A5 | BK7_IO20 | - | 101P | BK7_IO16 | - | 85P |
| - | - | - | - | GND (Bank 7) | - | - |
| A4 | BK7_IO21 | - | 101N | BK7_IO17 | - | 85N |
| B4 | BK7_IO22 | - | 102P | BK7_IO18 | - | 86P |
| - | GND (Bank 7) | - | - | - | - | - |
| B3 | BK7_IO23 | - | 102N | BK7_IO19 | - | 86N |
| A3 | TDO | - | - | TDO | - | - |
| A2 | VCCJ | - | - | VCCJ | - | - |
| C4 | TDI | - | - | TDI | - | - |

1. Not available for differential pairs.
2. If a sysHSI Block is used, the indicated sysHSI reserved pins are unavailable for general purpose I/O use.

# ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

| 516-Ball BGA Ball | LFX500 | | | LFX200 | | | LFX125 | | |
|---|---|---|---|---|---|---|---|---|---|
| | Signal Name | Second Function | LVDS Pair/ sysHSI Reserved[1] | Signal Name | Second Function | LVDS Pair/ sysHSI Reserved[1] | Signal Name | Second Function | LVDS Pair/ sysHSI Reserved[1] |
| D21 | BK6_IO20 | - | 136P | BK6_IO8 | - | 82P | BK6_IO8 | - | 70P |
| C21 | BK6_IO21 | VREF6 | 136N | BK6_IO9 | VREF6 | 82N | BK6_IO9 | VREF6 | 70N |
| B21 | BK6_IO22 | DATA5 | 137P | BK6_IO10 | DATA5 | 83P | BK6_IO10 | DATA5 | 71P |
| - | - | - | - | GND (Bank 6) | - | - | - | - | - |
| A21 | BK6_IO23 | DATA4 | 137N | BK6_IO11 | DATA4 | 83N | BK6_IO11 | DATA4 | 71N |
| D20 | BK6_IO24 | - | 138P | BK6_IO12 | - | 84P | BK6_IO12 | - | 72P |
| - | - | - | - | - | - | - | GND (Bank 6) | - | - |
| C20 | BK6_IO25 | - | 138N | BK6_IO13 | - | 84N | BK6_IO13 | - | 72N |
| B20 | BK6_IO26 | DATA3 | 139P | BK6_IO14 | DATA3 | 85P | BK6_IO14 | DATA3 | 73P |
| - | GND (Bank 6) | - | - | - | - | - | - | - | - |
| A20 | BK6_IO27 | DATA2 | 139N | BK6_IO15 | DATA2 | 85N | BK6_IO15 | DATA2 | 73N |
| C19 | BK6_IO28 | - | 140P | BK6_IO16 | | 86P | BK6_IO16 | - | 74P |
| B19 | BK6_IO29 | - | 140N | BK6_IO17 | | 86N | BK6_IO17 | - | 74N |
| A19 | BK6_IO30 | DATA1 | 141P | BK6_IO18 | DATA1 | 87P | BK6_IO18 | DATA1 | 75P |
| - | - | - | - | GND (Bank 6) | - | - | GND (Bank 6) | - | - |
| A18 | BK6_IO31 | DATA0 | 141N | BK6_IO19 | DATA0 | 87N | BK6_IO19 | DATA0 | 75N |
| D18 | BK6_IO32 | - | 142P | BK6_IO20 | | 88P | BK6_IO20 | - | 76P |
| C18 | BK6_IO33 | - | 142N | BK6_IO21 | | 88N | BK6_IO21 | - | 76N |
| B18 | BK6_IO34 | - | 143P | BK6_IO22 | | 89P | NC | - | - |
| - | GND (Bank 6) | - | - | - | - | - | - | - | - |
| C17 | BK6_IO35 | - | 143N | BK6_IO23 | | 89N | NC | - | - |
| B17 | BK6_IO36 | - | 144P | NC | - | - | NC | - | - |
| A17 | BK6_IO37 | - | 144N | NC | - | - | NC | - | - |
| D16 | BK6_IO38 | - | 145P | NC | - | - | NC | - | - |
| C16 | BK6_IO39 | - | 145N | NC | - | - | NC | - | - |
| B16 | BK6_IO40 | - | 146P | BK6_IO24 | - | 90P | NC | - | - |
| A16 | BK6_IO41 | - | 146N | BK6_IO25 | - | 90N | NC | - | - |
| - | GND (Bank 6) | - | - | GND (Bank 6) | - | - | - | - | - |
| - | GND (Bank 7) | - | - | GND (Bank 7) | - | - | - | - | - |
| A15 | BK7_IO0 | - | 147P | BK7_IO0 | - | 91P | BK7_IO0 | - | 77P |
| B15 | BK7_IO1 | - | 147N | BK7_IO1 | - | 91N | BK7_IO1 | - | 77N |
| C15 | BK7_IO2 | - | 148P | BK7_IO2 | - | 92P | BK7_IO2 | - | 78P |
| - | - | - | - | - | - | - | GND (Bank 7) | - | - |
| D15 | BK7_IO3 | - | 148N | BK7_IO3 | - | 92N | BK7_IO3 | - | 78N |
| A14 | BK7_IO4 | - | 149P | BK7_IO4 | - | 93P | BK7_IO4 | - | 79P |
| B14 | BK7_IO5 | - | 149N | BK7_IO5 | - | 93N | BK7_IO5 | - | 79N |
| C14 | BK7_IO6 | - | 150P | BK7_IO6 | - | 94P | NC | - | - |
| - | GND (Bank 7) | - | - | GND (Bank 7) | - | - | - | - | - |
| A13 | BK7_IO7 | - | 150N | BK7_IO7 | - | 94N | NC | - | - |
| B13 | BK7_IO8 | - | 151P | BK7_IO8 | - | 95P | NC | - | - |
| C13 | BK7_IO9 | - | 151N | BK7_IO9 | - | 95N | NC | - | - |
| D13 | BK7_IO10 | - | 152P | BK7_IO10 | - | 96P | BK7_IO6 | - | 80P |
| B12 | BK7_IO11 | - | 152N | BK7_IO11 | - | 96N | BK7_IO7 | - | 80N |
| C12 | BK7_IO12 | - | 153P | BK7_IO12 | - | 97P | BK7_IO8 | - | 81P |
| - | - | - | - | - | - | - | GND (Bank 7) | - | - |
| A12 | BK7_IO13 | - | 153N | BK7_IO13 | | 97N | BK7_IO9 | - | 81N |
| A11 | BK7_IO14 | - | 154P | BK7_IO14 | - | 98P | BK7_IO10 | - | 82P |
| - | GND (Bank 7) | - | - | GND (Bank 7) | - | - | - | - | - |
| B11 | BK7_IO15 | - | 154N | BK7_IO15 | - | 98N | BK7_IO11 | - | 82N |
| C11 | BK7_IO16 | - | 155P | NC | - | - | NC | - | - |
| D11 | BK7_IO17 | - | 155N | NC | - | - | NC | - | - |

## ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

| LFX1200 | | | |
|---|---|---|---|
| **680-Ball fpBGA** | **Signal Name** | **Second Function** | **LVDS Pair/sysHSI Reserved[1]** |
| L3 | BK7_IO35 | - | 234N |
| J1 | BK7_IO36 | - | 235P |
| J2 | BK7_IO37 | - | 235N |
| M4 | BK7_IO38 | - | 236P |
| H1 | BK7_IO39 | - | 236N |
| J3 | BK7_IO40 | - | 237P |
| L4 | BK7_IO41 | - | 237N |
| M5 | BK7_IO42 | - | 238P |
| - | GND (Bank 7) | - | - |
| H2 | BK7_IO43 | - | 238N |
| K4 | BK7_IO44 | - | 239P |
| G1 | BK7_IO45 | - | 239N |
| H3 | BK7_IO46 | - | 240P |
| J4 | BK7_IO47 | VREF7 | 240N |
| K5 | BK7_IO48 | - | 241P |
| G3 | BK7_IO49 | - | 241N |
| H4 | BK7_IO50 | - | 242P |
| - | GND (Bank 7) | - | - |
| F2 | BK7_IO51 | - | 242N |
| G2 | BK7_IO52 | - | 243P |
| H5 | BK7_IO53 | - | 243N |
| F3 | BK7_IO54 | - | 244P |
| F1 | BK7_IO55 | - | 244N |
| G4 | BK7_IO56 | - | 245P |
| E1 | BK7_IO57 | - | 245N |
| F4 | BK7_IO58 | - | 246P |
| - | GND (Bank 7) | - | - |
| E2 | BK7_IO59 | - | 246N |
| F5 | BK7_IO60 | - | 247P |
| E3 | BK7_IO61 | - | 247N |
| D2 | TDO | - | - |
| D3 | VCCJ | - | - |
| D1 | TDI | - | - |

1. If a sysHSI Block is used, the indicated sysHSI reserved pins are unavailable for general purpose I/O use.

## ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

| 900 fpBGA Ball | LFX1200 | | | LFX500 | | |
|---|---|---|---|---|---|---|
| | Signal Name | Second Function | LVDS Pair/ sysHSI Reserved[1] | Signal Name | Second Function | LVDS Pair/ sysHSI Reserved[1] |
| K30 | BK5_IO22 | HSI7B_SOUTP | 166P/HSI8 | BK5_IO22 | HSI4B_SOUTP | 116P/HSI4 |
| - | - | - | - | GND (Bank 5) | - | - |
| K29 | BK5_IO23 | HSI7B_SOUTN | 166N/HSI8 | BK5_IO23 | HSI4B_SOUTN | 116N/HSI4 |
| L28 | BK5_IO24 | - | 167P/HSI8 | BK5_IO24 | - | 117P/HSI5 |
| L27 | BK5_IO25 | - | 167N/HSI8 | BK5_IO25 | - | 117N/HSI5 |
| L26 | BK5_IO26 | HSI8A_SINP | 168P/HSI8 | BK5_IO26 | HSI5A_SINP | 118P/HSI5 |
| - | GND (Bank 5) | - | - | - | - | - |
| L25 | BK5_IO27 | HSI8A_SINN | 168N/HSI8 | BK5_IO27 | HSI5A_SINN | 118N/HSI5 |
| K27 | BK5_IO28 | - | 169P/HSI8 | BK5_IO28 | - | 119P/HSI5 |
| K26 | BK5_IO29 | - | 169N/HSI8 | BK5_IO29 | - | 119N/HSI5 |
| J30 | BK5_IO30 | HSI8A_SOUTP | 170P/HSI8 | BK5_IO30 | HSI5A_SOUTP | 120P/HSI5 |
| - | - | - | - | GND (Bank 5) | - | - |
| J29 | BK5_IO31 | HSI8A_SOUTN | 170N/HSI8 | BK5_IO31 | HSI5A_SOUTN | 120N/HSI5 |
| J26 | BK5_IO32 | - | 171P/HSI8 | NC | - | - |
| J27 | BK5_IO33 | - | 171N/HSI8 | NC | - | - |
| H30 | BK5_IO34 | HSI8B_SINP | 172P/HSI8 | NC | - | - |
| - | GND (Bank 5) | - | - | - | - | - |
| H29 | BK5_IO35 | HSI8B_SINN | 172N/HSI8 | NC | - | - |
| J25 | BK5_IO36 | - | 173P/HSI9 | NC | - | - |
| J24 | BK5_IO37 | - | 173N/HSI9 | NC | - | - |
| G30 | BK5_IO38 | HSI8B_SOUTP | 174P/HSI9 | NC | - | - |
| G29 | BK5_IO39 | HSI8B_SOUTN | 174N/HSI9 | NC | - | - |
| H27 | BK5_IO40 | - | 175P/HSI9 | NC | - | - |
| H28 | BK5_IO41 | - | 175N/HSI9 | NC | - | - |
| F30 | BK5_IO42 | HSI9A_SINP | 176P/HSI9 | NC | - | - |
| - | GND (Bank 5) | - | - | - | - | - |
| F29 | BK5_IO43 | HSI9A_SINN | 176N/HSI9 | NC | - | - |
| G27 | BK5_IO44 | - | 177P/HSI9 | NC | - | - |
| G28 | BK5_IO45 | - | 177N/HSI9 | NC | - | - |
| E30 | BK5_IO46 | HSI9A_SOUTP | 178P/HSI9 | NC | - | - |
| E29 | BK5_IO47 | HSI9A_SOUTN | 178N/HSI9 | NC | - | - |
| H26 | BK5_IO48 | - | 179P/HSI9 | BK5_IO33 | - | 121N/HSI5 |
| H25 | BK5_IO49 | VREF5 | 179N/HSI9 | BK5_IO32 | VREF5 | 121P/HSI5 |
| D30 | BK5_IO50 | HSI9B_SINP | 180P/HSI9 | BK5_IO34 | HSI5B_SINP | 122P/HSI5 |
| - | GND (Bank 5) | - | - | - | - | - |
| D29 | BK5_IO51 | HSI9B_SINN | 180N/HSI9 | BK5_IO35 | HSI5B_SINN | 122N/HSI5 |
| F28 | BK5_IO52 | - | 181P | BK5_IO36 | - | 123P/HSI5 |
| F27 | BK5_IO53 | - | 181N | BK5_IO37 | - | 123N/HSI5 |
| C30 | BK5_IO54 | HSI9B_SOUTP | 182P | BK5_IO38 | HSI5B_SOUTP | 124P/HSI5 |
| - | - | - | - | GND (Bank 5) | - | - |
| C29 | BK5_IO55 | HSI9B_SOUTN | 182N | BK5_IO39 | HSI5B_SOUTN | 124N/HSI5 |
| G26 | BK5_IO56 | - | 183P | NC | - | - |

**"E-Series" Commercial (Cont.)**

| Part Number | Gates | Voltage | Speed Grade | Package | Balls |
|---|---|---|---|---|---|
| LFX500EC-04FN900C | 476K | 1.8 | -4 | Lead-Free fpBGA | 900 |
| LFX500EC-03FN900C | 476K | 1.8 | -3 | Lead-Free fpBGA | 900 |

**"E-Series" Industrial**

| Part Number | Gates | Voltage | Speed Grade | Package | Balls |
|---|---|---|---|---|---|
| LFX125EB-04FN256I | 139K | 2.5/3.3 | -4 | Lead-Free fpBGA | 256 |
| LFX125EB-03FN256I | 139K | 2.5/3.3 | -3 | Lead-Free fpBGA | 256 |
| LFX125EC-03FN256I | 139K | 1.8 | -3 | Lead-Free fpBGA | 256 |
| LFX200EB-04FN256I | 210K | 2.5/3.3 | -4 | Lead-Free fpBGA | 256 |
| LFX200EB-03FN256I | 210K | 2.5/3.3 | -3 | Lead-Free fpBGA | 256 |
| LFX200EC-03FN256I | 210K | 1.8 | -3 | Lead-Free fpBGA | 256 |
| LFX500EB-04FN900I | 476K | 2.5/3.3 | -4 | Lead-Free fpBGA | 900 |
| LFX500EB-03FN900I | 476K | 2.5/3.3 | -3 | Lead-Free fpBGA | 900 |
| LFX500EC-03FN900I | 476K | 1.8 | -3 | Lead-Free fpBGA | 900 |

## For Further Information

In addition to this data sheet, the following Lattice technical notes may be helpful when designing with the ispXPGA Family:

- TN1028, ispXPGA Memory Usage Guidelines
- TN1003, sysCLOCK PLL Usage and Design Guidelines
- TN1000, sysIO Usage Guidelines for Lattice Devices
- TN1026, ispXP Configuration Usage Guidelines
- TN1020, sysHSI Usage Guidelines
- TN1043, Power Estimation in ispXPGA Devices

## Revision History

| Date | Version | Change Summary |
|---|---|---|
| — | — | Previous Lattice releases. |
| September 2003 | 07 | Improved typical Icc data for LFX125B/C and LFX500B/C. |
| | | Improved external switching characteristics timing numbers for LFX125B/C. |
| | | Improved PIC timing numbers for LFX125B/C. |
| | | Improved $t_{IOINDLY}$ timing numbers for LFX125B/C. |
| | | Improved external switching characteristics timing numbers for LFX500B/C. |
| | | Improved PIC timing numbers for LFX500B/C. |
| | | Improved $t_{IOINDLY}$ timing numbers for LFX500B/C. |
| | | Enhanced CDR functionality description. |
| | | Logic Signal Connections and Signal Descriptions - removed CDRLOCK, LOSS and EXLOSS descriptions. |
| January 2004 | 07.1 | Added lead-free package designators. |
| June 2004 | 08.0 | Updated CDR specifications and reference notes. Removed Source Synchronous (SS:No CAL) mode references for the sysHSI blocks. |
| | | Revised Figures 16 and 24 for clarification. |
| | | Clarification of VCC sysHSI Block for 1.8V devices. |
| | | Updated IIL and IIH max specification. |
| | | Updated LVTTL and PCI 3.3 to support 5V tolerance. |

## Revision History (Cont.)

| Date | Version | Change Summary |
|---|---|---|
| June 2004 (cont.) | 08.0 (cont.) | Updated Global Clock Input Setup time specifications. |
| | | Clarification of Serial Out LVDS test condition. |
| | | Clarification of REFCLK, SS_CLKIN peak-to-peak period jitter condition. |
| | | Added sysHSI Reserved pins and footnote. |
| | | Removed industrial ordering part numbers. |
| July 2004 | 09.0 | Added “E” Series product family. |
| August 2004 | 10.0 | Final release. |
| December 2004 | 10.1 | Updated NC Connections table. |
| April 2005 | 10.2 | Clarification of IDK specification. |
| April 2005 | 11.0 | Select lead-free packages release. |
| July 2005 | 12.0 | Added lead-free 516 fpBGA ordering part numbers. |
| April 2007 | 13.0 | Removed lead-free 680 fpSBGA information from Part Number Description and Ordering Part Number tables. Removed lead-free 516 fpBGA for LFX125 from Ordering Part Number tables. |
| November 2007 | 14.0 | Removed lead-free 516 fpBGA information from Part Number Description and Ordering Part Number tables. |
| July 2008 | 14.1 | Added 516 fpBGA package without heat spreader to Part Number Description and Ordering Part Number tables. |
| February 2010 | 15.0 | Ordering part numbers and ispXPGA Family Selection Guide table have been updated per PCN #03A-10 (discontinuation of the ispXPGA 1200 devices). |
| | | References to "system gates" changed to "functional gates." |