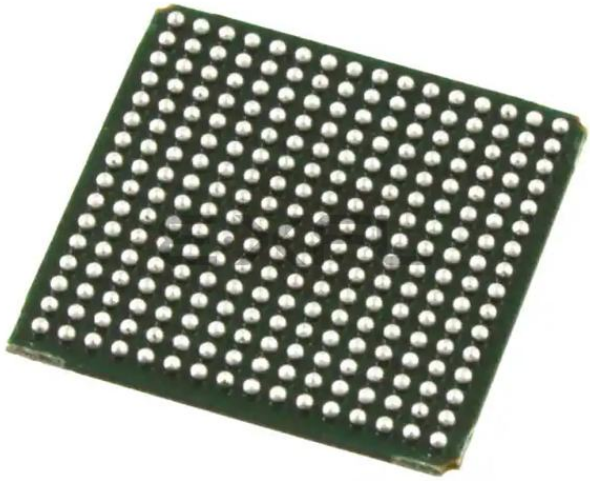
Lattice Semiconductor Corporation - LFX200EB-03FN256C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

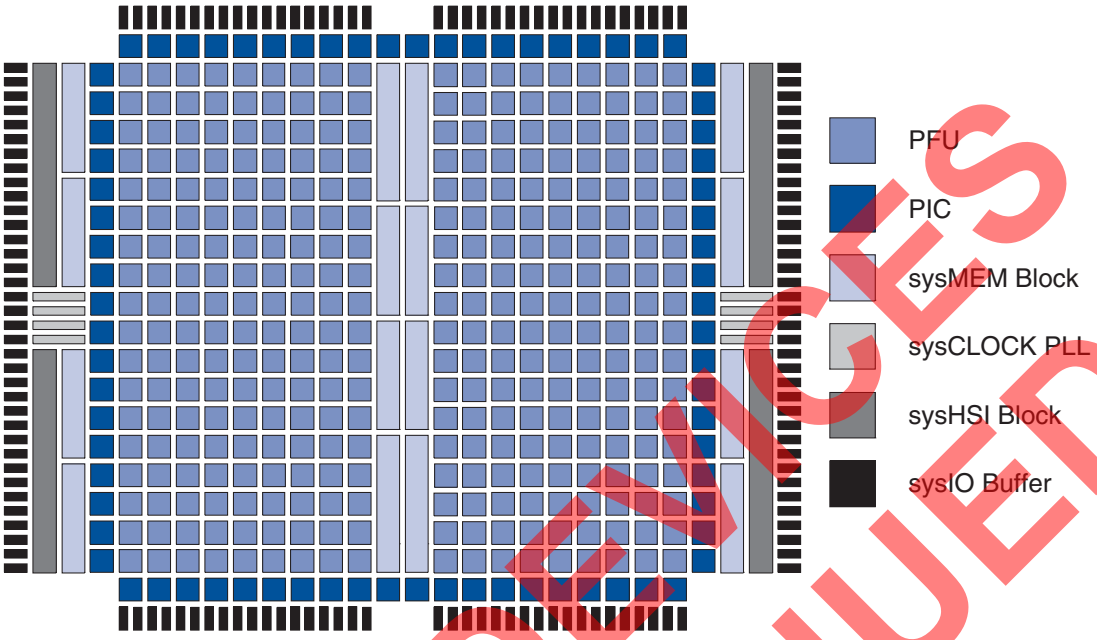
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	2704
Total RAM Bits	113664
Number of I/O	160
Number of Gates	210000
Voltage - Supply	2.3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx200eb-03fn256c

Figure 1. ispXPGA Block Diagram



Programmable Function Unit

The Programmable Function Unit (PFU) is the basic building block of the ispXPGA architecture. The PFUs are arranged in rows and columns in the device with PFU (1,1) referring to (row 1, column 1). Each PFU consists of four Configurable Logic Elements (CLEs), four Configurable Sequential Elements (CSEs), and a Wide Logic Generator (WLG). By utilizing these components, the PFU can implement a variety of functions. Table 3 lists some of the function capabilities of the PFU.

There are 57 inputs to each PFU and nine outputs. The PFU uses 20 inputs for logic, and 37 inputs drive the control logic from which six control signals are derived for the PFU.

Table 3. Function Capability of ispXPGA PFU

Function	Capability
Look-up table	LUT-4, LUT-5, LUT-6
Wide logic functions	Up to 20 input logic functions
Multiplexing	2:1, 4:1, 8:1
Arithmetic logic	Dedicated carry chain and booth multiplication logic
Single-port RAM	16X1, 16X2, 16X4, 32X1, 32X2, 64X1
Double-port RAM	16X1, 16X2, 32X1
Shift register	8-bit shift registers (up to 32-bit shift capability)

Configurable Logic Element

The CLE is made up of a four-input Look-up Table (LUT-4), a Carry Chain Generator (CCG), and a two-input AND gate. The LUT-4 creates various combinatorial and memory elements, the CCG creates a single one-bit full adder, and the two-input AND gate can expand the CCG to incorporate Booth Multiplier capability by feeding the output of the AND gate to one of the inputs of the CCG.

Of the five inputs that feed each CLE, two are dedicated inputs into each LUT-4 and the remaining three take on varying functionality. The third and fourth inputs can be used as either inputs to the LUT-4 or as a Feed-Thru to the CSE via the WLG. The fifth input can be a data port when the LUT is configured as Distributed Memory, a select line for multiplexer operation, or a Feed-Thru directly to the CSE via the WLG (Figure 2).

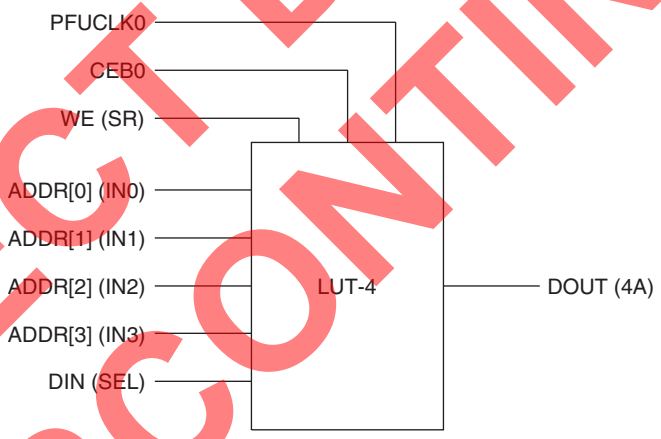
Look-Up Table – Combinatorial Mode

In combinatorial mode, the LUT-4 can implement any logic function up to four inputs. By using the carry chain and the WLG, each LUT-4 can be combined to form the enhanced functions listed in Table 3.

Look-Up Table – Distributed Memory Mode

In the distributed memory mode, the LUT functions as a memory element. The inputs to the LUT function as Address and Data. Each PFU is capable of implementing up to 64 SRAM bits. Both single and double port RAM can be performed in the PFU (Table 3). Furthermore, the distributed memory can be configured as either synchronous or asynchronous memory. Figure 3 illustrates the LUT while in distributed memory mode. When using any LUT in the PFU in memory mode, the Set/Reset signal will be used for Write Enable (WE(SR)) and the CLK0 signal will be used as the clock for synchronous read and write.

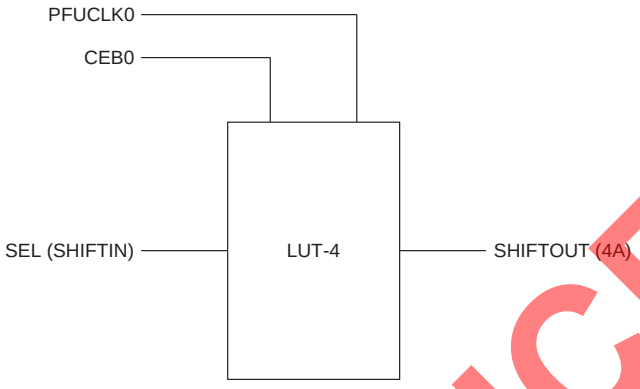
Figure 3. LUT in Distributed Memory Mode



Look-Up Table – Shift Register Mode

In the shift register mode, the LUT functions as a 1-bit to 8-bit shift register. This means that each PFU can implement up to four 8-bit shift registers or any cascaded combination. Figure 4 illustrates the LUT when configured in shift register mode.

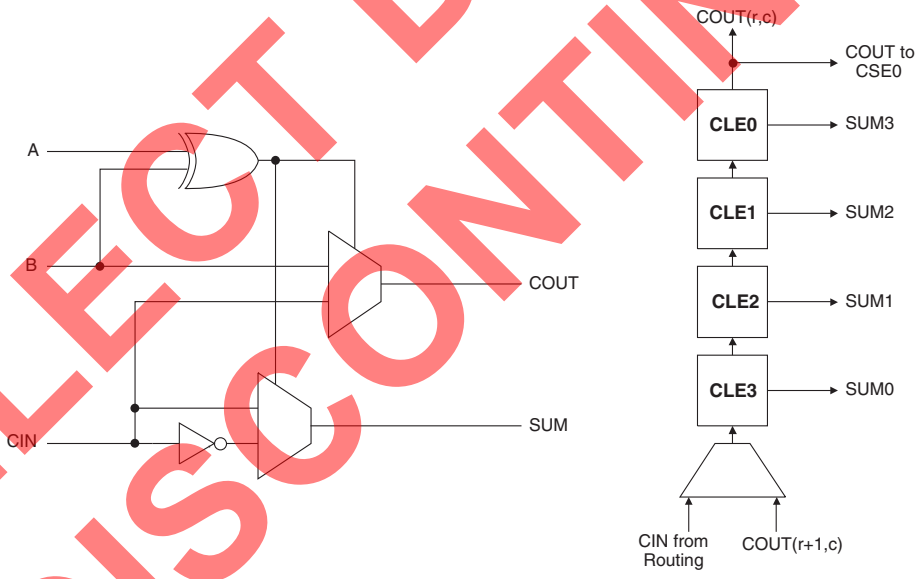
Figure 4. LUT in Shift Register Mode



Carry Chain Generator

The Carry Chain Generator is useful for implementing high-speed arithmetic functions. The CCG consists of a two-input XOR gate whose carryout can be cascaded with the input of the adjacent CCG. As shown in Figure 5, the carryin signal feeds CLE3 of the PFU and is propagated through CLE2 and CLE1 before reaching CLE0. The sum output of the CCG can be fed to the CSE through the WLG. The carryout must propagate to CLE0 for use outside the PFU. The carryout from the PFU can feed the W0 input of CSE0. The CCG also helps to effectively implement wider functions by using its logic elements to expand the capabilities of the LUT-4.

Figure 5. Carry Chain Generator



Wide Logic Generator

The WLG contains the logic necessary to implement wide gate functions. This is made up of a set of multiplexers that are located between the CLE and the CSE. The WLG helps in enhancing the wide gating capability of the PFU. The outputs of each CLE can be cascaded in the WLG to build wide gating functions. Wide multiplexing functions are also possible with a similar use of the WLG. Figure 6 illustrates the WLG.

Absolute Maximum Ratings[1, 2, 3]

	1.8V	2.5V/3.3V
Supply Voltage (V_{CC})	-0.5 to 2.5V	-0.5 to 5.5V
PLL Supply Voltage (V_{CCP})	-0.5 to 2.5V	-0.5 to 5.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V
IEEE 1149.1 TAP Supply Voltage (V_{CCJ})	-0.5 to 4.5V	-0.5 to 4.5V
Input Voltage Applied[4, 5]	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C
Junction Temperature (T_J) with Power Applied	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied (while programming, following the programming specifications).
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to (V_{IH} (MAX) + 2) volts not to exceed 6V is permitted for a duration of <20ns.
5. A maximum of 64 I/Os per device with V_{IN} > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage for 1.8V device[1]	1.65	1.95	V
	Supply Voltage for 2.5V device	2.3	2.7	V
	Supply Voltage for 3.3V device	3.0	3.6	V
V_{CCP}	Supply Voltage for PLL and sysHSI blocks, 1.8V devices[1]	1.65	1.95	V
	Supply Voltage for PLL and sysHSI blocks, 2.5V devices	2.3	2.7	V
	Supply Voltage for PLL and sysHSI blocks, 3.3V devices	3.0	3.6	V
V_{CCJ}	Supply Voltage for IEEE 1149.1 Test Access Port for LVCMOS 1.8V	1.65	1.95	V
	Supply Voltage for IEEE 1149.1 Test Access Port for LVCMOS 2.5V	2.3	2.7	V
	Supply Voltage for IEEE 1149.1 Test Access Port for LVCMOS 3.3V	3.0	3.6	V
T_J (COM)	Junction Temperature Commercial Operation	0	85	C
T_J (IND)	Junction Temperature Industrial Operation	-40	105	C

1. sysHSI specification is valid for V_{CC} and V_{CCP} = 1.7V to 1.9V.

E²CMOS Erase Reprogram Specifications

Parameter	Min	Max	Units
Erase/Reprogram Cycle[1]	1,000	—	Cycles

1. Valid over commercial temperature range.

Hot Socketing Characteristics[1, 2, 3, 4]

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DK}	Input or Tristated I/O Leakage Current	0 ð V_{IN} ð 3.0V	—	+/-50	+/-800	µA

1. Insensitive to sequence of V_{CC} and V_{CCO} when V_{CCO} ð 1.0V. For V_{CCO} > 1.0V, V_{CC} min must be present. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO}, provided (V_{IN} - V_{CCO}) ð 3.6V.
2. LVTTL, LVCMOS only.
3. 0 < V_{CC} ð V_{CC} (MAX), 0 < V_{CCO} ð V_{CCO} (MAX).
4. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until non-volatile cells are active.

sysIO Differential Standards DC Electrical Characteristics[1]

Parameter	Description	Test Conditions	Min.	Typ.	Max.
LVDS[2]					
V_{INP}, V_{INM}	Input voltage		0V	—	2.4V
V_{THD}	Differential input threshold	0.2V ð V_{CM} ð 1.8V	+/-100mV	—	—
I_{IN}	Input current	Power on	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	—	1.38V	1.60V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	0.9V	1.03V	—
V_{OD}	Output Voltage Differential	$\|V_{OP} - V_{OM}\|$, R_T = 100 ohm	250mV	350mV	450mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50mV
V_{OS}	Output Voltage Offset	$\|V_{OP} + V_{OM}\|/2$, R_T = 100 ohm	1.125V	1.25V	1.375V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50mV
I_{OSD}	Output short circuit current	V_{OD} = 0V Driver outputs shorted	—	—	24mA
BLVDS[1]					
V_{INP}, V_{INM}	Input voltage		0V	—	2.4V
V_{THD}	Differential input threshold	0.2V ð V_{CM} ð 1.8V	+/-100mV	—	—
I_{IN}	Input current	Power on	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 27Ω	—	1.4V	1.80V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 27Ω	0.95V	1.1V	—
V_{OD}	Output Voltage Differential	$\|V_{OP} - V_{OM}\|$, RT = 27Ω	240mV	300mV	460mV
ΔV_{OD}	Change in V_{OD} Between H and L				27mV
V_{OS}	Output Voltage Offset	$\|V_{OP} + V_{OM}\|$ /2, RT = 27Ω	1.1V	1.3V	1.5V
ΔV_{OS}	Change in V_{OS} Between H and L				27mV
I_{OSD}	Output Short Circuit Current	V_{OD} = 0. Driver Outputs Shorted.		36mA	65mA

1. Refer to TN1000, sysIO Usage Guidelines for Lattice Devices.
2. V_{OP} and V_{OM} are the two outputs of the LVDS/BLVDS output buffer.

LVPECL[1]								
DC Parameter	**Parameter Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
V_{CCO}		**3.0**		**3.3**		**3.6**		**V**
V_{IH}	Input Voltage High	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	Input Voltage Low	0.86	2.125	0.86	2.125	0.86	2.125	V
V_{OH}	Output Voltage High	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	Output Voltage Low	0.96	1.27	1.06	1.43	1.3	1.57	V
V_{DIFF}[2]	Differential Input threshold	0.3	—	0.3	—	0.3	—	V

1. These values are valid at the output of the source termination pack as shown above with 100-ohm differential load only (see Figure 23). The V_{OH} levels are 200mV below the standard LVPECL levels and are compatible with devices tolerant of the lower common mode ranges.
2. Valid for 0.2 ð V_{CM} ð 1.8V.

ispXPGA 125B/C & ispXPGA 125EB/EC Timing Adders

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	4.28	—	4.6	—	5.29	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

ispXPGA 200B/C & ispXPGA 200EB/EC PFU Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Functional Delays								
LUTs								
t_{LUT4}	4-Input LUT Delay	—	0.41	—	0.44	—	0.51	ns
t_{LUT5}	5-Input LUT Delay	—	0.73	—	0.79	—	0.91	ns
t_{LUT6}	6-Input LUT Delay	—	0.86	—	0.93	—	1.07	ns
Shift Register (LUT)								
t_{LSR_S}	Shift Register Setup Time	-0.64	—	-0.62	—	-0.53	—	ns
t_{LSR_H}	Shift Register Hold Time	0.61	—	0.63	—	0.72	—	ns
t_{LSR_CO}	Shift Register Clock to Output Delay	—	0.70	—	0.75	—	0.86	ns
Arithmetic Functions								
$t_{LCTHRUR}$	MC (Macro Cell) Carry In to MC Carry Out Delay (Ripple)	—	0.08	—	0.09	—	0.10	ns
$t_{LCTHRUL}$[2]	MC Carry In to MC Carry Out Delay (Look Ahead)	—	0.05	—	0.05	—	0.06	ns
t_{LSTHRU}	MC Sum In to MC Sum Out Delay	—	0.42	—	0.45	—	0.52	ns
$t_{LSINCOUT}$	MC Sum In to MC Carry Out Delay	—	0.29	—	0.31	—	0.36	ns
$t_{LCINSOUTR}$	MC Carry In to MC Sum Out Delay (Ripple)	—	0.36	—	0.39	—	0.45	ns
$t_{LCINSOUTL}$	MC Carry In to MC Sum Out Delay (Look Ahead)	—	0.26	—	0.28	—	0.32	ns
Feed-thru								
t_{LFT}	PFU Feed-Thru Delay	—	0.15	—	0.16	—	0.18	ns
Distributed RAM								
t_{LRAM_CO}	Clock to RAM Output	—	1.24	—	1.33	—	1.53	ns
t_{LRAMAD_S}	Address Setup Time	-0.41	—	-0.40	—	-0.34	—	ns
t_{LRAMD_S}	Data Setup Time	0.21	—	0.22	—	0.25	—	ns
t_{LRAMWE_S}	Write Enable Setup Time	0.45	—	0.46	—	0.53	—	ns
t_{LRAMAD_H}	Address Hold Time	0.58	—	0.60	—	0.69	—	ns
t_{LRAMD_H}	Data Hold Time	0.11	—	0.11	—	0.13	—	ns
t_{LRAMWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{LRAMCPW}$	Clock Pulse Width (High or Low)	2.91	—	3.00	—	3.45	—	ns
$t_{LRAMADO}$	Address to Output Delay	—	0.86	—	0.93	—	1.07	ns
Register/Latch Delays								
Registers								
t_{L_CO}	Register Clock to Output Delay	—	0.58	—	0.62	—	0.71	ns
t_{L_S}	Register Setup Time (Data before Clock)	0.14	—	0.14	—	0.16	—	ns
t_{L_H}	Register Hold Time (Data after Clock)	-0.12	—	-0.12	—	-0.10	—	ns
t_{LCE_S}	Register Clock Enable Setup Time	-0.11	—	-0.11	—	-0.09	—	ns
t_{LCE_H}	Register Clock Enable Hold Time	0.11	—	0.11	—	0.13	—	ns
Latches								
t_{L_GO}	Latch Gate to Output Delay	—	0.09	—	0.10	—	0.12	ns
t_{LL_S}	Latch Setup Time	0.14	—	0.14	—	0.16	—	ns
t_{LL_H}	Latch Hold Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{LLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns

ispXPGA 500B/C & ispXPGA 500EB/EC PFU Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Functional Delays								
LUTs								
t_{LUT4}	4-Input LUT Delay	—	0.41	—	0.44	—	0.51	ns
t_{LUT5}	5-Input LUT Delay	—	0.73	—	0.79	—	0.91	ns
t_{LUT6}	6-Input LUT Delay	—	0.86	—	0.93	—	1.07	ns
Shift Register (LUT)								
t_{LSR_S}	Shift Register Setup Time	-0.64	—	-0.62	—	-0.53	—	ns
t_{LSR_H}	Shift Register Hold Time	0.61	—	0.63	—	0.72	—	ns
t_{LSR_CO}	Shift Register Clock to Output Delay	—	0.70	—	0.75	—	0.86	ns
Arithmetic Functions								
$t_{LCTHRUR}$	MC (Macro Cell) Carry In to MC Carry Out Delay (Ripple)	—	0.08	—	0.09	—	0.10	ns
$t_{LCTHRUL}$[2]	MC Carry In to MC Carry Out Delay (Look Ahead)	—	0.05	—	0.05	—	0.06	ns
t_{LSTHRU}	MC Sum In to MC Sum Out Delay	—	0.42	—	0.45	—	0.52	ns
$t_{LSINCOUT}$	MC Sum In to MC Carry Out Delay	—	0.29	—	0.31	—	0.36	ns
$t_{LCINSOUTR}$	MC Carry In to MC Sum Out Delay (Ripple)	—	0.36	—	0.39	—	0.45	ns
$t_{LCINSOUTL}$	MC Carry In to MC Sum Out Delay (Look Ahead)	—	0.26	—	0.28	—	0.32	ns
Feed-thru								
t_{LFT}	PFU Feed-Thru Delay	—	0.15	—	0.16	—	0.18	ns
Distributed RAM								
t_{LRAM_CO}	Clock to RAM Output	—	1.24	—	1.33	—	1.53	ns
t_{LRAMAD_S}	Address Setup Time	-0.41	—	-0.40	—	-0.34	—	ns
t_{LRAMD_S}	Data Setup Time	0.21	—	0.22	—	0.25	—	ns
t_{LRAMWE_S}	Write Enable Setup Time	0.45	—	0.46	—	0.53	—	ns
t_{LRAMAD_H}	Address Hold Time	0.58	—	0.60	—	0.69	—	ns
t_{LRAMD_H}	Data Hold Time	0.11	—	0.11	—	0.13	—	ns
t_{LRAMWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{LRAMCPW}$	Clock Pulse Width (High or Low)	2.91	—	3.00	—	3.45	—	ns
$t_{LRAMADO}$	Address to Output Delay	—	0.86	—	0.93	—	1.07	ns
Register/Latch Delays								
Registers								
t_{L_CO}	Register Clock to Output Delay	—	0.58	—	0.62	—	0.71	ns
t_{L_S}	Register Setup Time (Data before Clock)	0.14	—	0.14	—	0.16	—	ns
t_{L_H}	Register Hold Time (Data after Clock)	-0.12	—	-0.12	—	-0.10	—	ns
t_{LCE_S}	Register Clock Enable Setup Time	-0.11	—	-0.11	—	-0.09	—	ns
t_{LCE_H}	Register Clock Enable Hold Time	0.11	—	0.11	—	0.13	—	ns
Latches								
t_{L_GO}	Latch Gate to Output Delay	—	0.09	—	0.10	—	0.12	ns
t_{LL_S}	Latch Setup Time	0.14	—	0.14	—	0.16	—	ns
t_{LL_H}	Latch Hold Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{LLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns

ispXPGA Power Supply and NC Connections[1] (Continued)

Signal	680-Ball fpBGA[3]	900-Ball fpBGA[3]
NC[2]	A3, B29, AW3, AV3, AW11, AV11, AV29, AW29, AW37, B3, AV37, C39, C38, AU39, AU38, AJ39, AJ38, N38, N39, C2, C1, AU1, AU2, AJ2, AJ1, N2, N1, B11, A11, A37, B37, A29	**LFX500:** A8, A9, A10, A11, A19, A20, A21, A22, B8, B9, B10, B11, B19, B20, B21, B22, C1, C2, C11, C12, C19, C20, C23, D3, D10, D11, D12, D19, D20, D21, D22, D23, E3, E5, E6, E10, E11, E12, E21, E22, E25, E26, E28, E29, E30, F1, F2, F6, F9, F10, F11, F12, F21, F22, F25, F26, F29, F30, G1, G2, G3, G4, G7, G8, G9, G10, G11, G12, G14, G15, G16, G17, G19, G20, G21, G22, G23, G24, G25, G26, G27, G28, G29, G30, H1, H2, H3, H4, H5, H6, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, H17, H18, H19, H20, H21, H22, H23, H24, H27, H28, H29, H30, J1, J2, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, K6, K7, K8, K9, K10, K12, K13, K14, K15, K16, K17, K18, K19, K21, K22, K23, K24, K25, L7, L8, L9, L22, L23, L24, M7, M8, M9, M10, M21, M22, M23, M24, N8, N9, N10, N21, N22, N23, P7, P8, P9, P10, P21, P22, P23, P24, R8, R9, R10, R21, R22, R23, R24, R25, T6, T7, T8, T9, T10, T21, T22, T23, T24, T25, U7, U8, U9, U10, U21, U22, U23, U24, V8, V9, V10, V21, V22, V23, W7, W8, W9, W10, W21, W22, W23, W24, W25, W26, Y3, Y4, Y5, Y6, Y7, Y8, Y9, Y22, Y23, Y24, Y25, Y26, Y27, Y28, AA4, AA5, AA6, AA7, AA8, AA9, AA10, AA12, AA13, AA14, AA15, AA16, AA17, AA18, AA19, AA21, AA22, AA23, AA24, AA25, AA26, AA27, AB1, AB2, AB4, AB5, AB6, AB7, AB8, AB9, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB18, AB19, AB20, AB21, AB22, AB23, AB24, AB25, AB26, AB27, AC1, AC2, AC3, AC4, AC5, AC6, AC7, AC8, AC9, AC10, AC11, AC12, AC13, AC14, AC15, AC16, AC17' AC18' AC19, AC20, AC21, AC22, AC23, AC24, AC27, AC28, AC29, AC30, AD1, AD2, AD7, AD8, AD9, AD10, AD11, AD12, AD14, AD15, AD16, AD17, AD19, AD20, AD21, AD22, AD23, AD24, AD29, AD30, AE6, AE9, AE10, AE11, AE12, AE19, AE20, AE21, AE22, AE25, AE29, AE30, AF5, AF6, AF10, AF11, AF12, AF19, AF20, AF21, AF22, AF25, AF26, AG10, AG11, AG12, AG19, AG20, AG21, AG22, AH11, AH12, AH19, AH20, AJ8, AJ9, AJ10, AJ11, AJ20, AJ21, AJ22, AK8, AK9, AK10, AK11, AK20, AK21, AK22 **LFX1200:** AA22, AA23, AA24, AA25, AB23, AC24, T21, T22, T23, T24, T25, U21, U22, U23, U24, V21, V22, V23, W21, W22, W23, W24, Y22, Y23, Y24, AA16, AA17, AA18, AA19, AA21, AB16, AB17, AB18, AB19, AB20, AB21, AB22, AC16, AC17, AC18, AC19, AC20, AC21, AC22, AC23, AD16, AD17, AD19, AD20, AD22, AD23, AD24, AE22, AE25, AF25, AF26, AA10, AA12, AA13, AA14, AA15, AB10, AB11, AB12, AB13, AB14, AB15, AB9, AC10, AC11, AC12, AC13, AC14, AC15, AC8, AC9, AD11, AD12, AD14, AD15, AD7, AD8, AD9, AE6, AE9, AF5, AF6, H24, J23, K22, K23, K24, K25, L22, L23, L24, M21, M22, M23, M24, N21, N22, N23, P21, P22, P23, P24, R21, R22, R23, R24, R25, AA6, AA7, AA8, AA9, AB8, AC7, T10, T6, T7, T8, T9, U10, U7, U8, U9, V10, V8, V9, W10, W7, W8, W9, Y7, Y8, Y9, H5, H6, H7, J8, K6, K7, K8, K9, L7, L8, L9, M10, M7, M8, M9, N10, N8, N9, P10, P7, P8, P9, R10, R8, R9, E25, E26, F22, F25, G16, G17, G19, G20, G22, G23, G24, H16, H17, H18, H19, H20, H21, H22, H23, J16, J17, J18, J19, J20, J21, J22, K16, K17, K18, K19, K21, E5, E6, F6, F9, G11, G12, G14, G15, G7, G8, G9, H10, H11, H12, H13, H14, H15, H8, H9, J10, J11, J12, J13, J14, J15, J9, K10, K12, K13, K14, K15

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, V_{CC} or GND.
3. Balls for GND, V_{CC} and V_{CCOx} are connected within the substrate to their respective common signals. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
D16	BK5_IO15	HSI3A_SOUTN	72N/HSI3	BK5_IO13	HSI1A_SOUTN	61N/HSI1
E13	BK5_IO16	VREF5	73P/HSI3	BK5_IO14	VREF5	62P/HSI1
E14	BK5_IO17	-	73N/HSI3	BK5_IO15	-	62N/HSI1
E15	BK5_IO18	HSI3B_SINP	74P/HSI3	BK5_IO16	HSI1B_SINP	63P/HSI1
-	-	-	-	GND (Bank 5)	-	-
D15	BK5_IO19	HSI3B_SINN	74N/HSI3	BK5_IO17	HSI1B_SINN	63N/HSI1
C16	BK5_IO22	HSI3B_SOUTP	76P/HSI3	BK5_IO20	HSI1B_SOUTP	65P/HSI1
-	GND (Bank 5)	-	-	-	-	-
B16	BK5_IO23	HSI3B_SOUTN	76N/HSI3	BK5_IO21	HSI1B_SOUTN	65N/HSI1
D14	BK5_IO24	-	77P/HSI3	BK5_IO18	-	64P/HSI1
C15	BK5_IO25	-	77N/HSI3	BK5_IO19	-	64N/HSI1
C13	CFG0	-	-	CFG0	-	-
A15	DONE	-	-	DONE	-	-
A14	PROGRAMb	-	-	PROGRAMb	-	-
D12	BK6_IO0	INITb	78P	BK6_IO0	INITb	66P
C12	BK6_IO1	CCLK	78N	BK6_IO1	CCLK	66N
B14	BK6_IO2	-	79P	BK6_IO2	-	67P
-	GND (Bank 6)	-	-	-	-	-
B13	BK6_IO3	-	79N	BK6_IO3	-	67N
A13	BK6_IO4	CSb	80P	BK6_IO4	CSb	68P
-	-	-	-	GND (Bank 6)	-	-
A12	BK6_IO5	Read	80N	BK6_IO5	READ	68N
D11	BK6_IO6	DATA7	81P	BK6_IO6	DATA7	69P
C11	BK6_IO7	DATA6	81N	BK6_IO7	DATA6	69N
B12	BK6_IO8	-	82P	BK6_IO8	-	70P
B11	BK6_IO9	VREF6	82N	BK6_IO9	VREF6	70N
D10	BK6_IO10	DATA5	83P	BK6_IO10	DATA5	71P
-	GND (Bank 6)	-	-	-	-	-
C10	BK6_IO11	DATA4	83N	BK6_IO11	DATA4	71N
-	-	-	-	GND (Bank 6)	-	-
A11	BK6_IO14	DATA3	85P	BK6_IO14	DATA3	73P
A10	BK6_IO15	DATA2	85N	BK6_IO15	DATA2	73N
D9	BK6_IO16	-	86P	BK6_IO16	-	74P
C9	BK6_IO17	-	86N	BK6_IO17	-	74N
B10	BK6_IO18	DATA1	87P	BK6_IO18	DATA1	75P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
B9	BK6_IO19	DATA0	87N	BK6_IO19	DATA0	75N
E9	BK6_IO20	-	88P	BK6_IO20	-	76P
E8	BK6_IO21	-	88N	BK6_IO21	-	76N
-	GND (Bank 6)	-	-	-	-	-
-	GND (Bank 7)	-	-	-	-	-
D8	BK7_IO0	-	91P	BK7_IO0	-	77P

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
C8	BK7_IO1	-	91N	BK7_IO1	-	77N
B8	BK7_IO2	-	92P	BK7_IO2	-	78P
B7	BK7_IO3	-	92N	BK7_IO3	-	78N
A9	BK7_IO6	-	94P	BK7_IO4	-	79P
-	GND (Bank 7)	-	-	-	-	-
A8	BK7_IO7	-	94N	BK7_IO5	-	79N
C7	BK7_IO10	-	96P	BK7_IO6	-	80P
D7	BK7_IO11	-	96N	BK7_IO7	-	80N
D6	BK7_IO12	-	97P	BK7_IO8	-	81P
-	-	-	-	GND (Bank 7)	-	-
C6	BK7_IO13	-	97N	BK7_IO9	-	81N
B6	BK7_IO14	-	98P	BK7_IO10	-	82P
-	GND (Bank 7)	-	-	-	-	-
B5	BK7_IO15	-	98N	BK7_IO11	-	82N
A7	BK7_IO16	VREF7	99P	BK7_IO12	VREF7	83P
A6	BK7_IO17	-	99N	BK7_IO13	-	83N
D5	BK7_IO18	-	100P	BK7_IO14	-	84P
C5	BK7_IO19	-	100N	BK7_IO15	-	84N
A5	BK7_IO20	-	101P	BK7_IO16	-	85P
-	-	-	-	GND (Bank 7)	-	-
A4	BK7_IO21	-	101N	BK7_IO17	-	85N
B4	BK7_IO22	-	102P	BK7_IO18	-	86P
-	GND (Bank 7)	-	-	-	-	-
B3	BK7_IO23	-	102N	BK7_IO19	-	86N
A3	TDO	-	-	TDO	-	-
A2	VCCJ	-	-	VCCJ	-	-
C4	TDI	-	-	TDI	-	-

1. Not available for differential pairs.
2. If a sysHSI Block is used, the indicated sysHSI reserved pins are unavailable for general purpose I/O use.

ispXPGA Logic Signal Connections: 516-Ball fpBGA

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
E4	BK0_IO0	-	0P	BK0_IO0	-	0P/HSI0	NC	-	-
D3	BK0_IO1	-	0N	BK0_IO1	-	0N/HSI0	NC	-	-
E3	BK0_IO2	HSI0A_SOUTP	1P/HSI0	BK0_IO2	HSI0A_SOUTP	1P/HSI0	BK0_IO0	HSI0A_SOUTP	0P
-	GND (Bank 0)	-	-	GND (Bank 0)	-	-	-	-	-
F3	BK0_IO3	HSI0A_SOUTN	1N/HSI0	BK0_IO3	HSI0A_SOUTN	1N/HSI0	BK0_IO1	HSI0A_SOUTN	0N
C2	BK0_IO4	-	2P/HSI0	BK0_IO4	-	2P/HSI0	BK0_IO2	-	1P/HSI0
B1	BK0_IO5	-	2N/HSI0	BK0_IO5	-	2N/HSI0	BK0_IO3	-	1N/HSI0
G4	BK0_IO6	HSI0A_SINP	3P/HSI0	BK0_IO6	HSI0A_SINP	3P/HSI0	BK0_IO4	HSI0A_SINP	2P/HSI0
-	-	-	-	-	-	-	GND (Bank 0)	-	-
G3	BK0_IO7	HSI0A_SINN	3N/HSI0	BK0_IO7	HSI0A_SINN	3N/HSI0	BK0_IO5	HSI0A_SINN	2N/HSI0
C1	BK0_IO8	-	4P/HSI0	BK0_IO8	-	4P/HSI0	BK0_IO6	-	3P/HSI0
D2	BK0_IO9	VREF0	4N/HSI0	BK0_IO9	VREF0	4N/HSI0	BK0_IO7	VREF0	3N/HSI0
H4	BK0_IO10	HSI0B_SOUTP	5P/HSI0	BK0_IO10	HSI0B_SOUTP	5P/HSI0	BK0_IO8	HSI0B_SOUTP	4P/HSI0
-	GND (Bank 0)	-	-	GND (Bank 0)	-	-	-	-	-
H3	BK0_IO11	HSI0B_SOUTN	5N/HSI0	BK0_IO11	HSI0B_SOUTN	5N/HSI0	BK0_IO9	HSI0B_SOUTN	4N/HSI0
D1	BK0_IO12	-	6P/HSI0	BK0_IO12	-	6P/HSI0	BK0_IO10	-	5P/HSI0
E1	BK0_IO13	-	6N/HSI0	BK0_IO13	-	6N/HSI0	BK0_IO11	-	5N/HSI0
E2	BK0_IO14	HSI0B_SINP	7P/HSI0	BK0_IO14	HSI0B_SINP	7P/HSI0	BK0_IO12	HSI0B_SINP	6P/HSI0
-	-	-	-	-	-	-	GND (Bank 0)	-	-
F2	BK0_IO15	HSI0B_SINN	7N/HSI0	BK0_IO15	HSI0B_SINN	7N/HSI0	BK0_IO13	HSI0B_SINN	6N/HSI0
G2	BK0_IO16	-	8P/HSI0	NC	-	-	NC	-	-
F1	BK0_IO17	-	8N/HSI0	NC	-	-	NC	-	-
J3	BK0_IO18	HSI1A_SOUTP	9P	NC	-	-	NC	-	-
-	GND (Bank 0)	-	-	-	-	-	-	-	-
K3	BK0_IO19	HSI1A_SOUTN	9N	NC	-	-	NC	-	-
K4	BK0_IO20	-	10P	NC	-	-	NC	-	-
L4	BK0_IO21	-	10N	NC	-	-	NC	-	-
H2	BK0_IO22	HSI1A_SINP	11P	NC	-	-	NC	-	-
J2	BK0_IO23	HSI1A_SINN	11N	NC	-	-	NC	-	-
G1	BK0_IO24	-	12P	NC	-	-	NC	-	-
H1	BK0_IO25	-	12N	NC	-	-	NC	-	-
L3	BK0_IO26	HSI1B_SOUTP	13P	NC	-	-	NC	-	-
-	GND (Bank 0)	-	-	-	-	-	-	-	-
M3	BK0_IO27	HSI1B_SOUTN	13N	NC	-	-	NC	-	-
K2	BK0_IO28	-	14P	NC	-	-	NC	-	-
L2	BK0_IO29	-	14N	NC	-	-	NC	-	-
K1	BK0_IO30	HSI1B_SINP	15P	NC	-	-	NC	-	-
L1	BK0_IO31	HSI1B_SINN	15N	NC	-	-	NC	-	-
M2	BK0_IO32	-	16P	BK0_IO16	-	8P	NC	-	-
M1	BK0_IO33	-	16N	BK0_IO17	-	8N	NC	-	-
N3	BK0_IO34	PLL_FBK0	17P	BK0_IO18	PLL_FBK0	9P	BK0_IO14	PLL_FBK0	7P/HSI0
-	GND (Bank 0)	-	-	GND (Bank 0)	-	-	-	-	-
N4	BK0_IO35	PLL_RST1	17N	BK0_IO19	PLL_RST1	9N	BK0_IO15	PLL_RST1	7N/HSI0
N2	BK0_IO36	-	18P	BK0_IO20	-	10P	BK0_IO16	-	8P/HSI0
N1	BK0_IO37	PLL_FBK1	18N	BK0_IO21	PLL_FBK1	10N	BK0_IO17	PLL_FBK1	8N/HSI0
P1	BK0_IO38	PLL_RST0	19P	BK0_IO22	PLL_RST0	11P	BK0_IO18	PLL_RST0	9P
-	-	-	-	-	-	-	GND (Bank 0)	-	-
R1	BK0_IO39	-	19N	BK0_IO23	-	11N	BK0_IO19	-	9N
P3	BK0_IO40	CLK_OUT0	20P	BK0_IO24	CLK_OUT0	12P	BK0_IO20	CLK_OUT0	10P
-	GND (Bank 0)	-	-	-	-	-	-	-	-
P2	BK0_IO41	CLK_OUT1	20N	BK0_IO25	CLK_OUT1	12N	BK0_IO21	CLK_OUT1	10N

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AJ25	BK3_IO32	-	79P	NC	-	-	NC	-	-
AG24	BK3_IO33	-	79N	NC	-	-	NC	-	-
AK26	BK3_IO34	-	80P	BK3_IO20	-	49P	BK3_IO16	-	41P
-	-	-	-	-	-	-	GND (Bank 3)	-	-
AH25	BK3_IO35	-	80N	BK3_IO21	-	49N	BK3_IO17	-	41N
AJ26	BK3_IO36	-	81P	BK3_IO22	-	50P	BK3_IO18	-	42P
-	-	-	-	GND (Bank 3)	-	-	-	-	-
AH26	BK3_IO37	-	81N	BK3_IO23	-	50N	BK3_IO19	-	42N
AK27	BK3_IO38	-	82P	NC	-	-	NC	-	-
-	GND (Bank 3)	-	-	-	-	-	-	-	-
AJ27	BK3_IO39	-	82N	NC	-	-	NC	-	-
AG26	BK3_IO40	-	83P	BK3_IO24	-	51P	BK3_IO20	-	43P
AH27	BK3_IO41	-	83N	BK3_IO25	-	51N	BK3_IO21	-	43N
AK28	GSR	-	-	GSR	-	-	GSR	-	-
AJ28	DXP	-	-	DXP	-	-	DXP	-	-
AK29	DXN	-	-	DXN	-	-	DXN	-	-
AH29	BK4_IO0	-	84P	BK4_IO0	-	52P/HSI2	BK4_IO0	-	44P
AG28	BK4_IO1	-	84N	BK4_IO1	-	52N/HSI2	BK4_IO1	-	44N
AF27	BK4_IO2	-	85P/HSI3	NC	-	-	NC	-	-
-	GND (Bank 4)	-	-	-	-	-	-	-	-
AF28	BK4_IO3	-	85N/HSI3	NC	-	-	NC	-	-
AJ30	BK4_IO4	-	86P/HSI3	NC	-	-	NC	-	-
AH30	BK4_IO5	-	86N/HSI3	NC	-	-	NC	-	-
AG29	BK4_IO6	-	87P/HSI3	NC	-	-	NC	-	-
AF29	BK4_IO7	-	87N/HSI3	NC	-	-	NC	-	-
AE28	BK4_IO8	-	88P/HSI3	NC	-	-	NC	-	-
AD27	BK4_IO9	-	88N/HSI3	NC	-	-	NC	-	-
AG30	BK4_IO10	HSI3A_SINP	89P/HSI3	BK4_IO2	HSI2A_SINP	53P/HSI2	BK4_IO2	-	45P
-	GND (Bank 4)	-	-	GND (Bank 4)	-	-	-	-	-
AF30	BK4_IO11	HSI3A_SINN	89N/HSI3	BK4_IO3	HSI2A_SINN	53N/HSI2	BK4_IO3	-	45N
AD28	BK4_IO12	-	90P/HSI3	BK4_IO4	-	54P/HSI2	BK4_IO4	-	46P
-	-	-	-	-	-	-	GND (Bank 4)	-	-
AC27	BK4_IO13	-	90N/HSI3	BK4_IO5	-	54N/HSI2	BK4_IO5	-	46N
AE29	BK4_IO14	HSI3A_SOUTP	91P/HSI3	BK4_IO6	HSI2A_SOUTP	55P/HSI2	NC	-	-
AE30	BK4_IO15	HSI3A_SOUTN	91N/HSI3	BK4_IO7	HSI2A_SOUTN	55N/HSI2	NC	-	-
AD29	BK4_IO16	-	92P/HSI3	BK4_IO8	-	56P/HSI2	BK4_IO6	-	47P
AD30	BK4_IO17	VREF4	92N/HSI3	BK4_IO9	VREF4	56N/HSI2	BK4_IO7	VREF4	47N
AC28	BK4_IO18	HSI3B_SINP	93P	BK4_IO10	HSI2B_SINP	57P/HSI2	NC	-	-
-	GND (Bank 4)	-	-	GND (Bank 4)	-	-	-	-	-
AB28	BK4_IO19	HSI3B_SINN	93N	BK4_IO11	HSI2B_SINN	57N/HSI2	NC	-	-
AA27	BK4_IO20	PLL_RST4	94P	BK4_IO12	PLL_RST4	58P/HSI2	BK4_IO8	PLL_RST4	48P
AB29	BK4_IO21	PLL_RST5	94N	BK4_IO13	PLL_RST5	58N/HSI2	BK4_IO9	PLL_RST5	48N
AC29	BK4_IO22	HSI3B_SOUTP	95P	BK4_IO14	HSI2B_SOUTP	59P/HSI2	BK4_IO10	-	49P
AC30	BK4_IO23	HSI3B_SOUTN	95N	BK4_IO15	HSI2B_SOUTN	59N/HSI2	BK4_IO11	-	49N
AA28	BK4_IO24	-	96P	NC	-	-	NC	-	-
Y27	BK4_IO25	-	96N	NC	-	-	NC	-	-
Y28	BK4_IO26	-	97P	NC	-	-	NC	-	-
-	GND (Bank 4)	-	-	-	-	-	-	-	-
AA29	BK4_IO27	-	97N	NC	-	-	NC	-	-
Y29	BK4_IO28	-	98P	BK4_IO16	-	60P	BK4_IO12	-	50P
-	-	-	-	-	-	-	GND (Bank 4)	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
D21	BK6_IO20	-	136P	BK6_IO8	-	82P	BK6_IO8	-	70P
C21	BK6_IO21	VREF6	136N	BK6_IO9	VREF6	82N	BK6_IO9	VREF6	70N
B21	BK6_IO22	DATA5	137P	BK6_IO10	DATA5	83P	BK6_IO10	DATA5	71P
-	-	-	-	GND (Bank 6)	-	-	-	-	-
A21	BK6_IO23	DATA4	137N	BK6_IO11	DATA4	83N	BK6_IO11	DATA4	71N
D20	BK6_IO24	-	138P	BK6_IO12	-	84P	BK6_IO12	-	72P
-	-	-	-	-	-	-	GND (Bank 6)	-	-
C20	BK6_IO25	-	138N	BK6_IO13	-	84N	BK6_IO13	-	72N
B20	BK6_IO26	DATA3	139P	BK6_IO14	DATA3	85P	BK6_IO14	DATA3	73P
-	GND (Bank 6)	-	-	-	-	-	-	-	-
A20	BK6_IO27	DATA2	139N	BK6_IO15	DATA2	85N	BK6_IO15	DATA2	73N
C19	BK6_IO28	-	140P	BK6_IO16		86P	BK6_IO16	-	74P
B19	BK6_IO29	-	140N	BK6_IO17		86N	BK6_IO17	-	74N
A19	BK6_IO30	DATA1	141P	BK6_IO18	DATA1	87P	BK6_IO18	DATA1	75P
-	-	-	-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
A18	BK6_IO31	DATA0	141N	BK6_IO19	DATA0	87N	BK6_IO19	DATA0	75N
D18	BK6_IO32	-	142P	BK6_IO20		88P	BK6_IO20	-	76P
C18	BK6_IO33	-	142N	BK6_IO21		88N	BK6_IO21	-	76N
B18	BK6_IO34	-	143P	BK6_IO22		89P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-	-	-	-
C17	BK6_IO35	-	143N	BK6_IO23		89N	NC	-	-
B17	BK6_IO36	-	144P	NC	-	-	NC	-	-
A17	BK6_IO37	-	144N	NC	-	-	NC	-	-
D16	BK6_IO38	-	145P	NC	-	-	NC	-	-
C16	BK6_IO39	-	145N	NC	-	-	NC	-	-
B16	BK6_IO40	-	146P	BK6_IO24	-	90P	NC	-	-
A16	BK6_IO41	-	146N	BK6_IO25	-	90N	NC	-	-
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-	-	-	-
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-	-	-	-
A15	BK7_IO0	-	147P	BK7_IO0	-	91P	BK7_IO0	-	77P
B15	BK7_IO1	-	147N	BK7_IO1	-	91N	BK7_IO1	-	77N
C15	BK7_IO2	-	148P	BK7_IO2	-	92P	BK7_IO2	-	78P
-	-	-	-	-	-	-	GND (Bank 7)	-	-
D15	BK7_IO3	-	148N	BK7_IO3	-	92N	BK7_IO3	-	78N
A14	BK7_IO4	-	149P	BK7_IO4	-	93P	BK7_IO4	-	79P
B14	BK7_IO5	-	149N	BK7_IO5	-	93N	BK7_IO5	-	79N
C14	BK7_IO6	-	150P	BK7_IO6	-	94P	NC	-	-
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-	-	-	-
A13	BK7_IO7	-	150N	BK7_IO7	-	94N	NC	-	-
B13	BK7_IO8	-	151P	BK7_IO8	-	95P	NC	-	-
C13	BK7_IO9	-	151N	BK7_IO9	-	95N	NC	-	-
D13	BK7_IO10	-	152P	BK7_IO10	-	96P	BK7_IO6	-	80P
B12	BK7_IO11	-	152N	BK7_IO11	-	96N	BK7_IO7	-	80N
C12	BK7_IO12	-	153P	BK7_IO12	-	97P	BK7_IO8	-	81P
-	-	-	-	-	-	-	GND (Bank 7)	-	-
A12	BK7_IO13	-	153N	BK7_IO13		97N	BK7_IO9	-	81N
A11	BK7_IO14	-	154P	BK7_IO14	-	98P	BK7_IO10	-	82P
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-	-	-	-
B11	BK7_IO15	-	154N	BK7_IO15	-	98N	BK7_IO11	-	82N
C11	BK7_IO16	-	155P	NC	-	-	NC	-	-
D11	BK7_IO17	-	155N	NC	-	-	NC	-	-

ispXPGA Logic Signal Connections: 680-Ball fpBGA

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
C4	BK0_IO0	-	0P
B4	BK0_IO1	-	0N
E6	BK0_IO2	-	1P
-	GND (Bank 0)	-	-
D6	BK0_IO3	-	1N
A4	BK0_IO4	-	2P
E8	BK0_IO5	-	2N
C5	BK0_IO6	HSI0A_SOUTP	3P
C6	BK0_IO7	HSI0A_SOUTN	3N
A6	BK0_IO8	-	4P
A5	BK0_IO9	-	4N
B6	BK0_IO10	HSI0A_SINP	5P/HSI0
-	GND (Bank 0)	-	-
B5	BK0_IO11	HSI0A_SINN	5N/HSI0
B7	BK0_IO12	VREF0	6P/HSI0
A7	BK0_IO13	-	6N/HSI0
D8	BK0_IO14	HSI0B_SOUTP	7P/HSI0
D7	BK0_IO15	HSI0B_SOUTN	7N/HSI0
D9	BK0_IO16	-	8P/HSI0
E10	BK0_IO17	-	8N/HSI0
C8	BK0_IO18	HSI0B_SINP	9P/HSI0
-	GND (Bank 0)	-	-
C7	BK0_IO19	HSI0B_SINN	9N/HSI0
A8	BK0_IO20	-	10P/HSI0
A9	BK0_IO21	-	10N/HSI0
C9	BK0_IO22	HSI1A_SOUTP	11P/HSI0
B8	BK0_IO23	HSI1A_SOUTN	11N/HSI0
B9	BK0_IO24	-	12P/HSI0
B10	BK0_IO25	-	12N/HSI0
D11	BK0_IO26	HSI1A_SINP	13P/HSI1
-	GND (Bank 0)	-	-
D10	BK0_IO27	HSI1A_SINN	13N/HSI1
A10	BK0_IO28	-	14P/HSI1
C12	BK0_IO29	-	14N/HSI1
D12	BK0_IO30	HSI1B_SOUTP	15P/HSI1
C11	BK0_IO31	HSI1B_SOUTN	15N/HSI1
A12	BK0_IO32	-	16P/HSI1
A13	BK0_IO33	-	16N/HSI1
B13	BK0_IO34	HSI1B_SINP	17P/HSI1
-	GND (Bank 0)	-	-
B12	BK0_IO35	HSI1B_SINN	17N/HSI1
E14	BK0_IO36	-	18P/HSI1

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
AU6	BK5_IO50	HSI9B_SINP	180P/HSI9
-	GND (Bank 5)	-	-
AV6	BK5_IO51	HSI9B_SINN	180N/HSI9
AR8	BK5_IO52	-	181P
AT7	BK5_IO53	-	181N
AU5	BK5_IO54	HSI9B_SOUTP	182P
AV5	BK5_IO55	HSI9B_SOUTN	182N
AW5	BK5_IO56	-	183P
AW4	BK5_IO57	-	183N
AT6	BK5_IO58	-	184P
-	GND (Bank 5)	-	-
AV4	BK5_IO59	-	184N
AR6	BK5_IO60	-	185P
AU4	BK5_IO61	-	185N
AT1	CFG0	-	-
AT3	DONE	-	-
AT2	PROGRAMb	-	-
AP4	BK6_IO0	INITb	186P
AP5	BK6_IO1	CCLK	186N
AR3	BK6_IO2	-	187P
-	GND (Bank 6)	-	-
AR2	BK6_IO3	-	187N
AP3	BK6_IO4	CSb	188P
AR1	BK6_IO5	Read	188N
AP2	BK6_IO6	-	189P
AP1	BK6_IO7	-	189N
AN4	BK6_IO8	-	190P
AM5	BK6_IO9	-	190N
AN3	BK6_IO10	-	191P
-	GND (Bank 6)	-	-
AN2	BK6_IO11	-	191N
AM4	BK6_IO12	VREF6	192P
AM3	BK6_IO13	-	192N
AN1	BK6_IO14	-	193P
AM2	BK6_IO15	-	193N
AL4	BK6_IO16	-	194P
AK5	BK6_IO17	-	194N
AM1	BK6_IO18	-	195P
-	GND (Bank 6)	-	-
AK4	BK6_IO19	-	195N
AL3	BK6_IO20	-	196P
AL2	BK6_IO21	-	196N
AL1	BK6_IO22	-	197P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

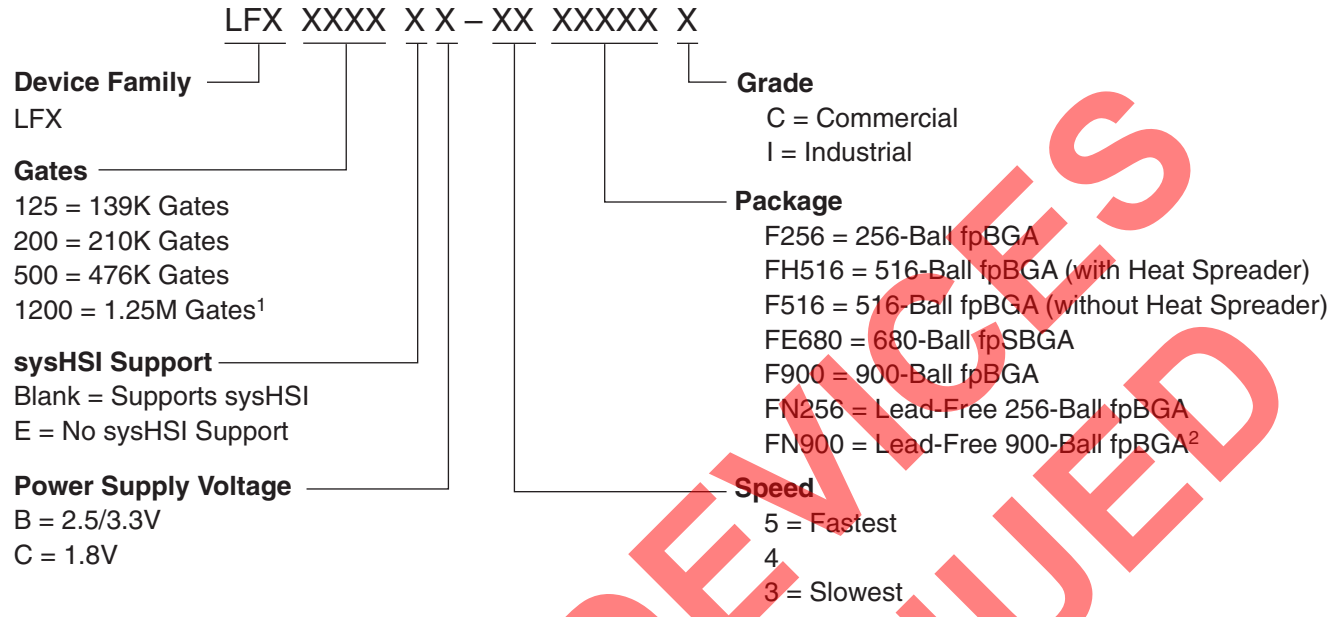
900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
-	-	-	-	GND (Bank 1)	-	-
T1	BK1_IO1	CLK_OUT3	31N	BK1_IO1	CLK_OUT3	21N
U2	BK1_IO2	SS_CLKOUT0P	32P	BK1_IO2	SS_CLKOUT0P	22P
-	GND (Bank 1)	-	-	-	-	-
U1	BK1_IO3	SS_CLKOUT0N	32N	BK1_IO3	SS_CLKOUT0N	22N
U3	BK1_IO4	PLL_FBK2	33P	BK1_IO4	PLL_FBK2	23P
U4	BK1_IO5	PLL_FBK3	33N	BK1_IO5	PLL_FBK3	23N
V1	BK1_IO6	SS_CLKIN0P	34P	BK1_IO10	SS_CLKIN0P	26P
V2	BK1_IO7	SS_CLKIN0N	34N	BK1_IO11	SS_CLKIN0N	26N
U5	BK1_IO8	-	35P	BK1_IO12	-	27P
U6	BK1_IO9	-	35N	BK1_IO13	-	27N
V4	BK1_IO10	-	36P	BK1_IO6	-	24P
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-
V3	BK1_IO11	-	36N	BK1_IO7	-	24N
V6	BK1_IO12	PLL_RST2	37P	BK1_IO20	PLL_RST2	31P
V7	BK1_IO13	PLL_RST3	37N	BK1_IO21	PLL_RST3	31N
W1	BK1_IO14	-	38P	BK1_IO8	-	25P
W2	BK1_IO15	-	38N	BK1_IO9	-	25N
W3	BK1_IO16	-	39P	BK1_IO14	-	28P
-	-	-	-	GND (Bank 1)	-	-
W4	BK1_IO17	-	39N	BK1_IO15	-	28N
W5	BK1_IO18	-	40P	BK1_IO16	-	29P
-	GND (Bank 1)	-	-	-	-	-
W6	BK1_IO19	-	40N	BK1_IO17	-	29N
Y6	BK1_IO20	-	41P/HSI3	NC	-	-
Y5	BK1_IO21	-	41N/HSI3	NC	-	-
Y4	BK1_IO22	-	42P/HSI3	NC	-	-
Y3	BK1_IO23	-	42N/HSI3	NC	-	-
AA5	BK1_IO24	-	43P/HSI3	NC	-	-
AA4	BK1_IO25	-	43N/HSI3	NC	-	-
Y2	BK1_IO26	HSI3A_SOUTP	44P/HSI3	BK1_IO18	HSI2A_SOUTP	30P
-	GND (Bank 1)	-	-	-	-	-
Y1	BK1_IO27	HSI3A_SOUTN	44N/HSI3	BK1_IO19	HSI2A_SOUTN	30N
AB7	BK1_IO28	-	45P/HSI3	NC	-	-
AB6	BK1_IO29	-	45N/HSI3	NC	-	-
AA2	BK1_IO30	HSI3A_SINP	46P/HSI3	BK1_IO22	HSI2A_SINP	32P
-	-	-	-	GND (Bank 1)	-	-
AA1	BK1_IO31	HSI3A_SINN	46N/HSI3	BK1_IO23	HSI2A_SINN	32N
AB5	BK1_IO32	-	47P/HSI3	NC	-	-
AB4	BK1_IO33	-	47N/HSI3	NC	-	-
AB2	BK1_IO34	HSI3B_SOUTP	48P/HSI3	NC	-	-
-	GND (Bank 1)	-	-	-	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
F10	BK7_IO36	-	235P	NC	-	-
G10	BK7_IO37	-	235N	NC	-	-
A8	BK7_IO38	-	236P	NC	-	-
B8	BK7_IO39	-	236N	NC	-	-
D9	BK7_IO40	-	237P	BK7_IO22	-	158P
-	-	-	-	GND (Bank 7)	-	-
E9	BK7_IO41	-	237N	BK7_IO23	-	158N
A7	BK7_IO42	-	238P	BK7_IO24	-	159P
-	GND (Bank 7)	-	-		-	-
B7	BK7_IO43	-	238N	BK7_IO25	-	159N
C8	BK7_IO44	-	239P	BK7_IO26	-	160P
D8	BK7_IO45	-	239N	BK7_IO27	-	160N
A6	BK7_IO46	-	240P	BK7_IO21	-	157N
B6	BK7_IO47	VREF7	240N	BK7_IO20	VREF7	157P
E8	BK7_IO48	-	241P	BK7_IO28	-	161P
F8	BK7_IO49	-	241N	BK7_IO29	-	161N
C7	BK7_IO50	-	242P	BK7_IO30	-	162P
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-
D7	BK7_IO51	-	242N	BK7_IO31	-	162N
E7	BK7_IO52	-	243P	BK7_IO32	-	163P
F7	BK7_IO53	-	243N	BK7_IO33	-	163N
A5	BK7_IO54	-	244P	BK7_IO34	-	164P
B5	BK7_IO55	-	244N	BK7_IO35	-	164N
C6	BK7_IO56	-	245P	BK7_IO36	-	165P
D6	BK7_IO57	-	245N	BK7_IO37	-	165N
D5	BK7_IO58	-	246P	BK7_IO38	-	166P
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-
C5	BK7_IO59	-	246N	BK7_IO39	-	166N
B4	BK7_IO60	-	247P	BK7_IO40	-	167P
A4	BK7_IO61	-	247N	BK7_IO41	-	167N
A3	TDO	-	-	TDO	-	-
B3	VCCJ	-	-	VCCJ	-	-
C4	TDI	-	-	TDI	-	-

1. If a sysHSI Block is used, the indicated sysHSI reserved pins are unavailable for general purpose I/O use.

Part Number Description



1. Discontinued via PCN #03A-10.
2. Select products only. See Ordering Information tables below for specific support.

Ordering Information

Conventional Packaging

Commercial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125B-05F256C	139K	2.5/3.3	-5	fpBGA	256
LFX125B-04F256C	139K	2.5/3.3	-4	fpBGA	256
LFX125B-03F256C	139K	2.5/3.3	-3	fpBGA	256
LFX125C-04F256C	139K	1.8	-4	fpBGA	256
LFX125C-03F256C	139K	1.8	-3	fpBGA	256
LFX125B-05F516C	139K	2.5/3.3	-5	fpBGA	516
LFX125B-04F516C	139K	2.5/3.3	-4	fpBGA	516
LFX125B-03F516C	139K	2.5/3.3	-3	fpBGA	516
LFX125C-04F516C	139K	1.8	-4	fpBGA	516
LFX125C-03F516C	139K	1.8	-3	fpBGA	516
LFX125B-05FH516C[1]	139K	2.5/3.3	-5	fpBGA	516
LFX125B-04FH516C[1]	139K	2.5/3.3	-4	fpBGA	516
LFX125B-03FH516C[1]	139K	2.5/3.3	-3	fpBGA	516
LFX125C-04FH516C[1]	139K	1.8	-4	fpBGA	516
LFX125C-03FH516C[1]	139K	1.8	-3	fpBGA	516
LFX200B-05F256C	210K	2.5/3.3	-5	fpBGA	256
LFX200B-04F256C	210K	2.5/3.3	-4	fpBGA	256
LFX200B-03F256C	210K	2.5/3.3	-3	fpBGA	256
LFX200C-04F256C	210K	1.8	-4	fpBGA	256
LFX200C-03F256C	210K	1.8	-3	fpBGA	256

"E-Series" Industrial (Cont.)

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX1200EB-04F900I[2]	1.25M	2.5/3.3	-4	fpBGA	900
LFX1200EB-03F900I[2]	1.25M	2.5/3.3	-3	fpBGA	900
LFX1200EC-03F900I[2]	1.25M	1.8	-3	fpBGA	900
LFX1200EB-04FE680I[2]	1.25M	2.5/3.3	-4	fpSBGA	680
LFX1200EB-03FE680I[2]	1.25M	2.5/3.3	-3	fpSBGA	680
LFX1200EC-03FE680I[2]	1.25M	1.8	-3	fpSBGA	680

1. FH516 package was converted to F516 via PCN #09A-08.
2. Discontinued via PCN #03A-10.

Lead-Free Packaging

Commercial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125B-05FN256C	139K	2.5/3.3	-5	Lead-Free fpBGA	256
LFX125B-04FN256C	139K	2.5/3.3	-4	Lead-Free fpBGA	256
LFX125B-03FN256C	139K	2.5/3.3	-3	Lead-Free fpBGA	256
LFX125C-04FN256C	139K	1.8	-4	Lead-Free fpBGA	256
LFX125C-03FN256C	139K	1.8	-3	Lead-Free fpBGA	256
LFX200B-05FN256C	210K	2.5/3.3	-5	Lead-Free fpBGA	256
LFX200B-04FN256C	210K	2.5/3.3	-4	Lead-Free fpBGA	256
LFX200B-03FN256C	210K	2.5/3.3	-3	Lead-Free fpBGA	256
LFX200C-04FN256C	210K	1.8	-4	Lead-Free fpBGA	256
LFX200C-03FN256C	210K	1.8	-3	Lead-Free fpBGA	256
LFX500B-05FN900C	476K	2.5/3.3	-5	Lead-Free fpBGA	900
LFX500B-04FN900C	476K	2.5/3.3	-4	Lead-Free fpBGA	900
LFX500B-03FN900C	476K	2.5/3.3	-3	Lead-Free fpBGA	900
LFX500C-04FN900C	476K	1.8	-4	Lead-Free fpBGA	900
LFX500C-03FN900C	476K	1.8	-3	Lead-Free fpBGA	900

"E-Series" Commercial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125EB-05FN256C	139K	2.5/3.3	-5	Lead-Free fpBGA	256
LFX125EB-04FN256C	139K	2.5/3.3	-4	Lead-Free fpBGA	256
LFX125EB-03FN256C	139K	2.5/3.3	-3	Lead-Free fpBGA	256
LFX125EC-04FN256C	139K	1.8	-4	Lead-Free fpBGA	256
LFX125EC-03FN256C	139K	1.8	-3	Lead-Free fpBGA	256
LFX200EB-05FN256C	210K	2.5/3.3	-5	Lead-Free fpBGA	256
LFX200EB-04FN256C	210K	2.5/3.3	-4	Lead-Free fpBGA	256
LFX200EB-03FN256C	210K	2.5/3.3	-3	Lead-Free fpBGA	256
LFX200EC-04FN256C	210K	1.8	-4	Lead-Free fpBGA	256
LFX200EC-03FN256C	210K	1.8	-3	Lead-Free fpBGA	256
LFX500EB-05FN900C	476K	2.5/3.3	-5	Lead-Free fpBGA	900
LFX500EB-04FN900C	476K	2.5/3.3	-4	Lead-Free fpBGA	900
LFX500EB-03FN900C	476K	2.5/3.3	-3	Lead-Free fpBGA	900